Σχεδίαση Αναλογικών Ηλεκτρονικών Συστημάτων

Βασικές Αρχιτεκτονικές PLL

Γ. Παναγόπουλος

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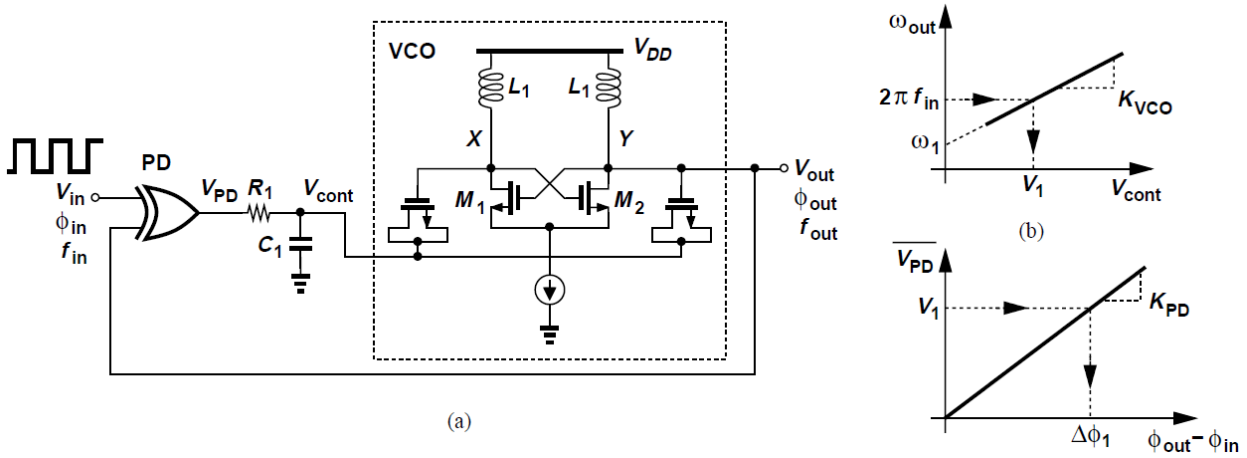
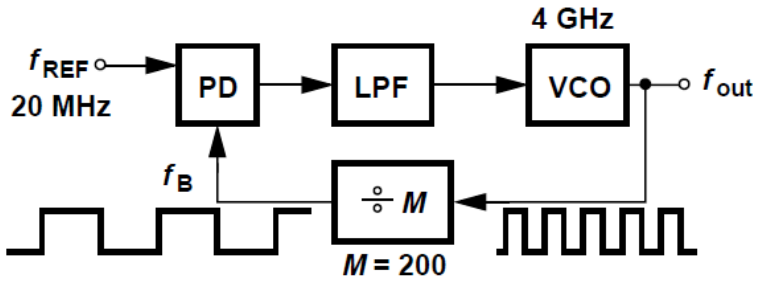
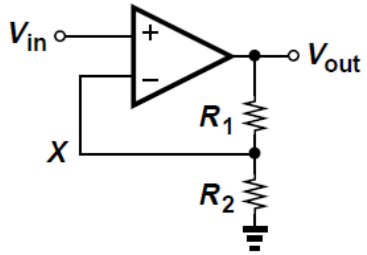
Analysis of Simple PLL – Static Behavior



- $\Phi_{in} - \Phi_{out}$ is constant; differentiating the equation tells us that the reference and output operate at the same frequency
- To maintain a frequency $f_{out} = f_{in}$ VCO needs a finite input voltage V1 which LPF needs to generate as the average of PD output. This translates into a finite static phase offset $\Delta\Phi_1$ which can be undesirable based on application

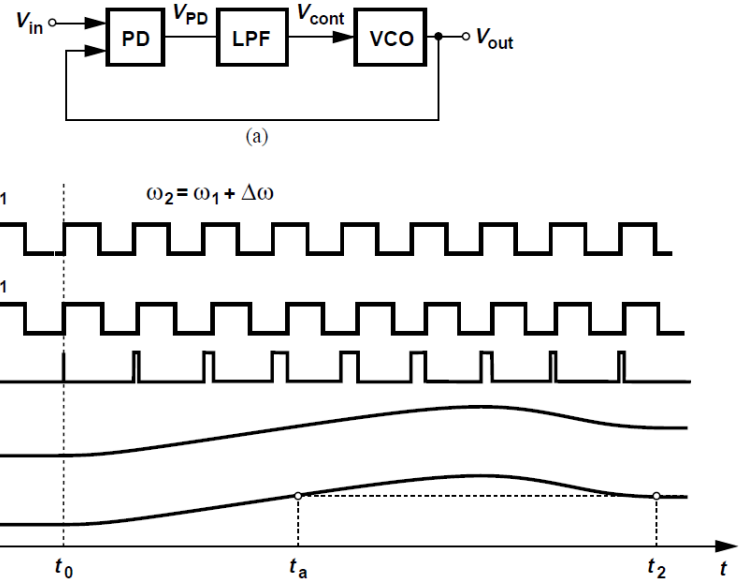
Frequency Multiplication





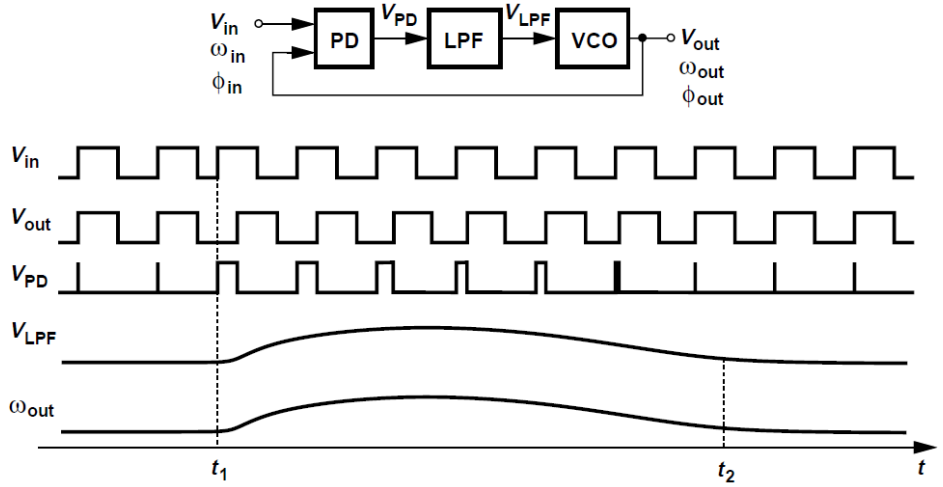
- If we wish to generate a 4GHz clock from a 20MHz reference, we can insert a frequency divider in the feedback path which is a counter which generates one pulse for every 200 input pulses
- The loop attempts to match the frequency of the output of the divider and the reference which inherently sets the output frequency to be ‘M’ times the reference
- This also provides programmable control over the output frequency by changing the value of M

Dynamic Behavior – Frequency Step



- Step the reference input voltage by Δω
- The Vcont and ω_{out} doesn't change immediately and phase difference grows which gradually raise Vcont and hence ω_{out} ; ω_{out} increases to new value ω_2
- To maintain the new higher frequency, higher Vcont and hence wider PD output pulses are required
- The exact characteristics depend on loop (example ringing if underdamped); loop not locked from t_a to t_2 as phase error changes with time

Dynamic Behavior – Phase Step

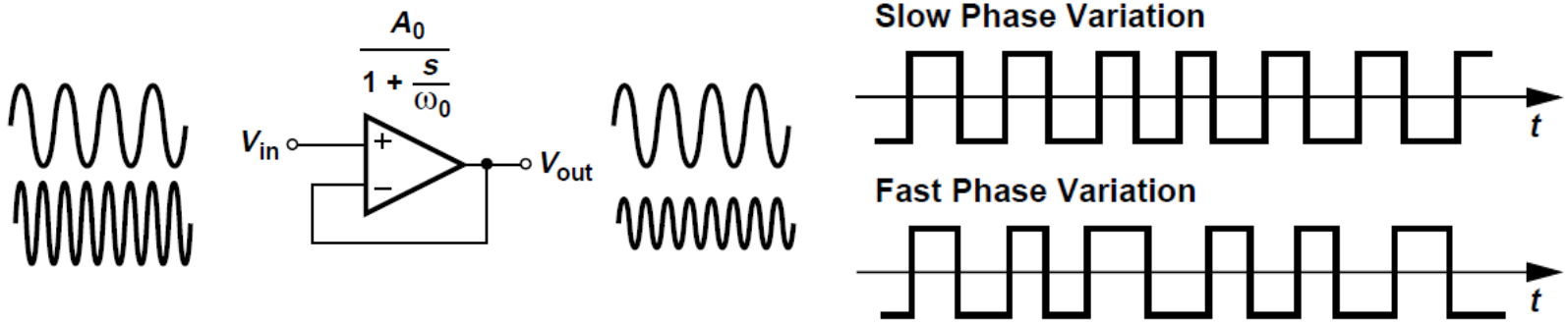


- Phase step is applied at t = t_1
- The step immediately converts to phase error and the PD output pulses grow wider
- Consequently the Vcont and ω_{out} increase and the output/feedback phase catches up to the input phase step
- The phase error and Vcont remain the same as before after the loop settles

Dynamic Behavior – Remarks

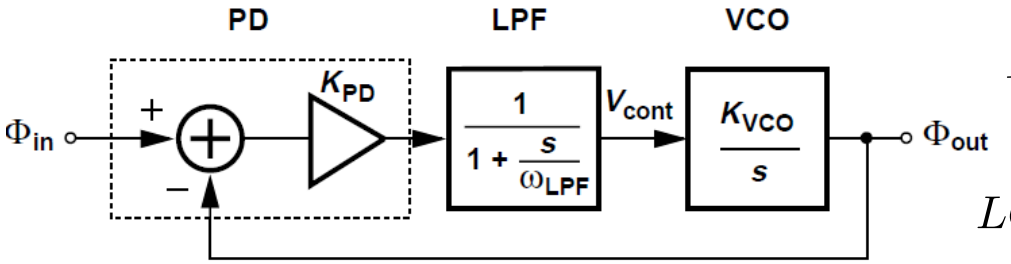
- In analogy with voltage domain circuits, amplifier can only detect and correct a voltage step at its input while a PLL can do the same for a phase step and a frequency step
- The most convenient point in a PLL for monitoring transient behavior is VCO control line since other quantities are not intuitive to interpret
- Loop doesn't settle at $t = t_a$ even though ω_{out} is at the correct value. For locking, PLL needs both "phase acquisition" and "frequency acquisition" i.e. both ω_{out} and $\Delta\Phi_1$ should settle to the correct value

PLL Transfer Function - I



- Following the analogy with voltage domain circuits, an amplifier can follow slow changes in frequency, but it can not track too fast changes in voltage frequency of which is beyond the closed loop bandwidth; functions like LPF
- An understanding of how PLL responds to slow or fast changes in phase is desired
- Prediction: only slow phase changes are tracked

PLL Transfer Function - II



$$H_{OL} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

$$H_{CL}(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{H_{OL}(s)}{1 - LG(s)}$$

$$LG(s) = -K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

$$H_{CL}(s) = \frac{K_{PD}K_{VCO}}{s^2/\omega_{LPF} + s + K_{PD}K_{VCO}}$$

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \qquad \omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$

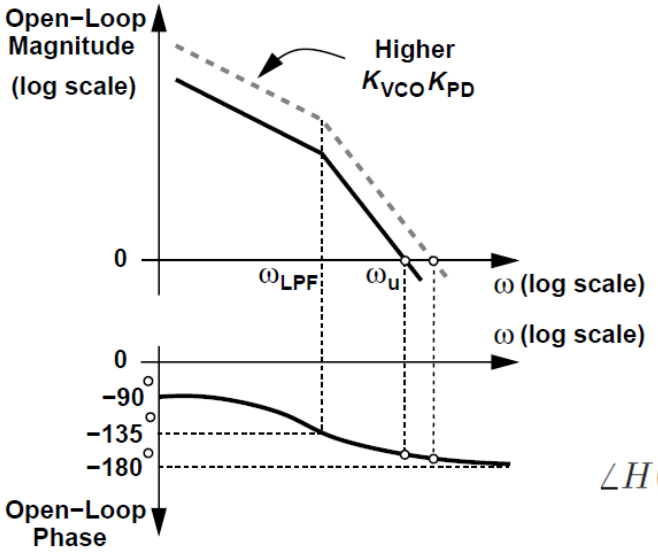
$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}.$$

- Blocks are replaced with their linear representation; VCO is modeled as an integrator because the output is a phase sensed by the PD
- Closed loop transfer function can be calculated
- The obtained expression is compared to the second order system general expression and damping factor (ζ) and natural frequency (ω_n) expressions are derived

PLL Transfer Function – III

- Z informs about the stability of the loop. For critical damping, the value is $\frac{\sqrt{2}}{2}$; typical value is between $\frac{\sqrt{2}}{2}$ and 1
- The discussed topology is called “type-I” PLL because the open loop transfer function contains a single ideal integrator (one pole at origin)
- The ω represent the rate of change of phase and not the input frequency of the loop
- For slow fluctuations, the output tracks the input variation in frequency, however, for faster input fluctuations (variation of phase at input outside loop bandwidth), the output phase fluctuations are smaller.

PLL Transfer Function - IV



$$\frac{K_{PD}^2 K_{VCO}^2}{(1+\frac{\omega_u^2}{\omega_{LPF}^2})\omega_u^2} = 1 \qquad \frac{\omega_u}{\omega_{LPF}} = \sqrt{\frac{K_{PD}^2 K_{VCO}^2}{\omega_u^2} - 1.}$$

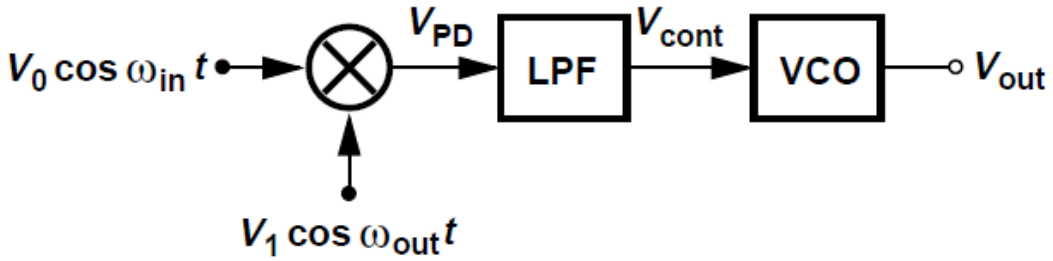
$$\angle H(j\omega_u) = -90^\circ - \tan^{-1}\frac{\omega_u}{\omega_{LPF}} = -90^\circ - \tan^{-1}\sqrt{\frac{K_{PD}^2 K_{VCO}^2}{\omega_u^2} - 1.}$$

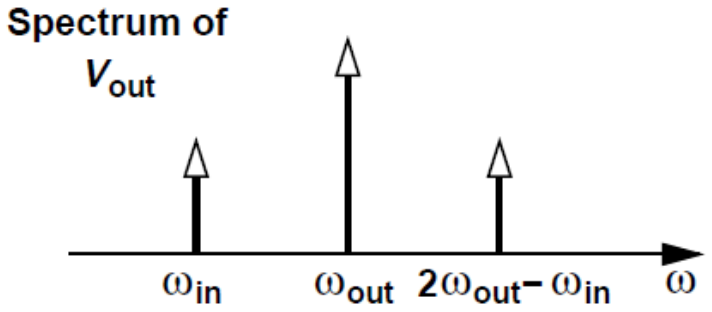
- Increasing $K_{PD}K_{VCO}$ decreases ζ, increases gain and raises ω_u ; phase plot is unaltered. This decreases the PM and hence stability
- ζ decreases if ω_{LPF} is reduced thus stability is reduced if we decrease ω_{LPF} to reduce PD injections

Drawbacks of Simple PLL – I

- Decreasing ω_{LPF} to reduce Vcont disturbances or increasing K_{PD} to reduce static phase error, both reduce the stability of the loop
- ω_{LPF} trades off with “acquisition range”, the maximum initial difference between output and reference frequency for which the loop can lock
- The loop readily fails to lock under PVT variations and other imperfections in the circuit or otherwise the performance takes a toll

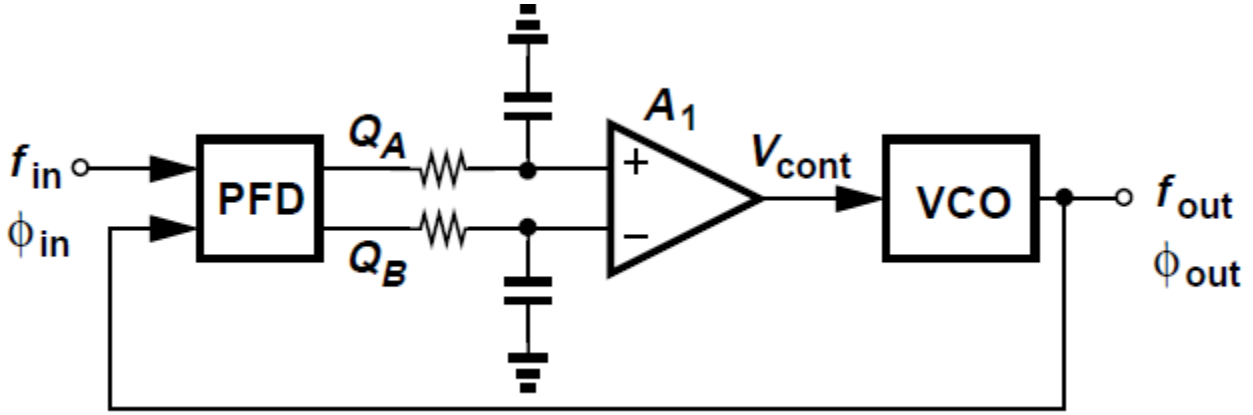
Drawbacks of Simple PLL – II





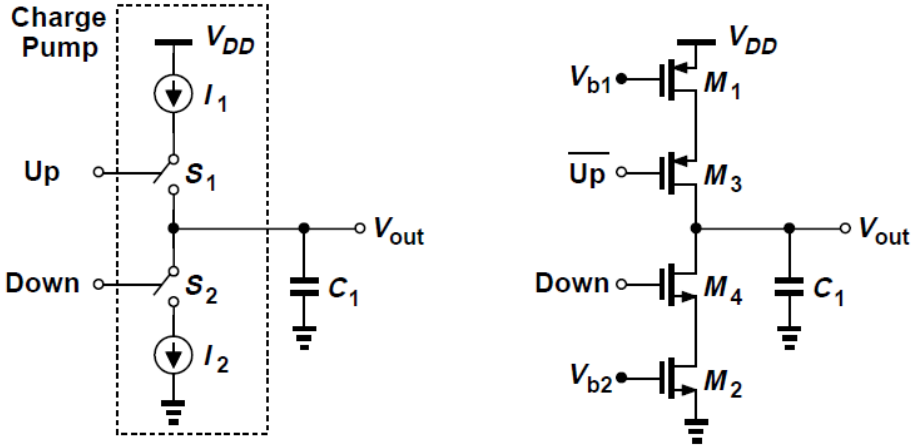
- If we take the PD to be a mixer, it generates $\omega_{in} - \omega_{out}$ component. This is modulated by VCO to generate $\omega_{out} \pm (\omega_{in} - \omega_{out})$ sidebands
- The band at ω_{in} mixes at the PD to generate Dc that drives ω_{out} towards ω_{in}
- If initial difference between ω_{out} and ω_{in} is large, the sideband gets more attenuated and not enough Dc can be generated, as a result the loop can not lock

PLL using PFD



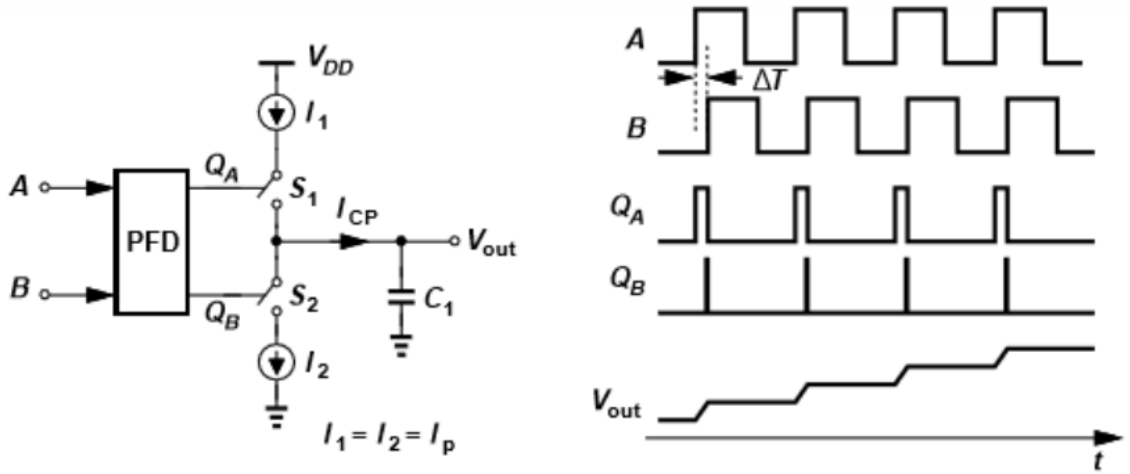
- PFD eliminates tradeoff between acquisition range and loop bandwidth
- PFD output is filtered and subtracted to produce V_{cont}
- Type – I loop still poses trade-offs between stability, loop bandwidth and static phase error

CP-PLLs – Charge Pump



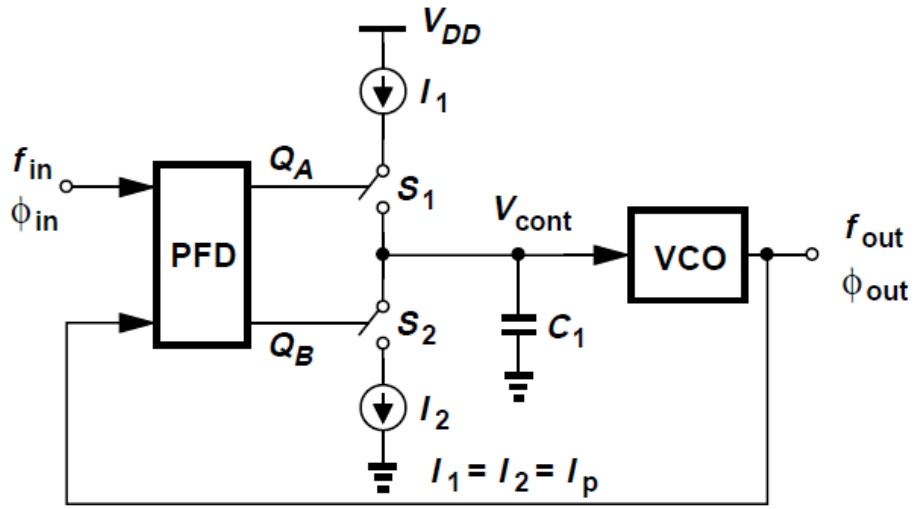
- Charge pumps (CP) are circuits which source or sink current for controlled amount of time
- I_1 charges C_1 and I_2 discharges it, given the appropriate switches are turned on
- The control signals are called Up and Down since they decide voltage of cap. rises or falls
- $I_1=I_2=I_p$; switches are placed in series with the drain of the current sources and hence this topology is called “drain-switched” CP

CP-PLLs – PFD/CP/Capacitor Cascade



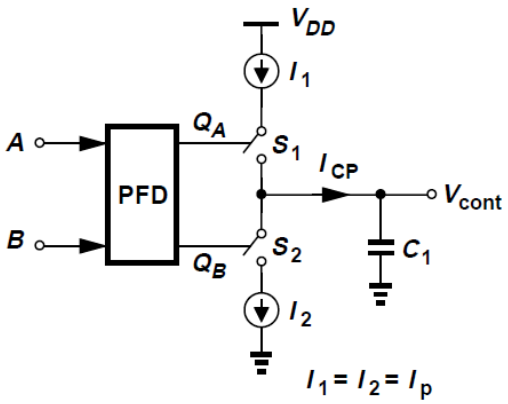
- If A and B have same frequency but finite phase error, whenever there is a comparison, Q_A goes high, S_1 turns on, I_1 charges C_1 and V_{out} rises by $\Delta V = (I_p/C_1)\Delta T$
- For a finite phase error, V_{out} rises indefinitely thus there is "infinite" gain
- For V_{out} to be finite, the phase error must be zero so that no net charge is is injected by CP in each cycle

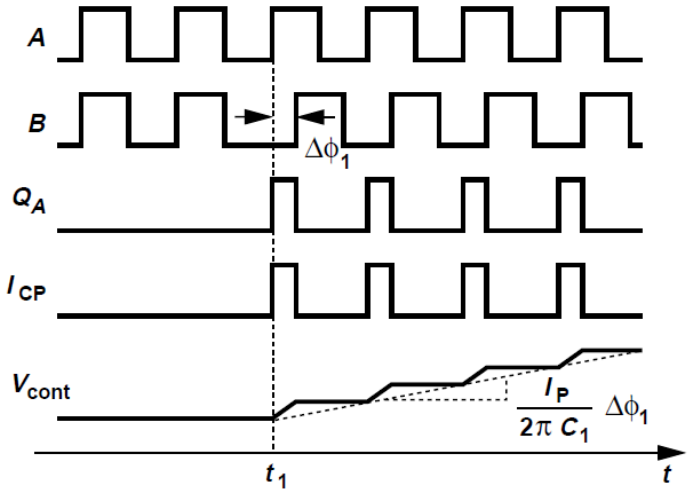
CP-PLLs – Basic CP-PLL



- If the loop is locked, $f_{in}=f_{out}$ and V_{cont} has a finite value for which the CP must not inject any charge into C_1 for which $\Phi_{in} = \Phi_{out}$
- Thus, the loop locks with zero static phase error regardless of input frequency, K_{VCO} and I_p
- This arises from the integration action of Charge Pump and capacitor combination

PFD/CP/Capacitor Transfer Function - I

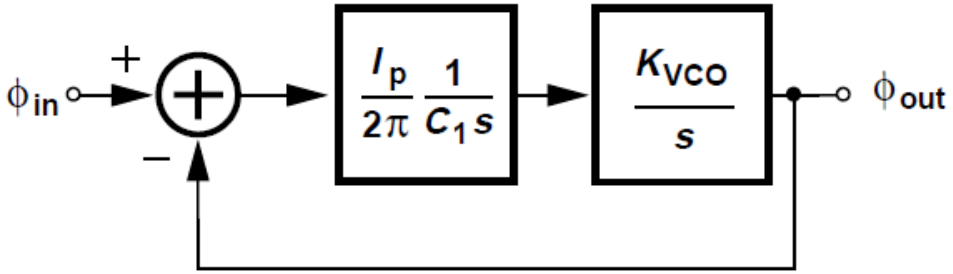




$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi C_1 s}.$$

- For a phase step $\Delta\Phi_1$ at B, Q_A remains high for $[\Delta\phi_1/(2\pi)]T_{in}$ seconds; control voltage rises by $\Delta V = [\Delta\phi_1/(2\pi)]T_{in}(I_p/C_1)$ at phase comparison
- The given figure is true step response of cascade; reveals that it is nonlinear since ramp slope doesn't change
- We can approximate the response by a continuous ramp with a slope of $\Delta V/T_{in} = [\Delta\phi_1/(2\pi)](I_p/C_1)$ which suggests integration
- Thus the impulse response is $[\Delta\phi_1/(2\pi)](I_p/C_1)u(t)$; the transfer function is given above

PFD/CP/Capacitor Transfer Function – II

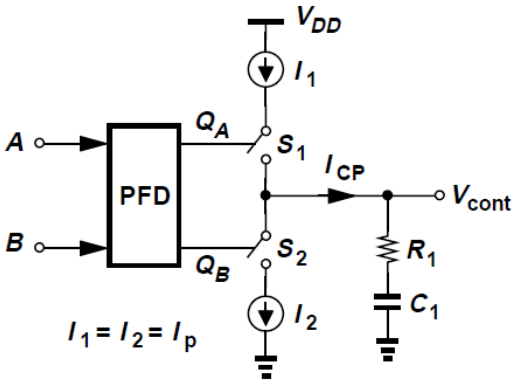


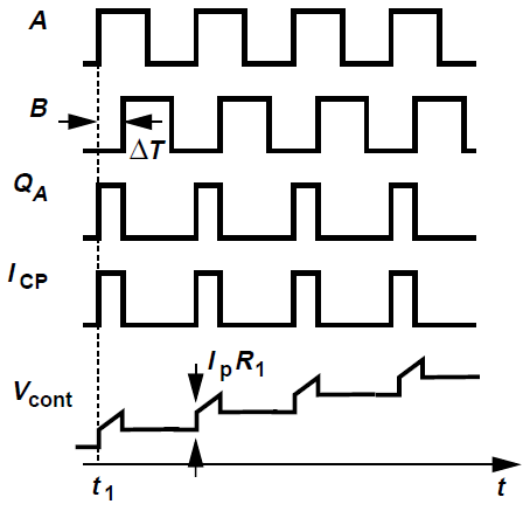
$$H(s) = \frac{I_p K_{VCO}}{2\pi C_1 s^2 + I_p K_{VCO}},$$

$$\frac{I_{CP}}{\Delta\phi}(s) = \frac{I_p}{2\pi}. \quad \textbf{(Equation 1)}$$

- 1/s signifies in the transfer function signifies pole at origin and hence an ideal integrator
- Taking the approximation one step further, we can say that the pole comes from the capacitor only and thus the transfer function of PFD/CP cascade is given by equation 1 above
- Using this we can make a linear phase model given above with open loop transfer function of $[I_p/(2\pi C_1 s)](K_{VCO}/s)$
- The closed loop transfer function is given by H(s) and has two poles which makes loop unstable
- This architecture is called “type-II” PLL since it has two poles at origin due to the two ideal integrators

PFD/CP/Capacitor Transfer Function – III

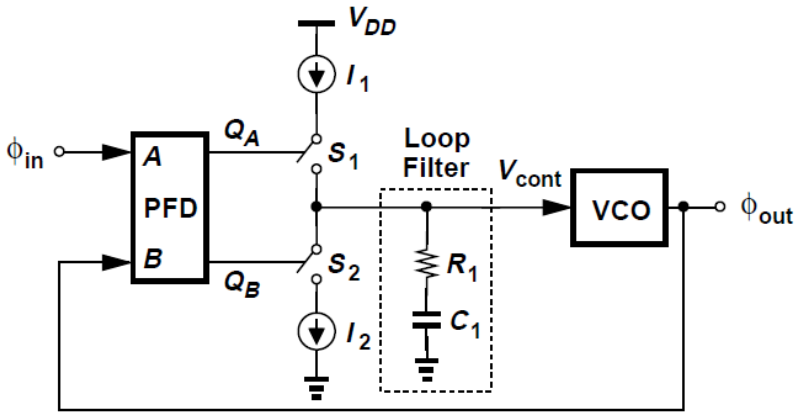




$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_{CP}}{\Delta\phi} \cdot \frac{V_{cont}}{I_{CP}}$$
$$= \frac{I_p}{2\pi}\left(\frac{1}{C_1 s} + R_1\right).$$

- To make the loop stable we can either make one of the integrators lossy or introduce a zero in the loop; we pursue the latter
- A resistor R_1 is placed in series with the capacitor. The control voltage abruptly jumps by I_pR_1 whenever CP turns ON or OFF
- Using the same approximation as before for transfer function of PFD/CP, we get a transfer function as given above. This cascade has a zero as $-1/(R_1C_1)$. The R_1C_1 branch is called “loop filter”

Charge Pump PLL (CPPLL) – I



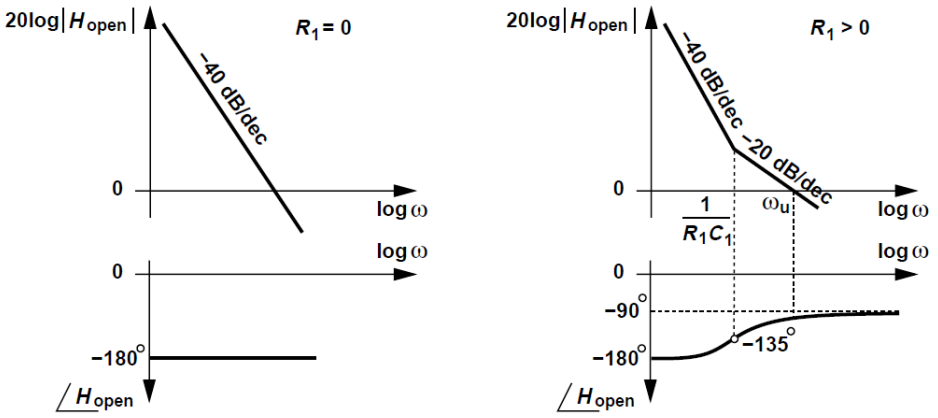
$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}}$$

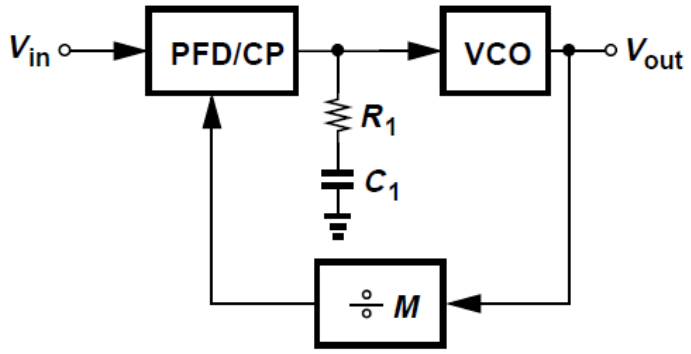
$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi}}.$$

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi} K_{VCO} R_1 s + \frac{I_p K_{VCO}}{2\pi C_1}}.$$

- Phase error of CPPLL is still zero
- Close loop transfer function is given by H(s)
- Thus ω_n and ζ can be obtained
- The system exhibits low pass response (slow phase fluctuations travel to output)
- ζ increases with C_1
- Architecture resolves all drawbacks of type-I PLL
- While changing I_p and K_{VCO} in opposite direction doesn't seem to have an effect on stability, too high K_{VCO} or low I_p can cause problems

Charge Pump PLL (CPPLL) – II





$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1 M}}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi M}}.$$

- Unlike type-I, CPPLL becomes more stable as K_{VCO} increases
- Higher K_{VCO} shifts up magnitude plot while not disturbing phase plot which increases ω_u and PM
- I_p has the same effect suggesting stability worse if $I_p K_{VCO}$ falls
- For a frequency multiplication topology, effective K_{VCO} and hence stability falls
- Value of R_1, I_p, or C_1 needs to be increased to compensate for M factor
- The ω_n and ζ for frequency multiplying CPPLL are given

CPPLL – Phase Margin Calculation

$$\left|\frac{I_p}{2\pi}\left(R_1+\frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}\right|^2_{s=j\omega u}=1.$$

$$\left(\frac{I_p K_{VCO}}{2\pi}\right)^2\frac{R_1^2C_1^2\omega_u^2+1}{C_1^2\omega_u^4}=1.$$

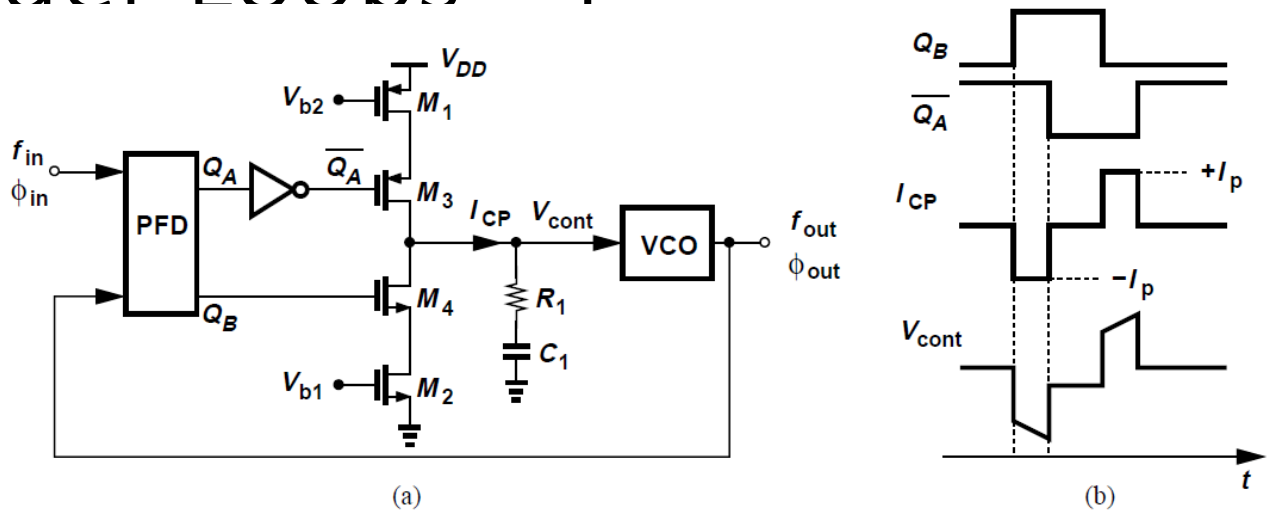
$$\omega_u^4-4\zeta^2\omega_n^2\omega_u^2-\omega_n^4=0.$$

$$\omega_u^2=(2\zeta^2+\sqrt{4\zeta^4+1})\omega_n^2.$$

$$\begin{aligned}\mathrm{PM}&=\tan^{-1}\frac{\omega_u}{\omega_z}\\&=\tan^{-1}(2\zeta\sqrt{2\zeta^2+\sqrt{4\zeta^4+1}}),\end{aligned}$$

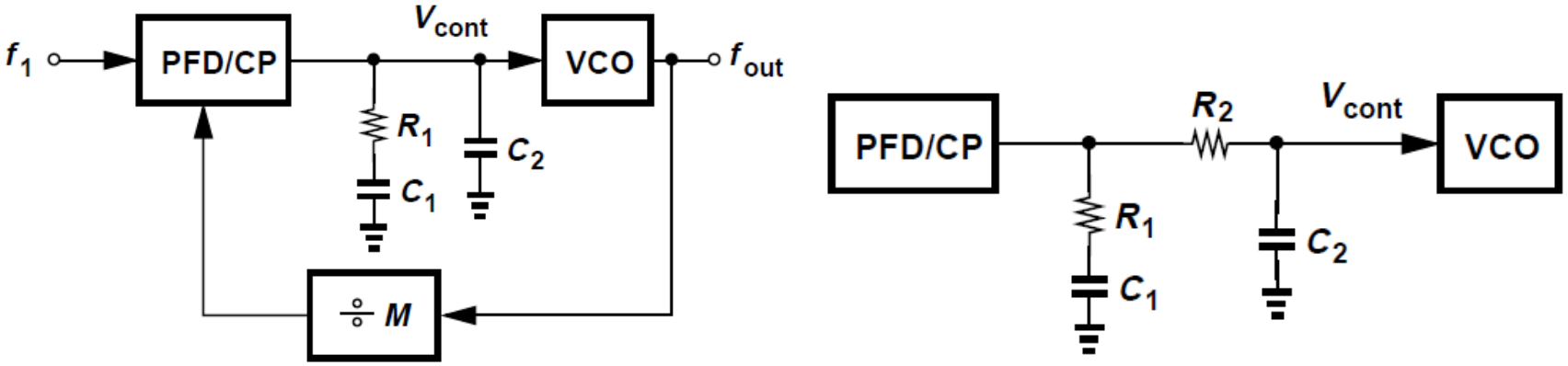
- To calculate phase margin, we need to calculate frequency at which the loop gain falls to unity (ω_u)
- The equations for ω_n and ζ are utilized
- Phase at $\omega = \omega_u$ is given by zero's contribution minus 180^0 (from two poles at origin)
- Note that $\omega_n/\omega_z = 2\zeta$
- For $\zeta > 0.8$, PM = $\tan^{-1} 4\zeta^2$
- If loop contains a divider, $\zeta = (R_1/2)\sqrt{\frac{I_p K_{VCO} C_1}{2\pi M}}$
- Typical case: $\zeta = 1$, PM = 76^0, $\omega_u/\omega_z = 4$; aggressive design: $\zeta = \frac{\sqrt{2}}{2}$, PM = 65^0, $\omega_u/\omega_z = 2.2$

Higher Order Loops – I



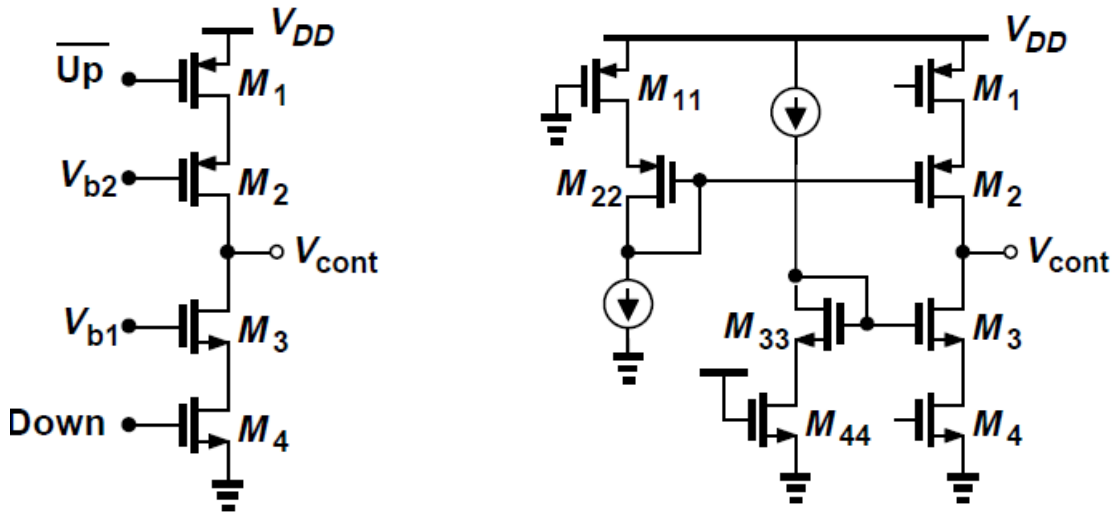
- Due to imperfections, control voltage has significant ripple
- For example if we precede M3 with an inverter to turn it ON when Q_A goes high, M3 turns on and off later than M4: Up and Down pulses have skew
- Late turn ON: negative jump of I_pR_1 and C_1 slightly discharge; turn OFF: positive jump of I_pR_1 and C_1 charges a bit
- Can be eliminated if we interpose a pass gate between PFD and M4
- Violent jumps of the order of 8.18V on control voltage

Higher Order Loop – II



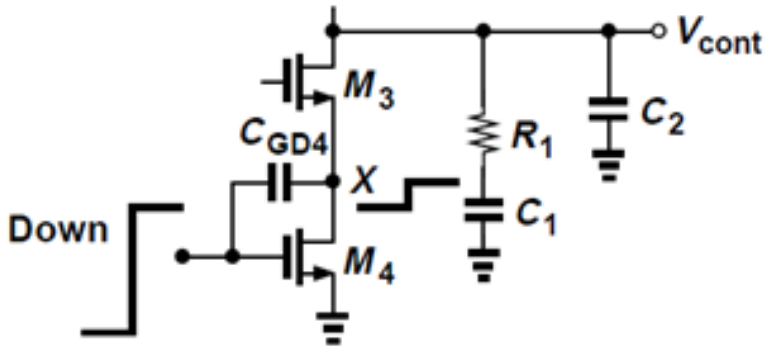
- Simple solution to problem in previous slide is to tie a capacitor between control line and ground
- Initial charge pump current flows through this capacitor reducing the ripple on control voltage
- For up/down skew, peak to peak ripple decreases to $(I_p/C_2)T_{sk}$ which is about 1mV (for same CP current as before)
- C_2 raise the order of the loop to 3 and degrades PM, however, C_2 as large as $0.2C_1$ negligibly affect settling time of the loop
- Topology on right provides similar results. Voltage on R_1 is allowed to jump but the second filter attenuates the ripple

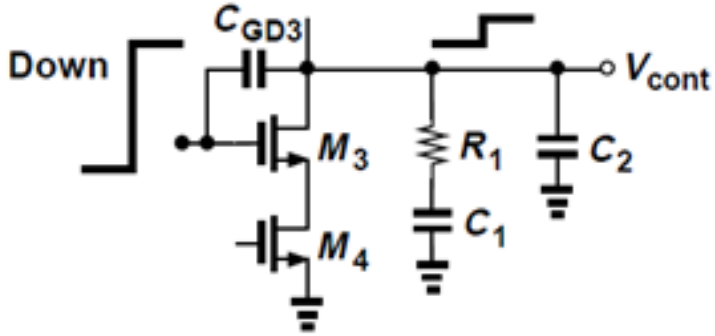
Basic Charge Pump Topologies – Source Switched CP



- M3 and M2 are current sources, M1 and M4 are switches which degenerate the former pair
- V_{b1} and V_{b2} are provided by the current mirror; M44 and M11 emulate the degeneration of M1 and M4
- Due to degeneration, for given voltage headroom, output resistance is higher in this topology

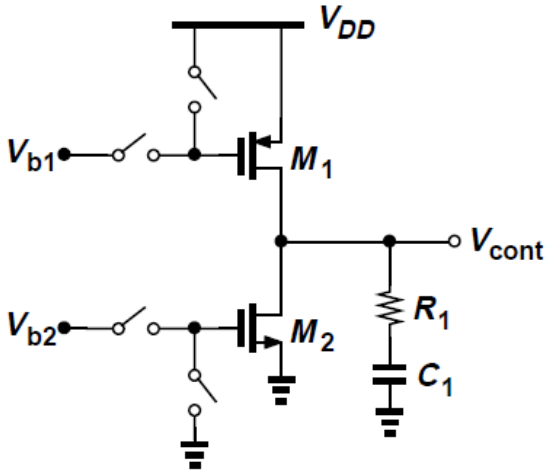
Source Switched CP – Clock Feedthrough

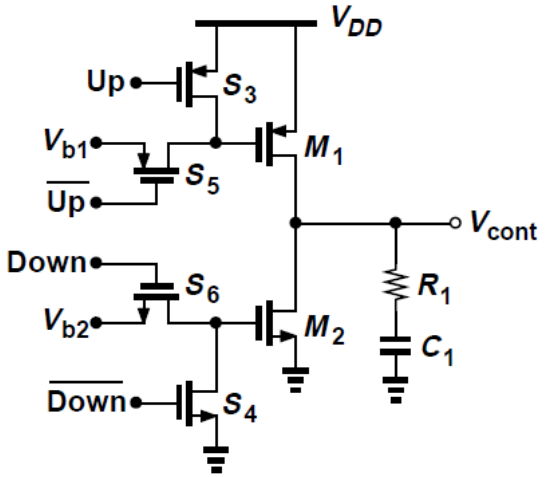




- In drain-switched topology, when Down goes from zero to V_{DD} , C_{GD3} conducts this edge output which makes V_{cont} jump by $V_{DD}C_{GD3}/(C_{GD3}+C_2)$
- In source-switched counterpart, the same transition will only cause node X to jump which in turn cause a jump in I_{D3} and hence no instantaneous jump in V_{cont}
- M3 essentially “shields” the filter from switch clock feedthrough to some extent

Basic Charge Pump Topologies – Gate Switched CP





- Drain and source switched CP face voltage headroom issues due to on-resistance of the switches
- Gate-switched CP topology controls the current sources by connecting their gates to a bias voltage or to their source terminal
- Voltage range is now $V_{DD} - |V_{GS1} - V_{TH1}| - (V_{GS2} - V_{TH2})$
- There is no charge sharing
- Drawback: skew between up and down paths => ripple on V_{cont}
- M1 on when !Up falls to $V_{DD} - |V_{TH1}| - |V_{TH5}|$; M2 on when Down rises to $V_{TH2} + V_{TH6}$ => on time of M1 M2 have significant mismatch in SF and FS corners