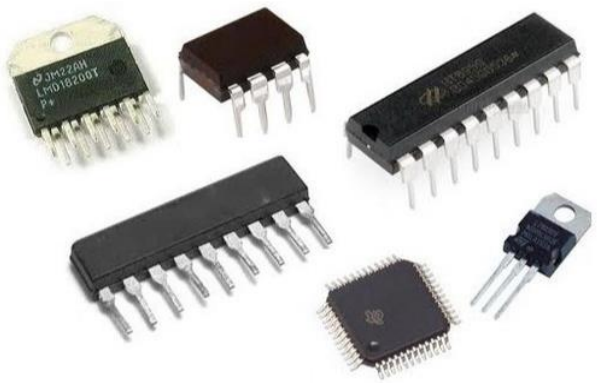
Digital Logic Family

Digital IC:

An Integrated Circuit (IC) is fabricated on a die of a silicon semiconductor crystal, called a chip, containing the electronic components for constructing digital gate. The various gates are interconnected inside the chip to form the required circuit. The chip is mounted in a ceramic or plastic container, and connections are welded to external pins to form the integrated circuit. The number of pins may range from 14 on a small IC package to several thousand on a larger package. Each IC has a numeric designation printed on the surface of the package for identification. Vendors provide data books, catalogs, and Internet websites that contain descriptions and information about the ICs that they manufacture.

Digital ICs are categorized based on

i) Level of integration-
ii) Logic families



1. LEVEL OF INTEGRATION

Digital ICs are often categorized according to the complexity of their circuits, as measured by the number of logic gates in a single package. They are

Small-scale integration (SSI)

- SSI devices contain several independent gates in a single package.
- The inputs and outputs of the gates are connected directly to the pins in the package.
- The number of gates is usually fewer than 10 and is limited by the number of pins available in the IC.

Medium-scale integration (MSI)

- MSI devices have a complexity of approximately 10 to 1,000 gates in a single package.
- They usually perform specific elementary digital operations.
- MSI digital functions aredecoders, adders, and multiplexers, registers and counters.

Large-scale integration (LSI)

- LSI devices contain thousands of gates in a single package.
- They include digital systems such as processors, memory chips, and programmable logicdevices.

Very large-scale integration (VLSI)

- VLSI devices now contain millions of gates within a single package.
- Examples are large memory arrays and complex microcomputer chips.

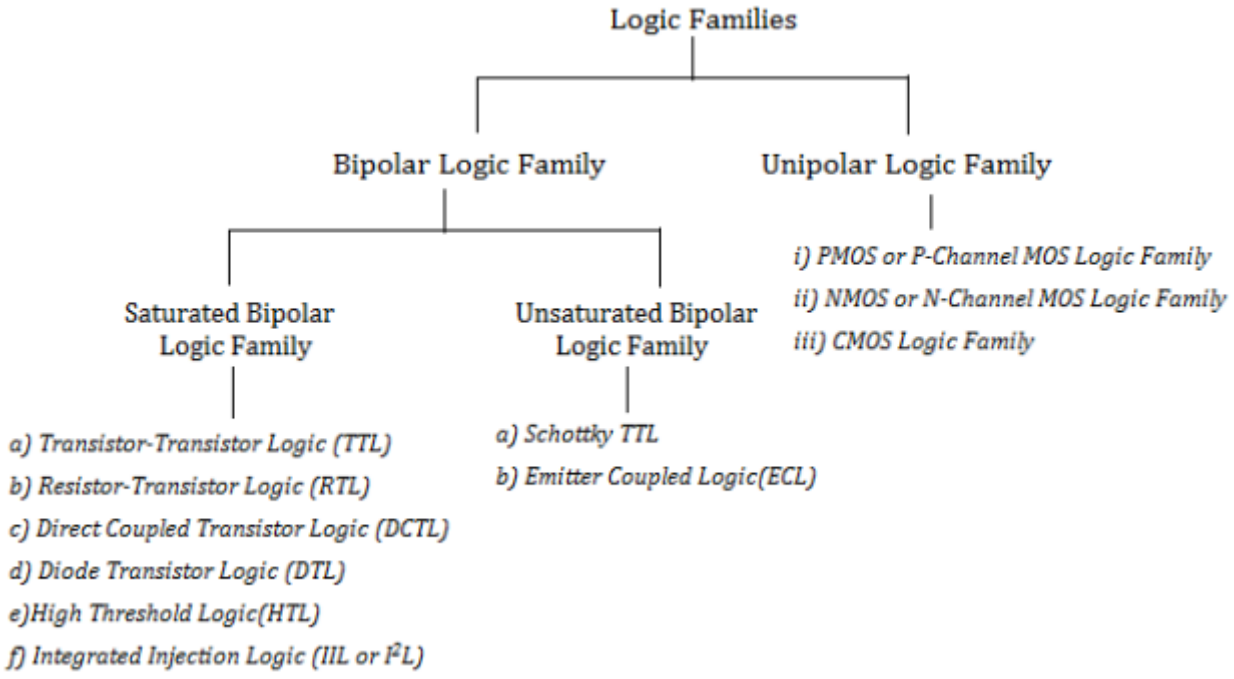
Ultra-large-scale integration (ULSI)

- ULSI devices now contain more than 1 million electronic components per chip.
- The Intel 486 and Pentium microprocessors use ULSI technology.

Name	Signification	Year	Transistors number	Logic gates number
SSI	*small-scale integration*	1964	1 to 10	1 to 12
MSI	*medium-scale integration*	1968	10 to 500	13 to 99
LSI	*large-scale integration*	1971	500 to 20,000	100 to 9,999
VLSI	*very large-scale integration*	1980	20,000 to 1,000,000	10,000 to 99,999
ULSI	*ultra-large-scale integration*	1984	1,000,000 and more	100,000 and more

2. Logic family

A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using specific circuit configuration which is referred to as logic family.



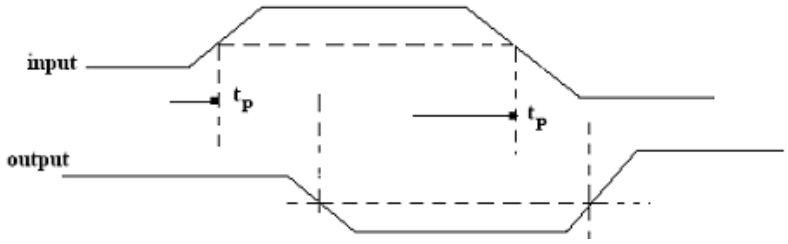
Characteristics of Digital IC's

The above classification of digital IC's is based on the complexity of the circuit. Some of the important characteristics or parameters are gives as follows

1. Speed of operation
2. Power dissipation
3. Figure of merit
4. Fan out
5. Fan in
6. Current and voltage parameter
7. Noise immunity
8. Operating temperature range

Characteristics of Digital Integrated Circuits

1. Speed of operation: The Speed of operation of a digital circuit is given in terms of the propagation delay time. The input delay times and output delay times can be demonstrated as:



The delay times are measured in between the 50% voltage levels of input and output wave forms. Here two delay times those are t, while the output goes from the high state to low state and t_{phl}, while output goes from low state to high state.

2. Power Dissipation: It is the amount of power dissipated in an IC. It is determined through the current, I_{CC} that this draws from the V_{cc} supply and is provided by V_{cc} x I_{cc}. I_{cc} is the average value of I_{CC} [O] and I_{CC} [1]. This is specified in mW.

3. Figure of merit: For digital IC, this is explained as the product of speed and power. This is specified in Pico joules i.e. ns x mw= pj. The low value of speed power product is required.

4. Fan Out: Fan out is the number of load gates connected to the output of the driving gate. High fan out is beneficial, as this reduces the requirement for additional drivers to drive more gates.

5. Fan in: Fan in is the number of inputs connected to the gate without any degradation in the voltage level.

6. Current and Voltage Parameter:

V_{IH}: HIGH-state input voltage, corresponding to logic 1 at input

V_{IL}: LOW-state input voltage, corresponding to logic 0 at input

V_{OH}: HIGH-state output voltage, corresponding to logic 1 at output

V_{OL}: LOW-state output voltage, corresponding to logic 0 at output

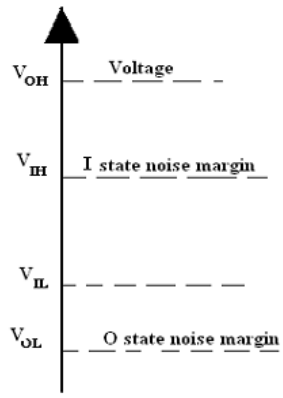
I_{IH}: HIGH-state input current; current flowing from input when the input voltage corresponds to logic 1.

I_{IL}: LOW-state input current; current flowing from an input when the input voltage corresponds to logic 0.

I_{OH}: HIGH-state output current; current flowing from output when the output voltage corresponds to logic 1.

I_{OL}: LOW-state output current; current flowing from an output when the output voltage corresponds to logic 0.

7. Noise Immunity/ Noise Margin: Stray electric and magnetic fields make unnecessary voltages termed as noise, on the connecting wires in between logic circuits. It may cause the voltage at the input to a logic circuit to drop below V_{ih} or fuse above V_{il} and may generate unwanted operation. The circuit's capability to tolerate noise signals is termed to as the noise immunity.



8. Operating Temperature: A range of temperature wherein an IC functions properly should be identified. The accepted temperature range for consumer IC' s are from 0 to 70 degree C and for industrial applications [from -55° C to +125° C for military applications].

9. Power supply requirements:
The supply voltage and the amount of power required by an IC are important characteristics required to choose the proper power supply.

10. Flexibilities Available: various flexibilities are available in different IC logic families and these must be considered while selecting a logic family for a particular job. Some of the flexibilities available are:

i. Wire-logic Capability: Connection of gate output terminals together or using them directly to perform additional logic functions without any extra hardware.

ii. Availability of Complement Outputs: This eliminates the need for additional inverters.

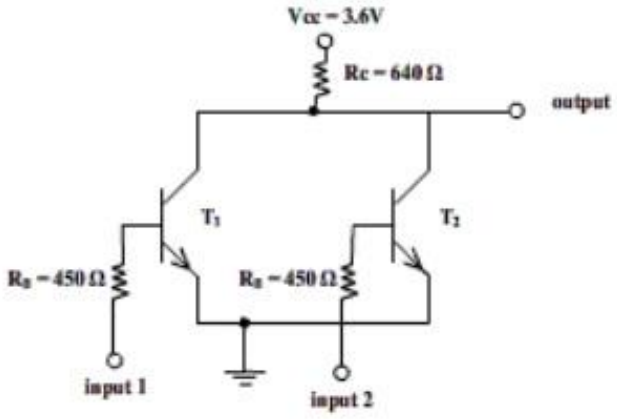
iii. Breadth of Series: Types of different logic functions available in the series.

iv. Popularity of Series: The cost of manufacturing depends upon the number of ICs manufactured. When the ICs are manufactured in a large number the cost per function is reduced and it will be easily available because of multiple resources.

v. Input-Output Facilities: The number of input terminals of a gate and its input/output impedance's in both 0 and 1 states are important. former governs the fan-in and the later its fan-out. For high fan-out, the gates have low output impedance for both 0 and 1.

No single logic configuration gives the best results for all circuit applications. Table 1 gives a comparison of major IC digital logic families.

Resistor-Transistor Logic (RTL) family

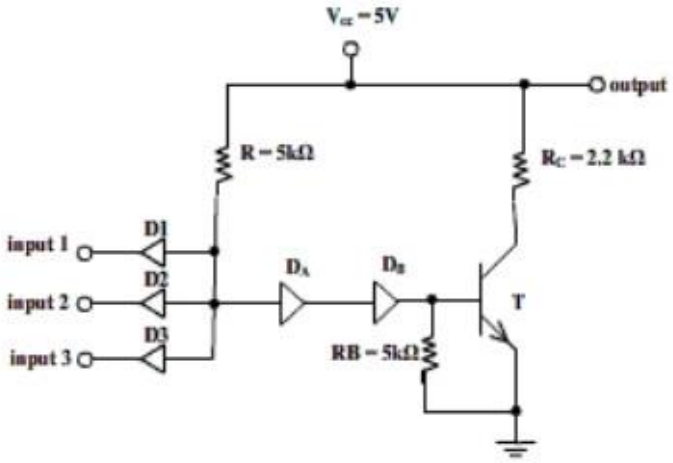


- The resistor-transistor logic, also termed as RTL, was most popular kind of logic before the invention of IC fabrication technologies.
- As its name suggests, RTL circuits mainly consists of resistors and transistors that comprises RTL devices.
- The basic RTL device is a NOR gate, shown in figure aside.
- Inputs to the NOR gate shown above are 'input1' & 'input2'. The inputs applied at these terminals represent either logic level HIGH (1) or LOW (0).
- The logic level LOW is the voltage that drives corresponding transistor in cut-off region, while logic level HIGH drives it into saturation region.
- If both the inputs are LOW, then both the transistors are in cut-off i.e. they are turned-off. Thus, voltage Vcc appears at output I.e. HIGH.
- If either transistor or both of them are applied HIGH input, the voltage Vcc drops across Rc and output is LOW.
- RTL family is characterized by poor noise margin, poor fan-out capability, low speed and high-power dissipation. Due to these undesirable characteristics, this family is now obsolete.

Limitations

When the transistor is switched on, the power dissipation increases as the current flows through base and collector. Also, the RTL gate has poor noise margin, poor fan-out and the propagation delay is more.

Diode-Transistor Logic (DTL) family



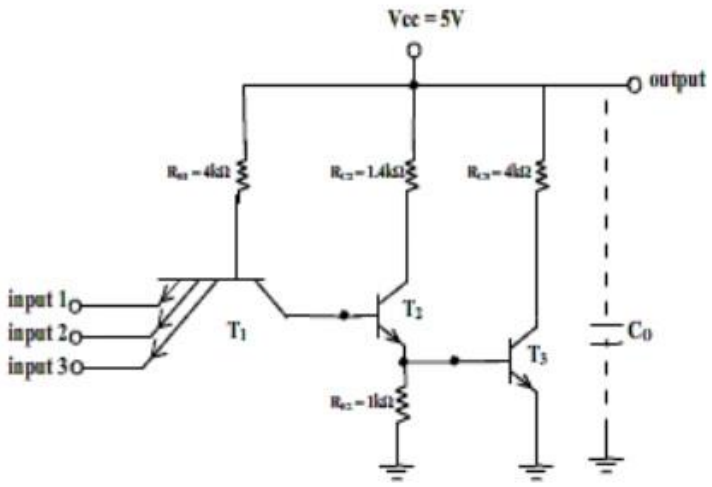
- The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin.
- As its name suggests, DTL circuits mainly consists of diodes and transistors that comprises DTL devices.
- The basic DTL device is a NAND gate, shown aside.
- Three inputs to the gate are applied through three diodes viz. D1, D2 and D3. The diode will conduct only when corresponding input is LOW.
- If any of the diode is conducting i.e. when at least one input is LOW, the voltage at cathode of didoe DA is such that it keeps transistor T in cut-off and subsequently, output of transistor is HIGH.
- If all inputs are HIGH, all diodes are non-conducting, transistor T is in saturation, and its output is LOW.

Advantages

It has better advantages than RTL Logic. The Diode Transistor Logic has improved noise margin, greater fan-out. However, the propagation delay is more for this device, when compared to Transistor-transistor logic(TTL). But the speed is better than RTL.

Transistor-Transistor Logic (TTL) family

- TTL family is a modification to the DTL. It has come to existence so as to overcome the speed limitations of DTL family. The basic gate of this family is TTL NAND gate.
- Modifications to DTL NAND-
- The diodes D1, D2 and D3 are replaced by emitter-base junctions of a multiple-emitter transistor labeled T1.
- Diode DA is replaced by collector-base junction of T1.
- Diode DB is replaced by emitter-base junction of transistor labeled T2.
- The working of this circuit is identical to that of DTL circuit.
- When at least one input is logic LOW, transistor T2 and T3 are in cut-off and hence, output of T3 is HIGH.
- When all inputs are HIGH, T1 operates in active inverse mode, driving T2 & T3 in saturation. Since T3 is ON, the output is LOW.
- While all inputs are HIGH, if any of the inputs suddenly goes LOW, then T2 and T3 will be turned off only when stored base charge is removed. The collector-base junction of T1 is back-biased and T1 operates in normal active region. A large collector current of T1 is in such direction that it helps removing base charge of T2 and T3. In this way, the circuit speed is increased in TTL over speed of DTL.



Advantages

- High-speed operation. The propagation delay is around 10 ms, which is fast compared to DTL and RTL logic devices.
- Less power dissipation compared to DTL and RTL.
- Low cost
- Better fan-out
- Reliable operation for noise.

Emitter Coupled Logic (ECL) family

In following circuit is shown in Fig. 5 is an ECL circuit, you'll see the transistor Q_A, Q_B and Q_2 two will form a differential amplifier. And the operation of this logic circuit will be depending upon the operation of our differential amplifier. Here you see the immediate terminal of transistor Q_2. Q_A and Q_B are coupled or connected together. Therefore, this will be known as Emitter coupled Logic and with -5.2 Volts. Terminal a fixed amount of current will flow through the resistor of 1 k-ohm and that current will be denoted as I_E. And the value of I_E will be more or less constant and it will be around 3 mA. Therefore, in some issue circuit, you'll see, this is replaced by an independent current source. The Fixed Current I_E is allowed to flow through the collective terminal of the transistor Q_A, Q_B and Q_2, depending upon the logical input at this terminal or this terminal. For logic 1 the amount of voltage is -1.7 v and for logic 0 the amount of voltage is 0.8 V. Now, let's say the current that is flowing through this transistor Q_B is I_B. The collector current of the transistor Q_A equal to I_A and the collector current of the transistor Q_2 is I_2. Therefore, if I apply KCL at this terminal, you'll see summation of incoming currents. I_A plus I_B plus I_2 will be equal to our I_E. The transistor Q_A Q_B and Q_2 will form our differential amplifier. And the transistor Q_3 and Q_4 four will form our Emitter follow circuit. Now see as our input will be at logic Zero. And this will be at logic Zero. Therefore, our transistor Q_A and Q_B will be in off state or in cut off mode. So when the transistor Q_A and Q_B will be in cut off Mode, their collector and emitter terminals will act like open switch.

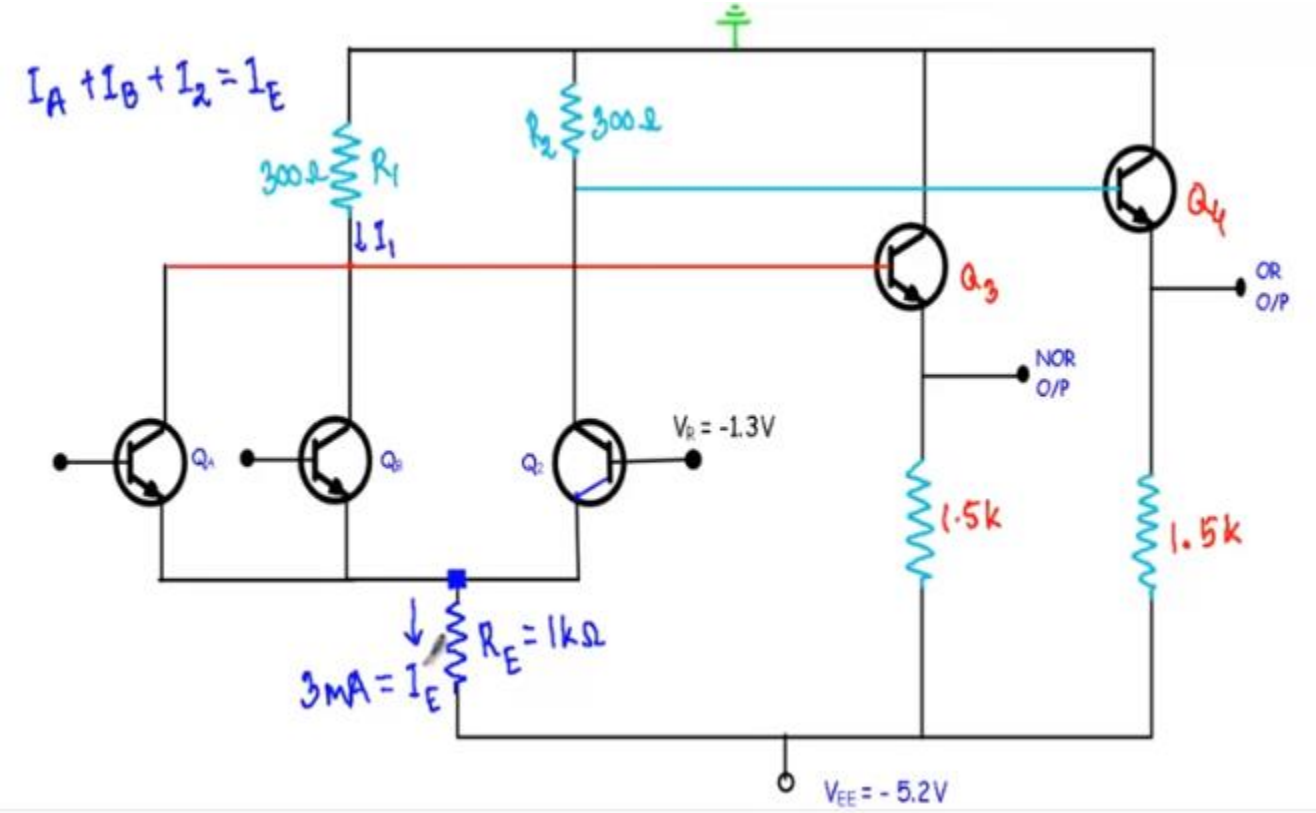


Fig. 5

Therefore, I can disconnect the collector and emitter terminals from the given network. As a result, you will see the collector current of the transistor Q_A, which is I_A will be equal to Zero. And the Collector current of the transistor Q_B will be equal to zero. Here it seems that the $I_A+I_B= I$. One should be the Sum of collector current I_A and I_B. Therefore, it will be equal to Zero. That means there will be no current flow through the register R_1. As the I_1 is equal to zero. You'll see from this terminal to this terminal voltage $I_1R_1 = 0$, so there is no voltage drop from this terminal to this terminal here I am applying -5.2 volts between this terminal to this ground terminal.

That means we are supplying a voltage source whose value is 5.2 volts, whose positive terminal is connected here. And the negative terminal is connected here. See from this terminal to this terminal as the voltage is equal to 0. Therefore, the 5.2 volts will be appeared between this terminal to this terminal here you will see this 5.2 v will be absorbed by the base Two inverter junction of the Transistor Q_3 and the 1.5 Kohm Resistor. As the base terminal of the transistor Q_3 will have a voltage of 5.2 volts. Therefore, I can expect that the transistor Q_3 will be in active region. Because in a circuit, our transistor will never saturate. Therefore, I can expect a base to imitate junction drop greater than 0.7 volts, which will be, let's say 0.8 volts between this terminal to this terminal. And the rest of the 4.4 volts will be absorbed by the 1.5 Kohm resistor from this terminal to this terminal I will get -4.4 and from this terminal to this terminal I will get 0.8 volt. And from this terminal to this terminal, I will get 0 volt. so -5.2 volts. The voltage at the terminal Q_3 is = -0.8v – 0v = -0.8v which means logic 1. So it works like NOR gate (A=0, B=0, Y=1). As our transistor Q_A and Q_B are in off state, our transistor Q_2 will be in active region. When the transistor Q_2 will be in active region, I will get the collector current through the collector terminal of the transistor Q_2. And here I will use the collector current I_2 and the inverter current of the transistor Q_2 synonymously. Because in a bipolar transistor collector current I_C should be nearly equal to our Emitter current I_E. Therefore, you will see this I_E will flow through the collector terminal of the transistor Q_2. And this same I_E will flow through the I_2 will be entering from this direction. Here the I_E, which is equal to 3mA, will flow through the collector terminal of the transistor Q_2. Therefore, our emitter current I_E should be Equal to Our collector current I_2, which is equal to 3mA. Therefore, I will get a voltage drop. I_2R_2 = (3mA*300 ohm) = 0.9 V. So here I will get 0.9 volts between this terminal to the terminal. Therefore, the rest of the 4.3 volts voltage will be the voltage between this terminal to this ground terminal. So I can say that the base terminal of the transistor Q_4 will be at a Voltage of 4.3 volts, which is sufficient to drive the transistor Q_4 in the active region. So when the transistor Q_4 will be in active region, its collector and immediate terminal is based on embedded junction. Drop will be 0.8 volts and the rest of the 3.50 v. So the collector voltage at Q4 is = 0.8V – 0.9V = -1.7 V = logic 0. So it works like OR gate (A=0, B=0, Y=0). Similarly, other functions of OR and NOR gate can be shown with ECL circuit.

Advantages

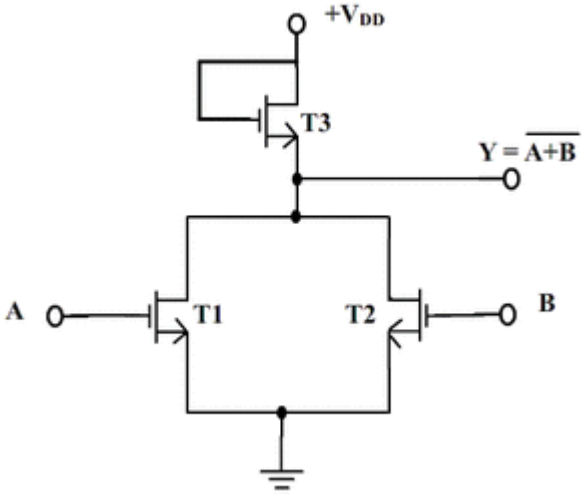
- High-speed operation is possible and so the fastest logic family.
- Since transistors are not allowed to enter into saturation, which reduces the storage delay.
- Fan-out capability is high.

Apart from the advantages, it also has its own disadvantage. For the fast switching of transistors, the low and high logic levels are kept close. It reduces the noise margin. Since transistors are not allowed to enter into saturation, the power consumption is more.

MOS Logic family

NOR Gate

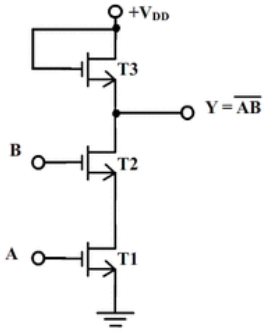
- MOS logic family implements the logic gates using MOSFET devices. MOSFETs are high density devices which can easily and economically fabricated on ICs. MOS logic gates can be fabricated using either only NMOS or only PMOS devices.
- MOS logic is vastly used in LSI and VLSI devices, such as microprocessor chips, due to their high-density characteristic. NMOS NOR gate is shown in figure.



NOR Gate

NAND Gate

- If both transistors T1 and T2 are off i.e. A = B = LOW, then output is HIGH = VDD.
- If either of the inputs is HIGH, then corresponding transistor(s) is/are ON, thus connecting output to GND i.e. LOW.



NAND Gate

- If both inputs are ON, then only both T1 and T2 are ON and output is LOW; otherwise (when either or both transistors are OFF,) the output is HIGH. This is NAND operation on applied inputs.

Limitation of MOS devices

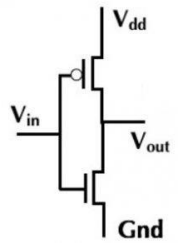
If any of input of MOS is left unconnected, the open input terminal which has very high input impedance may take any stray electric charge as input and can develop extreme dangerous high voltage which can damage the device and may also harm the person handling the device.
Thus, none of the un-used inputs of MOS device should be left unconnected. It must connect to ground or supply. Even for storage of device, all pins must be shorted.

CMOS Logic family

CMOS stands for complementary-MOS, in which both p-channel and n-channel enhancement MOSFET devices are fabricated on same chip. This causes density to be reduced and complex fabrication process. However, CMOS devices consume negligible power and hence are preferred over MOS devices in battery operated applications.

CMOS Inverter

- The inverter circuit as shown in the figure below. It consists of PMOS and NMOS FET. The input A serves as the gate voltage for both transistors.
- The NMOS transistor has input from V_{ss} (ground) and the PMOS transistor has input from Vdd. The terminal Y is output. When a high voltage (~ V_{dd}) is given at input terminal (A) of the inverter, the PMOS becomes an open circuit, and NMOS switched OFF so the output will be pulled down to Vss.



CMOS Inverter

- When a low-level voltage (<V_{dd}, 0v) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes V_{dd} or the circuit is pulled up to V_{dd}.

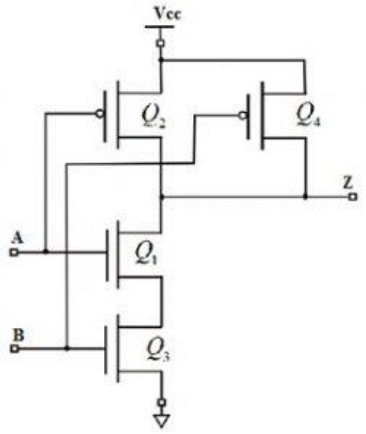
INPUT	LOGIC INPUT	OUTPUT	LOGIC OUTPUT
0 v	0	V_{dd}	1
V_{dd}	1	0 v	0

CMOS Logic family

CMOS NAND Gate

- The below figure shows a 2-input Complementary MOS NAND gate. It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and VDD.

- If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.



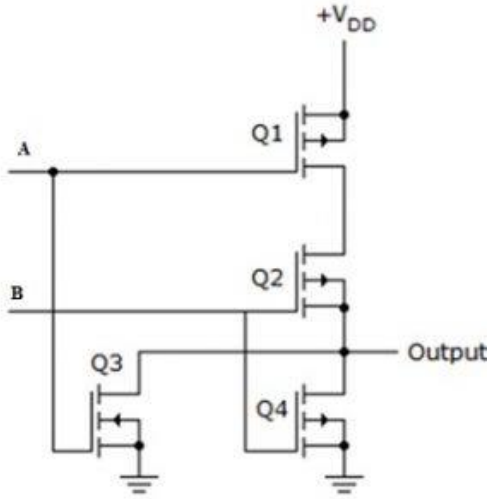
Two Input NAND Gate

- Hence, the output Y will be high. If both inputs are high, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be logic low. The truth table of the NAND logic gate given in the below table.

A	B	Pull-Down Network	Pull-up Network	OUTPUT Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

CMOS NOR Gate

A 2-input NOR gate is shown in the figure below. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in the below table. The output is never left floating.



Two Input NOR Gate

The truth table of the NOR logic gate given in the below table.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

CMOS Applications

Complementary MOS processes were widely implemented and have fundamentally replaced NMOS and bipolar processes for nearly all digital logic applications. CMOS technology has been used for the following digital IC designs.

- Computer memories, CPUs
- Microprocessor designs
- Flash memory chip designing
- Used to design application-specific integrated circuits (ASICs)

Table 1: Comparison of Main IC Digital Logic Families

S.N.	Parameter	DTL	HTL	TTL	RTL	ECL	MOS	CMOS
1.	Basic Gates (Positive Logic)	NAND	NAND	NAND	NOR	OR-NOR	NAND	NOR or NAND
2.	Fan out (Minimum)	8	10	10	5	24	20	>50
3.	Typical power dissipation per gate, mW	8-12	55	12-22	12	40-55	0.2-10	0.01 static 1 at 3 MHz
4.	Noise immunity	Good	Excellent	Very good	Medium	Good	Medium	Very good
5.	Typical propagation delay/gate, ns	30	90	12-6	12	4-1	300	70
6.	Clock rate (minimum frequency at which flip-flops operate), MHZ	12-30	4	15-60	8	60-400	2	5
7.	Number of functions	Fairy High	Medium	Very high	high	High	Low	Low

Some Questions

1. What is logic family? Write down the names of logic families.
2. Write down the classification of digital ICs in terms of the level of integration.
3. What are the important characteristics of digital ICs?
4. Explain the following characteristics of digital IC:

   (i) Noise immunity.
   (ii) Figure of merit.
   (iii) Speed of operation
   (iv) Fan-Out
   (v) Fan-In
   (vi) Power Dissipation

4. Draw the circuit diagram of a 3-input DTL basic gate and describe its function.
5. Draw the circuit diagram of RTL basic gate and describe its function.
6. Draw the circuit diagram of ECL basic gate and describe its function.
7. Draw the logic circuit and explain the operation of 2-input NMOS Inverter, NAND and NOR gates.
8. Draw the logic circuit and explain the operation of 2-input CMOS Inverter, NAND and NOR gates.