FR. CONCEICAO RODRIGUES COLLEGE OF ENGINEERING, BANDRA

CSC304: DIGITAL LOGIC AND COMPUTER ORGANIZATION AND ARCHITECTURE

SE COMPUTERS- B SEMESTER-III DATE: 19/11/2020

QUESTION BANK FOR TEST 2

Q.1. Differentiate between DRAM and SRAM
Note: (Refer CSC304:DL&COA Lecture 51 in Google Classroom) for Q.1

Q.2. Demonstrate the advantages of pipelining and explain various types of pipeline hazards and their solutions. Give examples

Note: (Refer CSC304:DL&COA Lecture 63 in Google Classroom) for Q.2

Q.3. Explain cache memory mapping techniques with an example
Note: (Refer CSC304:DL&COA Lecture 62 in Google Classroom) for Q.3

Q.4. Explain in detail hardwired control. Discuss state table method to implement it.
Note: (Refer CSC304:DL&COA Lecture 43 and Lecture 45 in Google Classroom) for Q.4

Q.5. Explain Flynn's classification for parallel processing systems.
Note: (Refer CSC304:DL&COA Lecture 62 in Google Classroom) for Q.5

Q.6. Draw and explain microprogrammed control unit
Note: (Refer CSC304:DL&COA Lecture47&48&49in Google Classroom) for Q. 6

Q.7. Consider a 4-way set associative cache mapping with cache block size=16bytes, Cache size= 8k, Main memory=64k. Design a cache structure and show how the processor address is interpreted.
Note: (Refer CSC304_DL&COA_Lecture59 in Google Classroom) for Q. 7

Q. 8. Expalin different types of RAM and ROM in detail.
Note: (Refer CSC304:DL&COA Lecture 51 in Google Classroom) for Q.8

Q. 9. Differentiate RAM and ROM
Note: (Refer CSC304:DL&COA Lecture 18 in Google Classroom) for Q. 8and Q.9.

Q. 10. For the following Program identify the Hazards

MOV (R5),R6

ADD R7,(R5)

Give the solution to eliminate the above identified Hazards.
Note: (Refer CSC304:DL&COA Lecture 63 in Google Classroom) for Q. 10

Q.11. Consider a Direct cache mapping with cache block size=16bytes, Cache size= 8k, Main memory=64k. Design a cache structure and show how the processor address is interpreted
Note: (Refer CSC304_DL&COA_Lecture55 in Google Classroom) for Q. 11

Q. 12. Consider a associative cache mapping with cache block size=16bytes, Cache size= 8k, Main memory=64k. Design a cache structure and show how the processor address is interpreted
Note:(Refer CSC304_DL&COA_Lecture58 in Google Classroom) for Q. 12

Q.13. write a note on
1. Types of Register
2. Instruction cycle
3. Instruction format.
4. Memory Hierarchy

Q.14. What is addressing modes? Explain different addressing modes
Note: (Refer CSC304_DL&COA_Lecture 42_AddressingModes)

Q.15. Draw and explain block diagram of the microprogram sequencer

Note:(Refer CSC304_DL&COA_Lecture47&48&49)