BCD to 7-Segment Display

In computing and electronic systems, binary-coded decimal (BCD) is used to encode decimal numbers (base-10 numbers) in a binary form where each decimal digit is represented by a nibble (4 bits).

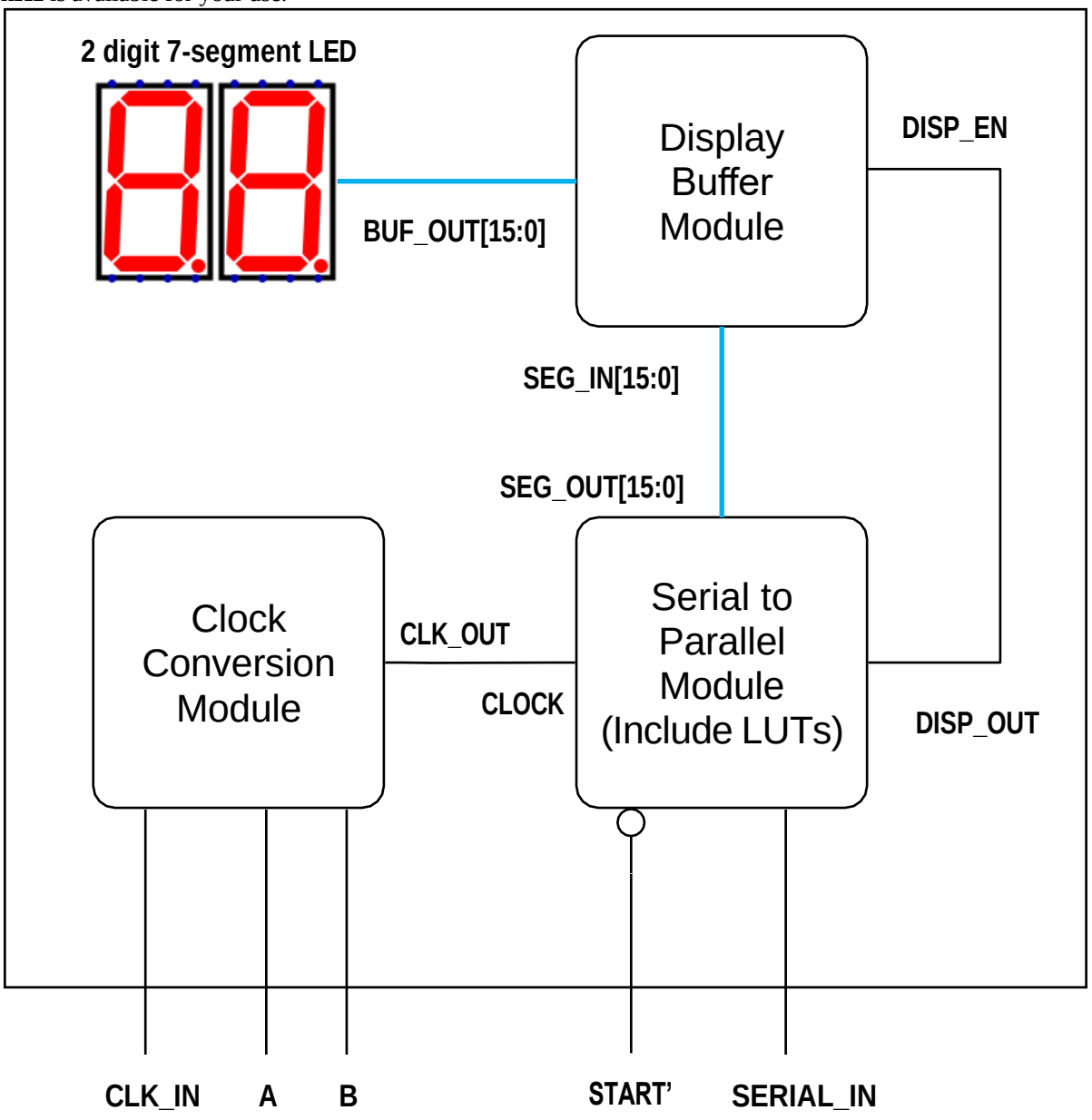
For instance, decimal number 5 is represented as 0101 in BCD as 5 = 4 + 1.

A lot of electronic devices use 7-segment displays (Watch, alarm clock, calculator etc.).

Typically 7-segment displays consist of seven individual coloured LED's (called the segments). Each segment can be turned on or off to create a unique pattern/combination.

Description

A 2 digit 7-Segment LED Display system is controlled via a 2-wire serial line connection from a separate location (see Figure below). To update the Display, an active low START' signal is asserted (LOW level). Starting on the next rising clock edge, the serial data will be received via the input SERIAL_IN. If the START' signal is de-activated (HIGH level) at any time during the data transfer, the system will reset and ignore any inputs until the START' signal is asserted again (LOW level). Assume that the serial communications uses TTL signal levels (no need to deal with voltage level conversions), and an existing clock signal **CLK_IN operating at 800 kHz** is available for your use.



The serial data is sent as a two Binary Coded Decimal (BCD) digits, with the most significant digit sent first. The bits for each digit are sent most significant bit first, for a total of 8 transmitted bits, without any additional data framing bits.

For example, to send the two BCD digits 29, the bit stream will be transmitted as '00101001'.

In order to support reliable connections across a variety of distances, the serial connection can operate at 4 different clock frequencies, selected using 2 control signals A and B, as shown in the table below:

A	B	CLK_OUT Frequency
0	0	400 kHz
0	1	200 kHz
1	0	100 kHz
1	1	50 kHz

The display system can be broken down into the following modules:

- Display Buffer Module
- Serial to Parallel Data Module
- Clock Conversion Module

Requirements

1. Derive the Look Up Table output for the LED segment bit-pattern to display the symbols for 0-9 on the 7-segment LED, given that the LUT input is a 4-bit BCD digit.
   i.e., input is 4-bit BCD, output is 8-bit LED bit-pattern. Illegal BCD digits will display dot '.'
   e.g., to display BCD digit 1, input is '0001', output is segment b and c, which is '00000110'

Input (D3 D2 D1 D0)	Output (dp g f e d c b a)
0000	00111111
0001	00000110
…	…

2. Design the Display Buffer Module which consist of 16 input signals SEG_IN[15:0] which accepts the 7-segment bit pattern values as input, and buffers it for output via BUF_OUT[15:0]. It is assumed that the input values will be present only for one clock cycle, and will therefore need to be latched using an input control signal DISP_EN.
3. Design the Serial to Parallel Data Module, which accepts serial data on SERIAL_IN, clocked using CLOCK, to accept two 4-bit BCD digits received via SERIAL_IN, and output it as 8-bits in

parallel to 2 4-bit LUTs. The 8-bit outputs of each LUT will be used to generate the 16-bit pattern SEG_OUT [15:0] which will be connected to SEG_IN[15:0] on the Display module. In addition, an output signal DISP_OUT will be generated to latch the output to the Display module. (DISP_OUT is connected to DISP_EN). The module is activated when START' is asserted (LOW level), and reset when START' is HIGH.

4. Design the Clock Conversion Module, which accepts the inputs A, B, and CLK_IN, to generate the appropriate clock frequency for CLK_OUT, to be used to drive the Serial to Parallel Data Module CLOCK signal.
5. Combine all the modules into a complete system, which consists of two 7-Segment display devices and the respective modules, which accepts the signals CLK_IN, START', A, B, and SERIAL_IN, to initialize the Display system to accept input from SERIAL_IN based on the specified clock rate via A&B.
6. Generate a Test Case, to send the digits '97' to be displayed on the Display system using a clock rate of 200 kHz. Include the Timing Diagram output of the test case in your report.

You may make use of any relevant devices available in the Digital simulator for this assignment. Each of the three modules should be saved in its *own.dig* circuit file together with a test case to illustrate each module's operation on its own. The overall system circuit file should include the various modules as custom devices. The overall system circuit file should also contain the test case to display '97' on the 7-segment LED. The input on SERIAL_IN will therefore be '10010111' which is 97 in BCD format.

Reporting

Submit a Group report in PDF format documenting each of the item listed above, including the circuit diagram and test case timing diagram for each circuit modules, and upload the *.dig* circuit files together with your report.

Please remember to indicate information about the group members in the first page of the report.

Warning: Any copying or plagiarism will be given 0 marks.

Grading Rubric for Assignment 2 (Each Item in List)

Partial marks may be given for each item based on level of completion of the specified requirements.

1. 20 marks
2. 20 marks
3. 30 marks
4. 10 marks
5. 10 marks
6. 10 marks