CST236- Digital System Design

SCHOOL OF COMPUTER SCIENCE

UNIVERSITI SAINS MALAYSIA

SEMESTER II 2022/2023

ASSIGNMENT 2		
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SUBMISSION DATE	29/06/2023
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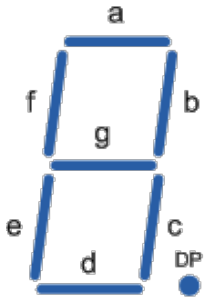
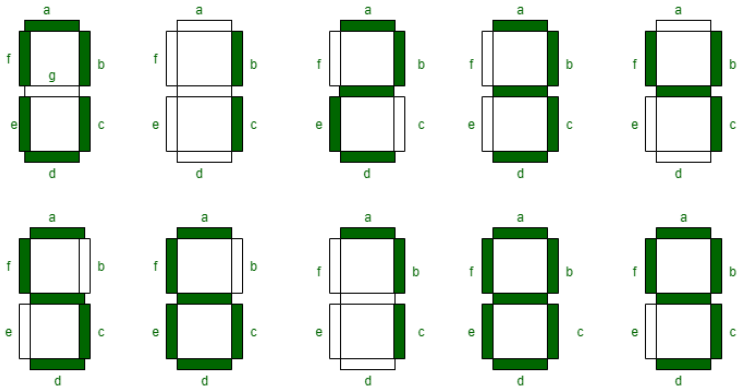
TOTAL MARK	**/100**

1. For the entire assignment, we will use this diagram as a reference for the label for each segment.



https://www.electronics-tutorials.ws/combination/comb_6.html



https://www.geeksforgeeks.org/seven-segment-displays/

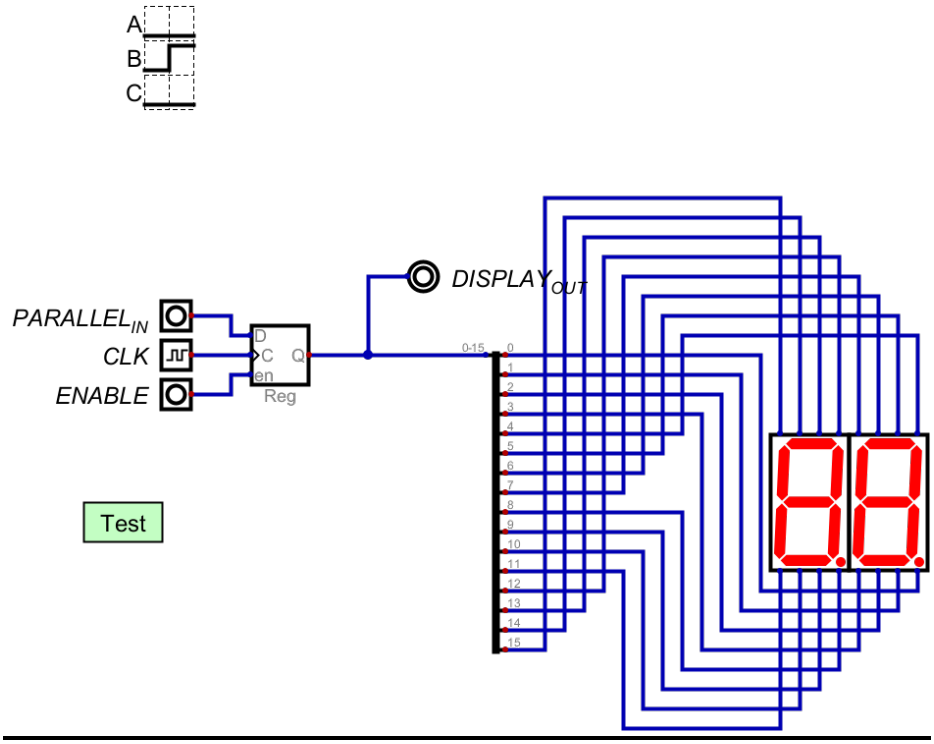
Based on the diagram above, we know which should be light up to display a specific digit. Based on this, we can derive the Look Up Table as below:

Decimal number	BCD input				Output							
	D3	D2	D1	D0	a	b	c	d	e	f	g	dp
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1	0
3	0	0	1	1	1	1	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0	0	1	1	0
5	0	1	0	1	1	0	1	1	0	1	1	0
6	0	1	1	0	1	0	1	1	1	1	1	0
7	0	1	1	1	1	1	1	0	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1	0
9	1	0	0	1	1	1	1	1	0	1	1	0
10	1	0	1	0	**INVALID**							**1**
11	1	0	1	1	**INVALID**							**1**
12	1	1	0	0	**INVALID**							**1**
13	1	1	0	1	**INVALID**							**1**
14	1	1	1	0	**INVALID**							**1**
15	1	1	1	1	**INVALID**							**1**

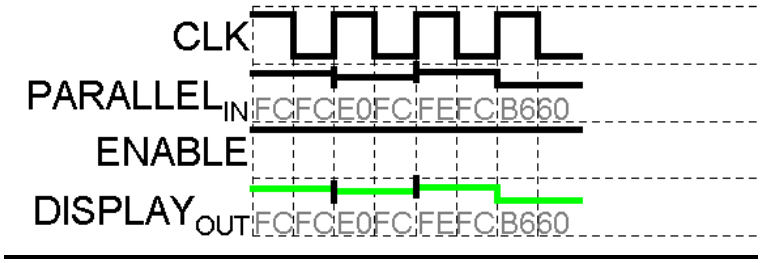
NOTE: DP is the most significant digit.

2. DISPLAY BUFFER

Circuit Diagram



Test Case Timing Diagram:

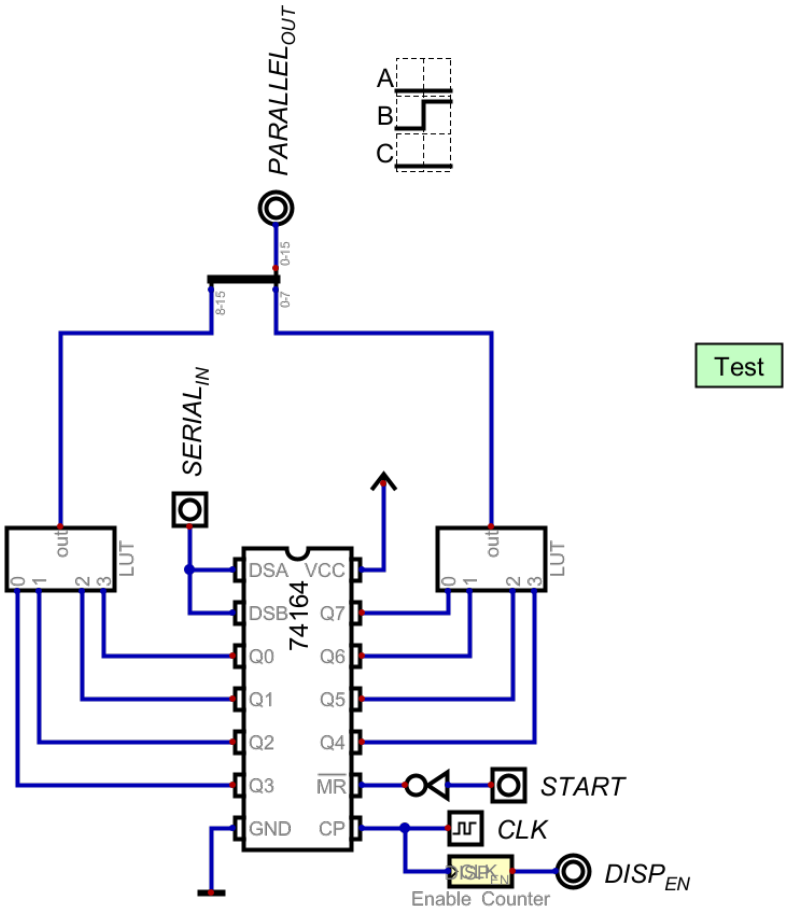


Test Case (Every test case is available in excel "TEST CASE)

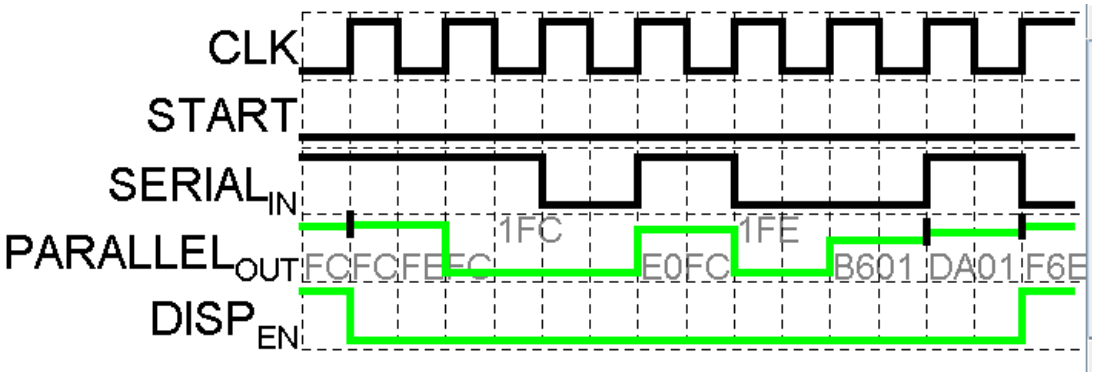
CLK	PARALLEL_IN	ENABLE	DISPLAY_OUT
1	0xFCFC	1	0xFCFC
0	0xFCFC	1	0xFCFC
1	0xE0FC	1	0xE0FC
0	0xE0FC	1	0xE0FC
1	0xFEFC	1	0xFEFC
0	0xFEFC	1	0xFEFC
1	0xB660	1	0xB660
0	0xB660	1	0xB660

3. SERIAL IN TO PARALLEL OUT

Circuit Diagram:



Test Case Timing Diagram:



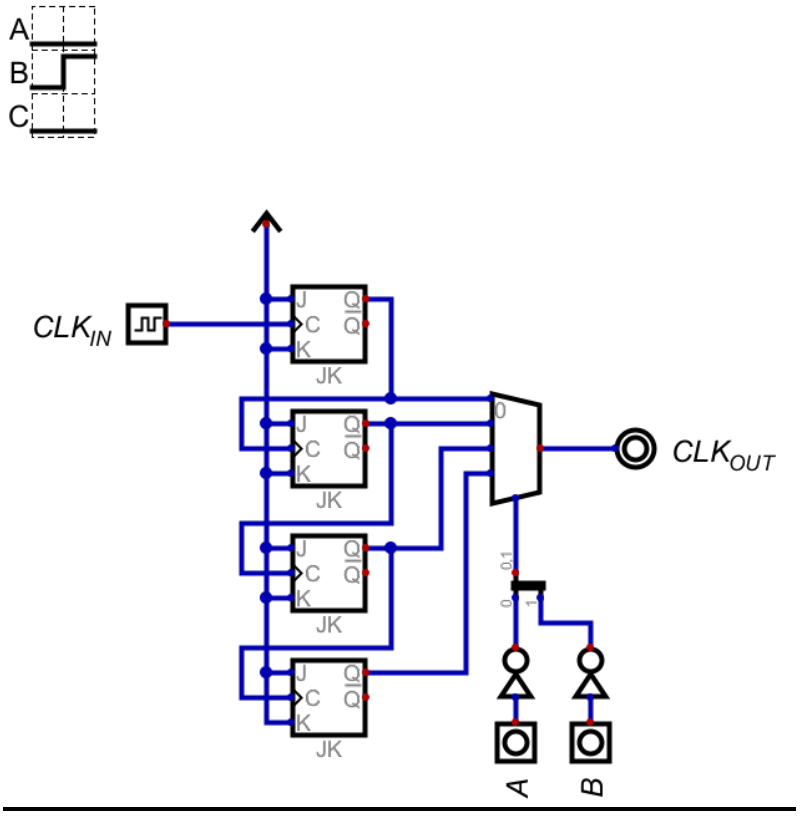
Test Cases (Every test case is available in excel "TEST CASE):

Note: The rightmost digit is the most significant digit, as such, to input BCD for digit 97 (10010111), the serial input must begin with the rightmost digit first. The HEX output for 97 is F6E0

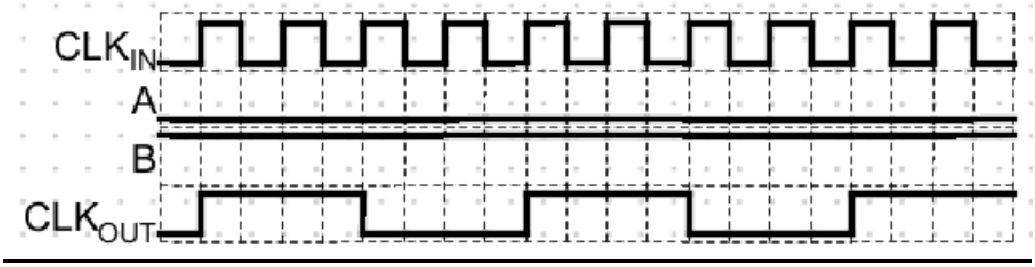
CLK	START	SERIAL_IN	PARALLEL_OUT	DISP_EN
0	0	1	0xFCFC	1
1	0	1	0xFEFC	0
0	0	1	0xFEFC	0
1	0	1	0x1FC	0
0	0	1	0x1FC	0
1	0	0	0x1FC	0
0	0	0	0x1FC	0
1	0	1	0xE0FC	0
0	0	1	0xE0FC	0
1	0	0	0x1FE	0
0	0	0	0x1FE	0
1	0	0	0xB601	0
0	0	0	0xB601	0
1	0	1	0xDA01	0
0	0	1	0xDA01	0
1	0	0	0xF6E0	1

4. CLOCK CONVERSION MODULE

Circuit Diagram:



Test Case Timing Diagram:



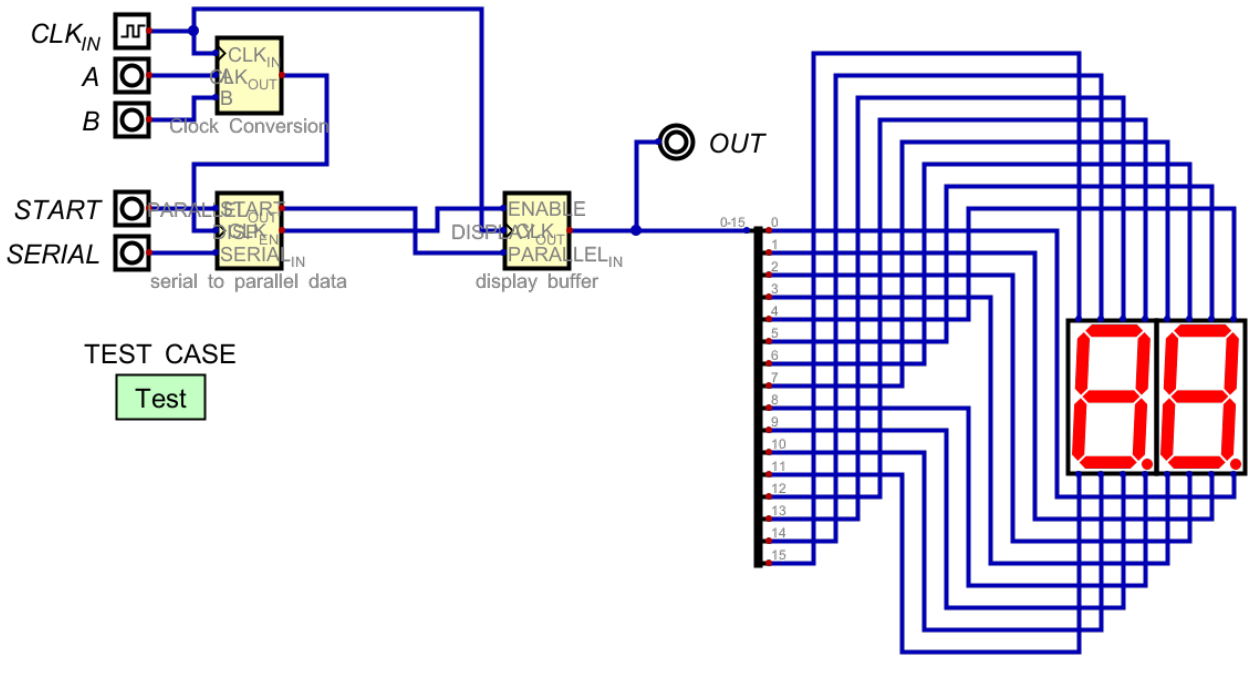
To determine CLK_OUT frequency, we will be referencing the input from the table below:

A	B	CLK_OUT Frequency
0	0	400 kHz
0	1	200 kHz
1	0	100 kHz
1	1	50 kHz

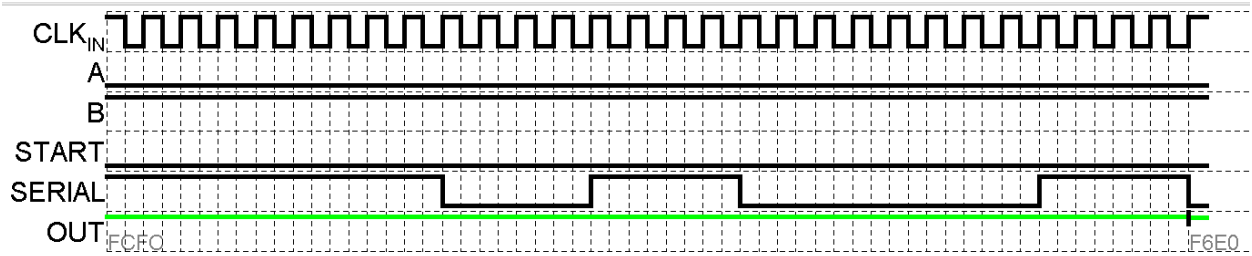
5. FULL CIRCUIT

NOTE!!: Sometimes it is possible for some modules and test data to be missing. We do not know what causes these issues. Please import the missing module again. The test cases can also be found in excel file “TEST CASE”.

Circuit Diagram



Test Case Timing Diagram:



Test Case (Every test case is available in excel “TEST CASE):

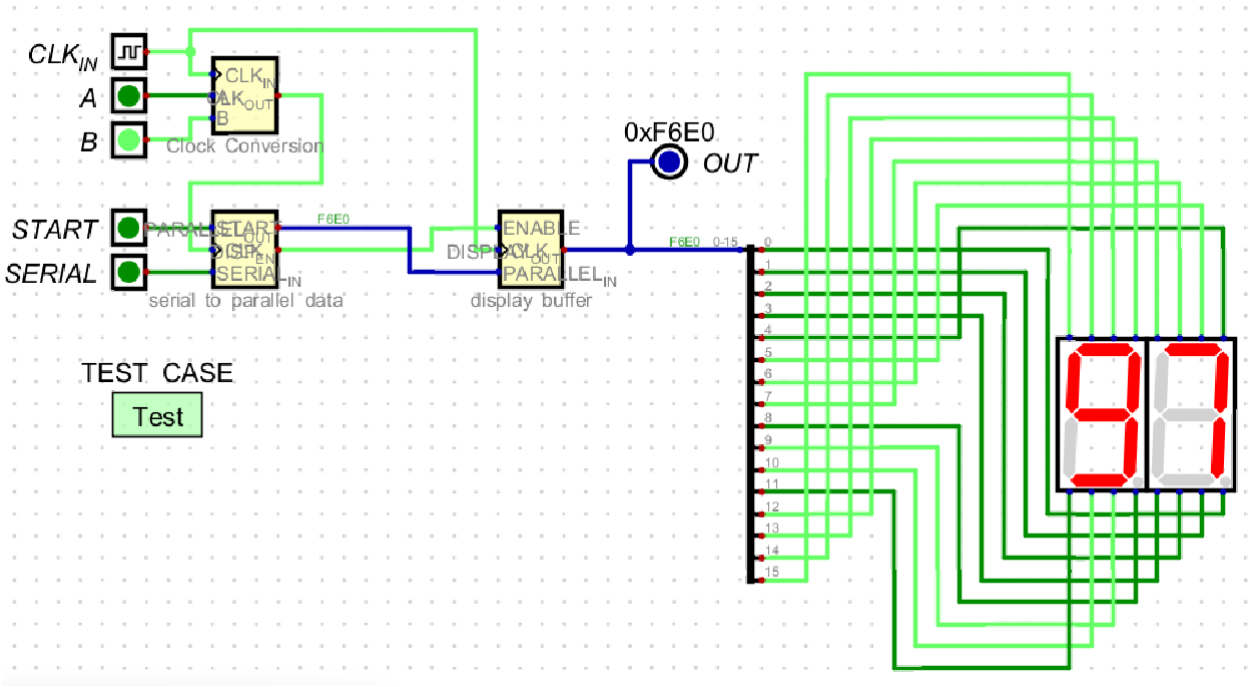
Frequency: 50 kHz   Expected output: 97

CLK_IN	A	B	START	SERIAL	OUT
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	0	0xFCFC
0	1	1	0	0	0xFCFC
1	1	1	0	0	0xFCFC
0	1	1	0	0	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	0	0xFCFC
0	1	1	0	0	0xFCFC
1	1	1	0	0	0xFCFC
0	1	1	0	0	0xFCFC
1	1	1	0	0	0xFCFC
0	1	1	0	0	0xFCFC
1	1	1	0	0	0xFCFC
0	1	1	0	0	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	1	0xFCFC
0	1	1	0	1	0xFCFC
1	1	1	0	1	0xF6E0

6. TEST CASE <u>(Every test case is available in excel "TEST CASE)</u>

FREQ: 200KhZ		EXPECTED OUTPUT: 97			
CLK_IN	A	B	START	SERIAL	OUT
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	0	0xFCFC
0	0	1	0	0	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	1	0xFCFC
0	0	1	0	1	0xFCFC
1	0	1	0	0	0xF6E0

SUCCESFUL OUTPUT



REFERENCES

Storr, W. (2013, August). *Display Decoder - BCD to 7 Segment Display Decoder*. Basic Electronics Tutorials. https://www.electronics-tutorials.ws/combination/comb_6.html

Seven Segment Displays. (2020, April 13). GeeksforGeeks; GeeksforGeeks. https://www.geeksforgeeks.org/seven-segment-displays/