Final Project
Tetris Game

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1 Project Description

Our project runs a game of Tetris that speeds up as the level increases, which is controlled by how many rows you have cleared. The orientation of the blocks is controlled by a joystick, and they are displayed on an LCD screen. The game keeps track of time using a real time clock and displays the current time whenever the game pauses or ends. When the game is running, it can be paused using a button that executes an interrupt. Two other buttons trigger two other interrupts that unpause and reset the game. The game will also pause via interrupt if the environment gets too dark, via input from a photoresistor. Clearing rows by filling a row with blocks levels the player up, which can trigger a change of state that speeds the game up. The game's theme song is played using a passive buzzer that replicates note frequencies using timers. LEDs are used to provide additional visual indicators for the state of the game.

2 Component Details

2.1 LCD

The LCD used for this project is a 128 by 64 pixel display with blue backlighting. This is used with the U8g2lib library to control what appears on the screen. The LCD can display the gameplay of the Tetris blocks falling, rotating, stacking on top of each other, and clearing complete rows. This is done by using matrix multiplication and a multidimensional array to calculate where each block is at on each step in the program's main loop. The multidimensional array is used to define the coordinate system of the Tetris game, and the matrix multiplication is used to calculate the translation and rotation of each block while they are falling. After each calculation is made, the U8g2lib is used to iterate through the array and draw out each block that is present in each coordinate location in the array.

2.2 Joystick

The joystick was used to control the movement, rotation, and hard drop of the falling Tetris blocks. Internally, it contains two potentiometers, one for the X-axis (horizontal)

and one for the Y-axis (vertical). As the stick moves, the resistance in each potentiometer changes, altering the output voltage. These analog voltages were sent to the Arduino Mega's analog input pins and read directly using the ADC hardware through register-level access. Thresholds were applied to interpret joystick input: ± 75 for the X-axis to detect left/right movement, and ± 150 for the Y-axis to detect rotation or a hard drop. These thresholds were checked on each loop cycle to determine whether an action should be triggered based on the joystick's position. The X-axis was assigned to ADC channel 15 and the Y-axis to channel 14. To configure this, we enabled the ADC through the ADCSRA register and selected AVCC as the reference voltage by setting bit 6 of ADMUX. Since channels above 7 require setting the MUX5 bit in ADCSRB, we included that logic conditionally in our `adc_read()` function. The channel number was set using the lower bits of ADMUX, and conversion was started by setting bit 6 of ADCSRA. We waited for the conversion to complete, then the resulting 10-bit value was retrieved from the data register.

2.3 Real Time Clock

This project uses a DS1307 RTC that communicates with the Arduino using I2C. The program uses the RTClib library to get the current time to display on both the 'pause' and 'game over' screens. The RTC is initialized with the current time during setup and then it keeps track of time for the project after that. When the game is paused or ends, the program gets the current time from the RTC and displays it on the LCD.

2.4 Buzzer

The passive buzzer mimics the Tetris theme song by replicating each note frequency in the song by using the timer registers from the Arduino Mega.

2.5 Photoresistor

The photoresistor was used to automatically pause the game if it is dark enough in the room that the system is in. This is done by having the Arduino Mega read the analog input of the photoresistor by using the analog-to-digital converter (ADC) registers.

2.6 Push Buttons

These were used to create input for the pause, unpause, and reset functionality of the Tetris game. Each push button is connected to its respective pin in the Arduino Mega, and, when pushed, an interrupt is activated to change the state of the game.

2.7 LEDs

There are four LEDs, one each green, yellow, red, and blue. When the green LED is on, the game is running. When the yellow LED is on, the game is paused. When the blue LED is on, the music is muted. The red LED turns on when the game ends.

3 System Overview

The game has no start screen and no external power source. The game starts as soon as it is plugged in, and is powered by the PC the arduino is connected to. The photoresistor has a threshold of 300, below which the game pauses. The joystick has thresholds of 75 for the x-direction and 150 for the y-direction.

4 Circuit Image

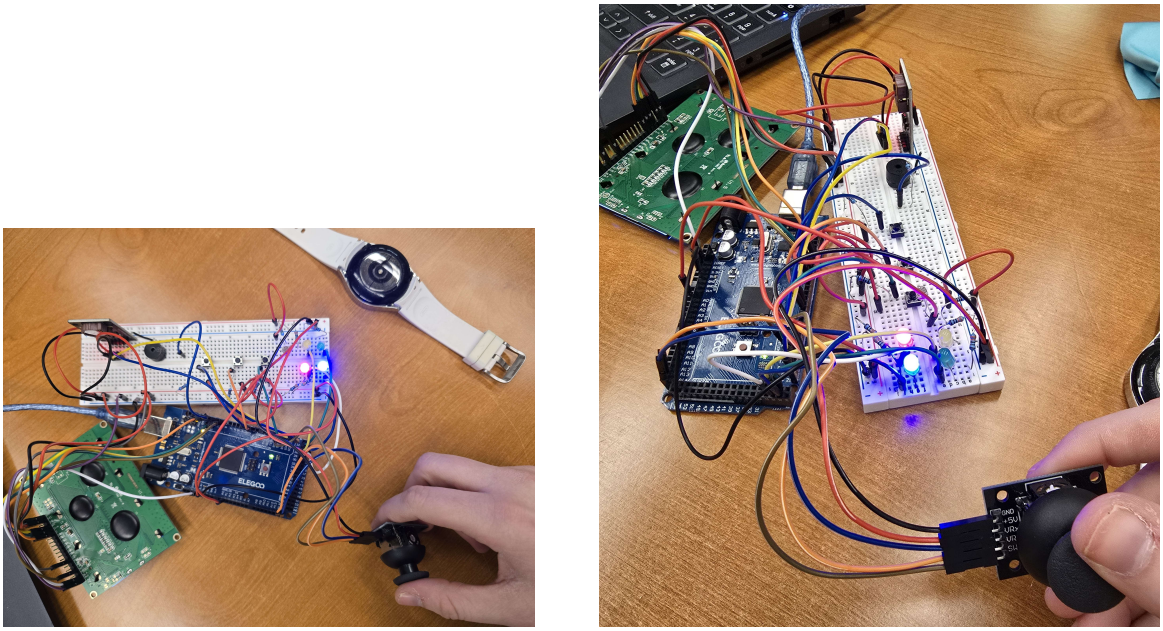


Figure 1: Pictures of Circuit

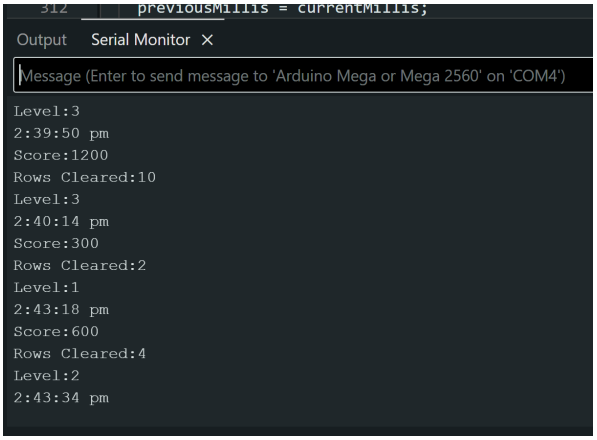


Figure 2: Screenshot of Serial Monitor

5 Schematic

5.1 Schematic

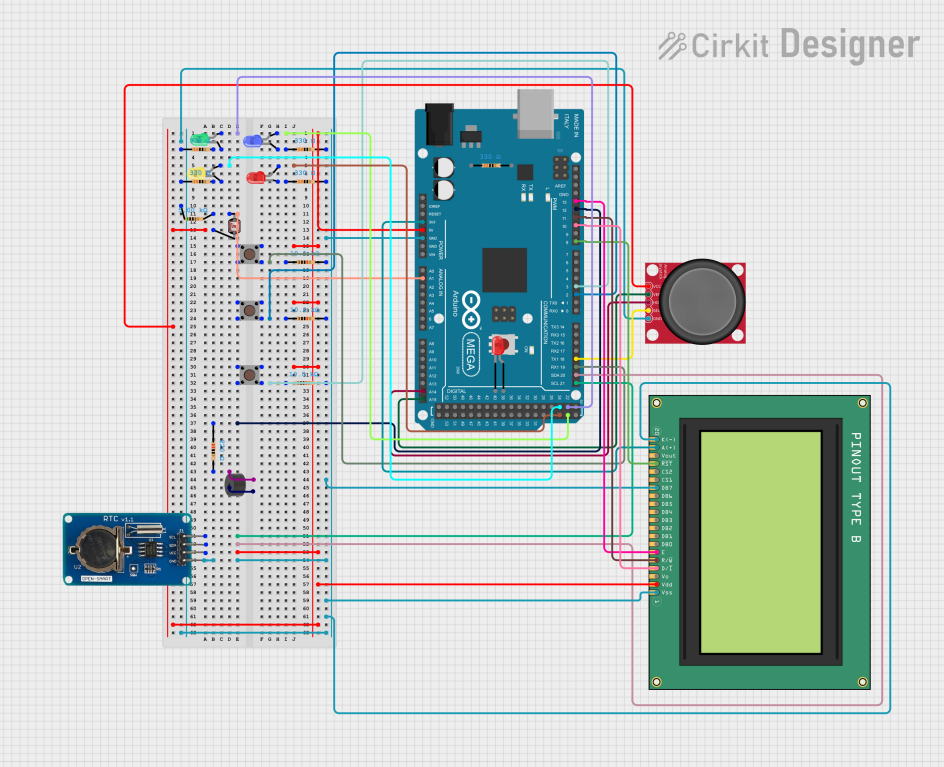


Figure 3: Circuit Schematic

5.2 Specification Sheets

Component Documentation Images

5.2.1 LCD

See Documentation

5.2.2 RTC

See Documentation

5.2.3 Joystick

See Documentation

5.2.4 Buzzer

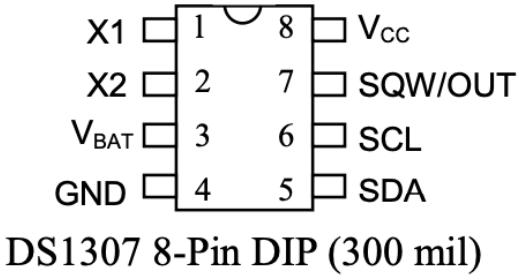
See Documentation

5.2.5 Photoresistor

See Documentation

Pin	Symbol	Level	Function
1	Vss	– –	GND (0V)
2	VDD	– –	Supply Voltage for Logic (+5v)
3	Vo	– –	Power supply for LCD
4	RS	H/L	H:Data L:Instruction code
5	R/W	H/L	H:Read L:Write
6	E	H	Enadle Signal
7	DB0	H/L	Data Bus Line
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	PSB	H/L	Interface selection: 0: serial mode; 1: 8/4-bit parallel bus mode.
16	NC		
17	RESET	H/L	Reset Signal
18	VEE	– –	Negative Votage(-10)to LCD
19	LED+	– –	LED Backight Power Supply +5V
20	LED–	– –	

Figure 4: LCD Pins

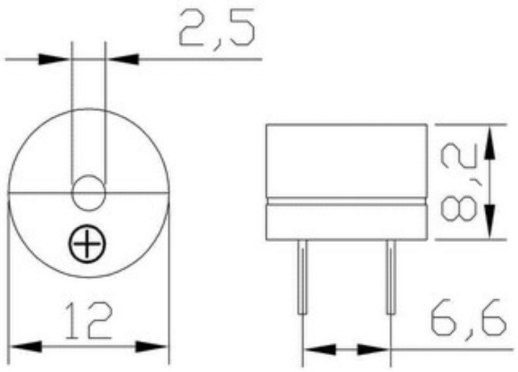


(a) RTC

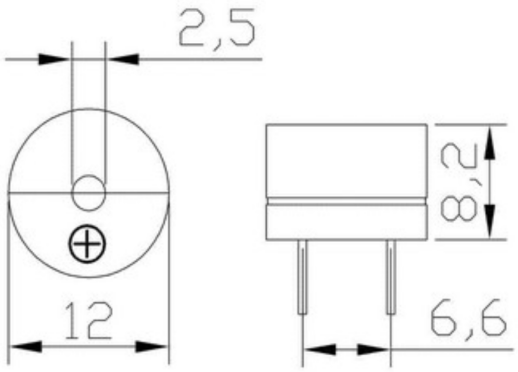
PIN CONFIGURATION:

1. GND: ground
2. +5V: 5V DC
3. VRx: voltage proportional to x position
4. VRy: voltage proportional to y position
5. SW: switch pushbutton

(b) Joystick



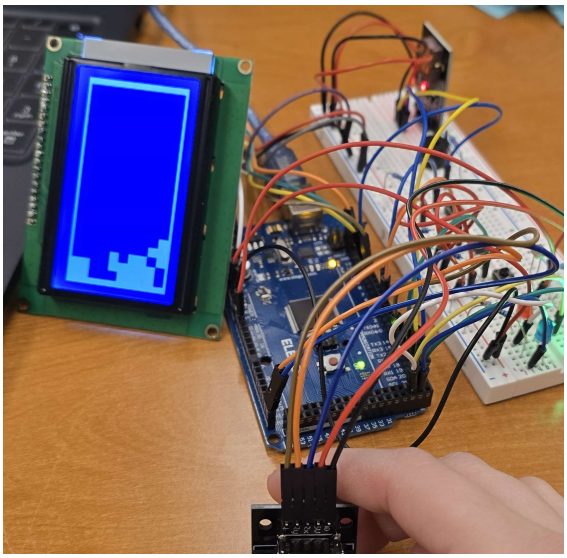
(c) Buzzer



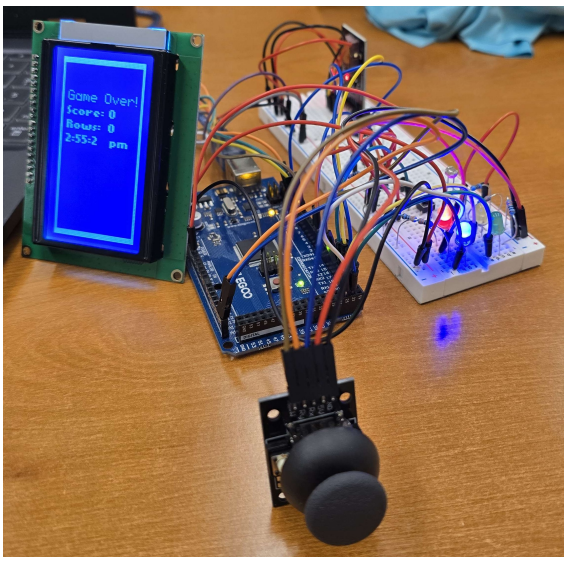
(d) Photoresistor

Figure 5: Kit Components

6 Demonstration

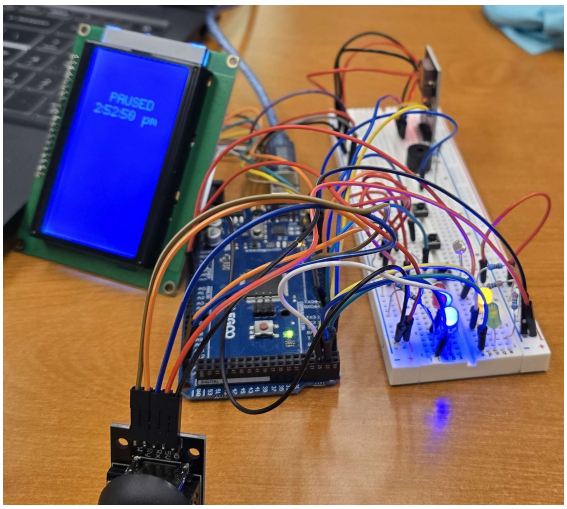


(a) Gameplay Screen

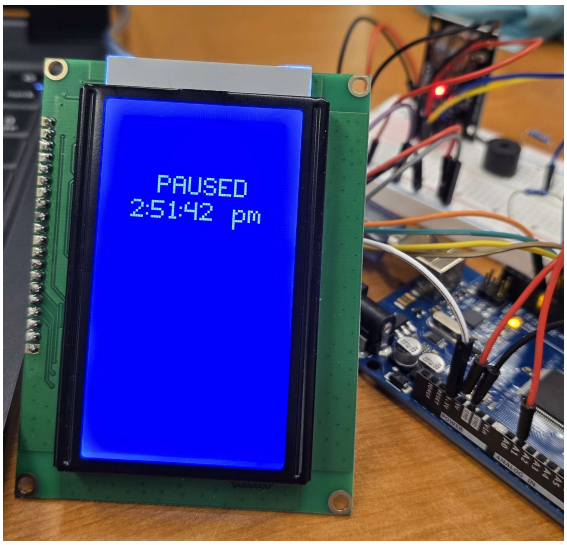


(b) Gameover Screen

Figure 6: Gameplay and Gameover Screens



(a) Paused Game LED



(b) Paused Game Screen

Figure 7: Pause Screen

The demonstration video is linked in the Links section.

7 Links

7.1 Github

Github Repository

7.2 Video

Link to the Youtube video.

7.3 Overleaf

The Overleaf for this PDF

8 Documentation Files

8.1 Sources

LCD
Kit Components

8.2 The Files

RTC Documentation Return to Report

DS1307
64 X 8 Serial Real Time Clock

www.dalsemi.com

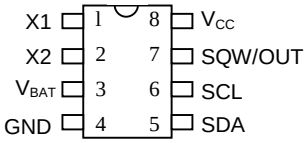
FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 56 byte nonvolatile RAM for data storage
- 2-wire serial interface
- Programmable squarewave output signal
- Automatic power-fail detect and switch circuitry
- Consumes less than 500 nA in battery backup mode with oscillator running
- Optional industrial temperature range -40°C to +85°C
- Available in 8-pin DIP or SOIC
- Recognized by Underwriters Laboratory

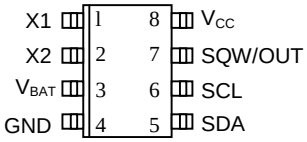
ORDERING INFORMATION

DS1307	8-Pin DIP
DS1307Z	8-Pin SOIC (150 mil)
DS1307N	8-Pin DIP (Industrial)
DS1307ZN	8-Pin SOIC (Industrial)

PIN ASSIGNMENT



DS1307 8-Pin DIP (300 mil)



DS1307Z 8-Pin SOIC (150 mil)

PIN DESCRIPTION

V_{CC}	- Primary Power Supply
X1, X2	- 32.768 kHz Crystal Connection
V_{BAT}	- +3V Battery Input
GND	- Ground
SDA	- Serial Data
SCL	- Serial Clock
SQW/OUT	- Square wave/Output Driver

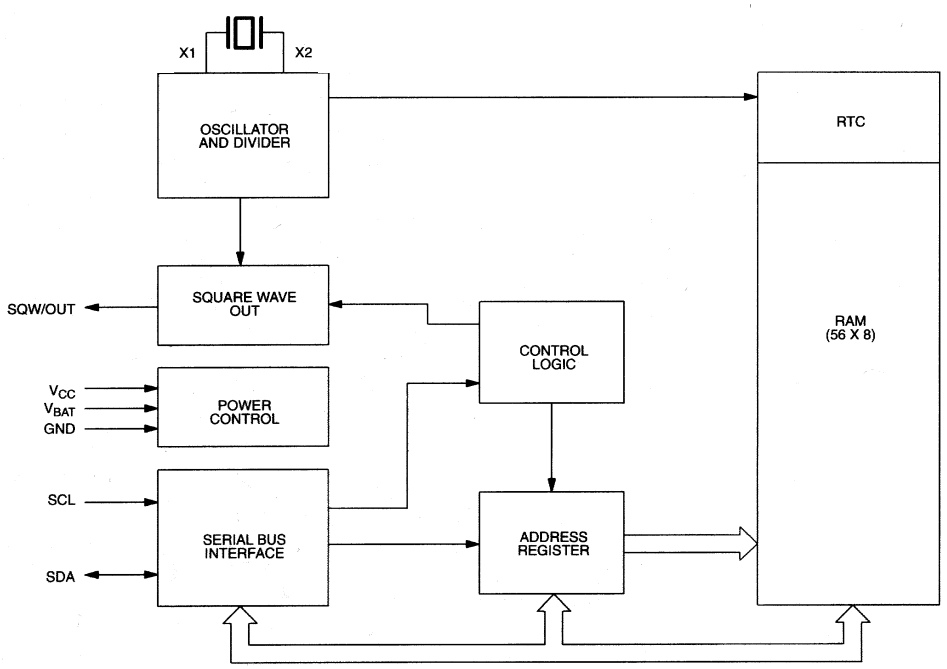
DESCRIPTION

The DS1307 Serial Real Time Clock is a low power, full BCD clock/calendar plus 56 bytes of nonvolatile SRAM. Address and data are transferred serially via a 2-wire bi-directional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1307 has a built-in power sense circuit which detects power failures and automatically switches to the battery supply.

OPERATION

The DS1307 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. When V_{CC} falls below 1.25 x V_{BAT} the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT} the device switches into a low current battery backup mode. Upon power up, the device switches from battery to V_{CC} when V_{CC} is greater than V_{BAT} +0.2V and recognizes inputs when V_{CC} is greater than 1.25 x V_{BAT}. The block diagram in Figure 1 shows the main elements of the Serial Real Time Clock.

DS1307 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC}, GND - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts is applied within normal limits, the device is fully accessible and data can be written and read. When a 3-volt battery is connected to the device and V_{CC} is below 1.25 x V_{BAT}, reads and writes are inhibited. However, the Timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{BAT} the RAM and timekeeper are switched over to the external power supply (nominal 3.0V DC) at V_{BAT}.

V_{BAT} - Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.0 and 3.5 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.25 x V_{BAT} nominal. A lithium battery with 48 mAhr or greater will back up the DS1307 for more than 10 years in the absence of power at 25 degrees C.

SCL (Serial Clock Input) - SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) - SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open drain which requires an external pullup resistor.

SQW/OUT (Square Wave/ Output Driver) - When enabled, the SQWE bit set to 1, the SQW/OUT pin outputs one of four square wave frequencies (1 Hz, 4 kHz, 8 kHz, 32 kHz). The SQW/OUT pin is open drain which requires an external pullup resistor. SQW/OUT will operate with either Vcc or Vbat applied.

X1, X2 - Connections for a standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5 pF.

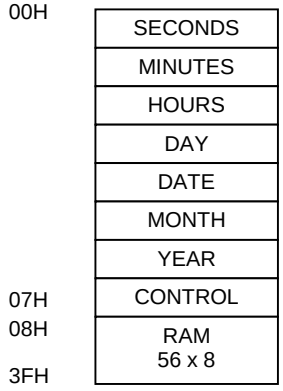
For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks." The DS1307 can also be driven by an external 32.768 kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

Please review Application Note 95, "Interfacing the DS1307 with a 8051-Compatible Microcontroller" for additional information.

RTC AND RAM ADDRESS MAP

The address map for the RTC and RAM registers of the DS1307 is shown in Figure 2. The real time clock registers are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multi-byte access, when the address pointer reaches 3Fh, the end of RAM space, it wraps around to location 00h, the beginning of the clock space.

DS1307 ADDRESS MAP Figure 2



CLOCK AND CALENDAR

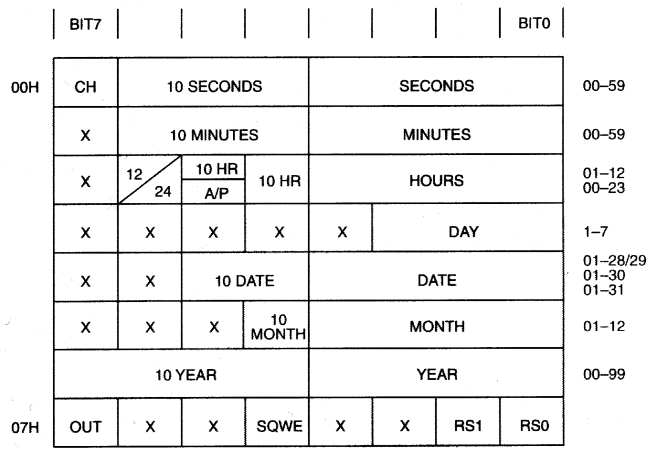
The time and calendar information is obtained by reading the appropriate register bytes. The real time clock registers are illustrated in Figure 3. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the Binary-Coded Decimal (BCD) format. Bit 7 of Register 0 is the Clock Halt (CH) bit. When this bit is set to a 1, the oscillator is disabled. When cleared to a 0, the oscillator is enabled.

Please note that the initial power on state of all registers is not defined. Therefore it is important to enable the oscillator (CH bit=0) during initial configuration.

The DS1307 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

On a 2-wire START, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

DS1307 TIMEKEEPER REGISTERS Figure 3



CONTROL REGISTER

The DS1307 Control Register is used to control the operation of the SQW/OUT pin.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	X	X	SQWE	X	X	RS1	RS0

OUT (Output control): This bit controls the output level of the SQW/OUT pin when the square wave output is disabled. If SQWE=0, the logic level on the SQW/OUT pin is 1 if OUT=1 and is 0 if OUT=0.

SQWE (Square Wave Enable): This bit, when set to a logic 1, will enable the oscillator output. The frequency of the square wave output depends upon the value of the RS0 and RS1 bits.

RS (Rate Select): These bits control the frequency of the square wave output when the square wave output has been enabled. Table 1 lists the square wave frequencies that can be selected with the RS bits.

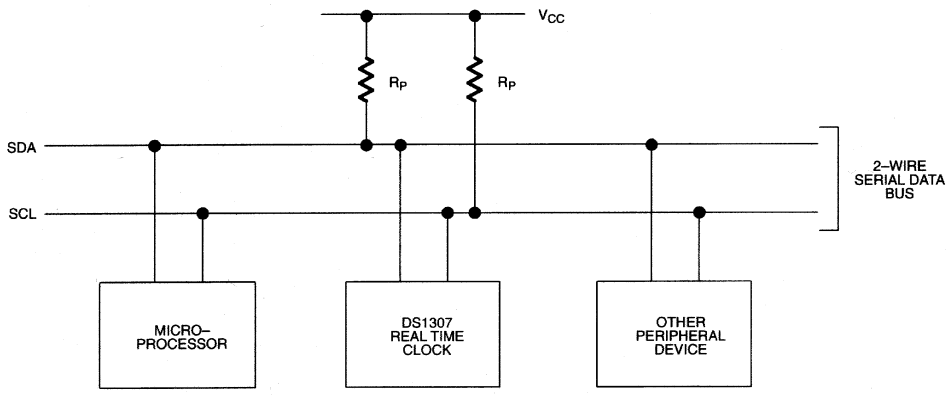
SQUAREWAVE OUTPUT FREQUENCY Table 1

RS1	RS0	SQW OUTPUT FREQUENCY
0	0	1 Hz
0	1	4.096 kHz
1	0	8.192 kHz
1	1	32.768 kHz

2-WIRE SERIAL DATA BUS

The DS1307 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1307 operates as a slave on the 2-wire bus. A typical bus configuration using this 2-wire protocol is show in Figure 4.

TYPICAL 2-WIRE BUS CONFIGURATION Figure 4



Figures 5, 6, and 7 detail how data is transferred on the 2-wire bus.

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

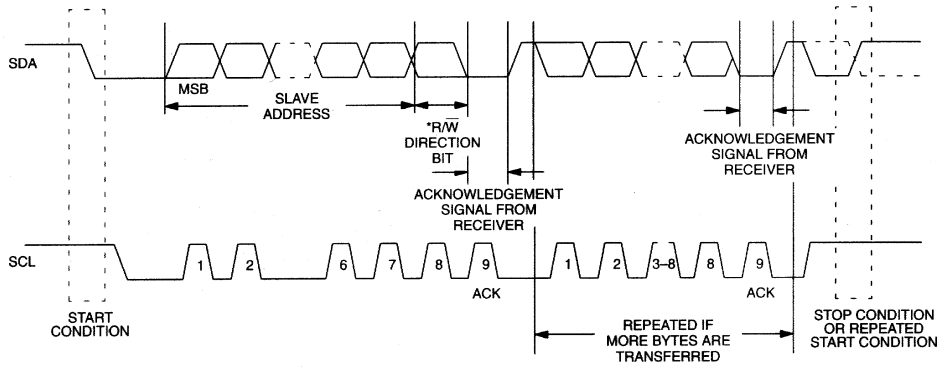
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the 2-wire bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1307 operates in the regular mode (100 kHz) only.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2-WIRE SERIAL BUS Figure 5



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

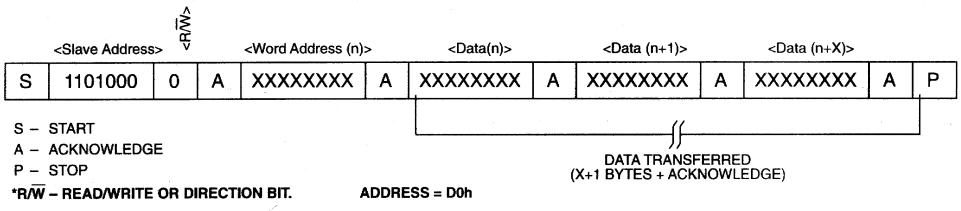
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The DS1307 may operate in the following two modes:

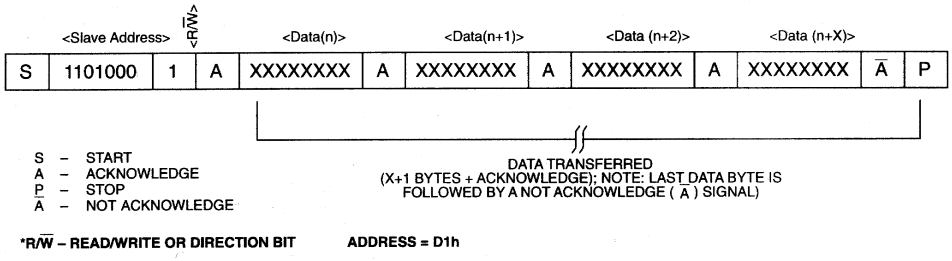
1. **Slave receiver mode (DS1307 write mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and *direction bit (See Figure 6). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7 bit DS1307 address, which is 1101000, followed by the *direction bit ($R/\overline{W}$) which, for a write, is a 0. After receiving and decoding the address byte the device outputs an acknowledge on the SDA line. After the DS1307 acknowledges the slave address + write bit, the master transmits a register address to the DS1307 This will set the register pointer on the DS1307. The master will then begin transmitting each byte of data with the DS1307 acknowledging each byte received. The master will generate a stop condition to terminate the data write.

DATA WRITE - SLAVE RECEIVER MODE Figure 6



2. **Slave transmitter mode (DS1307 read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the *direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1307 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (See Figure 7). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7-bit DS1307 address, which is 1101000, followed by the *direction bit ($R/\overline{W}$) which, for a read, is a 1. After receiving and decoding the address byte the device inputs an acknowledge on the SDA line. The DS1307 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1307 must receive a Not Acknowledge to end a read.

DATA READ - SLAVE TRANSMITTER MODE Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C (-40°C to 85°C for industrial)
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds DIP See JPC/JEDEC Standard J-STD-020A for Surface Mount Devices

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C or -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
V_{BAT} Battery Voltage	V_{BAT}	2.0		3.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C or -40°C to +85°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}			1	µA	10
I/O Leakage	I_{LO}			1	µA	11
Logic 0 Output	V_{OL}			0.4	V	2
Active Supply Current	I_{CCA}			1.5	mA	9
Standby Current	I_{CCS}			200	µA	3
Battery Current (OSC ON); SQW/OUT OFF	I_{BAT1}		300	500	nA	4
Battery Current (OSC ON); SQW/OUT ON (32 kHz)	I_{BAT2}		480	800	nA	4

AC ELECTRICAL CHARACTERISTICS

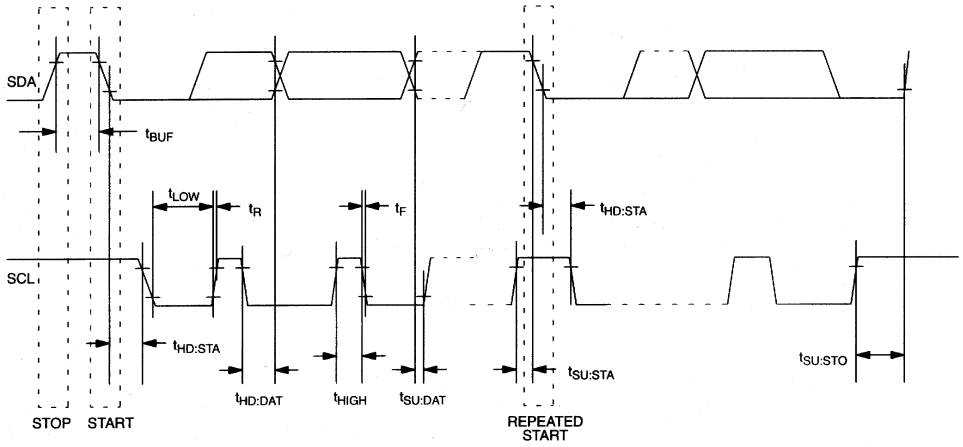
(0°C to 70°C or -40°C to +85°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	0		100	kHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	4.0			µs	5
LOW Period of SCL Clock	t_{LOW}	4.7			µs	
HIGH Period of SCL Clock	t_{HIGH}	4.0			µs	
Set-up Time for a Repeated START Condition	$t_{SU:STA}$	4.7			µs	
Data Hold Time	$t_{HD:DAT}$	0			µs	6, 7
Data Set-up Time	$t_{SU:DAT}$	250			ns	
Rise Time of Both SDA and SCL Signals	t_R			1000	ns	
Fall Time of Both SDA and SCL Signals	t_F			300	ns	
Set-up Time for STOP Condition	$t_{SU:STO}$	4.7			µs	
Capacitive Load for each Bus Line	C_B			400	pF	8
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Specified Load Capacitance			12.5		pF	

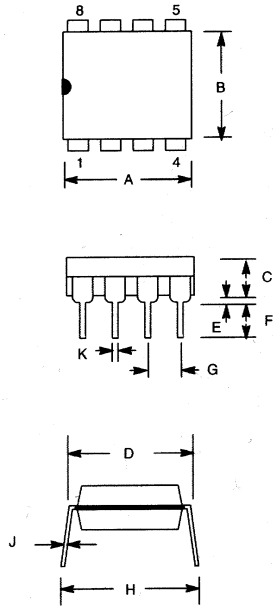
NOTES:

1. All voltages are referenced to ground.
2. Logic zero voltages are specified at a sink current of 5 mA at V_{CC}=4.5V, V_{OL}=GND for capacitive loads.
3. I_{CCS} specified with V_{CC}=5.0V and SDA, SCL=5.0V.
4. V_{CC}=0V, V_{BAT}=3V.
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. C_B - total capacitance of one bus line in pF.
9. I_{CCA} - SCL clocking at max frequency = 100 kHz.
10. SCL only.
11. SDA and SQW/OUT

TIMING DIAGRAM Figure 8

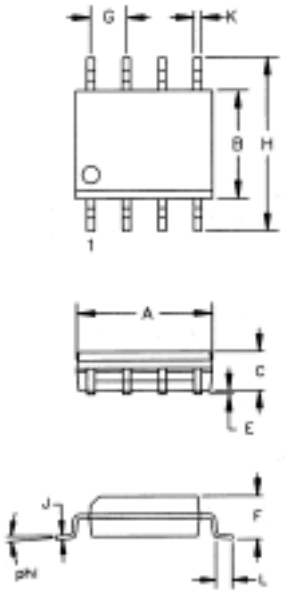


DS1307 64 X 8 SERIAL REAL TIME CLOCK
8-PIN DIP MECHANICAL DIMENSIONS



PKG	8-PIN	
DIM	MIN	MAX
A IN.	0.360	0.400
MM	9.14	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.40
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1307Z 64 X 8 SERIAL REAL TIME CLOCK
8-PIN SOIC (150-MIL) MECHANICAL DIMENSIONS



PKG	8-PIN (150 MIL)	
DIM	MIN	MAX
A IN.	0.188	0.196
MM	4.78	4.98
B IN.	0.150	0.158
MM	3.81	4.01
C IN.	0.048	0.062
MM	1.22	1.57
E IN.	0.004	0.010
MM	0.10	0.25
F IN.	0.053	0.069
MM	1.35	1.75
G IN.	0.050 BSC	
MM	1.27 BSC	
H IN.	0.230	0.244
MM	5.84	6.20
J IN.	0.007	0.011
MM	0.18	0.28
K IN.	0.012	0.020
MM	0.30	0.51
L IN.	0.016	0.050
MM	0.41	1.27
phi	0°	8°

56-G2008-001

Joystick Documentation Return to Report

JOYSTICK MODULE

DESCRIPTION:

Lots of robotic projects need a joystick. This module offers an affordable solution to that. The Joystick module is similar to analog joysticks found in gamepads. It is made by mounting two potentiometers at a 90 degrees angle. The potentiometers are connected to a short stick centered by springs.

This module produces an output of around 2.5V from X and Y when it is in resting position. Moving the joystick will cause the output to vary from 0v to 5V depending on its direction. If you connect this module to a microcontroller, you can expect to read a value of around 512 in its resting position (expect small variations due to tiny imprecisions of the springs and mechanism) When you move the joystick you should see the values change from 0 to 1023 depending on its position.

SPECIFICATIONS:

- Directional movements are simply two potentiometers - one for each axis
- Compatible with Arduino interface
- The biaxial XY Joystick Module KY-023 applies ARDUINO
- Dimensions: 1.57 in x 1.02 in x 1.26 in (4.0 cm x 2.6 cm x 3.2 cm)
- 5 Pin
- Color: Black

PIN CONFIGURATION:

1. GND: ground

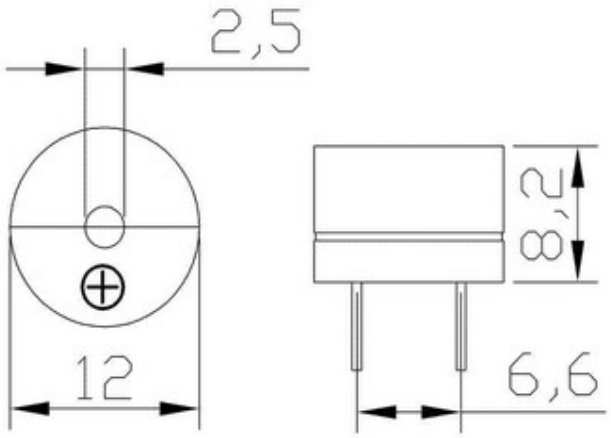
2. +5V: 5V DC

3. VRx: voltage proportional to x position

4. VRy: voltage proportional to y position

5. SW: switch pushbutton

Passive Buzzer Documentation Return to Report



5V　Passive buzzer　alternating current（SOT laminate tube ）

Specification of tact switch series：

voltage：3—12V

resistance：16R

Photoresistor Documentation Return to Report

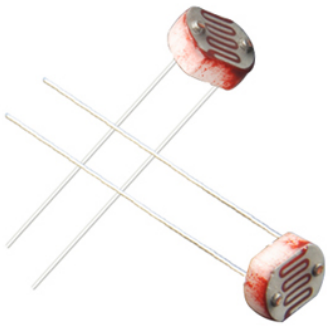
CdS Photoconductive cells

KLS electronic
www.cnkls.com

3mm CdS photosensitive resistor

Pruduct Model: KLS6-3537

VI



FEATURE:

- Epoxy encapsulated
- Quick Response
- Small Size
- High Sensitivity
- Reliable Performance
- Good Characteristic of Spectrum

TYPICAL APPLICATIONS:

- Auto Flash For Cameras
- photoelectric Control
- Optical Control Lamp
- Room Light Control
- Photomusical I.C.
- Industrial control
- Photoswitch
- Electronic Toys

DESCRIPTION:

CdS Photoconductive Cells is a resistor which made of semi-conductor material,and the conductance change with luminance variation. The CdS Photoconductive cells can be manufactured with different figures and illuminated area based on this characteristic.CdS Photoconductive cells is widely used in many industries,such as toys,lamps,camera,etc.

ELECTRO-OPTICAL CHARACTERICTICS :

Parameter		Characterictics	Unit
Light Resistance(at 10lux)		18-50	KΩ
Dark Resistance(at 0 lux/Min)		2.0	MΩ
Gamma Value(at 100-10lux)		0.7	γ_{10}^{100}
Power Dissipation(at 25℃)		50	MW
Max Voltage(at 25℃)		100	VDC
Spectral Response peak(at 25℃)		540	nm
Ambient Temperature Range		-30～+70	℃
Response time	Increase	30	ms
	Decrease	30	ms

※ Light resistance : Measured at 10lux(standard Light source)at a color temperature of 2856K. color temperature)and 2h pre-illumination at 400-600 lux priorto testing .

※ Dark resistance: measured 10 senconds after pulsed 10 lux.

※ Gamma Characteristic:between 10lux and 100lux and given by $T = \frac{\mathrm{Lon}(R10/R100)}{\mathrm{Log}(100/10)} = \mathrm{Log}(R10/R100)$

※ Pmax: Max.power dissipation at ambient temperature of 25℃.

※ Vmax:Max.voltage in darkness that may be applied to the cell continuously .

VI

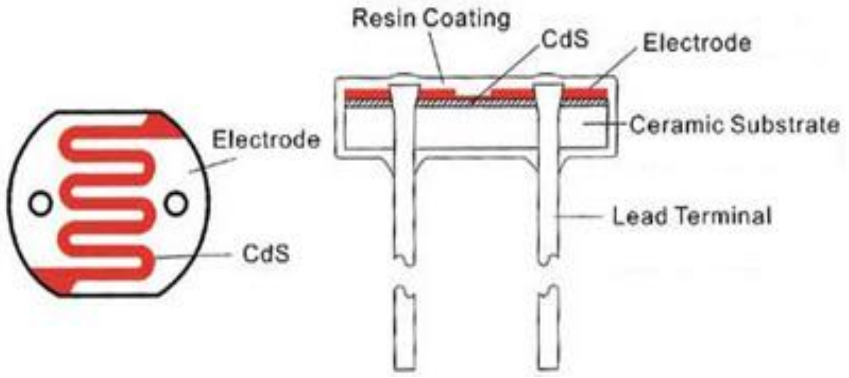
3mm CdS photosensitive resistor

Pruduct Model: KLS6-3537

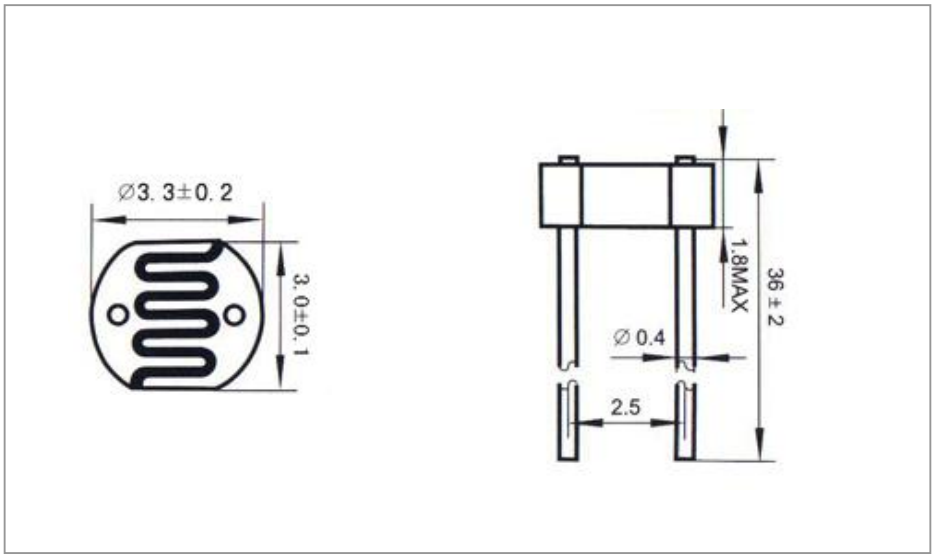
Component Information :

Component Name	ROSH	Notice
Resin Coating	YES	--
CdS	NO	Composition than 100 PPM
Electrode	YES	--
Ceramic Substrate	YES	--
Lead Terminal	YES	--

SCHEMATIC DRAWING :



OUTLINE:(Unit: mm)

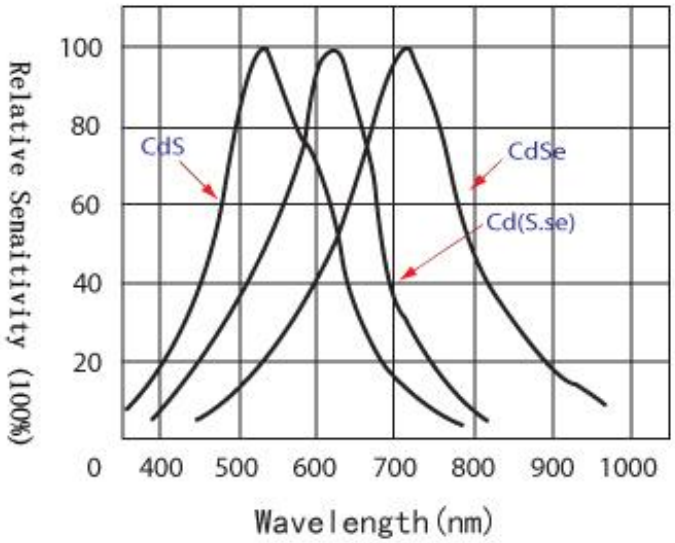


3mm CdS photosensitive resistor

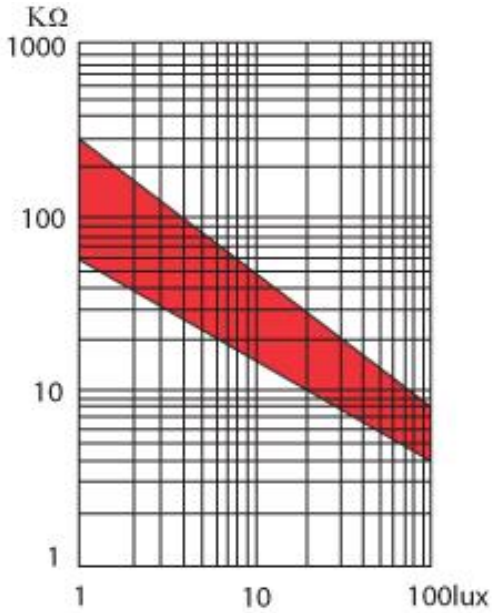
Pruduct Model: KLS6-3537

VI

SPECTRAL RESPONSE :



ILLUNINANCE Vs. PHOTO RESISTANCE



CdS Photoconductive cells

3mm CdS photosensitive resistor

Pruduct Model: KLS6-3537

TEST CONDITIONS

Light Resistance Dark Resistance	**Light resistance:A light source(2856k) At 10Lux Dark resistance:data@10sec,after cutting off 10Lux light r=Lg（R10/R100）**	**Workable**
Tempture Change Testing	**Hight tempture:：70℃±5℃ Time:30M Incideng light:dark placing Testing time:24hr Low tempture::-30℃±5℃ Time:30min Incident light:above dark placing as a recycle,testing time:24hr**	**Workable**
Constant Tempture Testing	**Tempture:40±5℃ Moisture :90-95% Incident light:dark placing Testing time:48hr**	**Workable**
Lead High Tempture Testing	**At the root of lead 90 degree curving,5mm above the root,loading 100g charge Welding tempture:：260℃ Heating time:Max.35,distance between welding and base:5mm**	**Workable**

PACKING AND PRECAUTION:

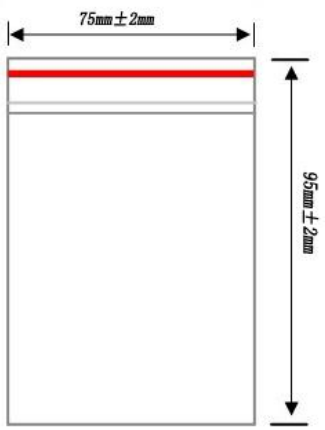


Image -01

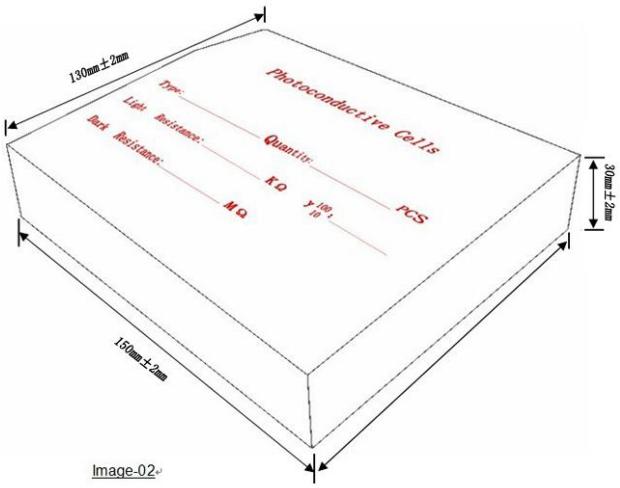


Image-02

CdS Photoconductive cells

3mm CdS photosensitive resistor

Pruduct Model: KLS6-3537

VI

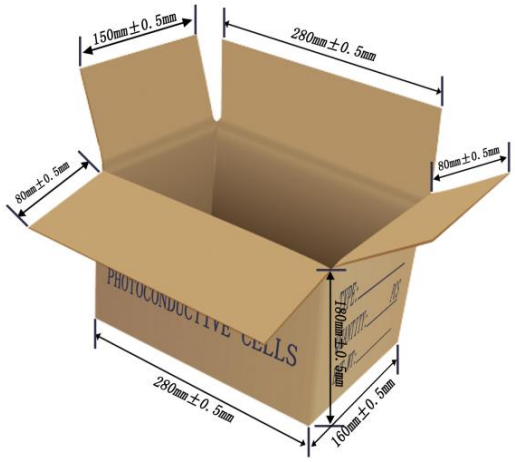
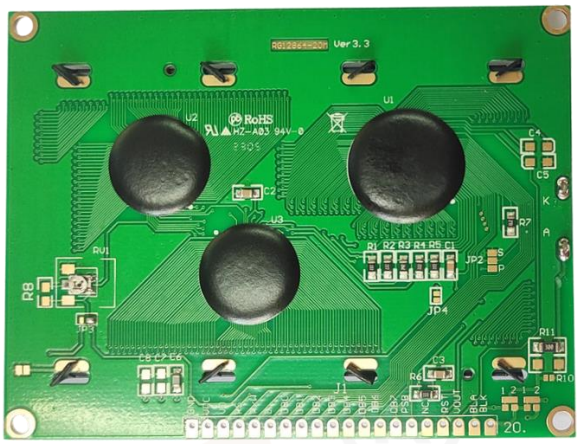


Image-03

IMAGE NO.	NAME	QUANTITY
Image-01	Bag	200Pcs /bag
Image-02	Box	10Bag/Box = 2000Pcs
Image-03	Carton	20000PCS = 10 Box = 100 Bag = 1 Carton

- This product is packed with the environmental protection material,200pcs per small package,2000pcs per big package.
- Avoid high temperature and humidity fot storing.
- Soldering should be completed in the shortest possible time.
- It is recommended that the soldering should keep 4mm away from ceramic substrate.

RG12864 Serial Interface Display 128×64 BLUE



1. Features:

The features of LCD are as follows:

- Display mode : STN /BLUE, NEGATIVE, TRANSMISSIVE
- Colour : Display dot : WHITE
  Background: BLUE
- Display Format : 128 (characters) × 64 (line)
- * IC : ST7920 ST7921
- Interface Input Data : 8 Bits
- Driving Method : 1/65 Duty, 1/9 Bias
- Viewing Direction: 6 O'clock
- Backlight : LED (WHITE)

2. Mechanical Specifications:

Item	Specification	Unit
Module Size	93.00(W) X70.00(H) X12.5(T)	mm
Viewing Area	72.00(W) X 39.90(H)	mm
Effective Display Area	66.52(W) X 33.24(H)	mm
Number of Dots	128 X 64 Dots	-
Dot Size	0.48(W) X 0.48(H)	mm
Dot Pitch	0.52(W) X 0.52(H)	mm

3. Electrical Specifications:

1. Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Standard Value			Unit
		Min.	Typ.	Max.	
Supply Voltage For Logic	V_{DD}	-0.3	-	5.0	V
Supply Voltage For LCD Drive	V_0, V_{OUT}	-0.3	-	14.5	V
Operating Temp.	T_{OP}	-20	-	+70	°C
Storage Temp.	T_{ST}	-30	-	+80	°C
Static Electricity	Be sure that you are ground when handing LCM				

2. Electrical Characteristics:

Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic		$V_{DD} – V_{SS}$	Ta=25℃	4.7	5.0	5.3	V
Supply Voltage For LCD		$V_{DD} – V_0$	Ta=25℃	-	-	-	V
Input Voltage	“H” Level	V_{IH}	Ta=25℃	0.8V_{DD}	-	V_{DD}	V
	“L” Level	V_{IL}		V_{SS}	-	0.2V_{DD}	V
Output Voltage	“H” Level	V_{OH}	I_{OUT}= -0.5mA	0.8V_{DD}	-	V_{DD}	V
	“L” Level	V_{OL}	I_{OUT}= 0.5mA	V_{SS}	-	0.2V_{DD}	V
Current Consumption		I_{DD}	V_{IN} = V_{DD}	-	-	1.0	mA

NOTE: 1) Duty ratio=1/65, Bias=1/9
2) Measured in Dots ON-state

3. BACKLIGHT:

3.1 Absolute Maximum Ratings:

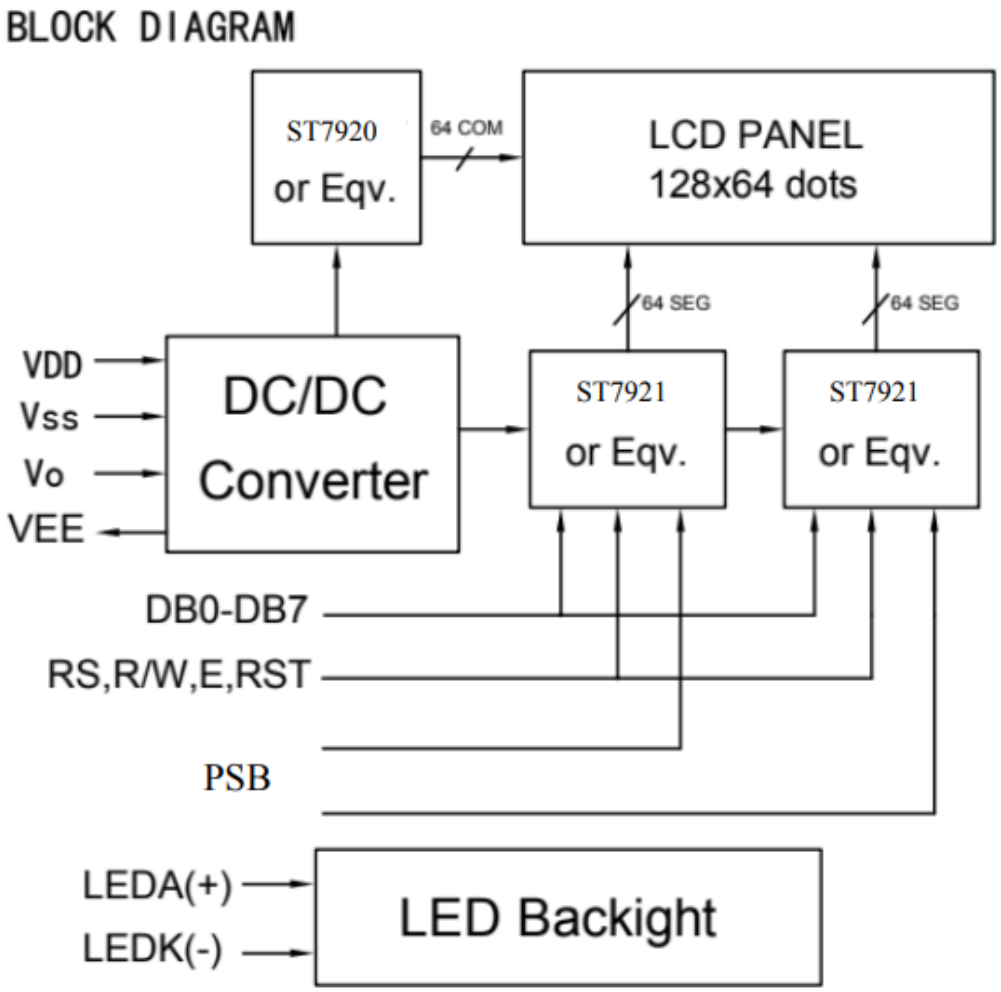
Item	Symbol	Condition	Min.	Typ.	Max	Unit
Forward Current	IF	Ta= 25℃	-	-	20	mA
Reverse Voltage	VR		-	-	5	V
Power Dissipation	PD	Ta= 25℃	-	-	100	mW

3.2 Opto-electronic Characteristics:

Item	Symbol	Condition	Min.	Typ.	Max	Unit
Forward Voltage	VF	Ta= 25℃ IF= 60mA	2.8	3.0	3.2	V
Luminous	-		100	150	-	cd/m²

** The brightness is measured without LCD panel*

4. Schematic Design:



5. Interface Pin Function:

Pin	Symbol	Level	Function
1	Vss	– –	GND (0V)
2	VDD	– –	Supply Voltage for Logic (+5v)
3	Vo	– –	Power supply for LCD
4	RS	H/L	H:Data L:Instruction code
5	R/W	H/L	H:Read L:Write
6	E	H	Enadle Signal
7	DB0	H/L	Data Bus Line
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	PSB	H/L	Interface selection: 0: serial mode; 1: 8/4-bit parallel bus mode.
16	NC		
17	RESET	H/L	Reset Signal
18	VEE	– –	Negative Votage(-10)to LCD
19	LED+	– –	LED Backight Power Supply +5V
20	LED–	– –	

6. Command List:

ST7920 offers basic instruction set and extended instruction set:

Instruction Set 1: (RE=0: Basic Instruction)

Inst.	Code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H" and set DDRAM address counter (AC) to "00H".	1.6 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00H", and put cursor to origin : the content of DDRAM are not changed	72 us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and display shift when doing write or read operation	72 us
Display Control	0	0	0	0	0	0	1	D	C	B	D=1: Display ON C=1: Cursor ON B=1: Character Blink ON	72 us
Cursor Display Control	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control; the content of DDRAM are not changed	72 us
Function Set	0	0	0	0	1	DL	X	0 RE	X	X	DL=1 8-bit interface DL=0 4-bit interface **RE=1: extended instruction** **RE=0: basic instruction**	72 us
Set CGRAM Address.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address to address counter (AC) **Make sure that in extended instruction SR=0 (scroll or RAM address select)**	72 us
Set DDRAM Address.	0	0	1	0 AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address to address counter (AC) AC6 is fixed to 0	72 us
Read Busy Flag (BF) & AC.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) for completion of internal operation, also Read out the value of address counter (AC)	0 us
Write RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to internal RAM (DDRAM/CGRAM/GDRAM)	72 us
Read RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/GDRAM)	72 us

Instruction set 2: (RE=1: extended instruction)

Inst.	Code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Standby	0	0	0	0	0	0	0	0	0	1	Enter standby mode, any other instruction can terminate. COM1…32 are halted.	72 us
Scroll or RAM Address. Select	0	0	0	0	0	0	0	0	1	SR	SR=1: enable vertical scroll position SR=0: enable CGRAM address **(basic instruction)**	72 us
Reverse (by line)	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction **R1,R0 initial value is 0,0**	72 us
Extended Function Set	0	0	0	0	1	DL	X	1 RE	G	0	DL=1 :8-bit interface DL=0 :4-bit interface **RE=1: extended instruction set** **RE=0: basic instruction set** G=1 :graphic display ON G=0 :graphic display OFF	72 us
Set Scroll Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5~AC0 the address of vertical scroll	72 us
Set Graphic Display RAM Address	0	0	1	0 0	0 AC5	0 AC4	AC3 AC3	AC2 AC2	AC1 AC1	AC0 AC0	Set GDRAM address to address counter (AC) Set the vertical address first and followed the horizontal address by consecutive writings Vertical address range: AC5…AC0 Horizontal address range: AC3…AC0	72 us

Note:

1. Make sure that ST7920 is not in busy state by reading the busy flag before sending instruction or data. If using delay loop instead, please make sure the delay time is enough. Please refer to the instruction execution time.
2. "RE" is the selection bit of basic and extended instruction set. After setting the RE bit, the value will be kept. So that the software doesn't have to set RE every time when using the same instruction set.

DDRAM data (char. code)					CGRAM Addr.						CGRAM data (higher byte)								CGRAM data (lower byte)							
B15~ B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	00	X	00			0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
							0	0	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0
							0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0
							0	0	1	1	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0
							0	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0
							0	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	1	0	0
							0	1	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	0	0
							0	1	1	1	1	0	1	0	0	1	1	0	0	1	0	0	1	0	0	0
							1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0
							1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0
							1	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0
							1	0	1	1	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0
							1	1	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0
							1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
							1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	01	X	01			0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0
							0	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0
							0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0
							0	0	1	1	0	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0
							0	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
							0	1	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							0	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							0	1	1	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							1	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							1	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							1	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0
							1	0	1	1	0	1	0	1	1	1	1	1	1	0		0	0	1	0	0
							1	1	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	1	0	0
							1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1	1	0	0
							1	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5: DDRAM data (character code) vs. CGRAM data/address map

7. Timing Characteristics (Continued):

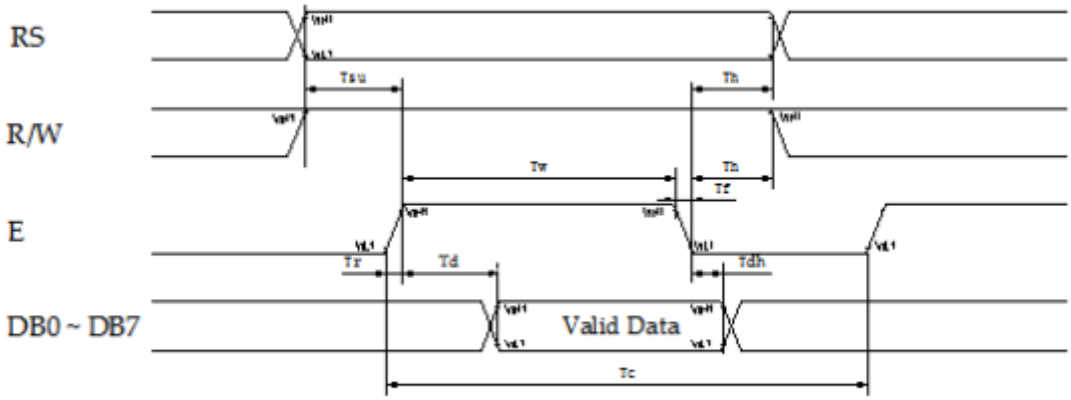


Figure 7. Read Mode Timing Diagram

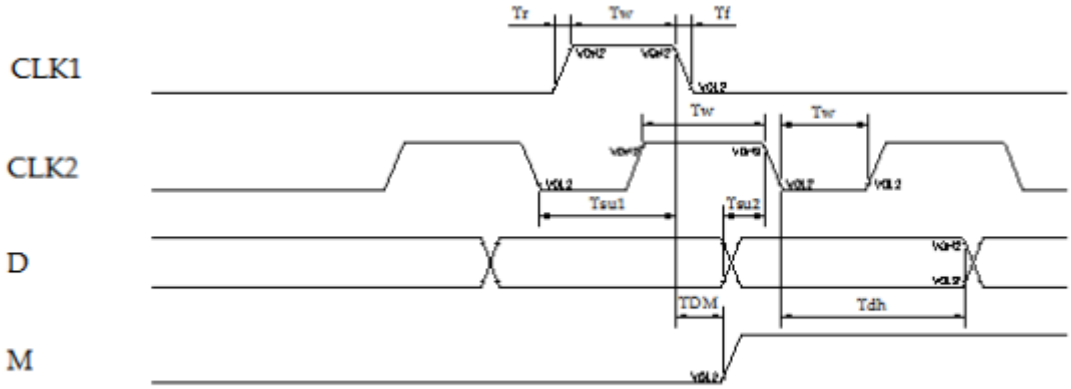


Figure 8. Interface Mode With Extension Driver Timing Diagram

AC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 4.5V) Serial Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
		Internal Clock Operation				
f_{OSC}	OSC Frequency	R = 33KΩ	470	530	590	KHz
		External Clock Operation				
f_{EX}	External Frequency	-	470	530	590	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
T_{SCYC}	Serial clock cycle	Pin E	400	-	-	ns
T_{SHW}	SCLK high pulse width	Pin E	200	-	-	ns
T_{SLW}	SCLK low pulse width	Pin E	200	-	-	ns
T_{SDS}	SID data setup time	Pins RW	40	-	-	ns
T_{SDH}	SID data hold time	Pins RW	40	-	-	ns
T_{CSS}	CS setup time	Pins RS	60	-	-	ns
T_{CSH}	CS hold time	Pins RS	60	-	-	ns

AC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 2.7V) Serial Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
		Internal Clock Operation				
f_{OSC}	OSC Frequency	R = 18KΩ	470	530	590	KHz
		External Clock Operation				
f_{EX}	External Frequency	-	470	530	590	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
T_{SCYC}	Serial clock cycle	Pin E	600	-	-	ns
T_{SHW}	SCLK high pulse width	Pin E	300	-	-	ns
T_{SLW}	SCLK low pulse width	Pin E	300	-	-	ns
T_{SDS}	SID data setup time	Pins RW	40	-	-	ns
T_{SDH}	SID data hold time	Pins RW	40	-	-	ns
T_{CSS}	CS setup time	Pins RS	60	-	-	ns
T_{CSH}	CS hold time	Pins RS	60	-	-	ns

8. Quality Specification (Continued):

8-3. Sampling Plan and Acceptance

1. Sampling Plan

MIL - STD - 105E (**II**) ordinary single inspection is used.

2. Acceptance

Major defect: AQL = 0.25%

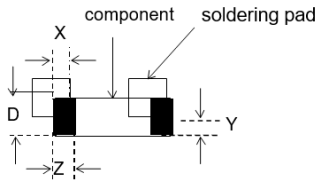
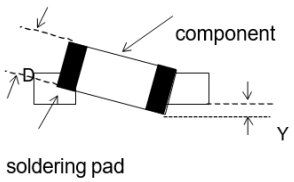
Minor defect: AQL = 0.65%

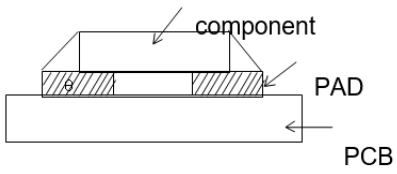
8-4. Criteria

a) COB

Defect	Inspection Item	Inspection Standards	
Major	PCB copper flakes peeling off	Any copper flake in viewing Area should be greater than 1.0mm^2	Reject
Major	Height of coating epoxy	Exceed the dimension of drawing	Reject
Major	Void or hole of coating epoxy	Expose bonding wire or IC	Reject
Major	PCB cutting defect	Exceed the dimension of drawing	Reject

b) SMT

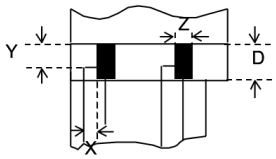
Defect	Inspection Item	Inspection Standards	
Minor	Component marking not readable		Reject
Minor	Component height	Exceed the dimension Of drawing	Reject
Major	Component solder defect (missing , extra, wrong component or wrong orientation		Reject
Minor	 Component position shift	X < 3/4Z Y > 1/3D	Reject Reject
Minor	 Component tilt	Y > 1/3D	Reject

Minor	Insufficient solder 	$\theta \leq 20^{\circ}$	Reject

3. Metal (Plastic) Frame

Defect	Inspection Item	Inspection Standards		
Major	Crack / breakage	Anywhere		Reject
Minor	Frame Scratch	W	L	Acceptable of Scratch
		w<0.03mm	Any	Ignore
		0.03mm≤w<0.05mm	L≤5.0mm	2
		0.05mm<w<0.1mm	L<3.0mm	1
		w>0.1mm	Any	0
		Note: 1. Above criteria applicable to scratch lines with distance greater than 5mm. 2. Scratch on the back side of frame (not visible) can be ignored.		
Minor	Frame Dent, Prick $\Phi = \frac{L + W}{2}$			Acceptable of Dents / Pricks
		$\Phi \leq 1.0$mm		2
		$1.0 < \Phi \leq 1.5$mm		1
		$1.5\text{mm} > \Phi$		0
		Note: 1. Above criteria applicable to any two dents / pricks with distance greater than 5mm 2. Dent / prick on the back side of frame (not visible) can be ignored		
Minor	Frame Deformation	Exceed the dimension of drawing		
Minor	Metal Frame Oxidation	Any rust		

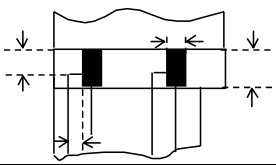
4. Flexible Film Connector (FFC)

Defect	Inspection Item		Inspection Standards	
Minor	Tilted soldering		Within the angle ±3°	Acceptable
Minor	Uneven solder joint /bump			Reject
Minor	Hole	$\Phi = \frac{L+W}{2}$	Expose the conductive line	Reject
			Φ > 1.0mm	Reject
Minor	Position shift 		Y > 1/3D	Reject
			X > 1/2Z	Reject

5. Screw

Defect	Inspection Item	Inspection Standards	
Major	Screw missing/loosen		Reject
Minor	Screw oxidation	Any rust	Reject
Minor	Screw deformation	Difficult to accept screw driver	Reject

6. Heat seal、TCP、FPC

Defect	Inspection Item		Inspection Standards	
Major	Scratch expose conductive layer			Reject
Minor	HS Hole	$\Phi = \frac{L+W}{2}$	Φ > 0.2mm	Reject
Major	Adhesion strength		Less than the specification	Reject
Minor	Position shift 		Y > 1/3D	Reject
			X > 1/2Z	Reject
Major	Conductive line break			Reject

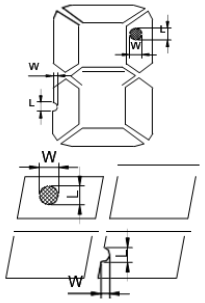
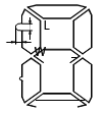
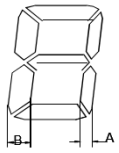
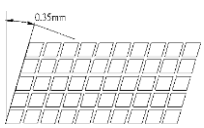
7. LED Backing Protective Film and Others

Defect	Inspection Item	Inspection Standards	
Minor	LED dirty, prick	Acceptable number of units	
		Φ≤0.10mm	Ignore
		0.10<Φ≤0.15mm	2
		0.15<Φ≤0.2mm	1
		Φ>0.2mm	0
		The distance between any two spots should be ≥10mmAny spot/dot/void outside of viewing area is acceptable	
Minor	Protective film tilt	Not fully cover LCD	Reject
Major	COG coating	Not fully cover ITO circuit	Reject

8. Electric Inspection

Defect	Inspection Item	Inspection Standards	
Major	Short		Reject
Major	Open		Reject

9. Inspection Specification of LCD

Defect	Inspect Item		Inspection Standards			
Minor	Linear Defect	* Glass Scratch * Polarizer Scratch * Fiber and Linear material	W	W<0.03	0.03<W<0.05	W>0.05
			L	L<5	L<3	Any
			ACC. NO.	1	1	Reject
			Note	L is the length and W is the width of the defect		
Minor	Black Spot and Polarizer Pricked	* Foreign material between glass and polarizer or glass and glass * Polarizer hole or protuberance by external force	Φ	Φ≤0.1	0.1<Φ≤0.15	0.15<Φ≤0.2	Φ>0.2
			ACC. NO.	3EA /1PC	2	1	0
			Note	Φ is the average diameter of the defect.Distance between two defects > 10mm.			
Minor	White Spot and Bubble in polarizer	* Unobvious transparent foreign material between glass and glass or glass and polarizer * Air protuberance between polarizer and glass	Φ	Φ≤0.1	0.1<Φ≤0.15	0.15<Φ≤0.2	Φ>0.2
			ACC. NO.	3EA / 1PC	2	1	0
			Note	Φ is the average diameter of the defect.Distance between two defects > 10mm.			
Minor	Segment Defect		Φ	Φ≤0.10	0.10<Φ≤0.20	Φ>0.2
			ACC. NO.	3EA /1PC	2	0
			Note	W is more than 1/2 segment width		Reject
				$\Phi = \frac{L+W}{2}$ Distance between two defect is 10mm		
Minor	Protuberant Segment	 Φ = (L + W) / 2	Φ	Φ≤0.10	0.10<Φ≤0.20	Φ>0.2
			W	Glue	W≤1/2 Seg , W≤0.2	Ignore
			ACC. NO.	3EA /1PC	2	0
Minor	Assembly Mis-alignment		1. Segment			
			B	B≤0.4mm	0.4<B≤1.0mm	B>1.0mm
			B-A	B-A<1/2B	B-A<0.2	B-A<0.25
			Judge	Acceptable	Acceptable	Acceptable
			2. Dot Matrix			
			Deformation>0.35mm			Reject

Minor	Stain on LCD Panel Surface		Accept when stains can be wiped lightly with a soft cloth or a similar one. Otherwise, judged according to the aboveitems: “Black spot” and “White Spot”

9. Reliability:

NO.	Item	Condition	Criterion
1	High Temperature Operating	70℃, 96Hrs	No defect in cosmeticand operational function allowable. Total current Consumption shouldbe below double of initial value.
2	Low Temperature Operating	-20℃, 96Hrs	
3	High Humidity	40℃, 90%RH, 96Hrs	
4	High Temperature Storage	80℃, 96Hrs	
5	Low Temperature Storage	-30℃, 96Hrs	
6	Vibration	Random wave 10 ~ 100Hz Acceleration: 2g 2 Hrs per direction(X,Y,Z)	
7	Thermal Shock	-10℃ to 25℃ to 60℃ (60Min) (5Min) (60Min) 16Cycles	
8	ESD Testing	Contract Discharge Voltage: +1 ~ 5kV and –1 ~ –5kV	There will be discharged ten times at every discharging voltage cycle. The voltage gap is 1kV.
		Air Discharge Voltage: +1 ~ 8kV and –1 ~ -8kV	

Note: 1) Above conditions are suitable for XIN NUO YA standard products.

2) For restrict products, the test conditions listed as above must be revised.

10. Handling Precaution:

(1) Mounting Method

The panel of the LCD Module consists of two thin glass plates with polarizerswhich easily get damaged since the Module is fixed by utilizing fitting holes in the printed circuit board. Extreme care should be taken when handling
the LCD Modules.

(2) Caution of LCD handling & cleaning

When cleaning the display surface, use soft cloth with solvent (recommendedbelow) and wipe lightly.

- Isopropyl alcohol
- Ethyl alcohol
- Trichlorotrifloroethane

Do not wipe the display surface with dry or hard materials that will damage thepolarizer surface.

Do not use the following solvent:

- Water
- Ketone
- Aromatics

(3) Caution against static charge

The LCD Module use C-MOS LSI drivers, so we recommend that you connect any unused input terminal to VDD or VSS, do not input any signals before poweris turned on. And ground your body, Work/assembly table. And assembly equipment to protect against static electricity.

(4) Packaging

- Modules use LCD elements, and must be treated as such. Avoid intense shockand falls from a height.

- To prevent modules from degradation. Do not operate or store them exposeddirectly to sunshine or high temperature/humidity.

(5) Caution for operation

- It is indispensable to drive LCD's within the specified voltage limit since the higher voltage than the limit shorten LCD life. An electrochemical reaction due to direct current causes LCD deterioration, Avoid the use of direct current drive.

Handling Precaution (Continued):

- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show darkcolor in them. However those phenomena do not mean malfunction or out of order with LCD's.Which will come back in the specified operating temperature range.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the relative condition of 60□C, 90%RH or less is required.

(6) Storage

In the case of storing for a long period of time (for instance, for years) for thepurpose or replacement use, The following ways are recommended.

- Storage in a polyethylene bag with sealed so as not to enter fresh air outside in it,And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light is.

Keeping temperature in the specified storage temperature range.

- Storing with no touch on polarizer surface by the anything else. (It is recommendedto store them as they have been contained in the inner container at the time of delivery)

(7) Safety

- It is recommendable to crash damaged or unnecessary LCD into pieces and washoff liquid crystal by using solvents such as acetone and ethanol.

Which should be burned up later.

When any liquid crystal leaked out of a damaged glass cell comes in contact withyour hands, please wash it off well with soap and water.

11. Outline Dimensions: