MSP432P401R Device Erratasheet

1 Revision History

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev B
ADC44	✓
ADC45	✓
ADC46	✓
ADC47	✓
ADC48	✓
ADC49	✓
ADC51	✓
ADC52	✓
ADC53	✓
ADC54	✓
ADC55	✓
ADC56	✓
ADC57	✓
ADC58	✓
ADC59	✓
ADC60	✓
ADC61	✓
ADC62	✓
BSL13	✓
COMP8	✓
CS5	✓
CS6	✓
CS8	✓
DMA12	✓
FLASH38	✓
FLASH39	✓
FLASH40	✓
PCM1	✓
PCM2	✓
PMAP2	✓
PORT25	✓
PORT27	✓
PSS1	✓
PSS2	✓
REF3	✓
REF4	✓

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Errata Number	Rev B
REF7	✓
REF8	✓
RST1	✓
RST2	✓
RTC9	✓
RTC11	✓
RTC12	✓
RTC13	✓
SRAM1	✓
SRAM2	✓
SYS21	✓
SYSTICK1	✓
WDG7	✓

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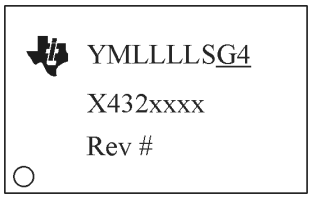
2 Package Markings

PZ100

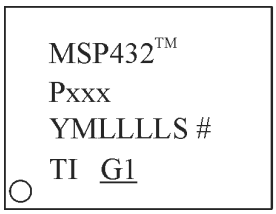
LQFP (PZ) 100 Pin



YM = Year and Month Date Code
S = Assembly Site Code
# = Die Revision
LLLL = Assembly Lot Code
○ = Pin 1

ZXH80

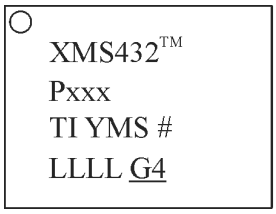
BGA, 80 Pin



YM = Year and Month Date Code
LLLL = Assembly Lot Code
S = Assembly Site Code
# = Die Revision
○ = Pin 1

RGC64

QFN (RGC), 64 pin



YM = Year and Month Date Code
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# = Die Revision
LLLL = Assembly Lot Code
○ = Pin 1

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3 Detailed Bug Description

ADC44 *ADC14 Module*

Function ADC stops converting during repeat-single-channel operation

Description The ADC module might hang if ADC14CTL0.ADC14ENC bit is reset during a repeat-single-channel operation. No subsequent triggers can start a conversion. Operation can only be restored after a module reset.

Workaround If a conversion needs to be stopped during a Repeat-Single-Channel conversion, reset both ADC14ENC & ADC14CONSEQ bits (ADC14CTL0.ADC14ENC = 0 & ADC14CTL0.ADC14CONSEQ =0) instead of just ADC14CTL0.ADC14ENC bit.

ADC45 *ADC14 Module*

Function Erroneous ADC busy bit value

Description ADC14CTL0.ADC14BUSY bit might not reflect true ADC busy state when the ADC is configured to use timer trigger source (ADC14CTL0.ADC14SHSx != 0) and the timer trigger arrives prior to ADC14CTL0.ADC14ENC bit being toggled.

Workaround 1. When timer is used as a trigger source, ensure to toggle the ADC14CTL0.ADC14ENC bit before the trigger arrives.

OR

2. Do not use ADC14CTL0.ADC14BUSY bit as completion indication. Instead use the conversion completion interrupt flag to service the interrupt upon conversion completion.

ADC46 *ADC14 Module*

Function Sequence of Channel conversion mode with temperature sensor and battery monitor

Description ADC Sequence & Repeat Sequence conversion modes generate wrong conversion results for all channels when either temperature sensor or battery monitor is selected as one of the channels in the sequence.

Workaround None.

ADC47 *ADC14 Module*

Function Byte write to ADC14MEMx registers

Description A byte write to ADC14MEMx register corrupts the entire 32-bit data content of the register.

Workaround None.

ADC48 *ADC14 Module*

Function Stopping sequence-of-channel conversion modes

Description In a sequence-of-channel or repeat-sequence-of-channel conversion mode, de-assertion of the ADC14CTL0.ADC14ENC bit stops ADC14 operation only at the end of a sequence of channels instead of at the end of the current channel conversion.

Workaround None.

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ADC49 *ADC14 Module*

Function Switching reference in sequence-of-channel conversion modes

Description When an ADC sampling sequence (in either sequence-of-channel or repeated-sequence-of-channel mode) transitions from a channel using internal reference to a channel using external reference, ADC14RDYIFG is incorrectly set for the channel using external reference and the ADC conversion for this channel generates erroneous conversion result.

Workaround None.

ADC51 *ADC14 Module*

Function ADC operation with internal reference

Description When the ADC uses the internal reference buffer (ADC14MCTLx.ADC14VRSEL=1) in the buffer continuously on mode (ADC14CTL1.ADC14REFBURST=0), the reference buffer is unavailable for 5us after ADC14CTL0.ADC14ON and ADC14CTL0.ADC14ENC bits are set. ADC operation triggered before this 5us window will result in incorrect values.

Workaround Wait for 5us after ADC14CTL0.ADC14ON and ADC14CTL0.ADC14ENC bits are set before starting any ADC operation.

ADC52 *ADC14 Module*

Function ADC14IV register read

Description If ADC14IV register is read while another ADC14IFGx bit is being set, the ADC14IV read does not clear the ADC14IFGx bit.

Workaround Manually clear the ADC14IFGx bit in software.

ADC53 *ADC14 Module*

Function DMA request in repeat sequence of channel

Description ADC14 does not assert DMA request at the end of each sequence of conversions in a repeat sequence of channels mode of conversion, resulting in no DMA transfer triggered.

Workaround None.

ADC54 *ADC14 Module*

Function ADC window comparison incorrect result in signed binary data format

Description ADC14IFG1.ADC14LOIFG is erroneously set if:

1) When signed binary data format is selected (ADC14CTL1.ADC14DF=1)

AND

2) ADC14LOx threshold value and the ADC14 conversion result value are both negative

AND

3) Conversion result is greater than the ADC14LOx threshold value.

Similarly, ADC14IFG1.ADC14HIIFG is erroneously set if:

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1) When signed binary data format is selected (ADC14CTL1.ADC14DF=1)

AND

2) ADC14HIx threshold value and conversion result are both negative

AND

3) Conversion result is lower than ADC14HIx threshold value.

Workaround None.

ADC55 *ADC14 Module*

Function REFOUT availability on pin during ADC operation

Description When the internal reference is output to a port pin (REFCTL0.REFOUT=1) and the ADC14 is converting an ADC channel using the AVCC reference, the ADC conversion results in incorrect values and the internal reference voltage is not available on the external REFOUT pin during ADC operation.

Workaround None.

ADC56 *ADC14 Module*

Function Extended sample pulse mode

Description In extended sample pulse mode (ADC14CTL0.ADC14SHP=0), ADC channel selection changes on the rising edge of the sample pulse. This may result in incorrect ADC conversion results. The issue occurs in single-conversion mode and only on the first conversion in a sequence or repeat mode of operations.

Workaround None.

ADC57 *ADC14 Module*

Function ADC operation in extended pulse sample mode

Description In low-speed ADC operation (ADC using 128-500kHz clock source) and extended pulse sample mode, conversion trigger might be missed during a time window consisting of the source oscillator starting up and two additional ADC cycles.

Workaround None.

ADC58 *ADC14 Module*

Function ADC14 ready flag not set in extended pulse mode in low-speed

Description ADC14 ready flag ADC14IFG1.ADC14RDYIFG does not get set after buffer is powered up when ADC is in buffered mode and extended pulse mode if the total time of (ADC clock start up time + 6 ADC clock cycles) exceeds 5us.

Workaround In extended pulse mode, delay 5us after sample time before de-asserting the trigger.

ADC59 *ADC14 Module*

Function ADC14MEMx registers writes with varying access sizes

Description Back-to-Back register writes to different ADC14MEMx registers with varying access sizes (any combinations of 32-bit, 16-bit, and 8-bit accesses) could corrupt the register data.

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Workaround Always use the same access size when writing to ADC14MEMx registers back-to-back.

ADC60 *ADC14 Module*

Function Changing buffer mode in sequence-of-channel conversion modes

Description During a sequence of channel, the ADC conversion result for the second conversion of any consecutive pair will be erroneous if:

1) ADC14CTL0.ADC14SHP = 1 and ADC14CTL0.ADC14MSC = 1,

AND

2) The first channel in the consecutive pair uses non-buffered mode,

AND

3) The second channel in the consecutive pair uses buffered mode.

Workaround Add a dummy channel using buffered mode in between the two channels and disregard the conversion result for this dummy channel.

ADC61 *ADC14 Module*

Function Changing buffer mode in sequence-of-channel conversion modes

Description The ADC conversion results in a sequence or repeat sequence mode of operation will be erroneous if:

1) (ADC14CTL0.ADC14MSC = 0 and ADC14CTL1.ADC14REFBURST =0) or ADC14CTL0.ADC14MSC =1

AND

2) external reference buffered mode and internal reference modes used as consecutive channels

Workaround Add a dummy channel using buffered mode in between the two channels and disregard the conversion result for this dummy channel.

ADC62 *ADC14 Module*

Function Insufficient trigger width in extended sample mode

Description ADC can generate incorrect conversion results in extended sample mode, if the trigger width is less than:

1) 8 MODOSC cycles if MODOSC clock is already active (CSCLKEN.MODOSC_EN = 1).

OR

2) 8 MODOSC cyles + MODOSC startup time if MODOSC clock is not always on (CSCLKEN.MODOSC_EN = 0).

Workaround When using ADC in extended sample mode, ensure trigger width is equal or more than:

1) 8 MODOSC cycles if MODOSC clock is always on (CSCLKEN.MODOSC_EN = 1).

OR

2) MODOSC startup time + 8MODOSC cycles if MODOSC clock is not always on (CSCLKEN.MODOSC_EN = 0).

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BSL13 *BSL Module*

Function BSL scans all three interfaces even when configured to use one

Description BSL re-configures the module register settings of all three serial interfaces and scans for serial communication on these three interfaces even when BSL is configured to use only one interface.

Workaround None.

COMP8 *COMP_E Module*

Function Reference module enabled when comparator not used

Description The shared reference module is erroneously enabled in static mode operation if the comparator module is configured to use the shared reference (CECTL2.CERFLx=1 or 2 or 3) with or without the resistor ladder (CECTL2.CERSELx=2 or 3) even if the comparator module is disabled (CECTL1.CEON=0). This also override any reference sample mode request.

Workaround Disable the reference source for the comparator (CECTL2.CERSELx=0) when not using the comparator.

CS5 *CS Module*

Function DCO failure in external resistor mode

Description The DCO might overshoot and get stuck at high frequency (>110MHz) if interference or disturbance occurs on the DCO external resistor pin.

Workaround None.

CS6 *CS Module*

Function DCO overshoot when switching to external resistor mode

Description The DCO might overshoot and get stuck at higher frequency (>110MHz) when switching from internal resistor (IR) mode to external resistor (ER) mode in RSEL=5 mode (CSCTL0.DCORSELx = 5) irrespective of the frequency to which the DCO is tuned in RSEL=5 mode.

Workaround Switch from IR mode to ER mode at lower frequency range (CSCTL0.DCORSELx <= 4).

CS8 *CS Module*

Function Unreliable DCO operation during DCO external resistor short

Description Unreliable DCO operation can occur if the ROSC pin gets shorted to ground during run-time before DCO can switch to the internal resistor-based fail-safe mode. If MCLK is sourced by DCO, this could cause the device to hang.

Workaround None.

DMA12 *DMA Module*

Function Multiple DMA interrrupts

Description When the DMA cycle for a channel is complete, the DMA internally disables that

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channel. If DMA receives another trigger on this disabled channel before the completion interrupt is serviced, additional interrupts might be observed.

Workaround 1. Set DMA trigger source as the last step in DMA configuration routine.

And

2. In DMA ISR, disable DMA trigger source first.

FLASH38 *FLASH Module*

Function Application Benchmarking Counter counts all non-flash access in Buffered Read Mode

Description When FLCTL_RDCTL_BNKx.BUFD or FLCTL_RDCTL_BNKx.BUFI bit is set, the application benchmark counter counts all data or instruction accesses made to the flash memory including the accesses accounted by the 128-bit flash buffer. Since the counter does not exclude the buffer accesses, it does not reflect the actual flash accesses, which will be lower than the amount reported.

Workaround None.

FLASH39 *FLASH Module*

Function Re-programming same memory fails with pre-verify enabled

Description The word programming is aborted for these conditions:

1)The pre-verify option is enabled (FCTL_PRG_CTLSTAT.VER_PRE = 1).

AND

2) The location is already programmed with parity = 0.

AND

3) The new word parity is also 0.

Workaround Disable the program pre-verify option (FCTL_PRG_CTLSTAT.VER_PRE = 0).

FLASH40 *FLASH Module*

Function Burst program across bank-boundaries

Description When pre-verify is enabled and a burst program is initiated across bank-boundaries, the memory locations in the first bank are not programmed.

Workaround Use DriverLib API for Flash programming, FlashCtl_programMemory. The API includes the workaround to ensure proper programming mode across all Flash memory addresses.

PCM1 *PCM Module*

Function False interrupt when switching to DC-DC mode

Description The DC-DC error interrupt flag (PCMIFG.DCDC_ERROR) might get erroneously triggered when the device switches from LDO regulator to DC-DC regulator.

Workaround After DC-DC switching operation is complete, as indicated by PCMCTL0.PMR_BUSY bit being reset, clear the PCMIFG.DCDC_ERROR flag. Ensure VCC supply voltage meets the requirements for DC-DC operation per datasheet prior to switching from LDO to DC-DC regulator.

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PCM2 — *PCM Module*

Function Incorrect SRAM and ROM access during VCORE changes

Description Data accesses including reading from ROM and reading/writing to SRAM can be erroneous during VCORE change transition (from VCORE level 0 to 1 or vice versa).

Workaround Avoid all SRAM/ROM access during all VCORE transitions.

PMAP2 — *PMAP Module*

Function Unlocked PMAP module prevents LPM3/4/3.5/4.5 entrance

Description If the port mapper module is left unlocked after register configuration, the device is prevented from entering LPM3, LPM4, LPM3.5, and LPM4.5 modes in polite mode.

Workaround None.

PORT25 — *PORT Module*

Function RSTnNMI pin in NMI mode

Description When the RSTnNMI pin is configured with NMI functionality, the glitch filter is erroneously enabled. This prevents pulses with width<20ns from triggering an NMI in Active mode or waking up the device from low power modes (LPM0, LPM3).

Workaround None.

PORT27 — *PORT Module*

Function Wakeup from LPM

Description Interrupt wake-up from a port pin does not occur in low-power modes if the corresponding PxIFG flag is set prior to LPM entry.

Workaround Clear PxIFGs prior to entry to low power mode.

PSS1 — *SVS Module*

Function Reset triggered by SVSMH/SVSL

Description Spurious reset may be triggered when SVSMH/SVSL is disabled and then enabled again in software, or if device enters LPM4.5 mode after SVSL is disabled in software.

Workaround

1. For SVSMH:

- Never disable SVSMH if the function is required in the application.

- Disable SVSMH permanently at the beginning of the application code if the functionality is not required.

2. For SVSL:

- Never disable SVSL if application requires LPM4.5 entry or SVSL functionality.

- Disable SVSL permanently at the beginning of the application code if application does not use SVSL and does not enter LPM4.5 mode.

PSS2 — *PSS Module*

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Function	Power Supply System High-Side Reset
Description	A PSS High-Side reset occurs if device enters LPM3/LPM3.5 mode with SVSM high-side reset voltage level (SVSMCTL.SVSMHTHx) is set to 0x6 or 0x7. The SVSH flag in the RSTCTL_PSSRSTSTAT register is set.
Workaround	Use SVSMCTL.SVSMHTHx=[0-5] settings if application requires to enter LPM3/LPM3.5 mode.

REF3 *REF Module*

Function	Increased reference voltage temperature variation
Description	The temperature variation for the reference voltage is higher than specification, with temperature co-efficient increased up to 30-40 ppm/degree Celsius.
Workaround	None.

REF4 *REF Module*

Function	REFGENBUSY status bit
Description	The REFCTL0.REFGENBUSY bit is set when the ADC is configured to use the reference module in buffered mode (ADC14MCTLx.ADC14VRSEL= 1) even when the ADC is not actively converting.
Workaround	None.

REF7 *REF Module*

Function	REFOUT functionality not available on pin
Description	The internal reference voltage is not available on VREF pin unless both ADC module is enabled (ADC14CTL0.ADC14ON=1) and the internal reference is selected (ADC14MCTLx.ADC14VRSEL=1). The erroneous behavior occurs even when the reference module is on (REFCTL0.REFON=1) and output to a pin (REFCTL.REFOUT=1).
Workaround	1) Turn on the reference module (REFCTL0.REFON=1) AND 2) Enable the reference output pin (REFCTL0.REFOUT=1). AND 3) Enable the ADC 14 module (ADC14CTL0.ADC14ON=1). AND 4) Select the internal reference for one ADC channel (ADC14CTL1.ADC14CSTARTADD=x & ADC14MCTLx.ADC14VRSEL=1).

REF8 *REF Module*

Function	Reference ready status prematurely enabled
Description	The reference buffer ready status bit (REFCTL0.REFBGRDY or REFCTL0.REFGENRDY) might be triggered before the low-power buffer or reference buffer has settled.

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Workaround Insert a 50us delay after REFCTL0.REFBGRDY or REFCTL0.REFGENRDY bit is set before using the reference buffer for comparator or ADC operation.

RST1 *RSTCTL Module*

Function LPM3.5 and LPM4.5 status bits not reset on RSTNMI pin interrupt.

Description LPM3.5 and LPM4.5 status bits (RSTCTL_PCMRSTSTAT_REG.LPM35 and RSTCTL_PCMRSTSTAT_REG.LPM45) might not get reset after LPMx.5 wake-up triggered by an IO wake-up on RSTNMI pin interrupt.

Workaround Clear RSTCTL_PCMRSTSTAT_REG.LPM35 and RSTCTL_PCMRSTSTAT_REG.LPM45 status bits after RSTNMI pin wake-up from LPMx.5 power mode.

RST2 *RSTCTL Module*

Function LPM4.5 bit in RSTCTL_PCMRESET_STAT not cleared

Description The LPM4.5 bit in RSTCTL_PCMRESET_STAT (set after waking up from LPM4.5) cannot be cleared (by setting RSTCTL_PCMRESET_CLR.LPM45 bit) until after the PCMCTL0.LOCKLPM5 bit is cleared.

Workaround After LPM4.5 wake up, clear PCMCTL.LOCKLPM5 bit before clearing the LPM4.5 flag by setting RSTCTL_PCMRESET_CLR.LPM45 bit.

RTC9 *RTC_C Module*

Function RTCRDYIFG may cause unexpected wake-up from LPM3.5

Description RTCRDYIFG is not an LPM3.5 wake-up interrupt source. However due to the erratum, when the device is placed in LPM3.5 and RTCRDYIE is enabled, RTCRDYIFG being set can cause an inadvertent wake-up from LPM3.5.

Workaround Do not enable RTCRDYIE before the device is placed in LPM3.5

RTC11 *RTC_C Module*

Function RTC interrupt service after wake-up from LPM3.5

Description After device wakes up from LPM3.5 triggered by an RTC event, the device enters the RTC ISR when the NVIC is configured for RTC interrupt even when the RTC interrupt enable bits (RTCCTL0.RTCOFIE, RTCCTL0.RTCTEVIE, RTCCTL0.RTCAIE, RTCPS1CTL.RT1PSIE) are not set.

Workaround None.

RTC12 *RTC_C Module*

Function Real-time clock temperature compensation RTCTCOK bit not retained after LPM3.5 wake up

Description The RTC real-time clock temperature compensation write OK bit (RTCTCMP.RTCTCOK) is reset on wake up from LPM3.5 mode and does not get retained.

Workaround Store the RTCTCMP register content into Flash content or SRAM bank 0 for retention after wake up from LPM3.5

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RTC13 — *RTC_C Module*

Function Device enters LPM3 mode even when RTCCLK is output to a port pin

Description Device enters LPM3 mode even when RTCCLK is output to an external port pin of the device.

Workaround None.

SRAM1 — *SRAM Module*

Function SRAM access stalled when core voltage level changed

Description When the core voltage level is changed from 0 to 1, SRAM access is stalled for ~600ns after the transition is complete.

Workaround Insert a 600ns delay after the core voltage transition is complete (PCMCTL1.PMR_BUSY bit is clear). 3 SYSOSC cycles can be used for the 600ns delay.

SRAM2 — *SRAM Module*

Function SRAM bank enable and retention ready bits not set

Description The SRAM ready bits (SYS_SRAM_BANKEN.SRAM_RDY/SYS_SRAM_BANKRET.SRAM_RDY) are not set if both conditions apply:

1. The SRAM bank enable or retention bits are modified (SYS_SRAM_BANKEN/SYS_SRAM_BANKRET) .

2. A POR-class reset occurs prior to SRAM operation completion, which is indicated by the SRAM ready bits getting set.

Workaround None.

SYS21 — *SYS Module*

Function Write access to SYSCTL registers in low power modes

Description Debugger write access to the SYSCTL registers is not possible when the device is in LPM0 or LPM3.

Workaround None.

SYSTICK1 — *SYSTICK Module*

Function CLKSOURCE selection bit of Systick register-SCS_STCSR is read-writeable

Description The CLKSOURCE bit of SCS_STCSR (SYSTICK control and status register) is read/write-able instead of read-only. Do not write 0 to the SCS_STCSR.SCS_STCSR_CLKSOURCE bit since the device does not support external reference clock.

Workaround None.

WDG7 — *WDT_A Module*

Function Watchdog function when switching clock source

Description The watchdog timer module stops working when switching clock source from

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VLOCLK/BCLK to any other clock source.

Workaround None.

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4 Document Revision History

Changes from device specific erratasheet to document Revision A.

1. Errata ADC48 was added to the errata documentation.
2. Errata ADC46 was added to the errata documentation.
3. Errata ADC49 was added to the errata documentation.
4. Errata FLASH38 was added to the errata documentation.
5. Errata ADC47 was added to the errata documentation.
6. Errata DMA12 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. PSS1 Description was updated.
2. Errata REF8 was added to the errata documentation.
3. SYS21 Description was updated.
4. Errata RTC11 was added to the errata documentation.
5. Errata RST2 was added to the errata documentation.
6. SYS22 Description was updated.
7. PSS1 Workaround was updated.
8. Errata PCM1 was added to the errata documentation.
9. Errata CS8 was added to the errata documentation.
10. Errata USCI36 was removed from the errata documentation.
11. SYS21 Function was updated.
12. Errata FLASH39 was added to the errata documentation.
13. Errata ADC58 was added to the errata documentation.
14. SYS24 Description was updated.
15. SYS22 Function was updated.
16. SYS24 Function was updated.
17. Errata PORT25 was added to the errata documentation.
18. Errata PSS2 was added to the errata documentation.
19. Errata REF7 was added to the errata documentation.
20. Errata COMP8 was added to the errata documentation.
21. Silicon Revision B was added to the errata documentation.
22. Errata RST1 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. Errata ADC61 was added to the errata documentation.
2. Errata BSL13 was added to the errata documentation.
3. Errata RTC12 was added to the errata documentation.
4. Errata SRAM1 was added to the errata documentation.
5. Errata ADC51 was added to the errata documentation.
6. RST1 Description was updated.
7. Errata ADC57 was added to the errata documentation.
8. Errata PMAP2 was added to the errata documentation.
9. Errata ADC55 was added to the errata documentation.
10. Errata ADC56 was added to the errata documentation.
11. Errata ADC53 was added to the errata documentation.
12. Errata CS5 was added to the errata documentation.
13. Errata ADC52 was added to the errata documentation.

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14. Errata PORT27 was added to the errata documentation.
15. Errata SYSTICK1 was added to the errata documentation.
16. Errata PCM2 was added to the errata documentation.
17. Package Markings section was updated.
18. Errata ADC54 was added to the errata documentation.
19. Errata CS6 was added to the errata documentation.
20. Errata FLASH40 was added to the errata documentation.
21. RST1 Workaround was updated.
22. Errata ADC59 was added to the errata documentation.
23. RST1 Function was updated.

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