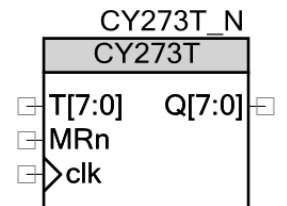


Octal T-Type Flip-Flop with Reset

CY273T v1.0

Features

- Common synchronous clock
- Common asynchronous reset
- Eight positive edge triggered T-type flip-flops
- Simple to deconstruct



General Description

This flip-flop is based on a component that was never built, but should have been. T flip-flops are very useful in the synthesis of sparse matrix state machines. This component has eight edge-triggered, T-type flip-flops with individual T inputs and Q outputs. The common clock (clk) and master reset (MRn) inputs load and reset (clear) all flip-flops simultaneously. All outputs are forced LOW independently of clock or data inputs by an active LOW to the MRn input.

This component was built as a teaching tool. This classic component's operation is well understood and this datasheet's function is to help understand how it was built through its deconstruction.

Pin Description

Pin	Type	Function
T[7:0]	inputs	data inputs
MRn	input	master reset input (active low)
clk	input	clock input
Q[7:0]	outputs	Flip-flop outputs

Function Table

Operating Modes	Inputs			Outputs
	MRn	clk	Tx	Qx
reset	0	x	x	0

Operating Modes	Inputs			Outputs
	MRn	clk	Tx	Qx
load	1	↑	0	Qx
	1	↑	1	~Qx

Deconstructing the Component

This example shows that with a couple simple changes of a single datapath instruction that a component can be changed from a octal D-type flip-flop to an octal T-type flip-flop. This component requires that the parallel input data be the permanent input to the left side of the ALU (ASRC). If you do not understand how this is done then first review the CY273 component. It also shows how to route a serial input into a register.

The parallel out (PO) interface is always available and connects to either A0 or A1. The parallel in (PI) interface must be routed into the left input of the ALU (ASRC). If the PI_SEL bit (CFG15.7) is set, the PI is the permanent input to ASRC.

The toggle operation is implements by taking the register (AO) and XOR with the parallel input data. The datapath instruction will implement this.

For this counter there are two different operations.

- Reset
- Load

While the reset operation will be handled with datapath reset circuitry, the load operation needs to be implemented with a datapath instruction.

Using PSoC Creator, open the CY273T example project to see the project schematic (*TopDesign.cysch*). It has a CY273T component connected to input switches, output LEDs, and a clock.

In the Workspace Explorer, click the **Components** tab. Then, right-click on the project and select **Import Component**. Navigate to where the CYCC_SimpleComponentLibrary project is, and select the CYCC_CY273T_v1_0 component. Click **OK** and the following files are shown for the component:

- Symbol file (cysym)
- Datasheet (pdf)
- Verilog File (v)

Open the symbol file to find a symbol with three inputs and one output. It looks like the symbol shown on the first page. There are no additional symbol parameters.

Open the Verilog file and notice that at lines 24 – 27, these definitions were passed to this Verilog file when it was created. The first 25 lines of this header list register usage and the datapath instruction definitions.

There is a need for intermediate signals and this is handled in lines 31 - 32. What follows is the datapath module definition. It was created and inserted by the Datapath Configuration Tool. This information is backward compatible so opening up the Datapath Configuration Tool for this Verilog file results in the following.

The screenshot shows the Datapath Configuration Tool interface. The 'Configuration' dropdown is set to 'OctalTs'. The 'CFGGRAM' tab is active, displaying a table of instructions. The first row is highlighted with a red circle around the 'XOR' value in the 'FUNC' column. Below this, other tabs like 'CFG9', 'CFG11-10', 'CFG13-12', 'CFG15-14', and 'CFG17-16' are visible. In the 'CFG15-14' tab, the 'PI SEL' field in the first row is circled in red.

Reset	Reg	Binary Value	FUNC	SRC A	SRC B	SHIFT	A0 WR SRC	A1 WR SRC	CFB EN	CI SEL	SI SEL	CMP SEL	Comment
	Reg0	10101000 01000000	XOR	A0	A0	PASS	ALU	NONE	DSBL	CFGA	CFGA	CFGA	load po = A0 = A0 XOR pi
	Reg1	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	NA
	Reg2	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	NA
	Reg3	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	NA
	Reg4	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	NA
	Reg5	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	NA
	Reg6	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	NA
	Reg7	00000000 00000000	PASS	A0	D0	PASS	NONE	NONE	DSBL	CFGA	CFGA	CFGA	NA

Reset	AMASK Value	A [7]	A [6]	A [5]	A [4]	A [3]	A [2]	A [1]	A [0]	Unused	Comment
FF		1	1	1	1	1	1	1	1	00000000	

Reset	CMASK1 Value	CMASK0 Value	C1 [7]	C1 [6]	C1 [5]	C1 [4]	C1 [3]	C1 [2]	C1 [1]	C1 [0]	C0 [7]	C0 [6]	C0 [5]	C0 [4]	C0 [3]	C0 [2]	C0 [1]	C0 [0]	Comment
FF	FF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Reset	Binary Value	CMP SELB	CMP SELA	CI SELB	CI SELA	CMASK1 EN	CMASK0 EN	A MSK EN	DEF SI	SI SELB	SI SELA	Comment
	00000000 00000000	A1_D1	A1_D1	ARITH	ARITH	DSBL	DSBL	DSBL	DEF_0	DEFSI	DEFSI	

Reset	Binary Value	PI SEL	SHIFT SEL	PI DYN	MSB SI	F1 INSEL	F0 INSEL	MSB EN	MSB SEL	CHAIN CMSB	CHAIN FB	CHAIN 1	CHAIN 0	Comment
	10000000 00000000	PIN	SL			BUS	BUS	DSBL	BIT0	NOCHN	NOCHN	NOCHN	NOCHN	

Reset	Binary Value	Unused [15:13]	ADD SYNC	Unused [11:10]	F1 DYN	F0 DYN	F1 CK INV	F0 CK INV	FIFO FAST	FIFO CAP	FIFO EDGE	FIFO ASYNC	EXT CRCPRS	WRK16 CONCAT	Comment
	00000000 00000000	000		00					DP	AX	LEVEL	SYNC	DSBL	DSBL	

Note that there is only a single instruction and it requires parallel data input. The PI_SEL bit has been enabled so the parallel input is the permanent ASRC input to the ALU.

For the load instructions the parallel input is XORed with A0 and placed back in A0.

When saved, this tool inserts the updated configuration data back into the Verilog file along with an instance of the datapath interface. Just pass the correct signals in to and out of it and you are

done. This counter parameter list may look ominous but only a few parameters have to be entered as shown below.

```
/* input          */ /* .reset(reset), // Connect reset to datapath
/* input          */ /* .clk(clk), // Connect clock to datapath
/* input [02:00] */ /* .cs_addr(3'b0), // Only one instruction (REG0) is used
/* input [07:00] */ /* .pi(T[7:0]), // Connect parallel data to datapath
/* output [07:00] */ /* .po(Q[7:0]) // Connect datapath to parallel output
```

These parameters do the following:

- Connect a reset signal to the datapath reset circuitry
- Connect a clock signal to the datapath clock circuitry
- Allows only a single instruction to be continuously processed
- Connect the parallel input to the datapath PI
- Connect the datapath PO to the parallel output

Support

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