

# Isaac Garibay

760-576-6829 | [isaacxg59@gmail.com](mailto:isaacxg59@gmail.com) | Santa Cruz, CA | [LinkedIn](#)

## EDUCATION

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**University of California, Santa Cruz**

*B.S. Computer Engineering*

Santa Cruz, CA

2025

## RELEVANT COURSEWORK

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- Data Structures/Algorithms, Circuit Analysis, Signals Systems, Principles of Systems Design, Computer Networks, Logic Design, Embedded Systems Design, VLSI Design, Intro to Software Engineering

## EXPERIENCE

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**Google - SWE Open Source Internship**

September 2023 – November 2023

*Timesketch Open Source Project*

- Contributed to Timesketch, a collaborative forensic timeline analysis platform for cybersecurity teams, with [2.7k GitHub stars](#)
- Investigated and resolved issue #255 involving inconsistencies in the timestamp feature's robustness.
- Unit tests were to ensure no further regression in the project occurs after patches in project and timestamps were properly being populated with compatible formats

**CSE Lab Tutor**

September 28, 2024 – Present

*University of California, Santa Cruz*

- Consulted on mastering logic design fundamentals at the register-transfer-level in SystemVerilog.
- Guided others in designing embedded systems software for ESP32 microcontrollers with C/C++
- Encouraged independent problem-solving skills to build a strong foundation in hardware-software integration

**Undergraduate Researcher**

September 23, 2024 – Present

*University of California, Santa Cruz*

- Collaborated on optimizing the conversion of SPICE netlists describing SKY130 PDK logic cells into scalable vector graphics (SVG) for high-quality schematics.
- Explored IoT solutions by integrating the ESP-WROOM-E microcontroller with Lattice FPGA chips, using Wi-Fi backscatter as a low-power solution for data transfer and device communication
- Performed testing and debugging of the ULX3S development board to meet project specifications

**Mentorship with Cisco Meraki**

June 2022 – December 2022

*Import-Export Logistics Division*

- Gained insights into import-export logistics processes while working closely with a project manager
- Developed a strong understanding of data management using Snowflake tools in a professional environment
- Learned essential best practices for communication and organization in a corporate setting

## PROJECTS

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**Multi-Threaded HTTP Server:** Constructed a httpserver in C to handle several concurrent GET and POST requests with reader/Writer locks and thread safe queue to implement a dispatcher/worker thread pooling design

**32-bit Ibex Core Chip Design:** Using the Openlane2 design flow, I implemented a chip design for the RISC-V [32-bit Ibex Core](#) from the layout and placement of SRAM macros, global/local wire routing, pin placement, and ensuring that timing using static timing analysis tools with NgSpice

**ESP32c3 Weather Station:** Using Python in Pythonista, a mobile IDE for IOS, I created a server to make http queries to interact with ipify and geolaction API's and serve a http client implemented in C flashed onto the ESP32c3 to generate a report on current weather conditions relative to the region where the client's ip was assigned

## TECHNICAL SKILLS

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**Languages:** C, C++, Python, SystemVerilog

**Tools:** ESP-IDF toolchain, CMake, I2C, Docker, Nix-shell, Git, GitLab, Jira, Wireshark, KLayout, OpenROAD/OpenLane, ngspice