

Bradley Manzo

Santa Cruz, CA 95060

bmanzo@ucsc.edu | Mobile: (951) 314-7983 | linkedin.com/in/bradley-r-manzo

Education:

University of California, Santa Cruz

September 2024 - Current

- Master of Science in Computer Science and Engineering
- Expected Graduation Spring 2026

GPA: 3.66/4.00

University of California, Davis

September 2019 - December 2023

- Bachelor of Science in Computer Engineering, Minor in Technology Management GPA: 3.43/4.00

Relevant Coursework: VLSI, Digital ICs, Embedded Systems, Circuits I and II, Applied ML

Work Experience:

University of California, Santa Cruz, CA

September 2024 - Current

Teaching Assistant

- Leading students in lab section, hosting office hours, grading and preparing instruction material.
- Instructing subjects including Embedded System Design Lab and Intro to Computer Networks.

Tiami Networks, Elk Grove, CA

January - April 2024

FPGA Networking Engineering Intern

- Implemented 5G NR Stack in hardware for SSB Detection using Intel's DSP Builder in Simulink.
- Designed and pipelined components such as peak detectors, correlational filters, and accumulators.

Hewlett Packard Enterprise, Roseville, CA

June - September 2023

ASIC-SDK Engineering Intern

- Collaborated with HPE Networking Engineers to identify the cause of faulty wired network link.
 - Developed internal tests using Python and designed an ML model using the TensorFlow library.
 - Designed a deep learning model exhibiting 86% accuracy, while the remaining 14% was within an acceptable margin of error.
-

Projects:

FPGA-Based Tensor Processing Unit

January - December 2023

- Led a group of four in designing a configurable FPGA-based TPU. Built around a systolic array synthesized in Verilog and communicated with through a custom driver program developed in C.
- TPU capable of sparse and dense matrix multiplication up to 4096x4096, 4x faster than software.
- Awarded Outstanding Senior Design by the UC Davis Electrical and Computer Engineering Dept.

Full Custom VLSI Chip Design

November - December 2023

- Designed a sliding window filter using Magic VLSI which returns the largest of four 12-bit values.
 - Laid out 0.18 μm CMOS with a core area of 24,291 μm^2 and top-level delay of 6.61 ns.
-

Leadership Experience:

UC Davis Triathlon Club President

June 2023 – June 2024

- Led a team of 12 officers, oversaw and facilitated all club logistics and operations.
 - Communicated with campus, our coach, other officers, and athletes through emails and meetings.
 - Upheld UC Davis and club policies and maintained an equitable and welcoming environment.
-

Skills:

Digital Design: Hardware acceleration using Quartus Verilog, DSP design using MATLAB Simulink.

Programming: C/C++, Python, TensorFlow, Chisel, Scala, Scripting, UNIX.

General: Effective communicator, written and verbal. Highly collaborative and resourceful leader.