# Front End Simulation Report

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## Summary

The purpose of this report is to outline the front-end design of the digital storage oscilloscope (DSO) and show it meets the specifications and outline expected performance.

The front-end design includes circuitry from the BNC input up until the input to the ADC.

| # | Specification | Criteria Met |
|---|---|---|
| **1.0.0** | The device will have one analogue input. | ✓ |
| **1.0.1** | The input will be through a BNC connector | ✓ |
| **1.0.2** | The input will have a 1MΩ ± 10% input impedance from DC to 10kHz. | ✓ |
| **1.0.3** | The input must have impedance between 10 kHz and 30 MHz of greater than 100 ohms. | ✓ |
| **1.0.4** | The input will have an input capacitance of less than or equal to 60pF | ✓ |
| **1.0.5** | The BNC input can accept a maximum input of ±5.6V after which the input voltage is clamped. | ✓ |
| **1.0.6** | The signal path from the BNC input to the ADC shall be DC coupled. | ✓ |
| **1.0.7** | An anti-aliasing filter appropriate to the 40MSPS maximum sample rate must be implemented with a minimum of a first-order 20dB per decade response and ±2dB maximum ripple in the pass band. | ✓ |
| **1.0.8** | All passive components must be selected from the values supplied in the passive components list to achieve the closest possible match to desired filter response. | ✓ |

Simulations in this report show that the design is able to meet the specifications. Namely that a +/-5V input signal to the BNC is converted to a 1.5V to 3.5V signal at the ADC input. Voltage clipping diodes protect the circuit in the case that high voltages are applied.
The filter design shows a flat pass band (<2dB ripple) and cut-off frequency at 20Mhz. Moreover the input impedance is 1Mohm for frequencies less than 10Khz and greater than 100ohms up to 30Mhz.

Although this design meets the specifications in simulation, there are a number of potential issues that may affect the performance of the circuit when realised.

1. The tolerance of selected components is +-10%. Simulation shows that the ADC input signal is affected by this variation up to 200mV in some key components. Trimpots have been placed in critical positions, however there is likely to still be deviation from the expected 1.5-3.5V range
2. ADC sampling rate (40MSPS) only just meets the required Nyquist criterion for a 20Mhz oscilloscope. As a result, higher frequency inputs are likely to contain more noise than lower frequency components.

3. Parasitic capacitances are likely to exist in real components that have not been modelled in simulation. This could affect the cut-off frequency of the anti-aliasing filter and the attenuation circuit at higher frequencies.

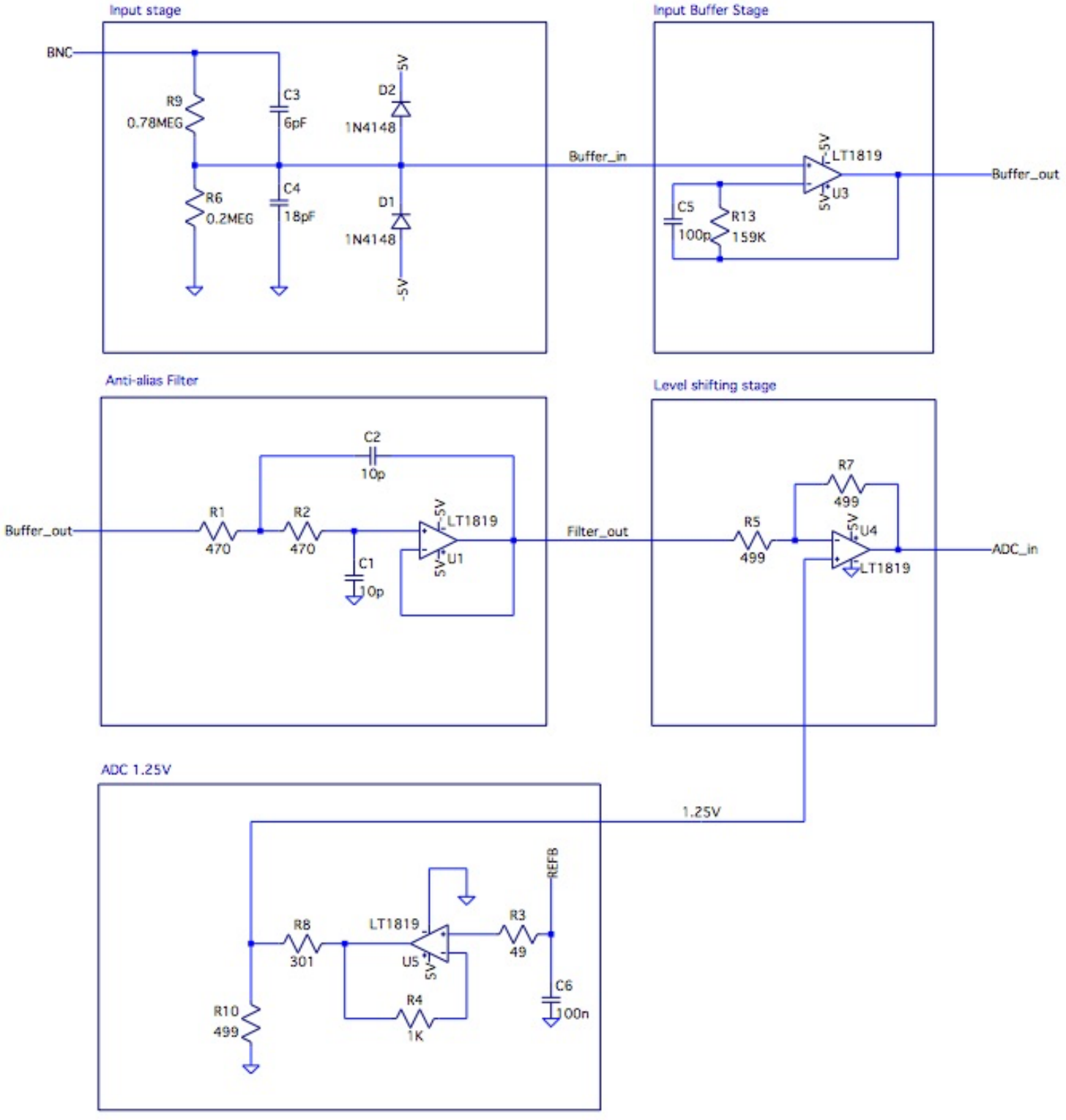
Some elements of the design are more robust.

1. Input impedance and capacitance should be resilient to variations in component values as they both exceed specifications
2. This protection circuit should be effective for any reasonable over voltage range given the diodes can withstand a forward current of up to 0.3A.

## Schematic

The schematic below shows the following design criteria have been met. All resistance/capacitance values were selected after considering parallel and series combinations of available components.

| | |
|---|---|
| **1.0.0** | The device will have one analogue input. |
| **1.0.1** | The input will be through a BNC connector |
| **1.0.6** | The signal path from the BNC input to the ADC shall be DC coupled. |
| **1.0.8** | All passive components must be selected from the values supplied in the passive components list to achieve the closest possible match to desired filter response. |

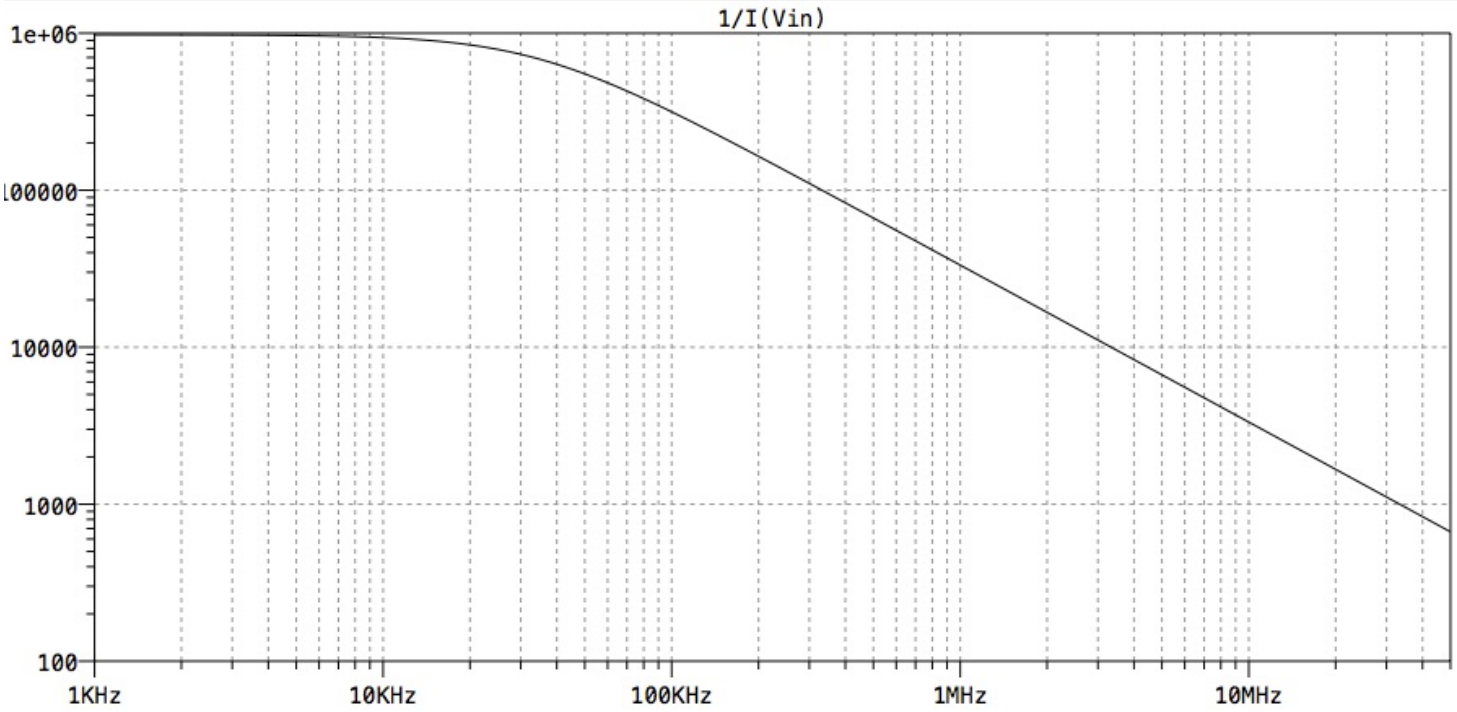


## BNC input

### Input impedance

| | |
|---|---|
| **1.0.2** | The input will have a 1MΩ ± 10% input impedance from DC to 10kHz. |
| **1.0.3** | The input must have impedance between 10 kHz and 30 MHz of greater than 100 ohms. |

The following plot shows the input impedance as a function of frequency. Input impedance is 936Kohms at 10Khz and 1.12Kohms at 30Mhz. Both values exceed specification limits therefore 1.0.2 and 1.0.3 have been met.



## Input capacitance

### 1.0.4 The input will have an input capacitance of less than or equal to 60pF

Input capacitance was calculated analytically and verified in simulation to be approx. 4.5pF. As 4.5pF is much less than 60pF, specification 1.0.4 has been satisfied.

*Analytic approach*

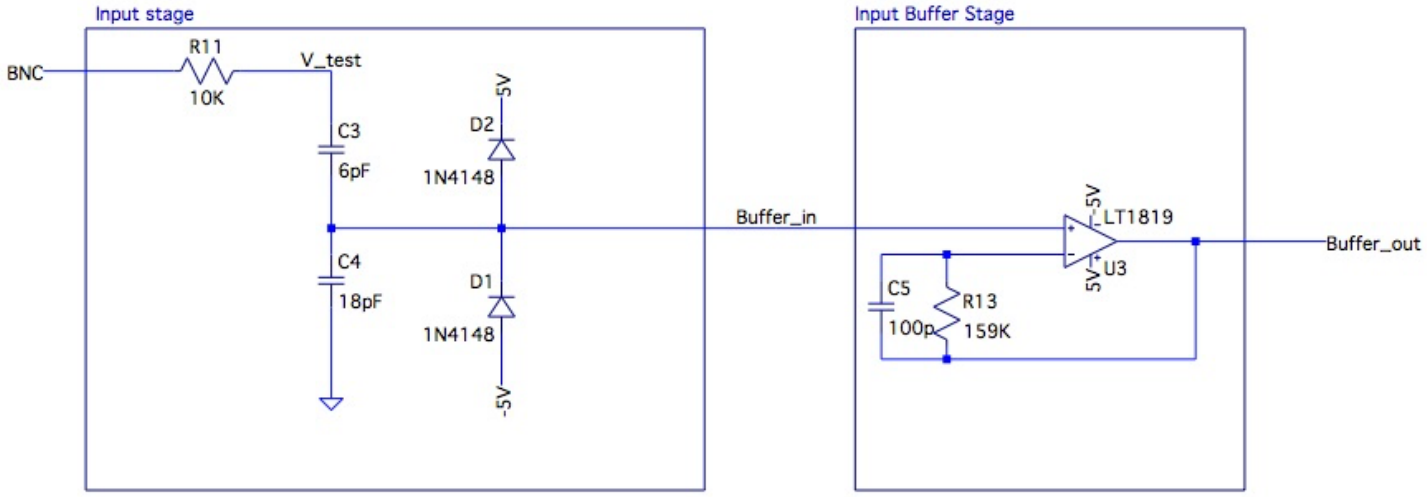
$$C_{TH} = 18p + 2p + 2p + 5.5p$$
$$= 23.5p$$

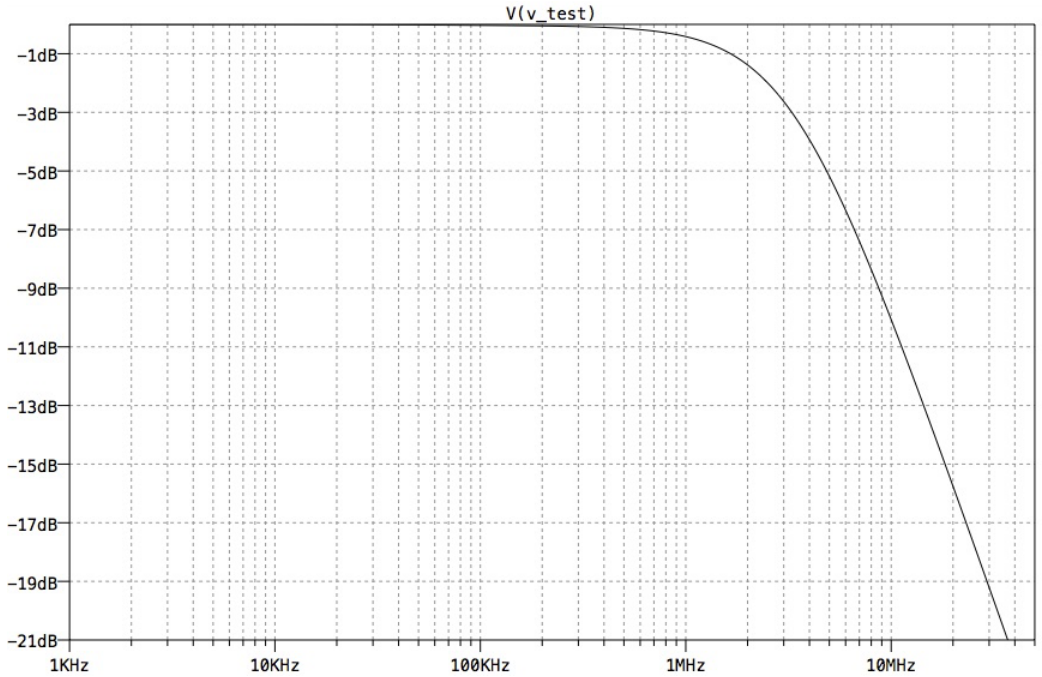
$$C_{in} = 6pF || C_{TH}$$
$$= 6p || 23.5p$$
$$= 4.5pF$$

*Simulation*

$$C_{in} = \frac{1}{2\dot{\pi} * 10K * 3.3M} = 4.8pF$$

Test Circuit

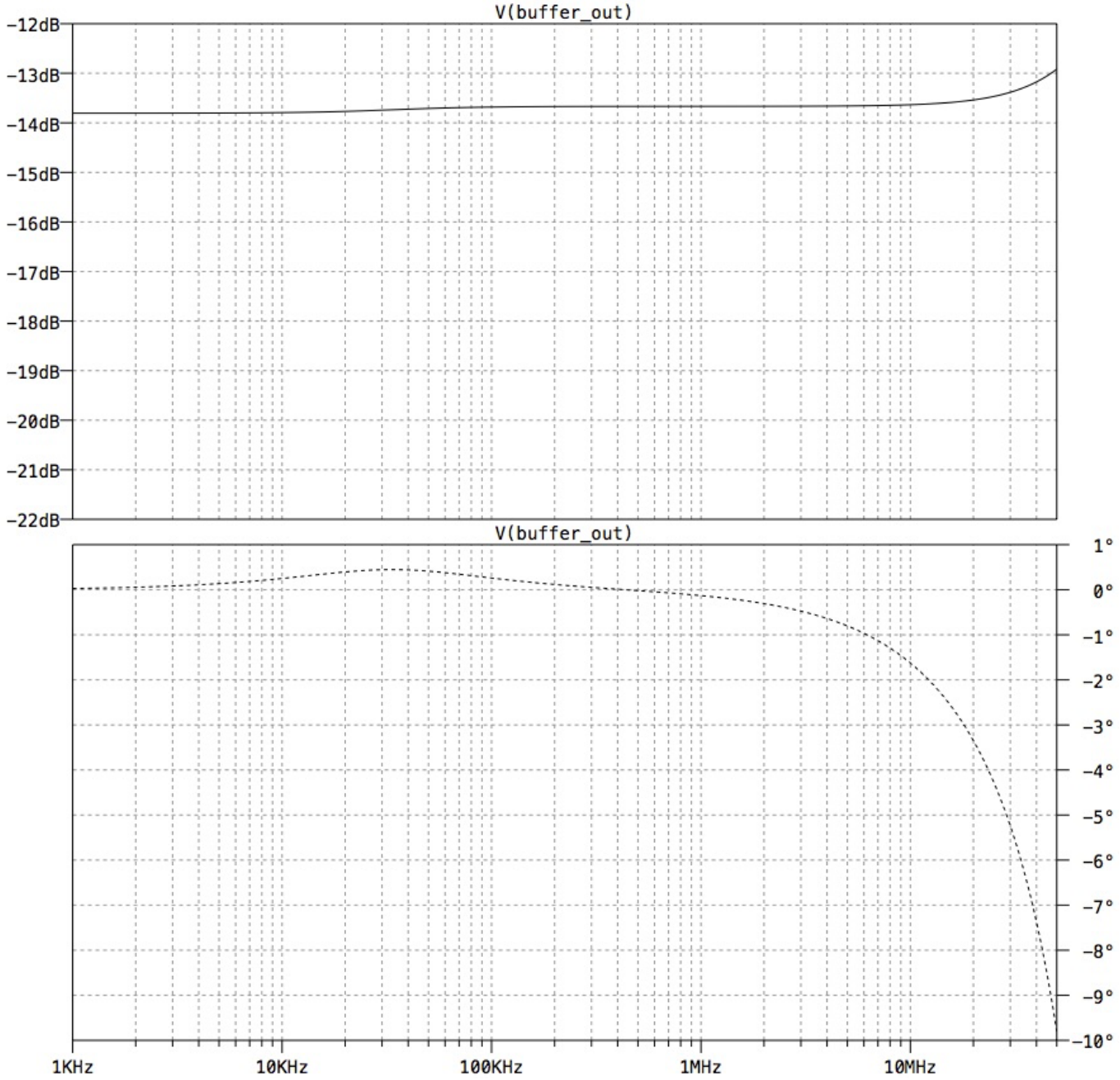


## Filter stage input

No specifications were explicitly given for the filter stage input. However the desired response is flat magnitude response at -13.97dB. The plot below shows a flat response from 0-20Mhz with only 0.3dB ripple.

Gain does begin to increase 20Mhz and peaks at -11dB (150MHz). However this is not an issue as this peak is attenuated at the filter output.



## DC operating points

**1.0.5 The BNC input can accept a maximum input of ±5.6V after which the input voltage is clamped.**

The table below shows simulation results for a number of operating points at each stage of the circuit.

The DC operating points show that input/output requirements have been met for the selected components. Namely:

- In the case of over voltages, the input to the ADC does not exceed its absolute maximum ratings (-0.3 to Vs+0.3V).
- In the case of over voltages, the input to the buffer stage does not exceed the absolute maximum rating of the LT1819 (±6V).
- For normal operation (±5V), the input to the anti-aliasing filter should be ±1V.
- For normal operation (±5V), the ADC input should be within the range 1.5 to 3.5V.

The results show that these requirements have been met.

| Mode | BNC(V) | Buffer_in(V) | Buffer_out(V) | Filter_out(V) | ADC_in(V) |
|---|---|---|---|---|---|
| **Clipped** | -50 | -5.418 | -4.115 | -3.986 | 4.021 |
| **Outside range** | -25 | -4.566 | -4.116 | -3.986 | 4.021 |
| | -10 | -1.695 | -2.039 | -2.036 | 4.043 |
| **Operating range** | -5 | -0.691 | -1.019 | -1.019 | 3.509 |
| | 0 | 313m | 365µ | 2.26m | 2.49 |
| | 5 | 1.318 | 1.020 | 1.021 | 1.472 |
| **Outside range** | 10 | 2.32 | 2.039 | 2.04 | 0.903 |
| **Clipped** | 25 | 4.970 | 4.119 | 4.076 | 0.925 |
| | 50 | 5.423 | 4.118 | 4.076 | 0.925 |

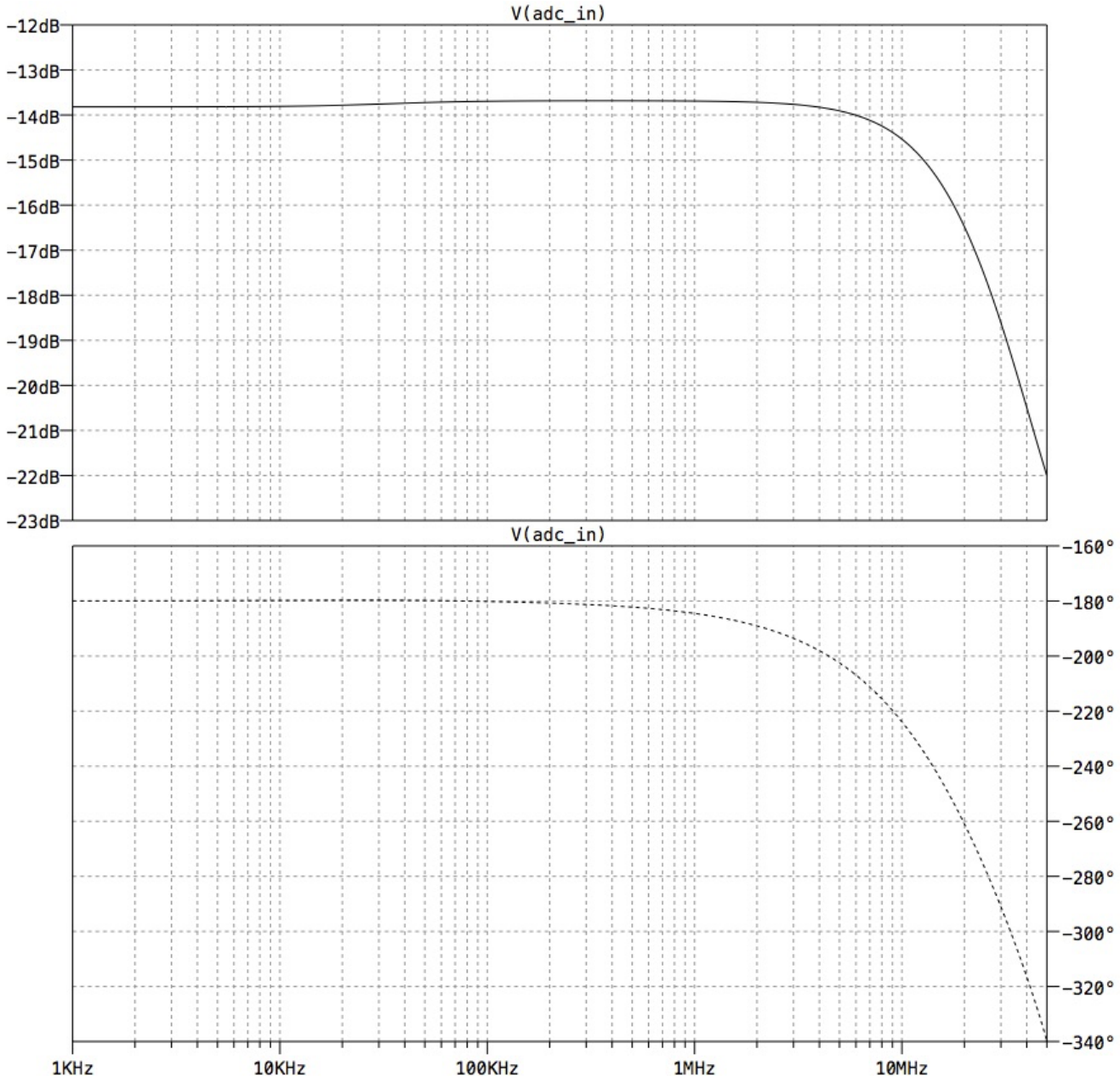
# ADC Input

## Frequency and Phase

| | |
|---|---|
| **1.0.7** | **An anti-aliasing filter appropriate to the 40MSPS maximum sample rate must be implemented with a minimum of a first-order 20dB per decade response and ±2dB maximum ripple in the pass band.** |

The plot below shows specification 1.0.7 has been satisfied. A flat response (-13.8 to -13.7dB) can be seen in the pass band, giving a ripple of less than 2dB. The 3dB cut-off point is at 20Mhz (-16.5dB) allowing for a maximum sampling rate of 40MSPS. The response can be seen to drop off by 20dB per decade.

The phase plot shows the signal is inverted (-180°), meaning signal should be passed into the inverting terminal of the ADC.



## Potential Issues

### Sampling rate

One issue with this design is that the sampling rate only meets the bare minimum requirement for a 20MHz input signal. As a result, higher frequency signals will be folded into the pass band after sampling. For example, at 30Mhz the signal only has an additional 2dB of attenuation than at 20Mhz. When aliased, this higher frequency signal will appear as a 10Mhz signal. A more robust design would be to use a faster ADC that is able to sample at ~4 times the cut-off frequency so folded signals are suitably attenuated (e.g. reached the stop band).

### Tolerances

E12 resistor and capacitor values are being used which have tolerance values of ±10%. The "ADC_in" signal is particularly sensitive to variations in resistor values at the voltage dividers. The following table shows variations at the "ADC_in" signal (for BNC=5V) when these resistors are reduced to their minimum limit.

| Modification | Frequency | ADC_in |
|---|---|---|
| No changes | DC | 1.47V |
| R6=180K | DC | 1.57V |
| R10=450 | DC | 1.37V |
| C4=5.4 | 1MHz | 1.54V |

Trimpots have been added to these voltage dividers (resistance and capacitive) to allow any manufacturing errors to be offset.