BRADLEY University

CS 220 Computer Architecture

HW 10 – Addressing Modes and Memory System

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DEPARTMENT OF COMPUTER SCIENCE AND INFORMATION SYSTEMS

Part 0: Reading

- **Chapter 14** - Addressing Modes and Formats
- **Chapter 4** - The Memory Hierarchy

Part 1: Questions on Addressing Modes [50 pts]

Question 1

Briefly describe the seven addressing modes. **[21 pts]**

#	Addressing Mode	Description
1	Immediate	The simplest form of addressing is immediate addressing, in which the operand value is present in the instruction
2	Direct	The address field contains the effective address of the operand
3	Indirect	Having the address field refer to the address of a word in memory, which in turn contains a full-length address of the operand
4	Register	When the address field refers to a register rather than a main memory address
5	Register Indirect	register indirect addressing is analogous to indirect addressing. In both cases, the only difference is whether the address field refers to a memory location or a register
6	Displacement	A very powerful mode of addressing combines the

		capabilities of direct addressing and register indirect addressing
7	Stack	A reserved block of locations. Items are appended to the top of the stack so that, at any given time, the block is partially filled.

Question 2

What is auto-indexing? What is the advantage of auto-indexing? **[5 pts]**

Auto-indexing	It is typical that there is a need to increment or decrement the index register after each reference to it. The advantage to auto-indexing is it makes it easier for people to search a document, as fast as a computer can

Question 3

Consider a 16-bit processor in which the following appears in main memory, starting at location 200. **[24 pts]**

a) The first part of the first word (content at 200) indicates that this instruction **loads** a value into an accumulator, the **value of 500** in location 201 may be part of the address calculator. The **mode** field specifies an addressing mode and, if appropriate, indicates a source register;
b) Assume that when used, the source **register R1,** which has a value of 400.
c) There is also a **base register** that contains the value 100,
d) Assume the **location** 399 contains the value 999, location 400 contains the value 1000, and so on.

address	Content

200	Load to AC	Mode
201	500	
202	Next instruction	
399	999	
400	1000	
	...	
500	1100	
600	1200	
702	1302	
1100	1700	

Determine the **effective address** and the **operand** to be loaded for the following address modes.

#	Mode	Effective Address	Operand
a	Direct	500	1100
b	Immediate	201	500
c	Indirect	**1100**	1700
d	PC Relative	202+500 = 702	1302
e	Displacement (offset + base)	**500+100 = 600**	1200
f	Register	R1	400
g	Register indirect	400	1000

Part 2: Memory Hierarchy [50 pts]

Question 1: Concepts and Review Questions [18 pts]

a. Compare and contrast sequential access, direct access, and random access.
b. Describe the general relationship among access time, memory cost, and capacity.
c. How does the principle of locality relate to the use of multiple memory levels?
d. Compare and contrast spatial locality and temporal locality.
e. What are the general strategies for exploiting spatial locality and temporal locality?
f. How do data locality and instruction locality relate to spatial locality and temporal locality?

a	Sequential access - Memory is organized into units of data, called records. Access must be made in a specific linear sequence Direct access - Individual blocks or records have a unique address based on physical location; based on a physical location Random access - each addressable location in memory has a unique, physically wired-in addressing mechanism that selects data at random
b	As access time becomes faster, the cost per bit increases. As memory size increases, the cost per bit is smaller. Also, with greater capacity, the access time becomes slower
c	Slower and less expensive memory is used in higher stages, with the most expensive being the registers in the processor as well as cache. Main memory is slower, less expensive, and is outside of the processor
d	The principle of spatial locality says that if a program accesses one memory address, there is a good chance that it will also access other nearby addresses. The principle of temporal locality says that if a program accesses one memory address, there is a good chance that it will access the same address again
e	Larger cache blocks and prefetching mechanisms are used to exploit spatial locality. Temporal locality is exploited by keeping recently used instructions and data values in cache memory, and by exploiting a cache hierarchy
f	Many programs exhibit both temporal and spatial locality for both instruction

	and data access. It has been found that data access patterns generally show a greater variance than instruction access patterns and instruction fetch addresses. Typically, each instruction execution involves fetching the instruction from memory and, during execution, accessing one or more data operands from one or more regions of memory. Thus, there is a dual locality of data spatial locality and instruction spatial locality

Question 2

Consider these terms: instruction spatial locality, instruction temporal locality, data spatial locality, data temporal locality. Match each of these terms to one of the following definitions: **[8 pts]**

a. Locality is quantified by computing the average distance (in terms of number of operand memory accesses) between two consecutive accesses to the same address, for every unique address in the program. The evaluation is performed in four distinct window sizes, analogous to cache block sizes.	Data Temporal Locality
b. Locality metric is quantified by computing the average distance (in terms of number of instructions) between two consecutive accesses to the same static instruction, for every unique static instruction in the program that is executed at least twice.	Instruction Temporal Locality
c. Locality for operand memory accesses is characterized by the ratio of the locality metric for window sizes mentioned in (a).	Data Spatial Locality
d. Locality is characterized by the ratio of the locality metric for the window sizes mentioned in (b).	Instruction Spatial Locality

Question 3

A computer has a cache, main memory, and a disk used for virtual memory. If a referenced word is in the cache, 20 ns are required to access it. If it is in the main memory but not in the cache, 60 ns are needed to load it into the cache, and then the reference is started again. If the word is not in the main memory, 12 ns are required to fetch the word from the disk, followed by 60 ns to copy it to the cache, and then the reference is started again. The cache hit ratio is 0.9 and the main-memory hit ratio is 0.6. What is the average time in nanoseconds required to access a referenced word on this system? **[24 pts]**

Location	Referenced Probability	Access time
In cache	0.9	20ns
Not in cache, but in main memory	(0.1)(0.6) = 0.06	20ns+60ns = 80ns
Not in cache or main memory	(0.1)(0.4) = 0.04	12ns + 60ns + 20ns = 92ns
Average: (0.9)(20ns) = 18ns (0.06)(80ns) = 4.8ns (0.04)(92ns) = 3.68ns		