COMP3222/9222 Digital Circuits & Systems

11. Course Wrap-up

Outline

- Learning objectives
- Topic list
- Assessment
- Exam
- Reminders
- myExperience

Learning objectives

- How to design digital logic circuits
  - Boolean algebra, logic minimization, combinational logic components, sequential circuits, simple systems
- How to specify/simulate/synthesize/implement designs
  - VHDL hardware description language
  - simulation techniques to verify the correct working of our designs
  - logic compilers to synthesize the hardware blocks of our designs
  - implementing designs using programmable hardware

Topic list – Digital circuits

- Boolean algebra
- SOP & POS form
- NAND/NOR-only forms
- Implementation technologies
- Logic/circuit minimization; circuit cost
- Factoring & functional decomposition
- Analyzing circuits
- Number representation
- Arithmetic circuits; circuit speed
- Combinational circuit blocks
- Implementing combinational functions using MUXes, DECoders & FPGAs
- Latches & flip-flops
- Counters, registers
- Timing properties & analysis of digital circuits
- Synchronous sequential circuit design involving FSMs, state transition diagrams, state tables, state minimization, state assignment etc.
- Algorithmic state machines
- Digital system design; datapath and control path design

Topic list – VHDL

- Entity/architecture parts
- Concurrent/sequential statement types; differences with sequential programming language semantics
- Describing combinational & sequential circuit components
- Structural vs behavioural description
- Use of sub-components in structural descriptions
- Packages
- Understanding & simulating delays in digital systems
- Understanding the discrete event simulation of VHDL design entities
- Understanding the three types of reliably synthesizable processes
- Specifying FSMs
- Specifying datapaths
- Describing complete digital systems comprising both data and control paths
- Experience with a CAD tool for synthesizing & simulating designs
- Experience implementing and testing circuits on an FPGA prototyping board

COMP3222/9222 Assessment details

- Assessment:
  - Lab exercises: 35%
  - 1 hr Week 5 Class Test: 15%
  - FINAL EXAM 1:15 PM TUESDAY 3 DECEMBER
    HELD IN THE K17 GROUND FLOOR BONGO, TABLA & OUD LABS AS WELL AS BASEMENT DRUM LAB
    - 1 hr Final Theory Test: 25%
    - 2 hr Final Practical Test: 25%

you must score >40% in this part to pass the course

Exam overview

- 3 hours of exams on Tuesday 3 December 13:15 – 17:45 (approx.)
- Exam will be held in the K17 Bongo, Tabla, Oud & Drum labs

- 1.0 hour theory paper followed by 2.0 hour practical paper
- Both parts held in the same lab
- You will be allocated a seat on the day
- Bring your student ID card AND your LAB KIT (Starter Board)

- **ANY MATERIALS ALLOWED**, BUT NO INTERNET OR INTRANET

- Textbooks and notes permitted
- USB memory device permitted
  - vm DOES NOT support USB3 devices directly – need to use a USB extension cable to connect USB3 drives
- **NO laptops, iDevices, phones, smartwatches, tablets etc.**

Exam details

Theory Part

- Covers all lecture material but concentrates on material presented after Wk 4
- Will comprise design questions like for Quiz and may contain MC questions
- ANY OFFLINE MATERIALS ALLOWED

Practical Part

- Will require you to design and implement a small digital system
- A practice problem is available under the link to this week's lecture and will be covered in the tute this week – the setting and resources for the practice problem are very similar to what you can expect in the practical part, but not exactly the same
  - Worth attempting under exam conditions i.e. prepare the materials you think you might need, then set aside two hours to solve the problem before this week's tute
- ALLOWED TO BRING ANY REFERENCE MATERIALS, but NETWORK ACCESS IS **NOT** ALLOWED – YOU WILL BE DISQUALIFIED IF YOU DISOBEY THIS
  - You may bring a flash/external drive with code/lecture slides etc.
- Please remember to bring your Starter Board for the exam

Reminders

- Today is the last lecture
- Tutorials finish this week
- Labs finish this week – check your lab marks and ask the demonstrator who marked you off to fix any discrepancies
- Stay tuned for an announcement regarding a catch-up lab marking session commencing at 2pm this Wednesday – this will be for students who did not manage to have their Labs 1 – 4 marked off by the end of their lab class in Week 7.
- We will collect your lab kits at the end of your prac exam
  - If you forget to bring it to the prac exam, please return it to Oliver after the exam…email o.diessel@unsw… to arrange a time
  - Please note that there are penalties for not returning your lab kit in good order – contact Oliver if you have concerns

Please fill in the myExperience Course Survey

- Your opinions are important to us
  - Course surveys help! We do take notice and make changes to improve quality

So PLEASE take 10 mins NOW and tell us what you thought of the course

- In particular, please provide written feedback:
  - If you usually attended the lectures, please let me know why you decided to do that…
  - Alternatively, if you did not usually attend lectures, please let me know why you did not.
  - THANK YOU!

- ✓ The survey is confidential; your identity is not shared with teaching staff
- ✓ Survey reports are not released until results have been officially published; your feedback won't impact your results.
- ✓ Your feedback matters – it's one way we can improve what we do – and keep doing the good things we do

➔ Access the survey on your laptop, tablet or phone:

- 🗋 Direct link on your Moodle course page
- 💻 http://myexperience.unsw.edu.au (use zID@ad.unsw.edu.au)
- ✉ Link in an email from myExperience