ECE 255 – Introduction to Digital Logic Design
Homework Assignment 4
Due October 13

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1. Minimize the following functions using the Quine-McCluskey method.

(a) $f(a, b, c, d) = \sum(m_0, m_2, m_4, m_5, m_7, m_9, m_{11}, m_{12})$

0000 0010 0100 0101 1001 1010 1011

Table I

Group I 0000

Group II 2 0010, 4 0100

Group III 5 0101, 9 1001, 12 1100

Group IV 7 0111, 11 1011

Table II

$m_0 m_2$ 00x0

$m_0 m_4$ 0x00

$m_4 m_5$ 010x

$m_4 m_{12}$ x100

$m_5 m_7$ 01x1

$m_9 m_{11}$ 10x1

MSOP =

$a'b'd' + a'bd + bc'd' + ab'd$

Prime Implicant Chart.

	0	2	4	5	7	9	11	12
$m_0 m_2$ 00x0	√	√						
$m_0 m_4$ 0x00	√		√					
$m_4 m_5$ 010x			√	√				
$m_4 m_{12}$ x100			√					√
$m_5 m_7$ 01x1				√	√			
$m_9 m_{11}$ 10x1						√	√	

prime prime prime

(b) $f(a, b, c, d, e) = \sum(m_0, m_1, m_2, m_7, m_9, m_{11}, m_{12}, m_{23}, m_{27}, m_{28})$

00000 00001 00010 00111 01001 01011 01100 10111 11011 11100

Table I

Group I m_0 00000

Group II m_1 00001, m_2 00010

Group III m_9 01001, m_{12} 01100

Group IV m_7 00111, m_{11} 01011, m_{28} 11100

Group V m_{23} 10111, m_{27} 11011

Table II

$m_0 m_1$ 0000x

$m_0 m_2$ 00x0

$m_1 m_9$ 0x001

$m_9 m_{11}$ 01x1

$m_{12} m_{28}$ x1100

$m_7 m_{23}$ x0111

$m_{11} m_{27}$ x1011

prime implicants

00x0, x1100, x1011, x0111, 0x001

MSOP = $\bar{a}\bar{c}\bar{d}e + \bar{a}\bar{b}\bar{c}\bar{e} + bc\bar{d}\bar{e} + \bar{b}cde + b\bar{c}de$

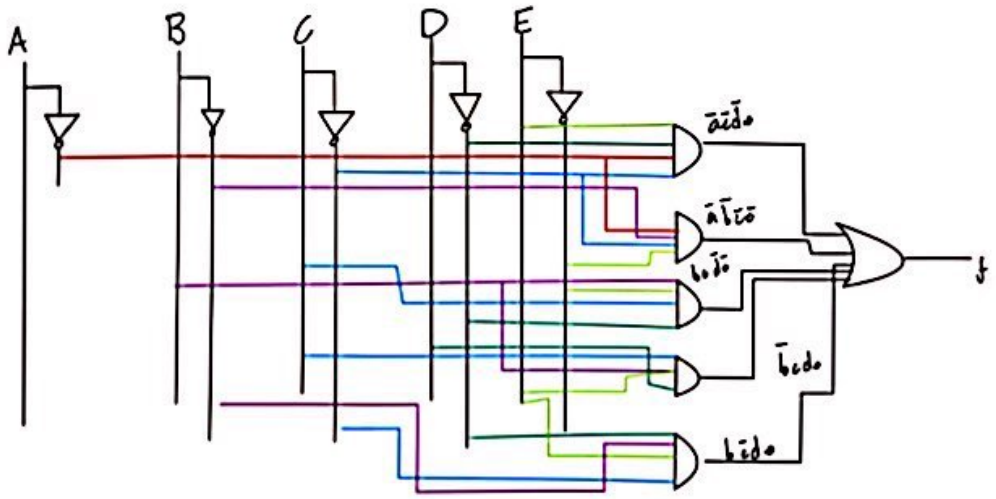
	0	1	2	7	9	11	12	23	27	28
$m_0 m_1$ 0000x	√	√								
$m_0 m_2$ 00x0	√		√							
$m_1 m_9$ 0x001		√			√					
$m_9 m_{11}$ 01x1					√	√				
$m_{12} m_{28}$ x1100							√			√
$m_7 m_{23}$ x0111				√				√		
$m_{11} m_{27}$ x1011						√		√	√	

a,b,c,d,e

max 2

(c) Sketch (or use Logisim) a schematic of the digital circuit that implements your Boolean function from (b).

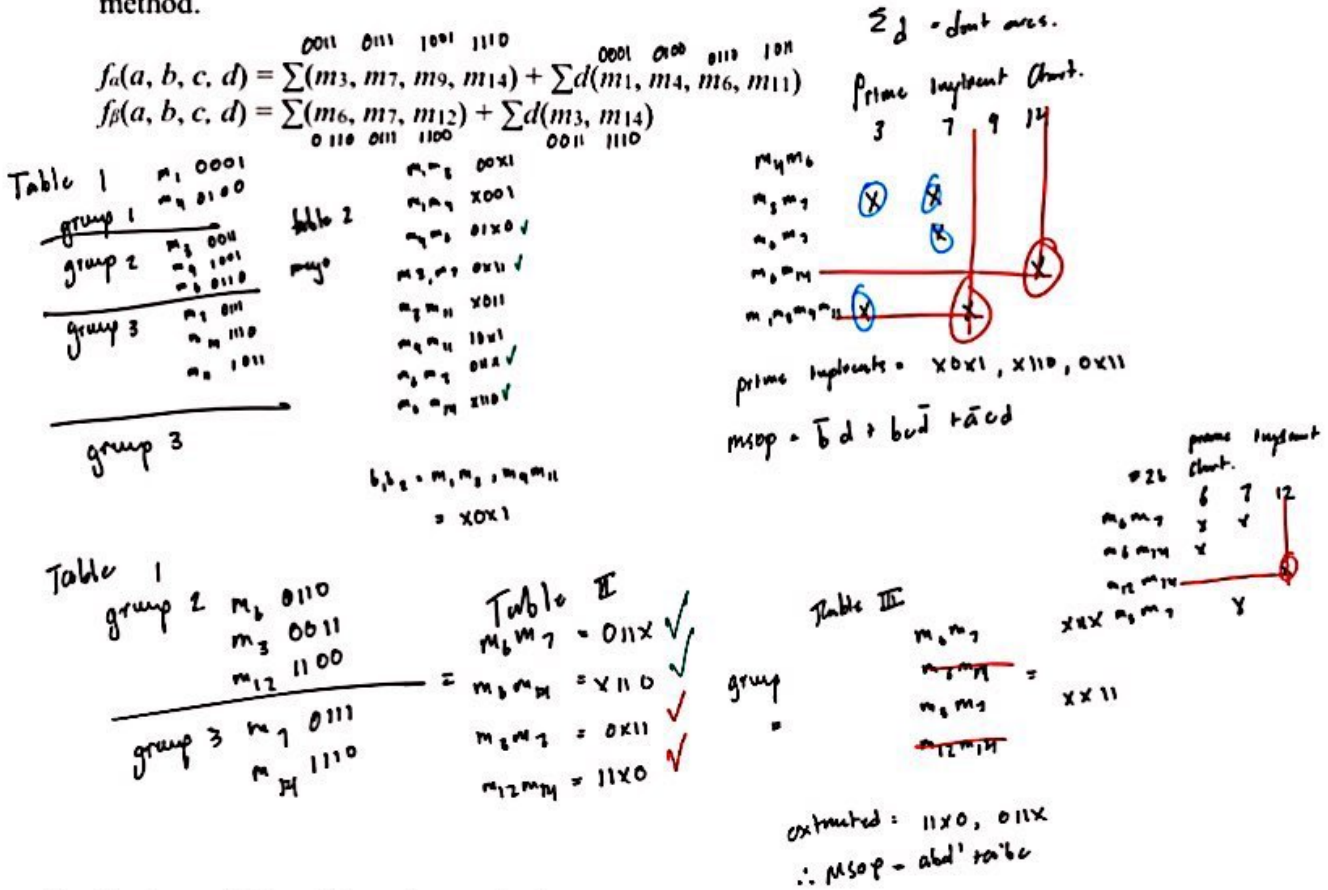
MSOP = $\bar{a}\bar{c}\bar{d}e + \bar{a}\bar{b}\bar{c}\bar{e} + bc\bar{d}\bar{e} + \bar{b}cde + b\bar{c}de$



2. Consider the following multi-output functions and minimize them using the Quine-McCluskey method.

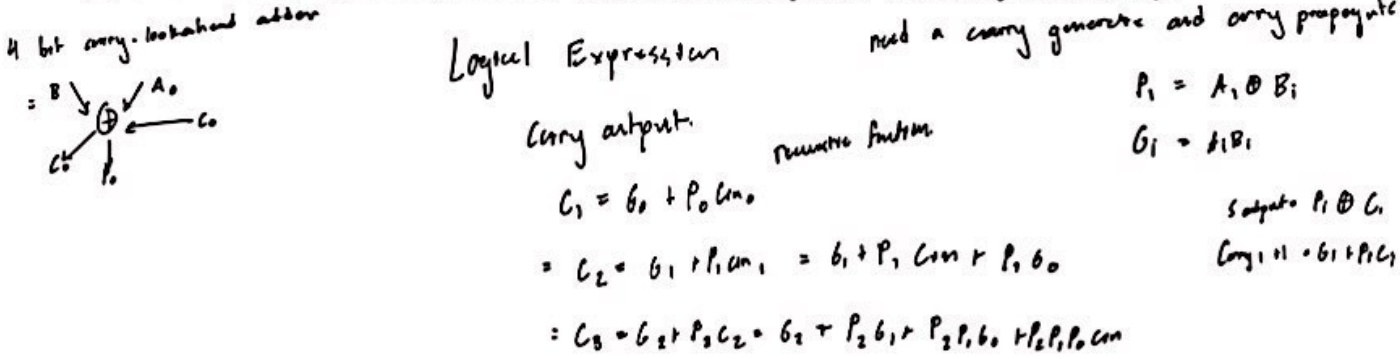
$f_\alpha(a, b, c, d) = \sum(m_3, m_7, m_9, m_{14}) + \sum d(m_1, m_4, m_6, m_{11})$

$f_\beta(a, b, c, d) = \sum(m_6, m_7, m_{12}) + \sum d(m_3, m_{14})$



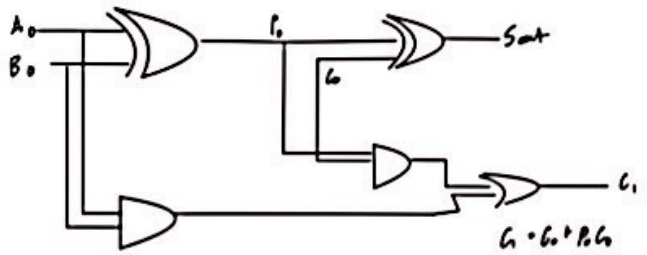
3. **Design a 3-bit adder using a single carry-lookahead circuit** (one 3-bit carry-lookahead group). and provide a schematic

(a) **Show all key logical expressions** (HINT: see example for 4-bit carry-lookahead).

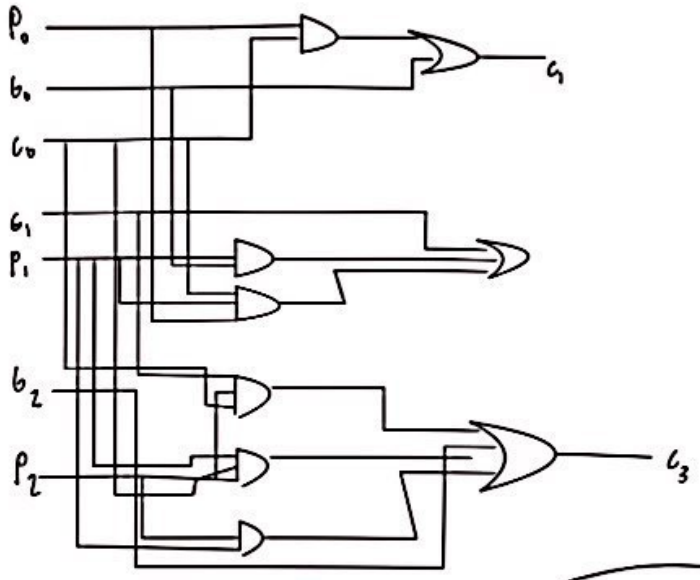


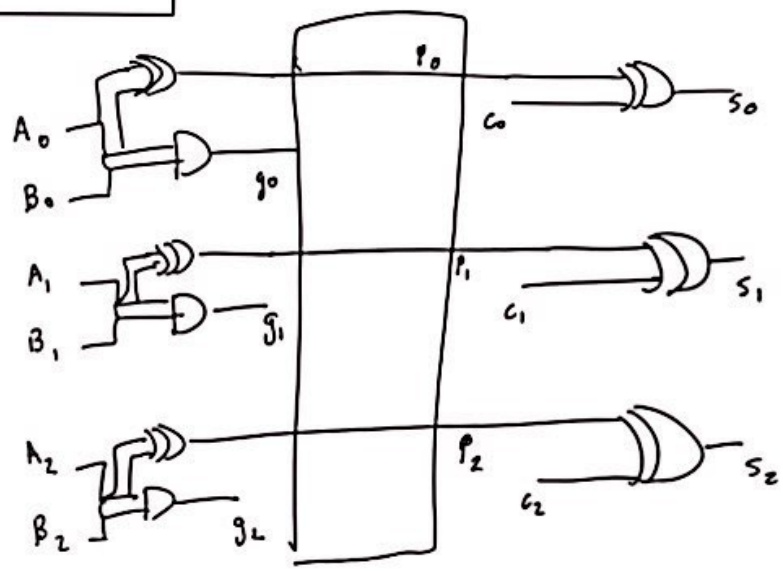
(b) **Draw a schematic of your 3-bit adder**, showing the carry-lookahead circuit. You can sketch by hand or use a tool such as Logisim to produce your schematic.

Adder propagators



full logic gate





roughly with adder.