

2. Consider the following multi-output functions and minimize them using the Quine-McCluskey method.

$f_a(a, b, c, d) = \sum(m_3, m_7, m_9, m_{14}) + \sum d(m_1, m_4, m_6, m_{11})$
 $f_b(a, b, c, d) = \sum(m_6, m_7, m_{12}) + \sum d(m_3, m_{14})$

Table 1
 group 1: m_1 0001, m_4 0100
 group 2: m_3 0011, m_9 1001, m_6 0110
 group 3: m_7 0111, m_{14} 1110, m_{11} 1011
 group 3

Table 2
 m_1, m_3 00x1
 m_1, m_4 x001
 m_4, m_6 01x0 ✓
 m_3, m_7 0x11 ✓
 m_3, m_{11} x011
 m_4, m_{11} 10x1
 m_6, m_7 011x ✓
 m_6, m_{14} x110 ✓
 $b_1, b_2 = m_1, m_3, m_4, m_{11} = x0x1$

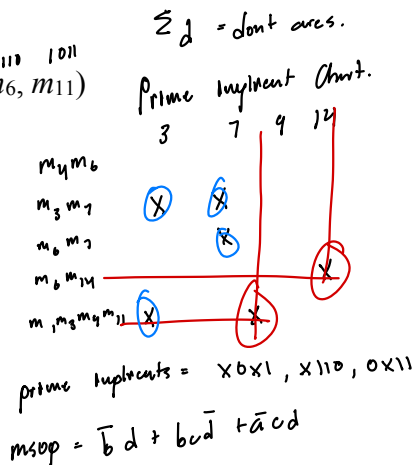
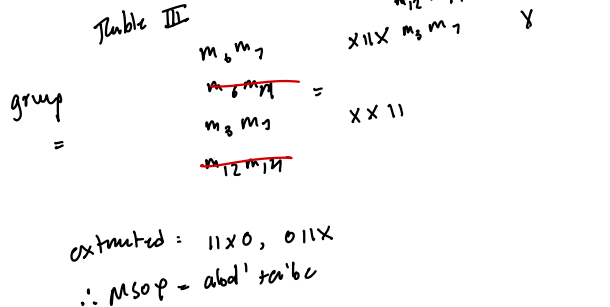


Table I
 group 2: m_6 0110, m_3 0011, m_{12} 1100
 group 3: m_7 0111, m_{14} 1110

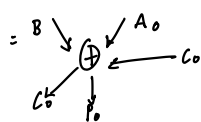
Table II
 $m_6, m_7 = 011x$ ✓
 $m_6, m_{14} = x110$ ✓
 $m_3, m_7 = 0x11$ ✓
 $m_{12}, m_{14} = 11x0$ ✓



3. Design a 3-bit adder using a single carry-lookahead circuit (one 3-bit carry-lookahead group). and provide a schematic

(a) Show all key logical expressions (HINT: see example for 4-bit carry-lookahead).

4 bit carry-lookahead adder



Logical Expression

Carry output.

$$C_1 = G_0 + P_0 C_0$$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$

need a carry generate and carry propagate

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

$$S_{\text{output}} = P_i \oplus C_i$$

$$\text{Carry}_{i+1} = G_i + P_i C_i$$