CG1112 Midterm quiz cheatsheet compiled by Lin Ruo

Binary Representation

- 0's and 1's as 1 bit to represent 0 volt and 5/3.3 volts. Circuit is able to ignore electric noise since the distance between the volts is large.
- *N* bits can represent up to 2^N values.
- To represent *M* values, $\log_2 M$ bits are required.

Masking

To clear a bit, create a "mask" where that bit is 0 and all others are 1, and do a bit-wise AND. To set a bit, create a "mask" where that bit is 1 and all others are 0, and do a bit-wise OR.

Value	1	1	0	1	1	1	1	1
	&	&	&	&	&	&	&	&
Mask	1	1	1	1	1	0	1	1
result	1	1	0	1	1	0	1	1

Clearing bit 3: value &= 0b1111 0111 or 0Xf7

Value	1	1	0	1	1	0	1	1
	|	|	|	|	|	|	|	|
Mask	0	0	1	0	0	0	0	0
result	1	1	1	1	1	0	1	1

Setting bit 5: value |= 0b0010 0000 or 0X20

GPIO Programming

- 3 GPIO ports labelled: DDRB, DDRC, DDRD (set the direction of pins)
- PORTx registers to write the pins

I/O Programming

1. **Polling**

Read data and process data in a loop while the CPU keeps waiting until every job is done.

2. **Interrupt-driven I/O**

- Call Interrupt Service Routine (Atmega328P can process <= 26 interrupts.)
- Bare-metal interrupts / external interrupts : pinNum = 2/3 (INT0 & INT1);
- to turn INT0 & INT1 on -> write 1 to EIMSK (enabling interrupt 1 and 0)
- cli() disable all interrupts
- sei() enable all interrupts
- EICRA configures how the interrupts can be triggered (at rising/falling)

EIMSK/EIFR							INTF1	INTF0
EICRA					ISC11	ISC10	ISC01	ISC00

ISC1n

Value	Description
00	The low level of INT1 generates an interrupt request.
01	Any logical change on INT1 generates an interrupt request.
10	The falling edge of INT1 generates an interrupt request.
11	The rising edge of INT1 generates an interrupt request.

ISC0n

Value	Description
00	The low level of INT0 generates an interrupt request.
01	Any logical change on INT0 generates an interrupt request.
10	The falling edge of INT0 generates an interrupt request.
11	The rising edge of INT0 generates an interrupt request.

PWM Programming

- Fast PWM for higher f (up-counting only: 255)
- Phase Correct PWM for symmetric waveform (up and down counting: 510)

Clock Source – PWM Frequency

$$f_{\text{OCnxPCPWM}} = \frac{f_{\text{clk\_I/O}}}{N \cdot 510}$$ N = prescalar factor

Time Complexity

- Consider only the leading term and analyse problem of large size
- Ignore coefficient of the leading term
- $O(1) < O(\log n) < O(n) < O(n \log n) < O(n^2) < O(n^3) < O(n^4)$

Git

- Version control that keeps track of changes made to file
- git status: check the state of the local repo since the last commit
- commit: records changes to the repo
- add: stage a file
- diff: -red lines for deleted content; +green lines for added content
- staging: undo the previous commit and commit different changes

Git Workflow

1. Fetch from remote
2. Merge with local version
3. Work on file + commit
4. Push the local version to remote repo

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Time/Counter Register TCCR0A

COM0A1	COM0A0	COM0B1	COM0B0			WGM01	WGM00

Mode	WGM02	WGM01	WGM00	Timer/Counter Mode of Operation
0	0	0	0	Normal
1	0	0	1	PWM, Phase Correct
2	0	1	0	CTC
3	0	1	1	Fast PWM
4	1	0	0	Reserved
5	1	0	1	PWM, Phase Correct
6	1	1	0	Reserved
7	1	1	1	Fast PWM

COM0A1	COM0A0	Description
0	0	Normal port operation, OC0A disconnected.
0	1	WGM02 = 0: Normal Port Operation, OC0A Disconnected. WGM02 = 1: Toggle OC0A on Compare Match.
1	0	Clear OC0A on Compare Match when up-counting. Set OC0A on Compare Match when down-counting.
1	1	Set OC0A on Compare Match when up-counting. Clear OC0A on Compare Match when down-counting.

Output Compare Unit OCR0A/B

$$D = \frac{OCR0A}{255} \text{ x } 100$$

-TCNT is the counter and OCR0A sets the boundary of the counter
-TIMSK generates interrupts whenever there's an output compare between TCNT and OCR0A/B

Timer Programming (CTC mode)

- Set the initial timer value of 0 into TCNT0
- Set the top count value V into OCR0A
- Prescalar frequency: $V = \frac{T_{cycle}}{res}$

$$\text{Resolution} = \frac{1}{(F_{clk} / P)}$$

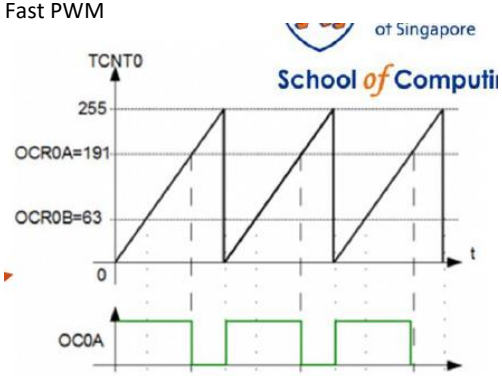
CS02	CS01	CS00	Prescalar P	Resolution (F_{clk}=16 MHz)
0	0	0	Stops the timer	-
0	0	1	1	0.0625 microseconds
0	1	0	8	0.5 microseconds
0	1	1	64	4 microseconds
1	0	0	256	16 microseconds
1	0	1	1024	64 microseconds
1	1	0	External clock on T0. Clock on falling edge.	-
1	1	1	External clock on T0. Clock on rising edge	-

Clock Select TCCR0B

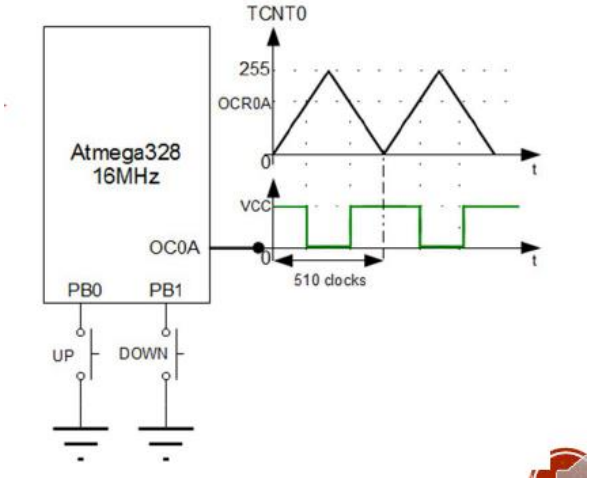
FOC0A	FOC0B			WGM02	CS02	CS01	CS00

PWM graph

1. Fast PWM



2. Phase-correct PWM



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