Coursework 1

Computer Processors (XJCO1212)

You should follow the instructions below on how to prepare your submission. Late submissions are accepted up to 7 days late. Each day, or part of a day, will incur a 5% penalty. Feedback on late submissions may not be provided within 3 weeks of submission.

Submission You **must** submit your work via Gradescope. You should submit two files, one called CW1Q1.hdl and one called CW1Q2.hdl.

Deadline **1700 19/03/2021**.

Weighting This piece of summative coursework is worth 25% of the module grade.

1. Produce an HDL file which implements the boolean function described by the following truth table.

s_1	s_2	x	y	$f(s_1, s_2, x, y)$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

The HDL file should have the following preamble.

```
CHIP CW1Q1 {
    IN s1, s2, x, y;
    OUT f;

    PARTS:
}
```

2. Produce an HDL file which implements the boolean function described by the following formula. Your should ensure that your implementation is minimised with respect to the number of gates used.

$$(\neg a \wedge b) \vee (b \wedge \neg c) \vee (b \wedge c) \vee (a \wedge \neg b \wedge \neg c)$$

The HDL file should have the following preamble.

```
CHIP CW1Q2 {
    IN a, b, c;
    OUT f;

    PARTS:
}
```

Each of the questions is worth 12.5 marks.