

## Coursework 2

### Computer Processors (XJCO1212)

You should follow the instructions below on how to prepare your submission. Late submissions are accepted up to 7 days late. Each day, or part of a day, will incur a 5% penalty. Feedback on late submissions may not be provided within 3 weeks of submission.

**Submission** You **must** submit your work via Gradescope.

**Deadline** 1700 1/04/2021.

**Weighting** This piece of summative coursework is worth 25% of the module grade.

The transmission of information can be either serial or parallel. In parallel communication multiple binary digits are transmitted simultaneously. In serial communication a word is transmitted as a sequence of binary digits, one after another. Both have advantages and disadvantages.

1. A shift register is a sequential logic circuit that has a single input and cascades the input across a set of outputs in order, that is, supposing we have a 4-bit shift register with input called *in* and output pins called *w*, *x*, *y* and *z* then the table below describes the behaviour.

| Time | in | <i>w</i> | <i>x</i> | <i>y</i> | <i>z</i> |
|------|----|----------|----------|----------|----------|
| 0    | 0  | 0        | 0        | 0        | 0        |
| 1    | 1  | 0        | 0        | 0        | 0        |
| 2    | 0  | 1        | 0        | 0        | 0        |
| 3    | 1  | 0        | 1        | 0        | 0        |
| 4    | 1  | 1        | 0        | 1        | 0        |
| 5    | 0  | 1        | 1        | 0        | 1        |
| 6    | 0  | 0        | 1        | 1        | 0        |
| 7    | 0  | 0        | 0        | 1        | 1        |
| 8    | 0  | 0        | 0        | 0        | 1        |
| 9    | 0  | 0        | 0        | 0        | 0        |

The input at time *t* is at output *w* at time *t* + 1, at output *x* at time *t* + 2, at output *y* at time *t* + 3, and at *z* at time *t* + 4.

Produce an HDL file that contains the design of an **8-bit shift register**. The chip should have the following preamble.

```
CHIP Shift8bit {  
    IN x;  
    OUT out[8];
```

```
PARTS:  
}
```

2. Produce an HDL file that contains the design of a circuit that implements the following description.

The circuit should implement a parallel to serial converter. The circuit should store an 8-bit binary value from the 8-bit wide input bus called *indata* when the *load* input is asserted (has value 1). When the *enable* input is asserted (has the value 1) then the circuit, over the next 8 clock cycles, should output each of the bits of the stored 8-bit binary value, from bit 0 to bit 7, sequentially via *sout*. When the circuit has completed the transmission of the 8 bits then the *complete* output should be asserted (set to value 1) for 1 clock cycle.

The chip should have the following preamble.

```
CHIP cw2 {  
    IN indata[8], enable, load;  
    OUT sout, complete;
```

```
PARTS:  
}
```

Question 1 is worth **10 marks**, and Question 2 is worth **15 marks**.