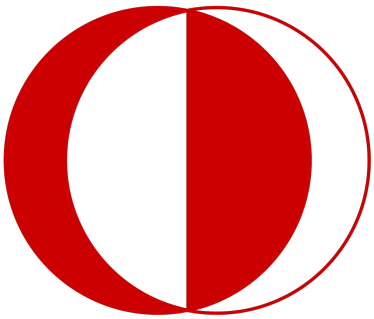

Middle East Technical University

EE464 Static Power Conversion II

Hardware Project Simulation and Magnetic Design Report

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1 Introduction

In this project, it is aimed to build an isolated DC-DC converter. The specifications of the project is given in the below Table 1 In this report, our thoughts on the potential topologies, their advantages and disadvantages are discussed. We have decided on building an isolated SEPIC converter whose circuit diagram can be seen in Figure 1. Then the team has decided on the transformer design and other components of the topology. Furthermore, computer simulations of the topology with ideal and non-ideal components are given.

Table 1: Project Specifications.

Input Voltage	12-18 V
Output Voltage	48 V
Output Voltage Ripple	3%
Output Power	48 W
Line Regulation	3%
Load Regulation	3%

2 Topology Selection

Starting the design, the topology selection must be covered first. The five isolated DC-DC converter topologies that were covered in the lectures are listed with their strengths and weaknesses in Table 2[8].

Table 2: Comparison of Isolated DC-DC Converter Topologies

Topology	**Advantages**	**Disadvantages**
Flyback	• Two-winding transformer • Low component count • Analog ICs are available for the duty cycle control	• High MOSFET voltage stress • Low controllability • Needs snubber due to leakage and parasitic inductances at primary side
Forward	• L_m has a discharge path on the auxiliary winding, no need for transformer snubber	• Utilizes a three-winding transformer, hard to implement by hand-winding • Has an additional inductor, may cause additional magnetic design work
Push-Pull	• Core utilization of the transformer is better, core can be smaller in size • Easier to filter at the output as the current and voltage waveforms ripple at twice the switching frequency	• Utilizes a centre-tap transformer, hard to implement by hand-winding • Two switches to control with additional measures to consider such as dead-time
Half-Bridge & Full-Bridge	• Similar considerations with Push-Pull such as better core utilization and easy filtering	• Similar considerations with Push-Pull such as hard to implement transformer and multiple switches to control

Considering the design challenges, the most difficult task will be the transformer implementation. It will be challenging to make transformer parameters match the simulated one, as it will be winded by hand. Therefore, choosing a topology with a simple two winding transformer would be more sensible. Moreover, flyback is the only option that is covered during the lectures utilizing a two winding transformer.

Flyback could be our choice of topology, but we decided against it due to two reasons. Firstly, Flyback needs a snubber circuit which not only decreases efficiency but also an additional design process; which we are not so experienced with. Secondly, we want to work on a unique topology in order to get extra points. In order to find a topology suited to our needs, we made some more research.

It is a common knowledge that Flyback converter was initially evolved from Buck-Boost converter by replacing the inductor with a transformer so that the isolation is achieved. We thought that there may be a similar derivation for SEPIC converter which also has an inductor with a connection to the return path just like the Buck-Boost Converter. We did our research to find out that there was indeed an isolated SEPIC converter which suits our previously mentioned needs which is shown in Figure 1.
Some design considerations regarding isolated SEPIC converter can be stated as

- The transformer acts similarly to the Flyback transformer, which sends power during off cycle.

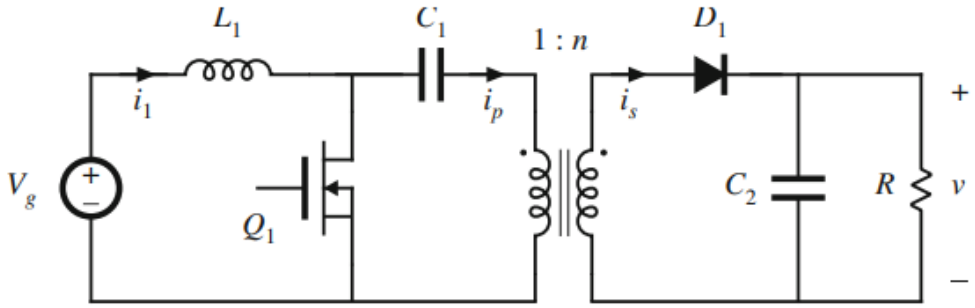

Figure 1: Isolated SEPIC Converter

- C_1 must be very large (ideally infinite).
- Assuming the previous requirement is met, $V_{C_1} \approx V_g$ and almost constant.
- Assuming $V_{C_1} = V_g$, I_{L_1} and I_{L_m} have exactly the same voltage waveforms during both the switch on and off cycles. If the magnetic design is done such that $L_1 \approx L_m$, their current waveforms will almost be identical too. Therefore, measuring and controlling the current (if desired) from the input will be enough to control transformer current as well.
- I_{Q_1} is approximately twice the input current during the on cycle, assuming $L_1 \approx L_m$.
- Assuming ideal components, MOSFET blocking voltage can be found as $V_{Q_1} = V_g + V_o/n$. Overshoots during the switching instants must be considered as well.

The voltage transfer ratio for an isolated SEPIC converter can be stated as

$$\frac{V_o}{V_s} = \frac{N_2}{N_1}\frac{D}{1-D}$$

After evaluating positives and negatives we have decided to go for an isolated SEPIC converter design for the project.

3 Magnetic Design

3.1 Wire Selection

To select the proper wires for transformer windings and inductor coil, we considered the average ratings of input and output currents. Also the skin effect ()is taken into account. Therefore looking at the AWG table (BURAYA REF) , we have selected the 26AWG. Parameters of the cable are given in Table 3

Table 3: AWG26 cupper conductor parameters.(REF)

Max. Amp rate:	0.361 A
Conductor diameter:	0.4 mm
Conductor cross-section area:	0.128 mm^2
Max. frequency for 100% skin depth:	107 kHz

Since its Amp. rate is very low but it gives 100% skin depth, we can parallel this wire for our primary and secondary windings. Considering the worst case scenario of 12 V input (giving 4 A input current), and accounting for the 10% losses on the design, we can assume that input current will be around 4.4 A. For the output side it is assumed to be around 1 A output current for 48 W output power.

Table 4: Transformer Wiring Configuration.

Transformer side	Assumed Current level	# of parallel wires
Primary	4.4 A	12
Secondary	1 A	3

3.2 Core Selection

We first decided on core geometry considering the recommendations from Ferrite Core Catalog by the Magnetics [9]. As the winding of the transformer is a topic that we are not very familiar of, we filtered our geometries to the ones that have a cylindrical winding surface to simplify the process. ETD core shape seemed to be best fit for our application and it is recommended for transformers by the catalog.
After doing some market research, we quickly realized that only ferrite cores are available to purchase in Turkey. Therefore, we decided to base our design for a ferrite core; so that we can quickly purchase a new core in case of an emergency. Ferrite cores also have a linear B-H characteristics until they are saturated, which simplifies the design process.
Considering the area that the windings occupy we have chosen ETD39 sized core to stay below a fill factor of 0.3.

3.3 Transformer Design

As the voltage transfer ratio has a $\frac{D}{1-D}$ dependence, we needed to fix our duty cycle range around 0.5 for a safe operation. Therefore, we decided on a duty cycle range of $0.4 < \mathrm{D} < 0.6$. We also chose $f_{sw} = 50\mathrm{kHz}$ as we not only believe it is a sweet-spot for the choice of switching frequency but also provides some margin for an increase in frequency until skin effect is observed at the wires. This margin may become useful during the implementation as real-world effects may lead us to increase the switching frequency.
We can calculate the required turns ratio for the extremities of the duty cycle and the input voltage as

$$\frac{48}{12} = \frac{N_2}{N_1}\frac{0.6}{1-0.6}$$

$$\frac{N_2}{N_1} = 2.67$$

$$\frac{48}{18} = \frac{N_2}{N_1}\frac{0.4}{1-0.4}$$

$$\frac{N_2}{N_1} = 1.78$$

As there will be some losses as well, choosing a turns ratio a little over the larger result would ensure the operation stays at $0.4 < \mathrm{D} < 0.6$. We chose our turns ratio to be 3.2 (i.e. 5:16),

around 1.2 times the calculated turns ratio. Furthermore, we also assumed $\Delta i_{L_m} = 2i_{L_m,avg} =$ 8A, to find the minimum inductance required for CCM operation.
We can write the inductor charging and discharging equations for 12V input (worst case), assuming ideal components and without explicitly stating duty cycles as

$$V_s D T_s = L_m \Delta i_{L_m}$$

$$D = \frac{L_m \Delta i_{L_m} f_{sw}}{V_s}$$

$$D = \frac{L_m \times 8 \times 50k}{12}$$

$$D = 33333.33\ L_m \tag{1}$$

$$\frac{V_o(1-D)T_s N_1}{N_2} = L_m \Delta i_{L_m}$$

$$1 - D = \frac{L_m \Delta i_{L_m} f_{sw} N_2}{V_o N_1}$$

$$1 - D = \frac{L_m \times 8 \times 50k \times 3.2}{48}$$

$$1 - D = 26666.67\ L_m \tag{2}$$

Adding equations (1) and (2) we get

$$1 = 60000\ L_m$$

$$L_m = 16.67\ \mu H$$

for CCM-DCM border operation.
We multiplied this number by 1.5 so that we are guaranteed to operate at CCM. Thus, $L_m =$ 25 μH can be stated as the absolute minimum inductance required. At this stage the core choice must be finalized in order to continue the design.
To select a suitable core we must either fix the operating flux density and find the primary number of turns or fix the number of turns and make sure that core does not saturate. We chose the second option and fixed the number of turns for the transformer as

$$N_p = 10,\ N_s = 32$$

Then we can calculate the total area the wires will occupy as

$$A_{wire} = 0.128mm^2 \times [(12 \times 10) + (32 \times 3)] = 27.65mm^2$$

Taking fill factor into account, we determined that both ETD34 and ETD39 sized cores are suitable for hand-winding. Core suppliers produce fixed various gapped versions of the cores as well as their inductance factors and effective permeabilities given in the datasheet for each version. The purpose behind this methodology was to avoid using a custom determined gap, which would be time consuming to implement accurately.
We quickly calculated the operating points for several different gap values and came up with a possible configuration for each size.

• ETD34 Core, g = 0.2mm, $A_L = 482\ nH/T^2$, $\mu_e = 310$, $l_e = 78.6$mm

$$L_m = A_L \times N_p^2 = 482n \times 100 = 48.2\mu H$$

Similar derivation with equations (1) and (2)

$$D = \frac{L_m \Delta i_{L_m} f_{sw}}{V_s}$$

$$D = \frac{48.2\mu \times \Delta i_{L_m} \times 50k}{12}$$

$$D = 0.2\ \Delta i_{L_m} \tag{3}$$

$$1 - D = \frac{L_m \Delta i_{L_m} f_{sw} N_2}{V_o N_1}$$

$$1 - D = \frac{48.2\mu \times \Delta i_{L_m} \times 50k \times 3.2}{48}$$

$$1 - D = 0.16\ \Delta i_{L_m} \tag{4}$$

Adding equations (3) and (4) we get

$$1 = 0.36\ \Delta i_{L_m}$$

$$\Delta i_{L_m} = 2.78\ A$$

Then the maximum current can be found as

$$i_{L_m,max} = i_{L_m,avg} \times 1.1 + \Delta i_{L_m}/2 = 4 \times 1.1 + 1.4 = 5.8\ A$$

where 1.1 multiplier is used as a safety margin. Using this result and applying Ampere's Law we can find the operating magnetic field of the core as

$$H \times l_e = N_p \times i_{L_m,max}$$

$$H = \frac{10 \times 5.8}{78.6 \times 10^{-3}} = 700\ A/m$$

The magnetic flux density for this operating point can be found as

$$B = \mu_e H = 310 \times 4\pi \times 10^{-7} \times 700 = 0.272\ T$$

- ETD39 Core, g = 0.5mm, $A_L = 326\ nH/T^2$, $\mu_e = 191$, $l_e = 92.2$mm

$$L_m = A_L \times N_p^2 = 326n \times 100 = 32.6\mu H$$

Similar derivation with equations (1) and (2)

$$D = \frac{L_m \Delta i_{L_m} f_{sw}}{V_s}$$

$$D = \frac{32.6\mu \times \Delta i_{L_m} \times 50k}{12}$$

$$D = 0.136\ \Delta i_{L_m} \tag{5}$$

$$1 - D = \frac{L_m \Delta i_{L_m} f_{sw} N_2}{V_o N_1}$$

$$1 - D = \frac{32.6\mu \times \Delta i_{L_m} \times 50k \times 3.2}{48}$$

$$1 - D = 0.109\ \Delta i_{L_m} \tag{6}$$

Adding equations (5) and (6) we get

$$1 = 0.245\ \Delta i_{L_m}$$

$$\Delta i_{L_m} = 4.08\ A$$

Then the maximum current can be found as

$$i_{L_m,max} = i_{L_m,avg} \times 1.1 + \Delta i_{L_m}/2 = 4 \times 1.1 + 2.1 = 6.5\ A$$

where 1.1 multiplier is used as a safety margin. Using this result and applying Ampere's Law we can find the operating magnetic field of the core as

$$H \times l_e = N_p \times i_{L_m,max}$$

$$H = \frac{10 \times 6.5}{92.2 \times 10^{-3}} = 705\ A/m$$

The magnetic flux density for this operating point can be found as

$$B = \mu_e H = 191 \times 4\pi \times 10^{-7} \times 705 = 0.17\ T$$

Both of the options suit the operation; however, ETD34 core option is very close to its saturation point. Hence, it can be risky to use that design for our project. We will use for the bigger core with the consequence of having high magnetic losses.

Calculating the fill factor for the selected ETD39 core we get

$$FF = \frac{A_{wire}}{A_e} = \frac{27.65\ mm^2}{125\ mm^2} = 0.22$$

Minimum transformer average current before the converter starts operating in DCM can be stated as

$$i_{L_m,avg,min} = \Delta i_{L_m}/2 = 2.04\ A$$

Therefore the minimum average load current can be found reflecting this value to the secondary side with the turns ratio as

$$i_{o,avg,min} = i_{L_m,avg,min}/3.2 = 2.04/3.2 = 0.6375\ A$$

The minimum transformer current at the CCM-DCM border is 0V as expected, whereas the maximum transformer current is equal to ripple current; which is 4.08A (ignoring current direction).

4 Computer Simulations

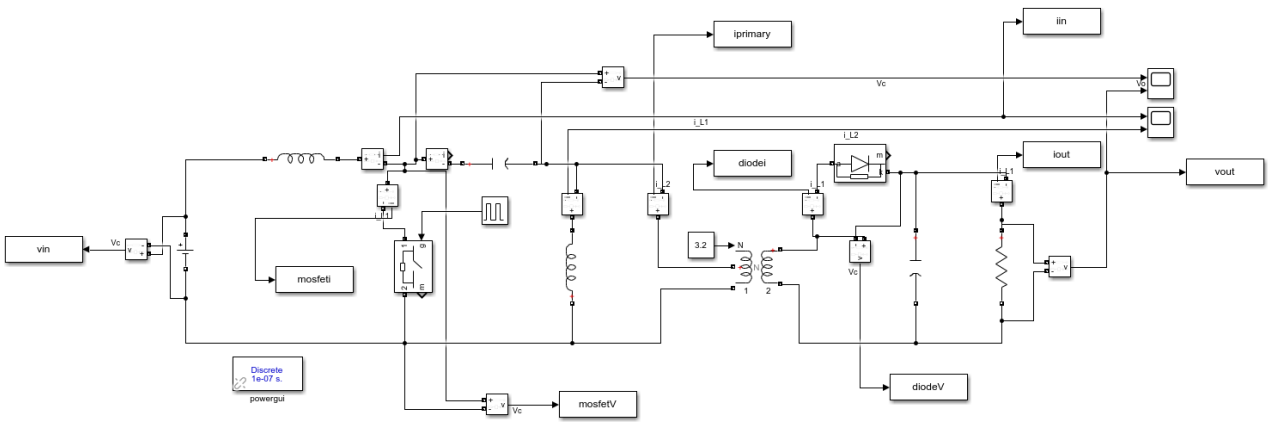

Figure 2: Simulink simulation circuit for ideal case.

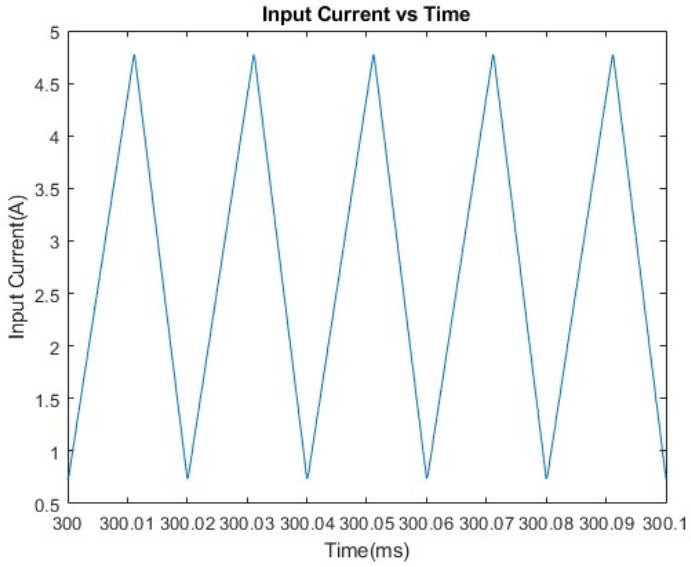

Figure 3: I_{in} versus time graph ideal case.

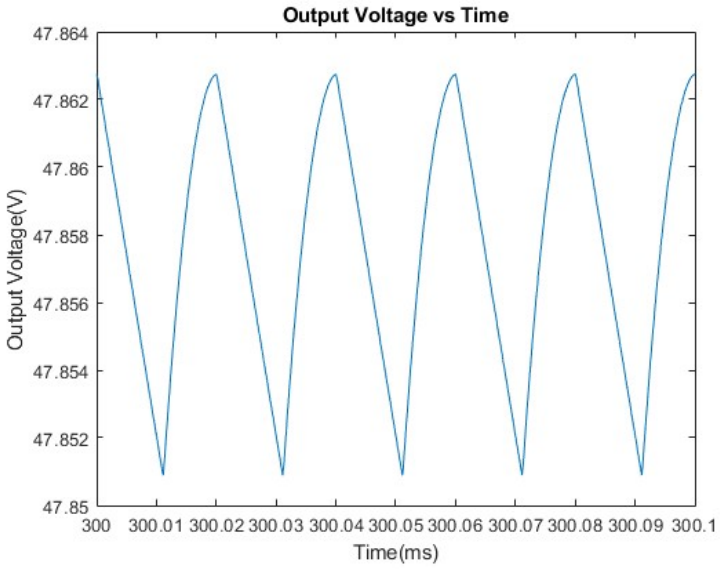

Figure 4: V_{out} versus time graph ideal case.

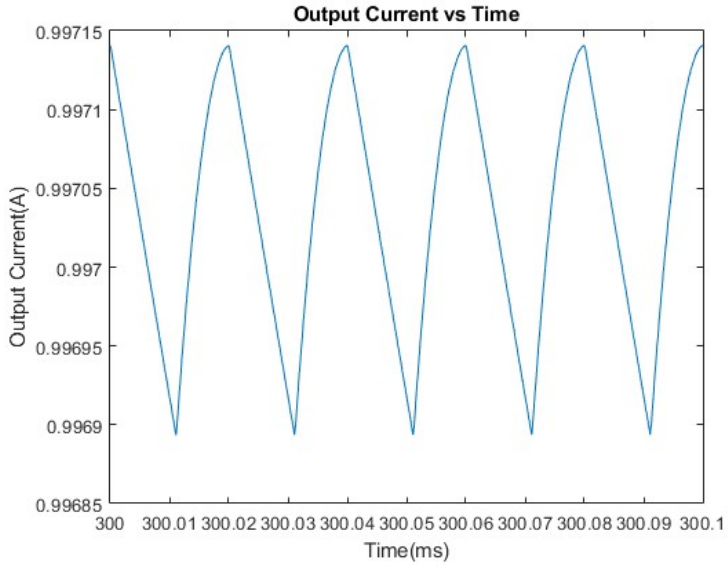

Figure 5: I_{out} versus time graph ideal case.

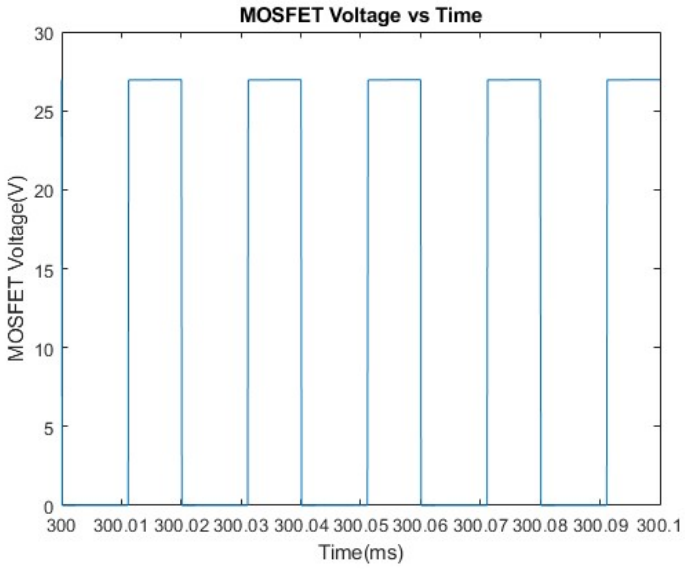

Figure 6: MOSFET voltage versus time graph ideal case.

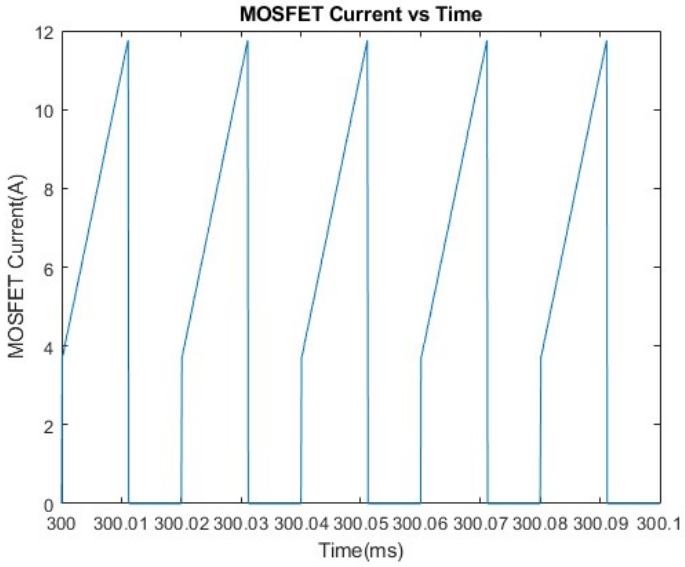

Figure 7: MOSFET current versus time graph ideal case.

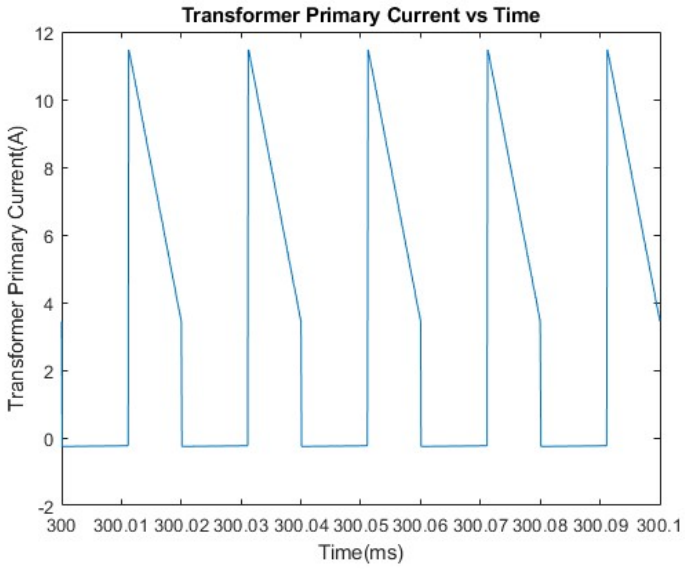

Figure 8: Current on the transformer primary winding versus time ideal case.

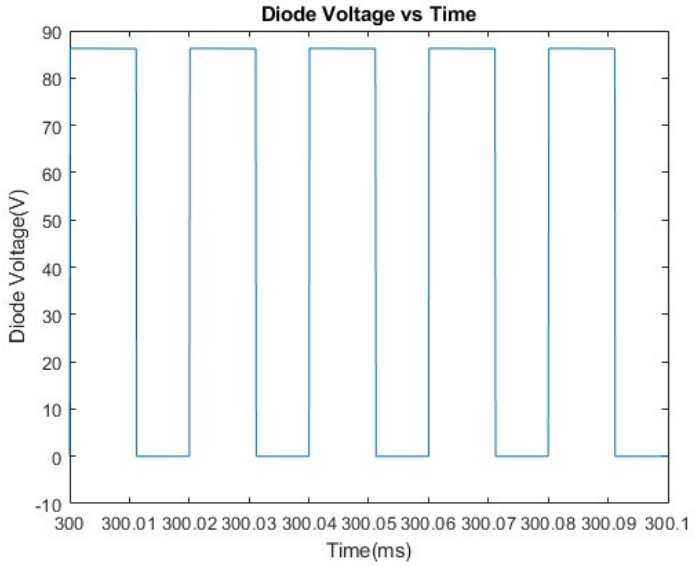

Figure 9: Diode voltage versus time graph ideal case.

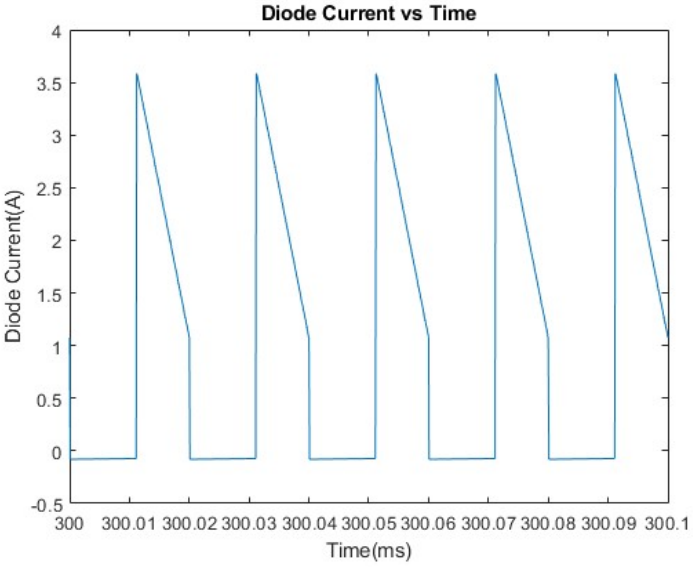

Figure 10: Diode current versus time graph ideal case.

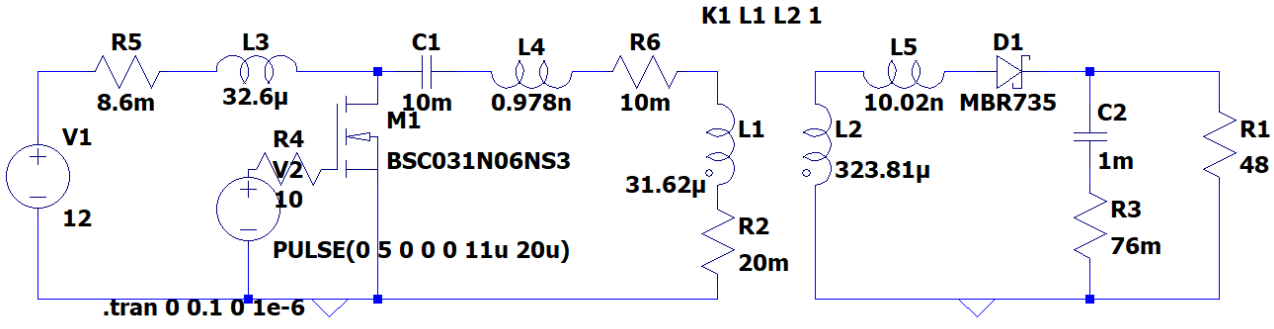

Figure 11: LTSpice Circuit Diagram used for simulating the circuit with parasitic.

Figure 12: V_{out} and V_{in} with parasitic included.

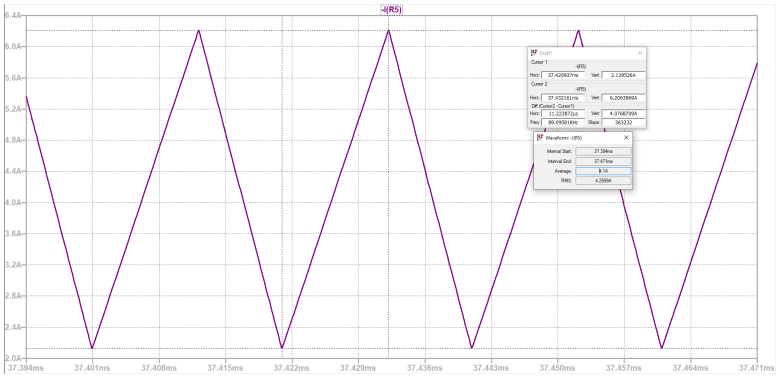

Figure 13: I_{in} waveform with parasitic included.

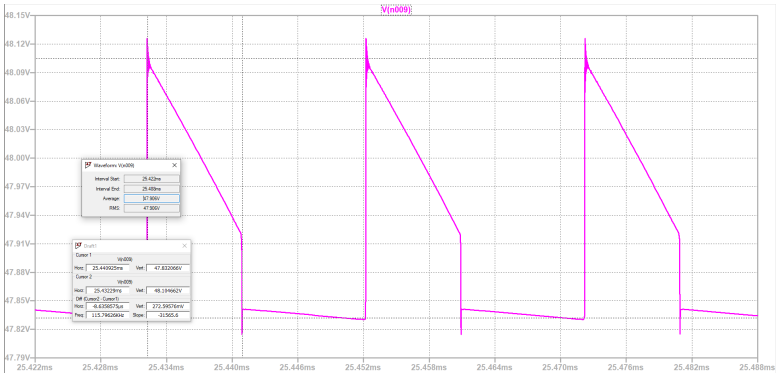

Figure 14: V_{out} waveform with parasitic included.

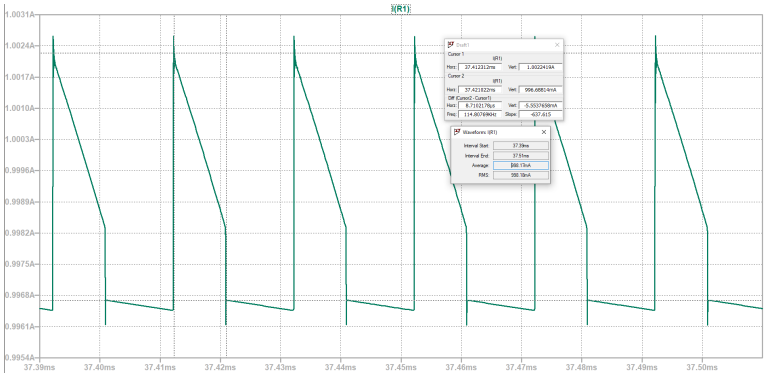

Figure 15: I_{out} waveform with parasitic included.

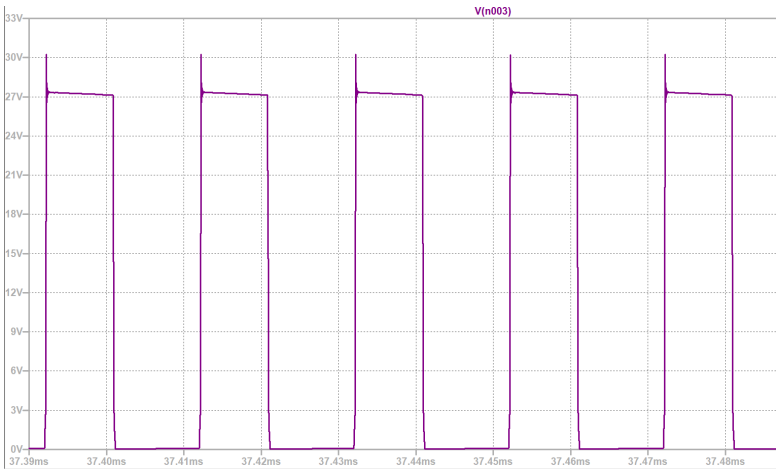

Figure 16: V_{Q_1} waveform with parasitic included.

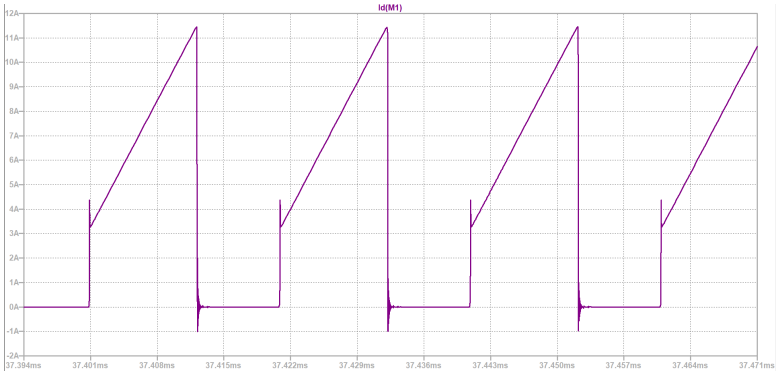

Figure 17: I_{Q_1} waveform with parasitic included.

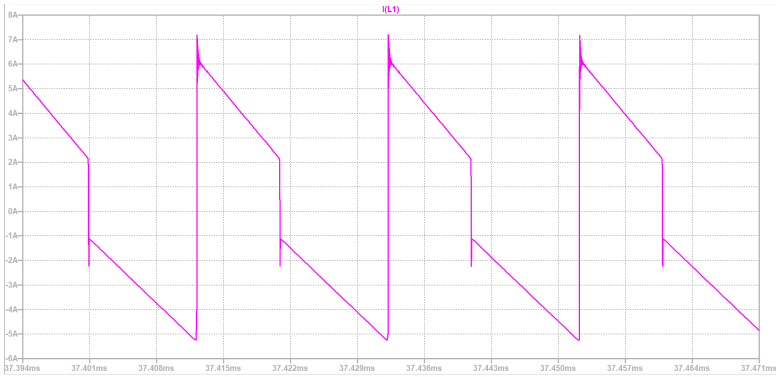

Figure 18: Caption

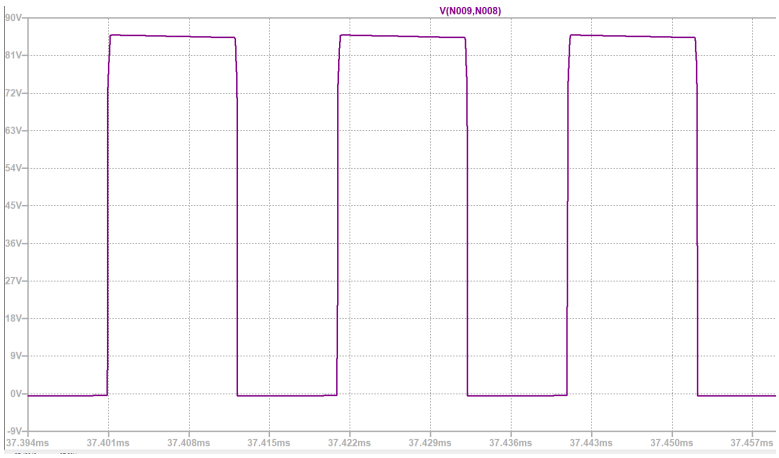

Figure 19: V_{D_1} waveform with parasitic included.

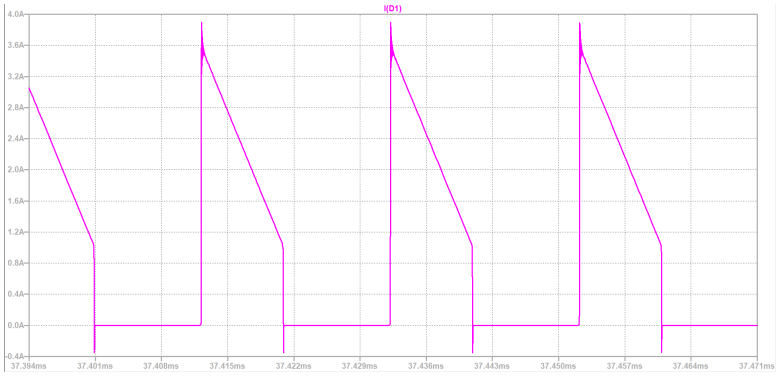

Figure 20: I_{D_1} waveform with parasitic included.

5 Component Selection

Other components of the isolated SEPIC converter is selected as given below. Considering the requirements of the topology and safety measures, we have selected potential candidates for the components.

5.1 Controller Selection

For the duty cycle calculation against the variation in input and output sides, and therefore gathering the current and voltage measurements from the sensors, we have decided our controller to be a digital one and we have selected the STM32-Nucleo-F334R8 board. Related information about the controller is given in Table 5.

Table 5: STM32-Nucleo-F334R8 board information.

Supply voltage:	5 V / 7-12 V
Max. CPU frequency:	72 MHz
Dimensions in mm:	70x82.5
Cost:	330 TL

5.2 Sensors

In order to adjust the duty cycle to compensate the changes in input and outputs of the converter, we should monitor the input and output voltages continuously. For this purpose we have selected an isolated Delta-Sigma modulator product for our voltage measurements. Its specifications are given in below Table 6. This product gives separates input from the output via capacitive double isolation barrier. The device can also be used for current measurements. Additional shunt resistances are not mentioned in this section.

Table 6: Isolated Delta-Sigma Modulator Specifications.[1]

Part no:	AMC1306M25DWVR
Sampling rate:	78k/s
Isolation strength:	7000 V
Cost:	143.5 TL

5.3 Switching Components

Looking at the topology as given in Figure 1, we have two switching components which are the MOSFET at the primary side and the diode at the secondary side of the transformer. Looking at the simulation results in Section 4, we have selected our switching components with the addition of safety factors. For the MOSFETs, we decided to parallel two MOSFET to decrease to losses due to $R_{ds,on}$.

Table 7: MOSFET Specifications.[2], will be paralleled.

Part no:	RSS070N05FRA
V_{ds}	45 V
I_d	7 A
$R_{ds,on}$	25 $m\Omega$
Total gate charge:	12 nC
Cost:	15.2 TL

To drive these MOSFETS properly, we have selected an isolated gate driver with specifications below in Table 8.

Table 8: Gate Driver Product Specifications.[3]

Part no:	UCC23313BDWYR
Current output peak:	5.3 A
Output supply:	14-33 V
Cost:	33.1 TL

For the diode, we have selected the following Schottky diode product for our design as given

below. Again we are not limited to this product, we can select another Schottky diode with similar ratings for our design if this one is not available during the implementation.

Table 9: Schottky Diode Specifications.[4]

Part no:	VSSAF512
V_r	12 V
I_f	5 A
$V_{f,max}$	0.88 V
Cost:	7.6 TL

5.4 Inductor Core Selection

For the inductor at the input side, in order not to saturate the core and obtain the desired inductance value, we have selected a Kool Mu core with its specifications below. Again we will be looking for alternative cores for our inductor design, considering our available space and limitations.

Table 10: Inductor Toroid core specifications.[5]

Part no:	0077548A7
Core material:	Kool Mu
Permeability:	125
Inductance Ratio:	127 nH/T^2
Dimensions in mm:	33x33x11
Cost:	52 TL

If we select and wind this core with $N = 16$ turns to get a $32.6\mu H$ inductor with AWG26 wire with the same paralleling configuration for the primary side, we get the ESR of the inductance as given below. Using the core dimensions, an estimate length for each winding is calculated as 48 mm.

$$ESR_L = \frac{48mm \times 16 \times 133m\Omega/m \times 10^{-3}m/mm}{12} = 8.6m\Omega \tag{7}$$

5.5 Capacitor Selection

Selecting the input capacitor, we desired a large enough capacitor with enough current rating. We have decided on paralleling three of the Aluminum capacitor with given parameters in Table 11. Since we are paralleling the capacitors, if the component will not be available, we can select smaller capacitance with similar ratings but this will result in higher volumes of the converter.

Table 11: Input Capacitor Specification.[6]

Part no:	KR3-035V332MJ250
Capacitance:	3300 μF
Rated voltage:	35 V
Ripple current:	1960 mA
Dimensions in mm	16x16x25
ESR:	not specified
Cost:	11 TL

For the output capacitor, since the output voltage ripple is desired to be very low, we agreed on putting a 1 mF capacitor to the output side. Parameters of the candidate capacitor is given below. We are not limited to using this capacitor, we can select another one with similar ratings in case of unavailability.

Table 12: Output Capacitor Specification.[7]

Part no:	KLH-100V102MK400
Capacitance:	1000 μF
Rated Voltage:	100 V
Ripple current:	2500 mA
ESR:	76 $m\Omega$
Dimensions(mm)	18x18x40
Cost:	23.3 TL

6 Loss Analysis

In this section the losses of the isolated SEPIC converter design, are calculated. For the calculations, steady state operation and below operation conditions are utilized. Losses on the MOSFET, diode, transformer and the input inductor are calculated. Summing up the below calculations, we have a total loss of 4.74 W. Also note that switching losses (gate opening and closing) are ignored compared to other losses.

Table 13: Operating Conditions for Loss Calculation.

Switching Frequency:	50 kHz
Duty Cycle:	0.5
Input Voltage:	16 V

6.1 MOSFET Conduction Losses

$$P_{MOS} = I^2 R_{ds,on} D = 8^2 \times 25 \times 10^{-3} \times 0.5 = 0.8W \tag{8}$$

6.2 Diode Conduction Losses

$$P_{diode} = I_o V_f (1 - D) = 2.25 \times 0.88 \times 0.5 = 1W \tag{9}$$

6.3 Transformer Core and Conduction Losses

Since we are working in CCM with a switching frequency $f_{sw} = 50kHz$, we have a core loss at most the quarter of the loss indicated in the datasheet [9].

$$P_{core,tr} = \frac{1}{4} \times 6 = 1.5W \tag{10}$$

For the conduction losses on the transformer, the average currents for (1-D) period is calculated from the simulation results.

$$I_{s,avg} = 2.25A \tag{11}$$

$$I_{p,avg} = 2.25 \times 3.2 = 7.2A \tag{12}$$

$$P_{cond,tr} = P_{primary} + P_{secondary} = (I_{p,avg}^2 \times R_p + I_{s,avg}^2 \times R_s)(1 - D) \tag{13}$$

$$P_{cond,tr} = 0.3W \tag{14}$$

6.4 Inductor Core and Conduction Losses

Looking at the toroid core datasheet, we have a $750mW/cm^3$ for 100 kHz and the core volume is 5.34 cm^3, giving 4 W for this core. Again we can assume quarter of this loss as a core loss since we work with 50 kHz and CCM.

$$P_{core,ind} = 1W \tag{15}$$

$$P_{cond,ind} = I_{in,avg}^2 ESR_{ind} = 0.14W \tag{16}$$

6.5 Efficiency Calculation for Different Load Cases

Above calculations are done for the 100% loading case where the output current is 1 A. For the 75%,50% and 25% loading cases, we can calculate the losses easily since the all the current averages will be the respective percentages of the loading cases. Therefore conduction (I^2R) losses will change by the square of the loading whereas the core losses will change by the loading percentage. Diode losses also will change by the loading percentage. Resulting efficiency table shows the results.

Table 14: Efficiency results of different cases.

Loading percentage	P_{loss}	P_{out}	Efficiency
100%	4.74 W	48 W	91.01%
75%	3.32 W	36 W	91.55%
50%	2.06 W	24 W	92.1%
25%	0.95 W	12 W	92.66%

7 Conclusion

In this report, design selections and selected components for the selected topology, are given. Magnetic design calculations and overall simulation results with both ideal and non-ideal components are given. Looking at the simulation results we observed some facts about our design. There are significant differences between the ideal and non-ideal simulation results. For instance, idealized duty calculation does not give the required duty for desired output voltage due to losses and drops on the non-idealities of the components. Also considering the starting operation, there might be overshoots on the components that could damage them. We will be more cautious about the non-idealities and further investigate alternative components to reduce the non-ideality effects on the topology.

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