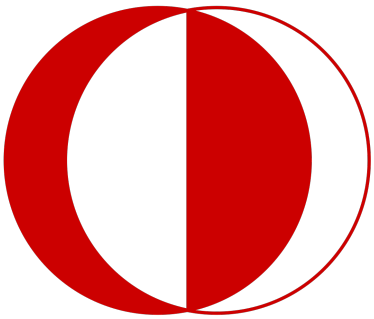

Middle East Technical University

EE464 Static Power Conversion II

Hardware Project Final Report

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1 Introduction

In this report the EE464 hardware project is finalized. The object was to implement an isolated DC-DC converter. Input range is 12-18 V and the regulated output is desired to be 48 V with maximum of 3% ripple. We have selected the isolated SEPIC topology for our design begun constructing the circuit. After some tests and calibration, we successfully run our design in the demonstration. In the following sections, finalized hardware and components, test results before the demo and finally the demonstration procedure are explained. Then the report is concluded.

2 Topology Selection

2.1 Available Topologies

The requirements of the project point that an isolated converter must be designed. The list of possible choices that were covered in lectures can be stated as:

- Flyback
- Two-switch Flyback
- Forward with reset circuit
- Forward with two primary windings
- Two-switch Forward
- Push-Pull
- Half-Bridge Isolating
- Full-Bridge Isolating

These topologies don't cover all of the available designs, though. The non-isolated DC-DC converters that are capable of either stepping-up and stepping-down depending on duty cycle, i.e. SEPIC, Cuk and Zeta, can also be isolated by replacing on of their inductors with a transformer. Also, there are converters that utilize resonance and achieve soft switching to decrease switching losses. Therefore, the list can be expanded by the addition of these converters below.

- Isolated SEPIC
- Isolated Cuk
- Isolated Zeta
- Resonant and Quasi-Resonant Converters

Design and implementation considerations are used as a filter for topology selection which turned out to be quite accurate based on the experiences of all groups that implemented the project. These considerations were based on concerns about the lack of knowledge on some design steps which will be discussed in detail.

2.2 Design Considerations

2.2.1 Transformer Design

Transformer design was the first building block of the design. All of the listed topologies utilize transformer for isolation and voltage level adjustment which makes the transformer design the most critical design step. Particularly, the implementation of the transformer (i.e. winding) was a large concern; which lead to a decision of selecting a topology with a single primary and a single secondary winding for easier implementation. The discarded topologies at this stage can be stated as:

- Forward with two primary windings
- Push-Pull
- Half-Bridge Isolating
- Full-Bridge Isolating

2.2.2 Switch Control

Some of the stated topologies utilize synchronous switching, which further increases complexity of the design and implementation. Those topologies are discarded in the sake of simplicity are given below.

- Two-switch Flyback
- Two-switch Forward

2.2.3 Snubber Design

As some of the isolated DC-DC converters are highly dependant on a snubber by nature (i.e. switch connected in series with primary transformer winding), these topologies are less efficient than others. Also designing a snubber is not very straight-forward and may require some iterations to be optimized. The said converters that are abondoned are:

- Flyback
- Forward with reset circuit
- Isolated Zeta

2.2.4 Resonance

The existance of inductors and capacitors in the circuit may result in resonance in several frequencies, increasing the difficulty of the design. Also, there are some topologies which intentionally utilize resonance for soft switching, which are briefly mentioned through the end of the course. Resonance would be very difficult to work on; thus it is decided to try avoid it altogether. Avoided topologies are:

- Isolated Cuk
- Resonant and Quasi-Resonant Converters

It was clear after the considerations that Isolated SEPIC was the topology of choice. The topology offers an easy implementation with a simple transformer, single switch, no snubber required and no resonance effects.

2.3 Isolated SEPIC

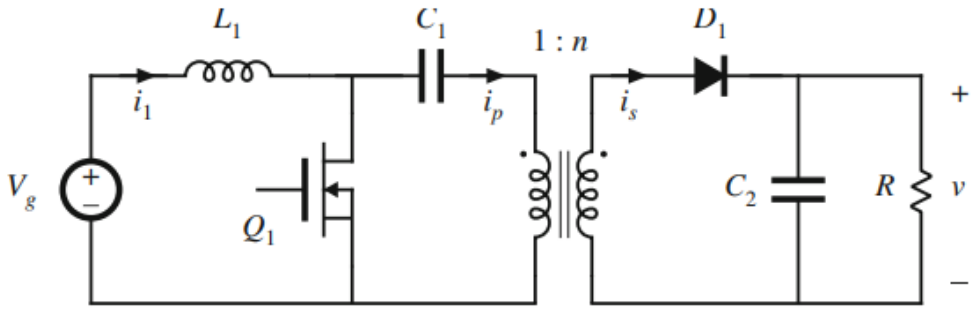

Figure 1: Isolated SEPIC

Isolated SEPIC (Figure.1) is derived from SEPIC, by changing the parallel inductor with a transformer. Initially, it seems redundant to use such topology due to extra components compared to Flyback converter; however, this converter is realized by the components seen in (Figure.1) only. To clarify, the circuit does not need extra circuitry that are used to deal with real world effects such as snubber and reset circuits.
Voltage transfer ratio of the isolated SEPIC converter is given as:

$$\frac{V_o}{V_s} = \frac{N_2}{N_1}\frac{D}{1-D}$$

Upsides and downsides of the isolated SEPIC converter can be discussed at this point.

2.3.1 Advantages

- Low-side switching
- Continuous input current
- Simple transformer design
- No snubber required

2.3.2 Disadvantages

- High component count (high cost in mass production)
- Extra inductor to be wound (due to high current rating in this project)
- Nonlinear relation between duty cycle and transfer ratio
- High MOSFET voltage levels ($V_{Q_1} = V_g + V_o/n$)
- High MOSFET current levels ($\approx 2I_1$)
- High current ripple in series capacitor

There is also an interesting effect in this converter. Assuming C_1 is very large ($V_{C1} = V_g$) and $L_{m,primary} = L_1$ is achieved, current waveform of the input inductor and magnetizing inductance of the transformer on primary side will be the same theoretically. Moreover, with a use of a Hall effect sensor connected in series with the input inductor at the input and designing a controller for input current would control both currents (may be useful).

3 Simulations

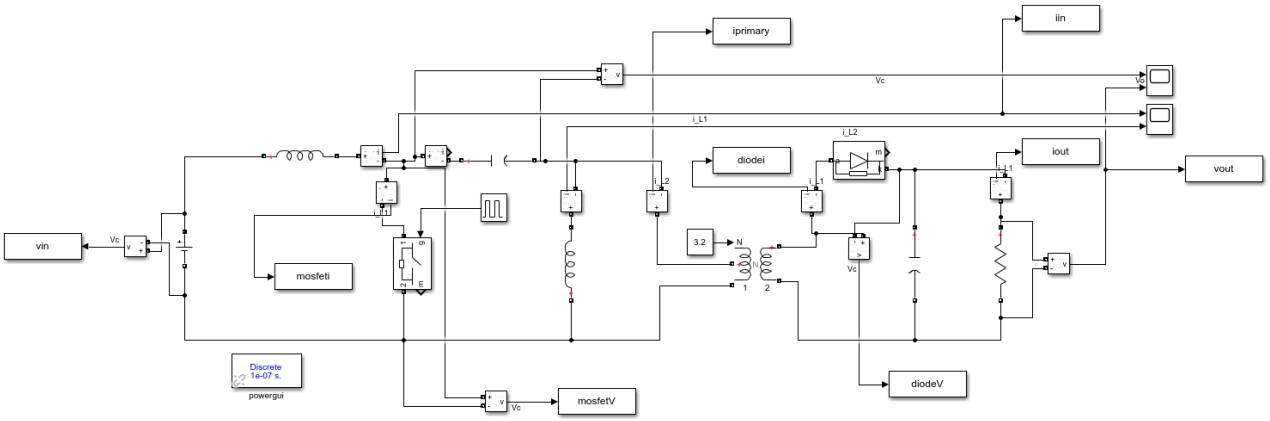

Figure 2: Simulink simulation circuit for ideal case.

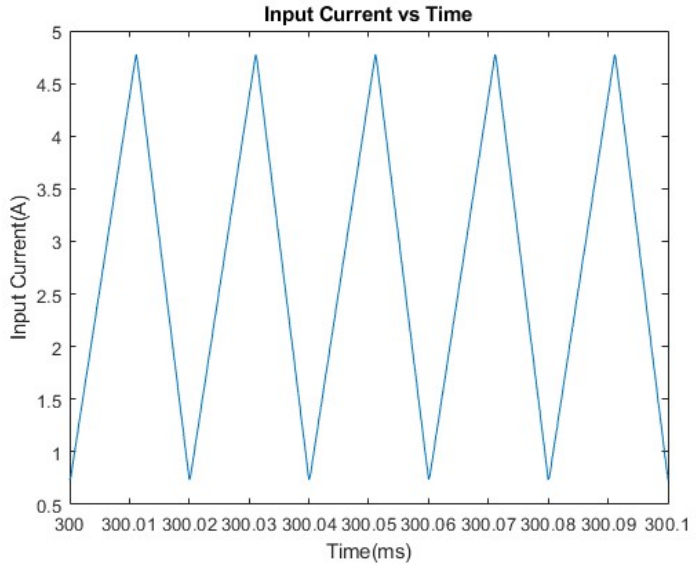

Figure 3: I_{in} versus time graph ideal case.

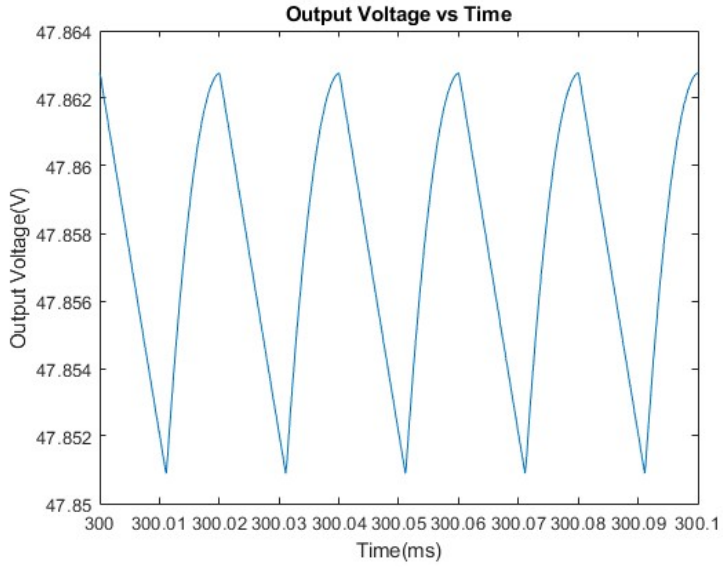

Figure 4: V_{out} versus time graph ideal case.

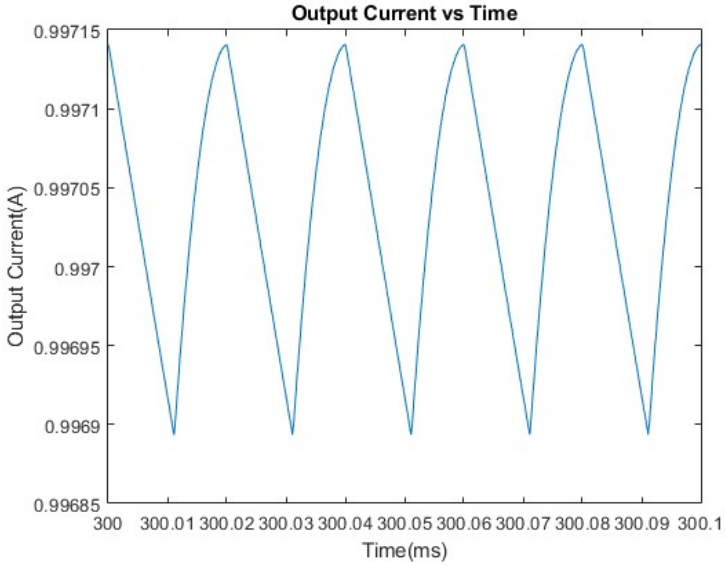

Figure 5: I_{out} versus time graph ideal case.

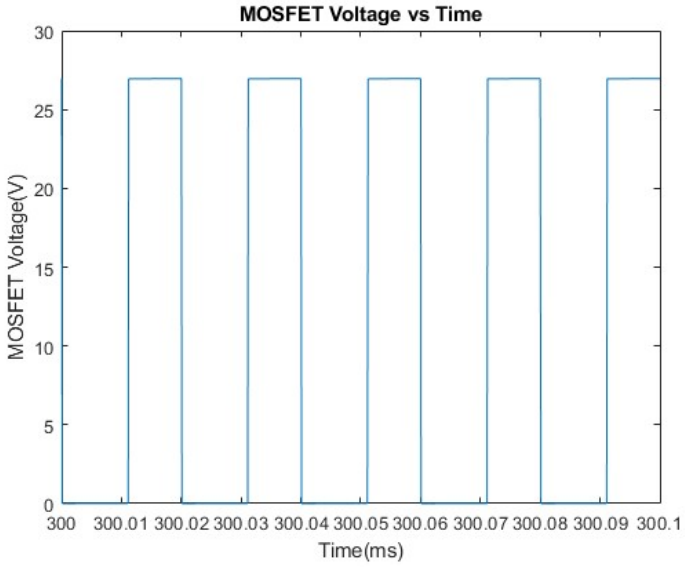

Figure 6: MOSFET voltage versus time graph ideal case.

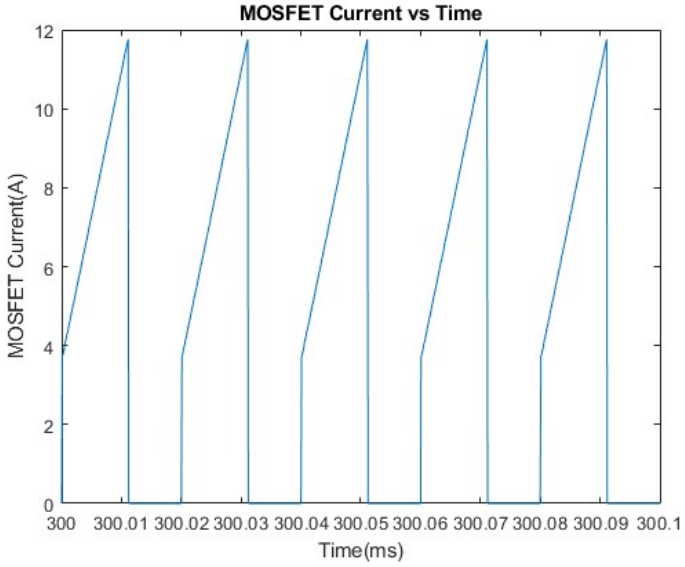

Figure 7: MOSFET current versus time graph ideal case.

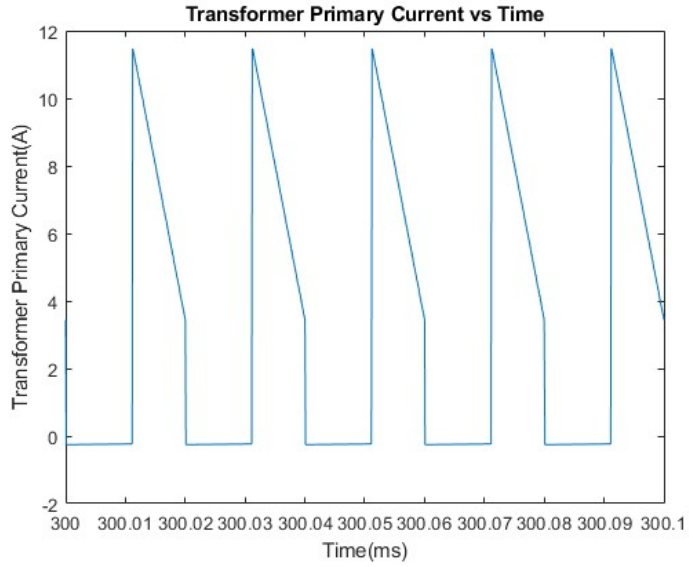

Figure 8: Current on the transformer primary winding versus time ideal case.

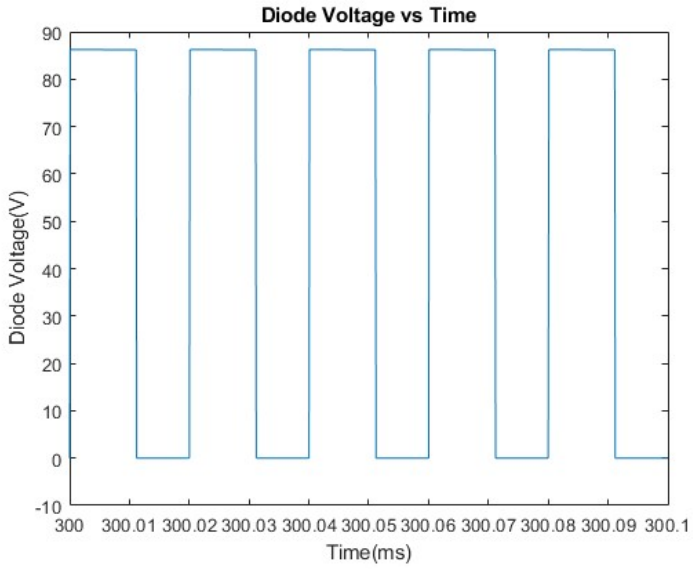

Figure 9: Diode voltage versus time graph ideal case.

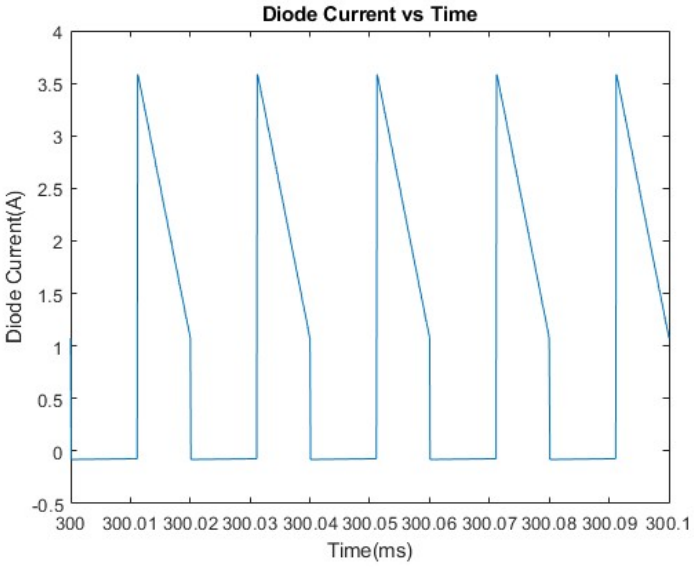

Figure 10: Diode current versus time graph ideal case.

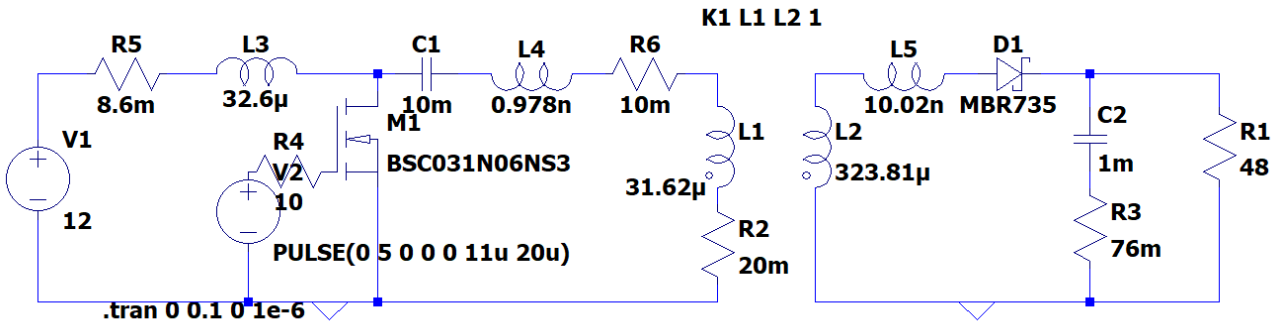

Figure 11: LTSpice Circuit Diagram used for simulating the circuit with parasitic.

Figure 12: V_{out} and V_{in} with parasitic included.

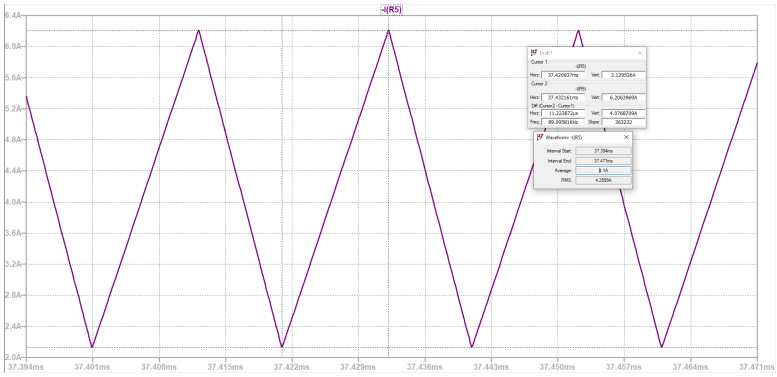

Figure 13: I_{in} waveform with parasitic included.

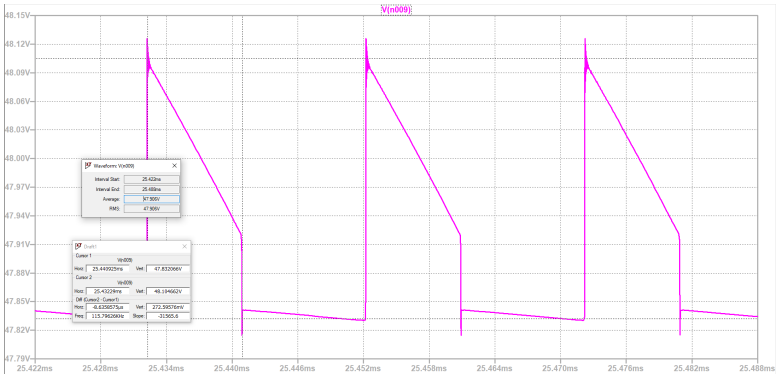

Figure 14: V_{out} waveform with parasitic included.

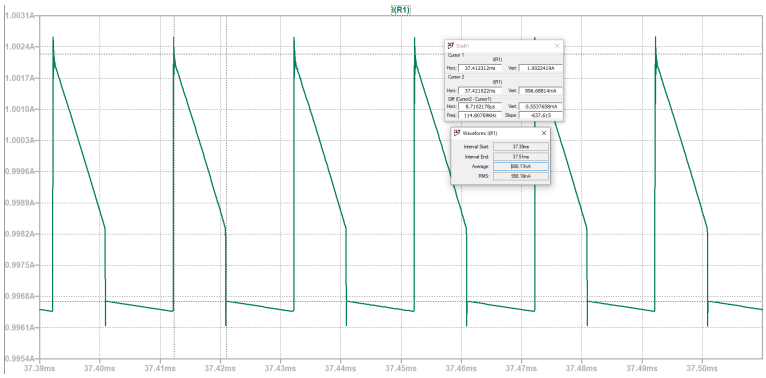

Figure 15: I_{out} waveform with parasitic included.

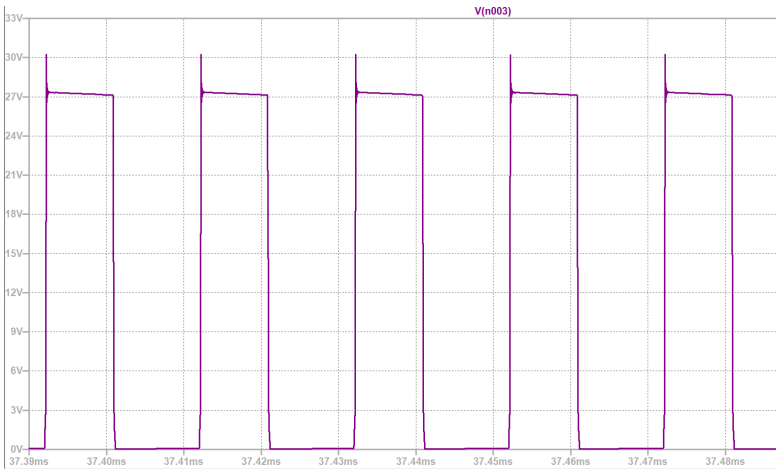

Figure 16: V_{Q_1} waveform with parasitic included.

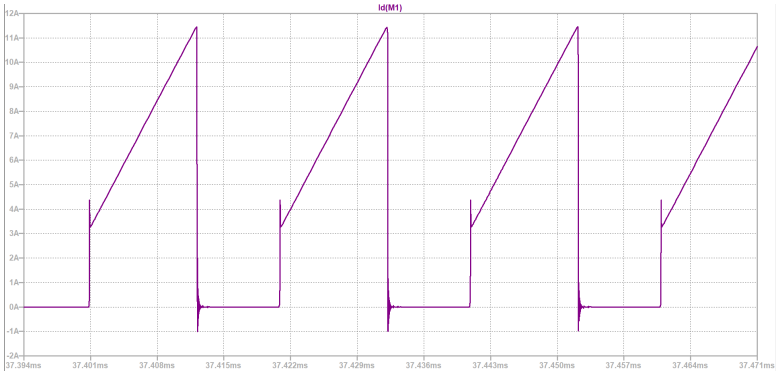

Figure 17: I_{Q_1} waveform with parasitic included.

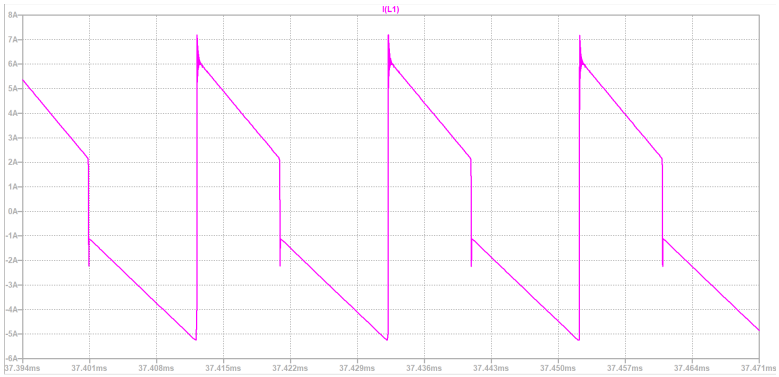

Figure 18: Caption

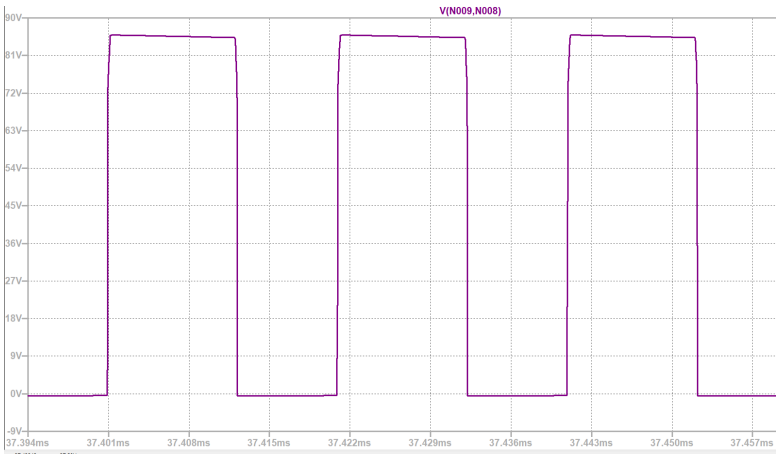

Figure 19: V_{D_1} waveform with parasitic included.

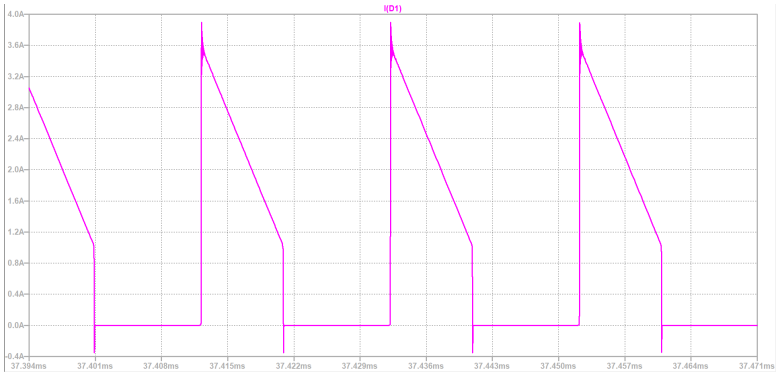

Figure 20: I_{D_1} waveform with parasitic included.

4 Hardware Design

Some design decisions were made initially and were followed throughout the design process. Digital control was chosen to add flexibility to design. These flexibilities are adjustable switching frequency, ability to implement soft start function and ability to limit the duty cycle. All of the design was made according to a switching frequency of $f_{sw} = 50\ kHz$; but the components were selected to operate up to 100 kHz to retain flexibility. Also, overall design was aimed to operate with a single supply.

4.1 Voltage Level Conversions

To achieve these aims, there was a need for a third isolated zone for digital signals and the controller. We have selected and implemented all the design with respect to this restriction such as implementing an extra isolated supply for the digital zone. Furthermore, we utilized isolated Analog to Digital Converters (ADCs) in order to measure input and output voltages in an isolated way. The ADCs operate between 3.3V and 5V which were needed to be converted from input and output voltage levels as well. Therefore, there are quite a lot of voltage level converters on the final design (Figure 21); which may be the biggest disadvantage of using a digital controller.

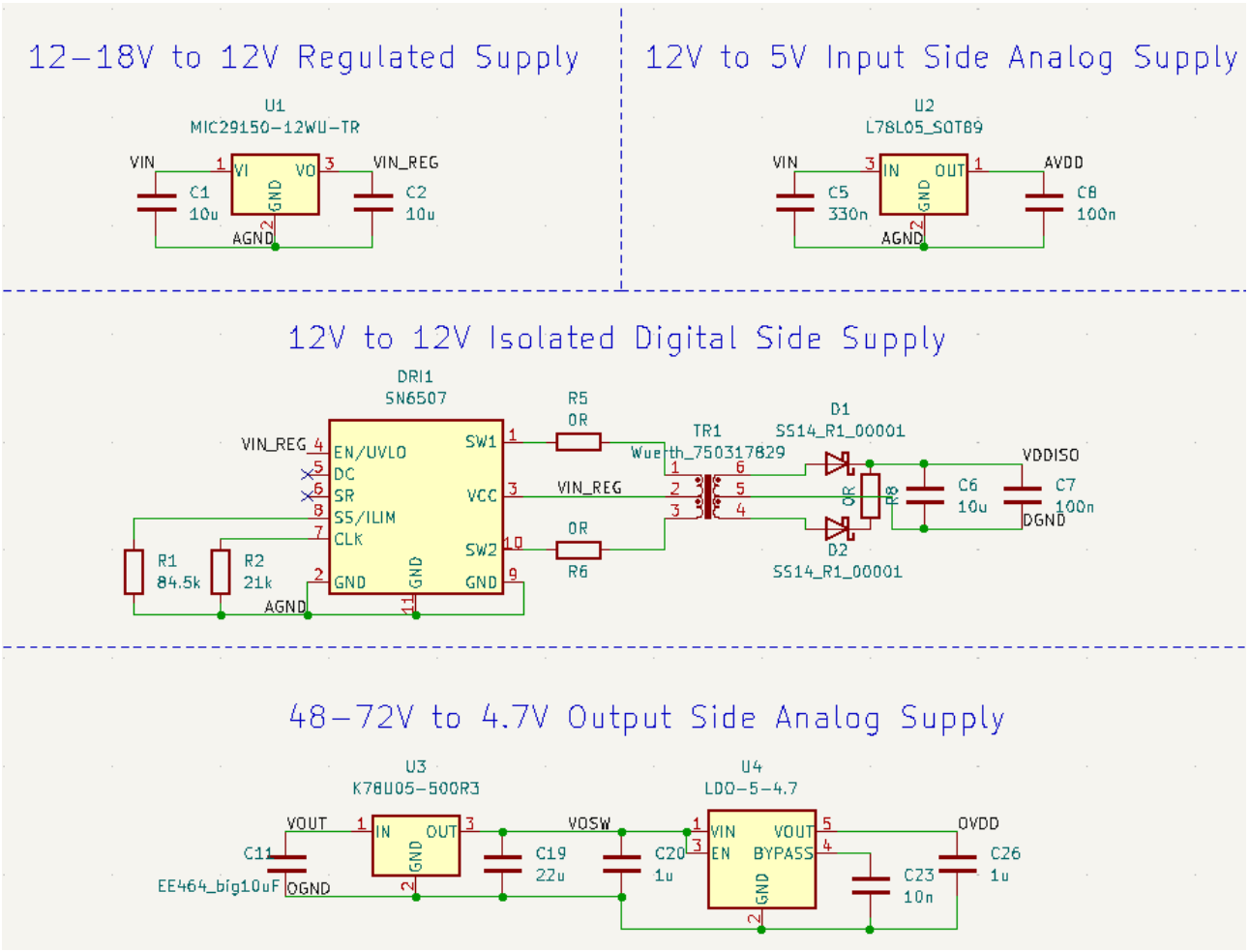

Figure 21: Different voltage level converters on the final design

4.2 Analog to Digital Converters

The mentioned ADCs are AMC1336 which utilize so called Delta-Sigma ($\Delta\Sigma$) modulation for conversion. The output of this modulation is a bitstream of highs and lows, where the ratio of highs to all bits on a time average gives the analog voltage level. The analog voltage reading range of AMC1336 is given as ± 1V [2], which is achieved by simple resistive dividers (Figure 22). We have connected these ADCs directly to the controller and digitally read the bits successfully using SPI interface.

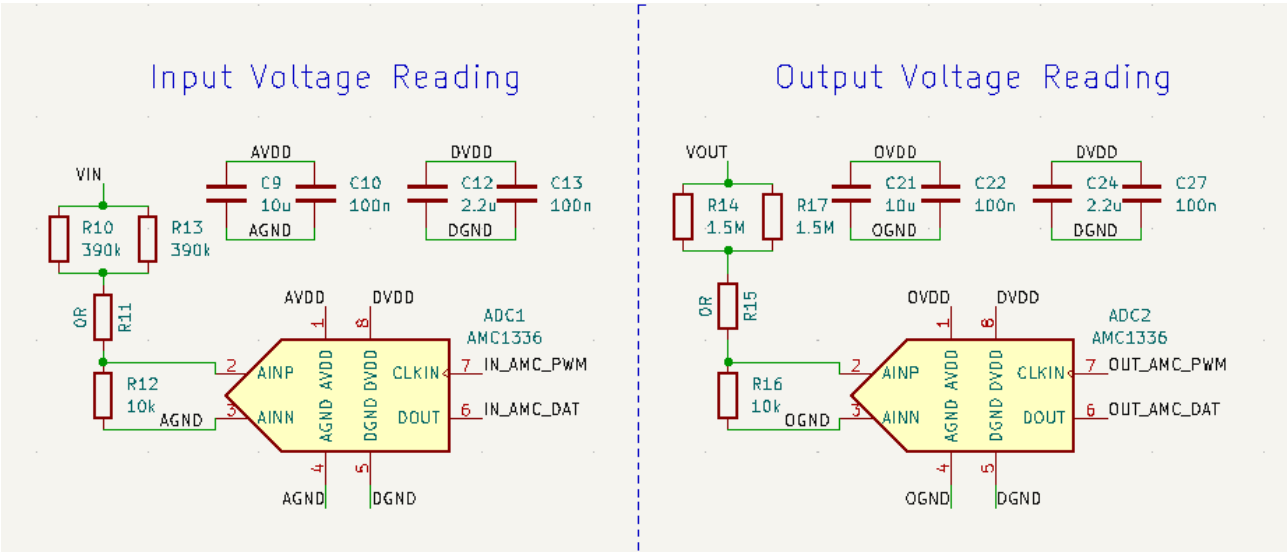

Figure 22: ADC implementation on the final design

4.3 Gate Driver

As the PWMs are generated in digital side, there is a need for an isolated gate driver to amplify and send these PWM signals to the MOSFET gate at the input side. UCC23313B was chosen as the driver which has an undervoltage lockout (UVLO) protection of 8V; which means it can drive with voltage levels higher than 8V. MOSFET gate is also protected with a Zener diode with 18V Zener voltage and a resistor is connected for passive discharge of the gate capacitance (Figure 23).

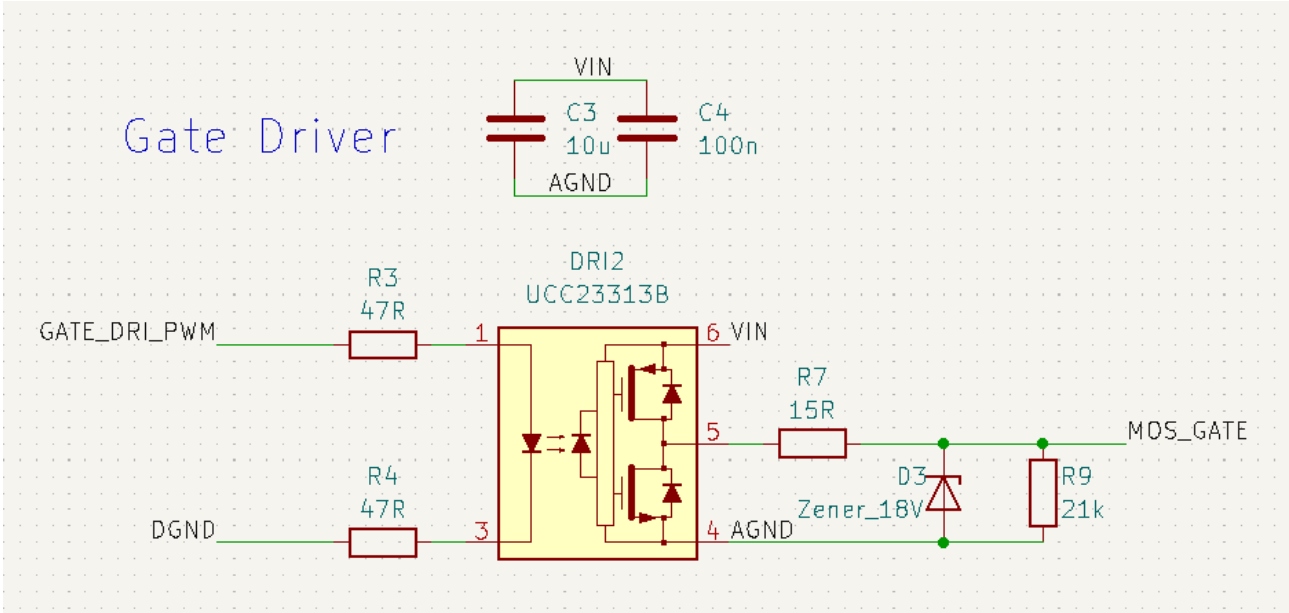

Figure 23: Gate Driver implementation on the final design

4.4 Isolated SEPIC

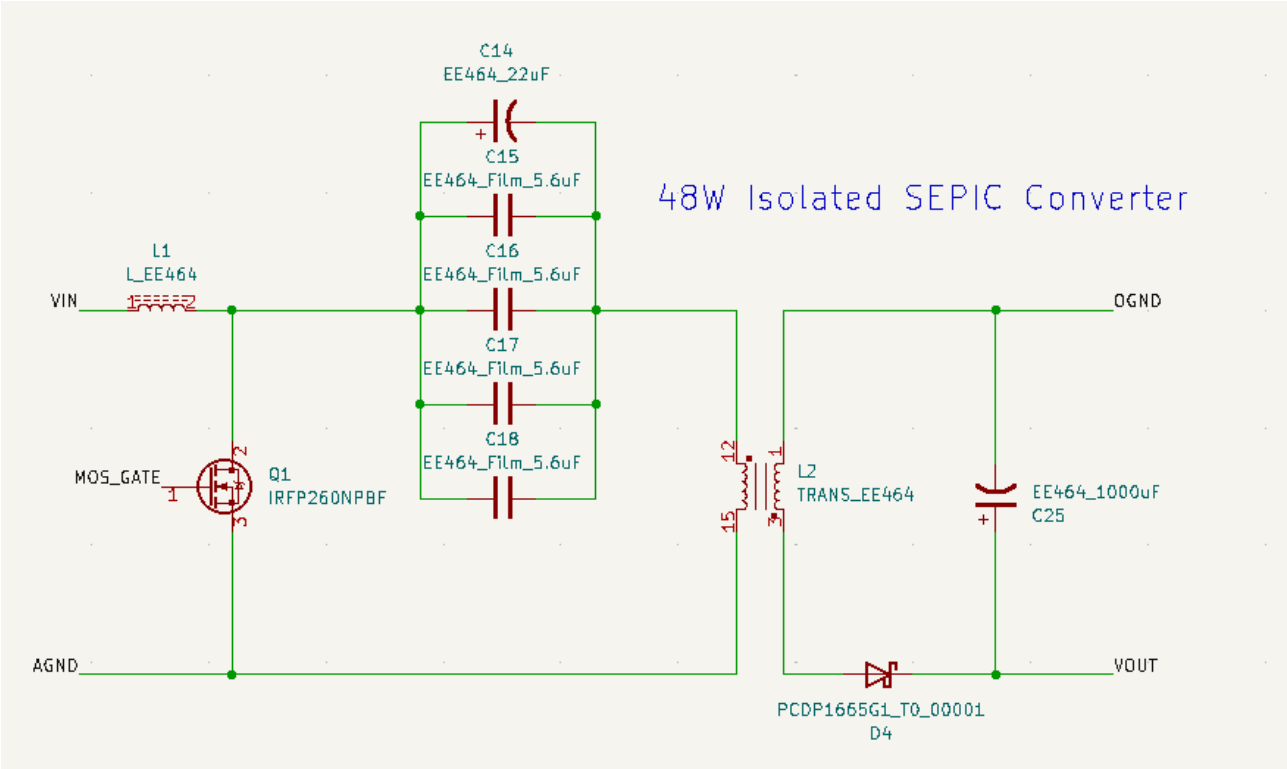

Figure 24: Isolated SEPIC implementation on the final design

The implemented isolated SEPIC is nothing different than the theoretical model (Figure 24). The only consideration was the current ripple of the series capacitors. Film capacitors in parallel were used in order to supply the required current at all times. Another electrolytic capacitor was used in parallel so that the capacitance value is elevated. The diode used is a Schottky diode, to eliminate reverse recovery time from consideration. DC-link capacitance is a very large 1000μF aluminum electrolytic capacitor. MOSFET is a discrete N-type with very high voltage and current rating to eliminate any faulty conditions. Magnetic components are discussed in Magnetic Design section of the report. Output side is reversed in the sake of a better PCB layout.

4.5 Terminals and Connectors

Input and output connections are done with screw terminals soldered on the PCB. Also, to reduce the size and cost, the digital controller haven't been put over the PCB; instead, jumper connectors were placed to the digital power and signal outputs (Figure 25).

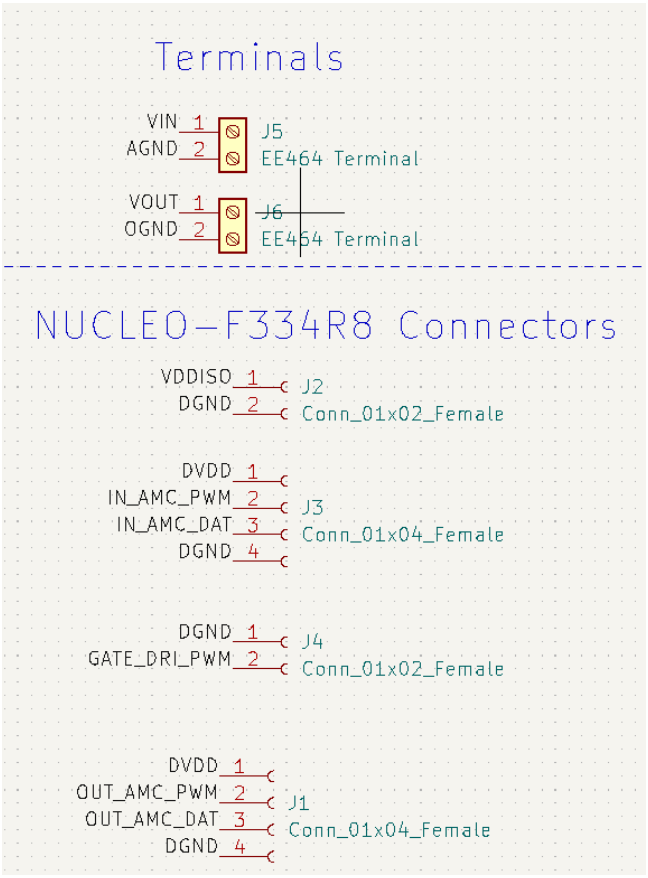

Figure 25: Terminals and connectors on the final design

5 PCB Design

PCB was designed on a single layer of copper with minimum number of holes to simplify the manufacturing process (Figure 26). Three isolated areas can be easily seen with transformer and isolated components are the only components connected to multiple areas. The power carrying paths are designed as large as possible, with extra wide clearances are given between each node in those paths for fault prevention. Signal carrying paths on the other hand, were drawn thinner in comparison; so that, they are loosely protected from high currents.

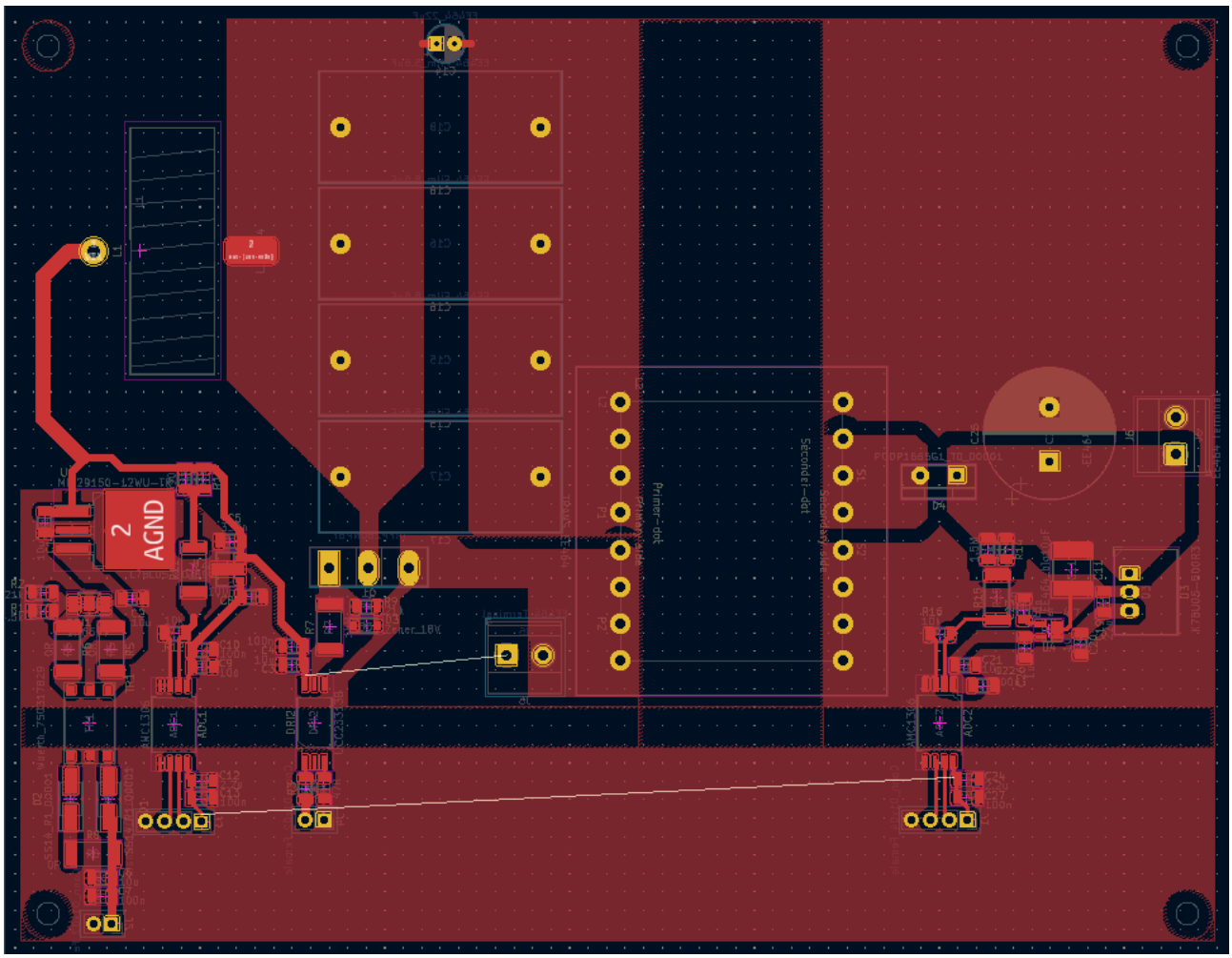

Figure 26: PCB design as seen on the PCB Editor of KiCad

As seen in Figure 24, there are disconnections at the input side and digital side. The digital side is handled with jumpers to the controller; however, the disconnection at the input side is intended. During the design, a need for a jump at the power carrying path has arisen. This was due to single copper layer design and could not be resolved in any orientation. Therefore, we have decided to make the jump in series with the input inductor using a wire; which would ultimately add additional inductance and a small resistance to the inductor (Figure 27).

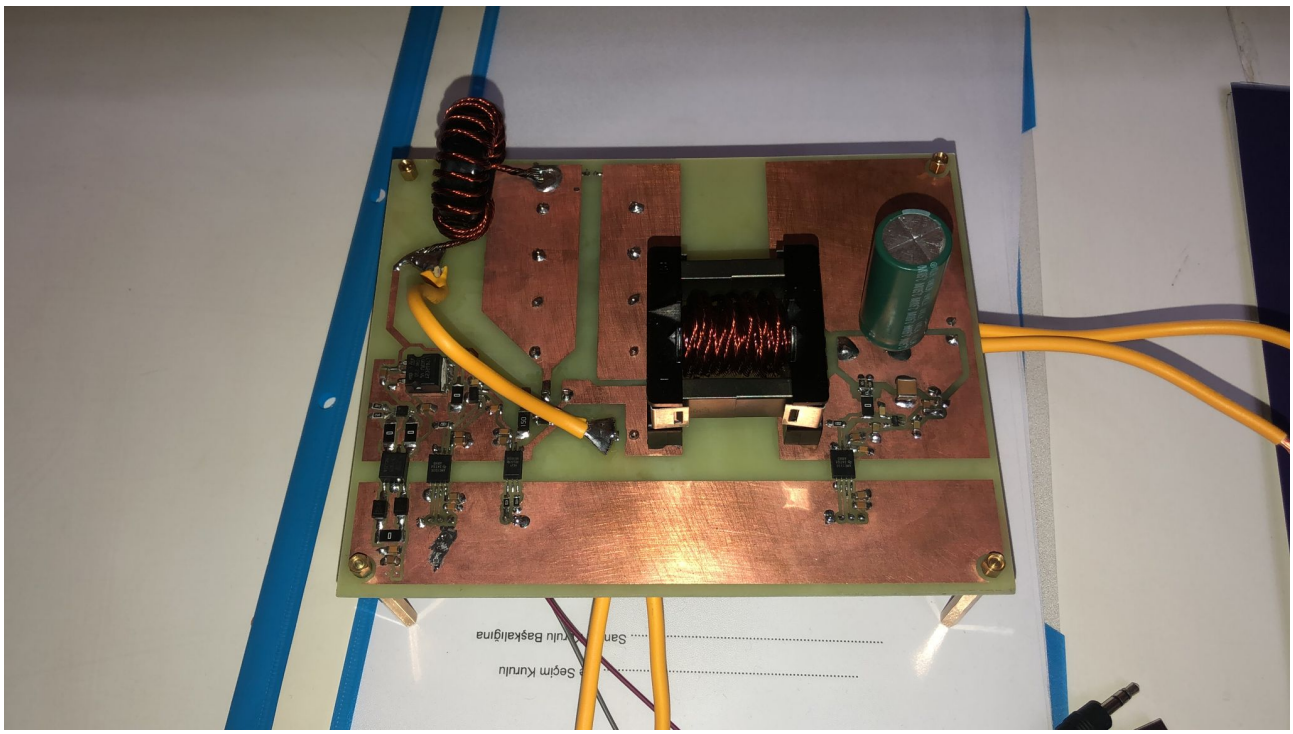

Figure 27: Top view of the converter, yellow wire over the PCB is the jump

Input side capacitors, MOSFET, diode, terminals, connectors and the DC-DC converter in the output side is mounted from the bottom as there is no copper on the back for through-hole components to be soldered (Figure 28).

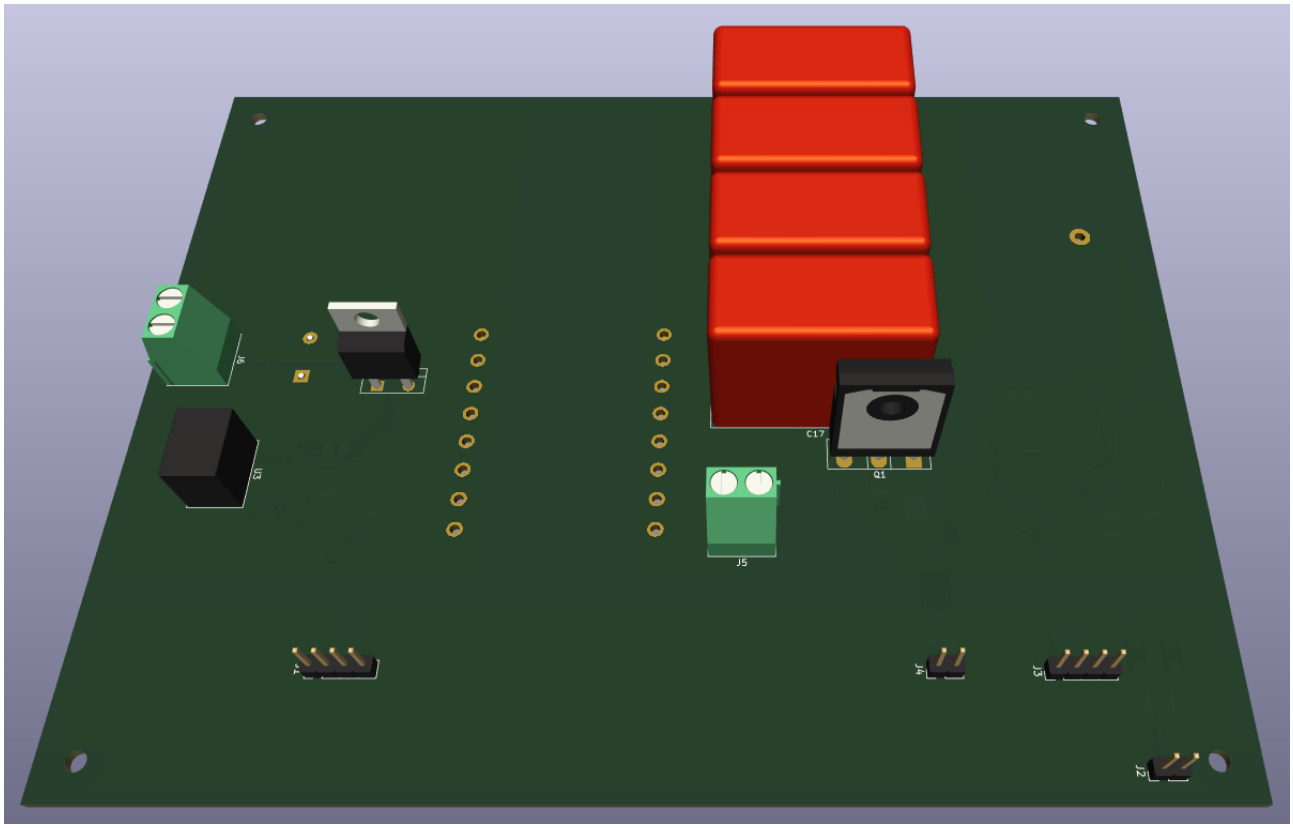

Figure 28: Bottom view of the converter as seen on 3D viewer of KiCad

6 Magnetic Design

6.1 Transformer

After selecting the topology of isolated SEPIC converter and proper switching frequency, the magnetic design for the transformer is performed. Starting with a proper cable selection we have selected AWG26 for our design. For our design requirements, paralleling of this wire for primary and secondary sides resulted in the configuration given in Table 2.

Table 1: AWG26 cupper conductor parameters.(REF)

Max. Amp rate:	0.361 A
Conductor diameter:	0.4 mm
Conductor cross-section area:	0.128 mm^2
Max. frequency for 100% skin depth:	107 kHz

Table 2: Transformer Wiring Configuration.

Transformer side	Assumed Current level	# of parallel wires	Winding number
Primary	4.4 A	12	10
Secondary	1 A	3	32

Then selecting the appropriate core material and geometry, we have performed some iterations and decided on ETD39 Ferrite core[7]. The fill factor of this configuration is calculated as 0.22. We obtained the transformer given in Figure 29. Primary windings are at the outside of the center leg of the core.

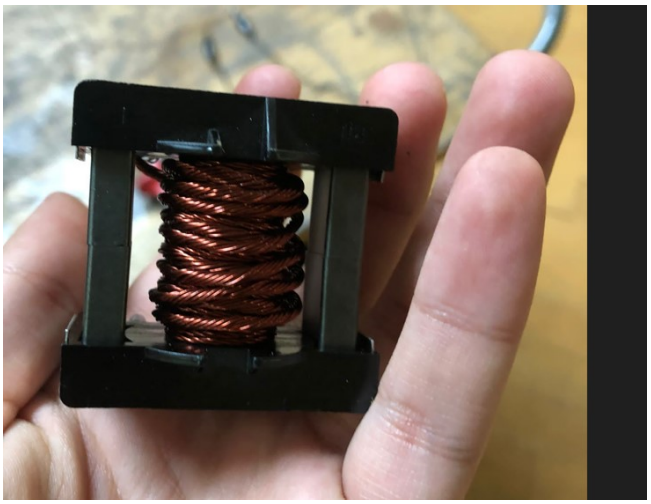

Figure 29: Finalized version of the transformer.

6.2 Input Side Inductor

For the input inductor of the topology, we selected a small Kool Mu toroidal core and used the wiring configuration we used for the primary side of the transformer. With this way we achieved a 37.56 μH inductance for the input.

Table 3: Inductor Toroid core specifications.[1]

Part no:	0077548A7
Core material:	Kool Mu
Permeability:	125
Inductance Ratio:	127 nH/T^2
Dimensions in mm:	33x33x11
Cost:	52 TL

Figure 30: Finalized version of the input inductor.

7 Other Components

7.1 Controller

For our design, we have selected a digital controller for the closed loop control. Selecting a STM32-Nucleo-F334R8 board, we have obtained a much less dependency on the control circuit. Correctly reading the input and output measurements would be enough for our digital controller.

Table 4: STM32-Nucleo-F334R8 board information.

Supply voltage:	5 V / 7-12 V
Max. CPU frequency:	72 MHz
Dimensions in mm:	70x82.5
Cost:	330 TL

7.2 Push Pull Converter

In order to supply the input and the controller from the same supply, we needed an isolated supply for our mmicrocontroller region. This supply will mainly be the push-pull controller with an analog controller. Proper circuit of the push-pull converter can be found in PCB section. For the specific components, transformer and driver of the push pull converter datasheets can be found in references [8] and [9].

7.3 Sensors

To read the input and output voltages in an isolated manner we have selected Delta-Sigma modulators. With appropriate shunt elements for the voltage division and power supply, we also needed a proper reading method in software as this device sends the reading information in a form of bit-stream.

Table 5: Isolated Delta-Sigma Modulator Specifications.[2]

Part no:	AMC1336M25DWVR
Sampling rate:	78k/s
Isolation strength:	7000 V
Cost:	143.5 TL

7.4 Switching Components

As our isolated SEPIC topology requires one MOSFET and a diode, we have selected some products and we have thought on paralleling our MOSFET selection. After the presentation and feedback sessions, we have decided to use one MOSFET with high ratings to ensure safe operation. We also selected another diode with higher ratings.

Table 6: Final selection of MOSFET".[3].

Part no:	IRFP260NPBF
V_{ds}	200 V
I_d	50 A
$R_{ds,on}$	40 $m\Omega$
Total gate charge:	234 nC
Cost:	59.8 TL

For the powering of the selected MOSFET, we used our pre-selected gate driver. It opens and closes the gate in an appropriate time with a proper gate circuitry.

Table 7: Gate Driver Product Specifications.[4]

Part no:	UCC23313BDWYR
Current output peak:	5.3 A
Output supply:	14-33 V
Cost:	33.1 TL

Table 8: Selected Schottky Diode Specifications.[5]

Part no:	PCDP1665G1
V_r	650 V
I_f	10 A
$V_{f,max}$	1.5 V
Cost:	117 TL

7.5 SEPIC Capacitor

As the isolated SEPIC topology requires a large capacitor between the input inductor and transformer, we have selected aluminum capacitors for this component. However, at the feedback session, we are advised that a film capacitor would be better option for this purpose since the film capacitors can loose their rated capacitances at an alternating current. Finally paralleling the film capacitors and a aluminum capacitor, we obtained our SEPIC capacitor.

7.6 Output Capacitor

Holding onto the selected output capacitor, we put a 1mF capacitor with its item specifications are given below:

Table 9: Output Capacitor Specification.[6]

Part no:	KLH-100V102MK400
Capacitance:	1000 μF
Rated Voltage:	100 V
Ripple current:	2500 mA
ESR:	76 $m\Omega$
Dimensions(mm)	18x18x40
Cost:	23.3 TL

8 Software

Isolated SEPIC converter is an unusual type of DC-DC converter. Thus, there is no analog controller produced for specifically Isolated SEPIC. Buck-Boost converter controllers might be used. However, we decided to use digital controller STM32 -Nulceo. First we tried to give open loop switchig PWM from controllers pin. First, we give 50kHz switching frequency. But the converter gets in DCM mode and we invrease the switching frequency to 64kHz. The reason of selecting 64kHz the controllers clock is 64MHz and we divided it with 1000. After we tried to close feedback loop by measuring the output voltage. We were planning to read both input and output voltage to get faster response thanks to feedforward. Our plan was reading the digital data comes from AMC1336 via controllers clock ports since the controller has only one SPI port. However, we were not able to read the data with clock since there were synchronization problem between AMC1336 and controller. We decided to measure only the output voltage with SPI port. The coming voltage data were nonlinear. We take the sensed data via controller and multimeter and put them into a polynomial fitter. We obtained 4th order polynomial. After the measuring problem is solved, we write PI block to closed loop control. The PI code is run with interrupt for every 0.1 seconds. We put a limiter if the PI block tries to give more than 60% duty cycle the PI code stops and we only give 60%. We also add a code that if the output voltage is between 47.5V and 48.5V for a while the code

fixes the duty cycle. Out Kp value were 0.001 and Ki value were 0.01. When we connect PI block to our Simulink simulation the high Kp Ki values caused 100% duty cycle. However, during the demonstration in the light of suggestion of our professor Ozan Keysan higher Kp Ki values gave better results.

9 Test Results

After implementing the PCB, we tested our circuit with open loop configuration. Before going into the load tests, we manually gave a constant duty PWM and observed the switching behavior. After observing the successful switching, we began load tests. Connecting a light load to the output we received the following voltage forms shown on the oscilloscope screen in Figure 31.

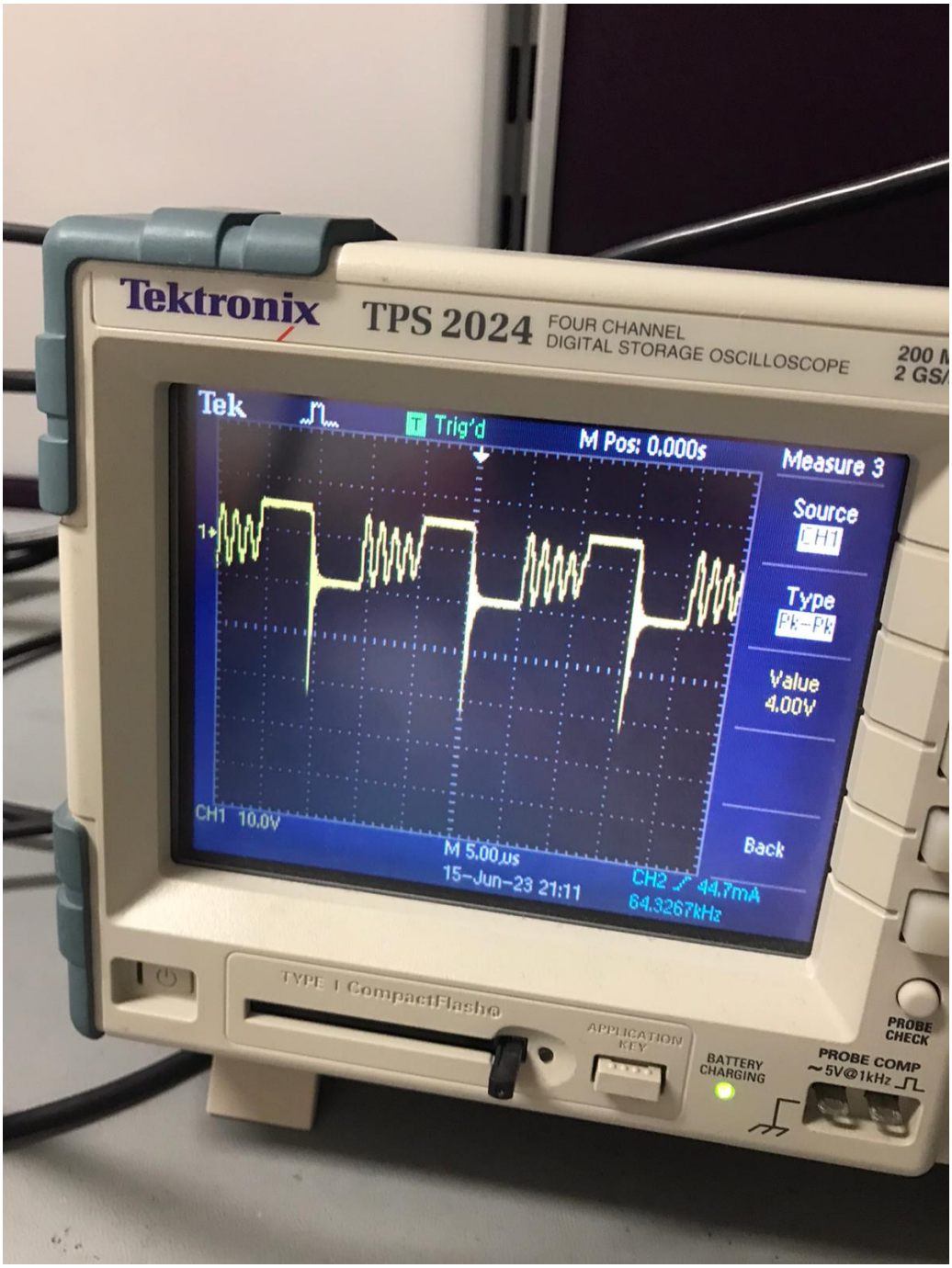

Figure 31: DCM operation under light load.

As seen in Figure 31, our converter works in DCM. Reasons of working in DCM is connected load draws high current and Mosfet switching frequency is low. We increased the switching frequency to 64kHz and connected a load, then converter starts to work in CCM. Figure 32 shows it clearly.

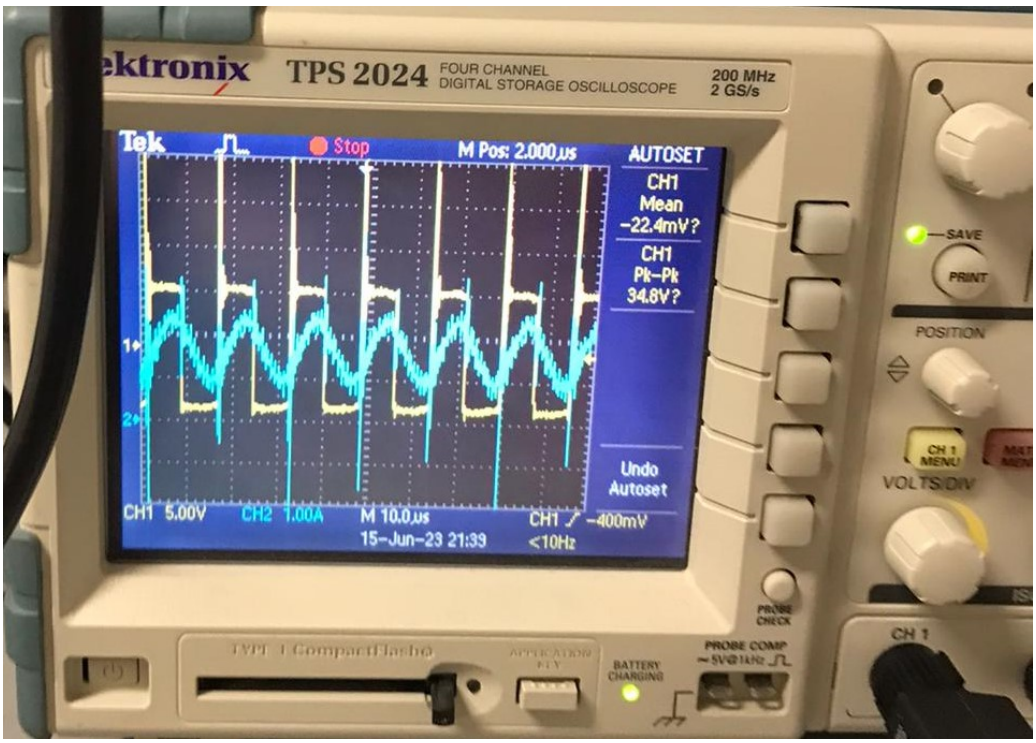

Figure 32: Open loop continuous conduction mode (CCM).

After we start to work in CCM, we closed the feedback loop via voltage output readings. We tested our converter with light and heavy load. We tested our circuit between 250Ω and 50Ω. At 250 and 125 Ω, converter reaches desired voltage in 0.5s. The efficiency is between 85-90%. When we decrease the loads resistance to 75-52Ω the converter reaches the steady state in 0.8s. Efficiency decreases to 75-80%. The reason of this response to the change in the load is increase in the drawn current. Output voltage gives more response to the change in duty cycle and it cause to increase in oscillations at transient. The efficiency decreased due to increase in conducting losses. We were expecting these efficiency decrease. As a result, the test results satisfied us.

10 Demonstration

In the demo day, we tried to put our converter in an industrial box. However, after we connected the converter our converter started to not working. We did our demonstration without box. Our converter worked very well with resistive load. The oscilloscope view is like in Figure 33.

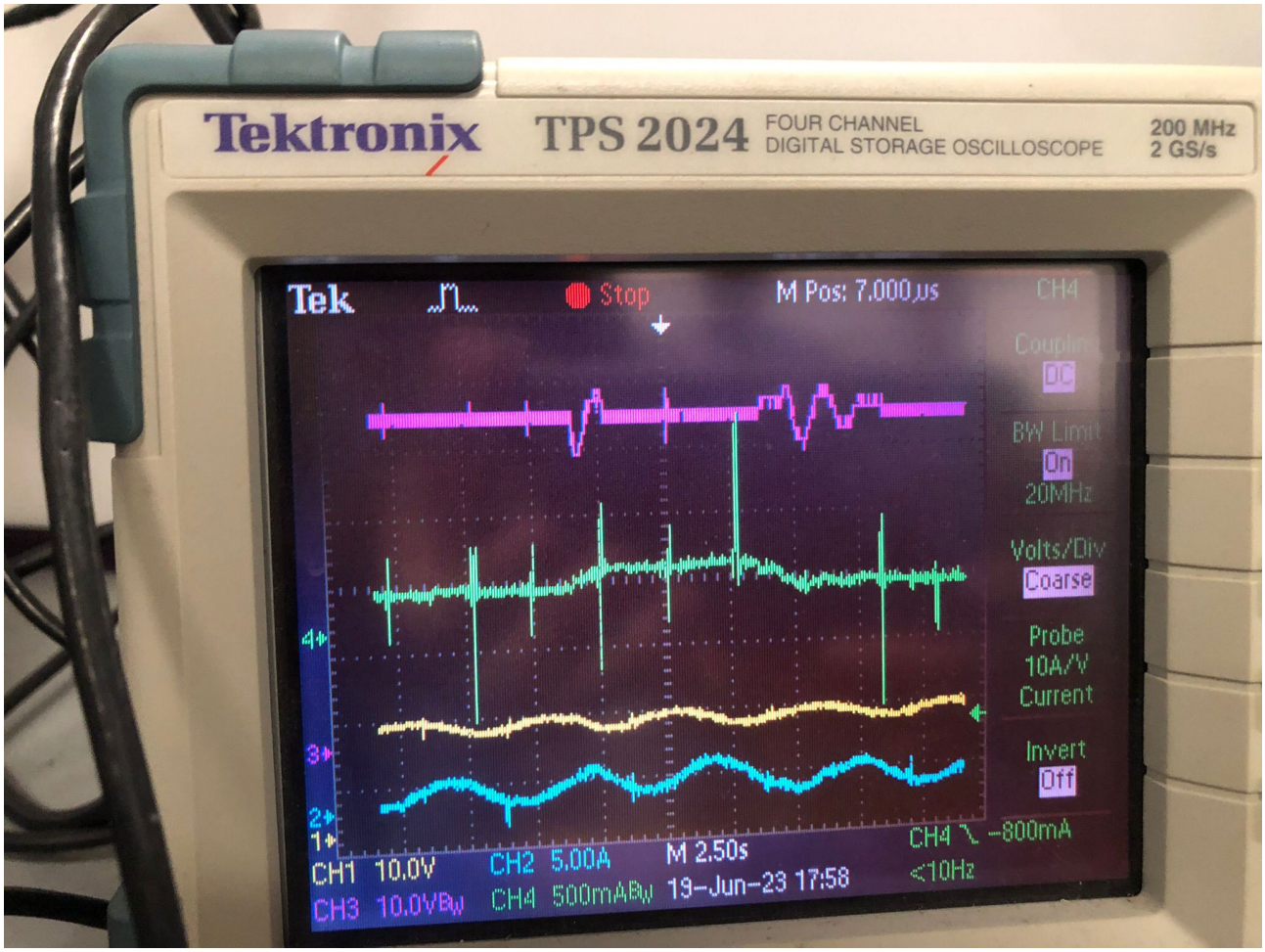

Figure 33: Oscilloscope output when resistive load is connected to converter.

The yellow line(CH1) is input voltage. Blue line(CH2) is input current. Purple line(CH3) is output voltage. Green line(CH4) is output current. Since at input side an inductor is connected the input voltage is oscillating. The oscillations at output voltage is due to change in load. The output voltage is gets in transient for a while when load changes. When we connect our converter to constant current load our converter starts to not settling to the desired 48V. We change the P and I values and get better result.

11 Conclusion

Coming to the last days of our undergraduate education, we are finishing the EE464 hardware project with this final report. It was a real-life engineering experience for us. From selecting the topology to tuning the PI control parameters of the design, we have learnt so much throughout the whole process. In this project, we designed and implemented an isolated DC-DC converter whose input voltage range is 12-18 V and output is regulated 48 V. We selected the Isolated SEPIC Converter topology with a digital controller. We performed the magnetic design of the transformer and inductor components of the converter, purchased products for switching, measurement and other components of the design, considering the safety margins all the time. Then we implemented our design on the PCB and after the open loop load tests, we moved onto the closed loop control and started regulating the output voltage. While reading the output voltage in real-time, we experienced that our voltage sensor was not linear and some calibration was needed. After meeting the requirements, we have performed the demonstration. With our professor Ozan Keysan and our assistant Ogün

Altun, we have done some fine tuning of the PI controllers. Just like the EE463 project, this project was a good opportunity for our professional careers before graduating. Thanks for everything..

Figure 34: After a successful demo procedure.

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