Isaiah Robert Grace

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Education

Purdue University Aug 2015 – Dec 2019
B.S. in Computer Engineering **Major GPA: 3.63**
Minor in History **Minor GPA: 3.93**

Relevant Coursework: Data Structures & Algorithms, Computer Architecture, Microcontrollers, Object-oriented Programming, Functional Programming, Artificial Intelligence, ASIC Design, Leadership Development

Technical Skills

C & C++	Assembly	Embedded Systems	Git	SystemVerilog	Regular expressions
Python	Bash	Linux	LaTeX	FPGA synthesis	Microsoft Office

Research and Project Experience

Independent Projects – link Mar 2020–present
Designed a cross platform IoT lighting system that dynamically responds to music attributes. Reverse-engineered a 1989 IBM keyboard and designed a custom PCB with an embedded RTOS, allowing use with modern computers. Created a Telegram Bot to notify me when the tide is low, for walks on the beach.

Senior design team: Polymorphic logic Aug–Dec 2019
Investigated the design and integration of experimental ambipolar transistors using CMOS as a proxy. Personally specified, documented, and implemented the digital control modules for custom logic cells. Integrated the team project into the larger SoCET system on a chip for fabrication at MIT Lincoln Labs.

MIPS dual-core processor – link Sep–Dec 2019
Designed, implemented, tested, and synthesized a MIPS-based processor featuring a five stage pipeline, and two cores with independent coherent L1 caches. Used SystemVerilog to implement RTL logic and testbench scripts for design validation. Synthesized design to target an Altera Cyclone FPGA.

Tetris hand-held game console – link Mar–May 2019
Developed an STM32-based handheld Tetris console as a member of a four-person team. Personally created an SPI driver for the embedded display using C++ and assembly.

ASIC module for USB to AHB bridge Nov 2018
Collaborated to design and test a USB to AHB bridge suitable for use on an SoC. Personally designed and wrote SystemVerilog code for the USB receiving/decoding submodule.

First place in ECE368: Data Structures & Algorithms "big data challenge" Oct 2017
Designed and optimized a Huffman encoding algorithm of an arbitrarily-large input using a multi-threaded approach. Applied principals of data structures and algorithms to heavily optimize C code. Placed first of 83 students for fastest compression of 64GB of data.

Work Experience

Student Researcher: Purdue SoCET team, physical design group Apr–Aug 2019
Developed layout, place and route, and floorplanning workflows using Cadence software for the SoCET system on a chip physical design.

Grader: ECE369 Discrete Mathematics Jan–May 2019
Graded Discrete Mathematics course assignments covering theory of computation, formal logic, graph theory, mathematical induction, state machines, and regular expressions.

Raft Guide: Outdoor Adventure Rafting, Ocoee River, TN May–Aug 2018

Operator: Purdue Rare Isotope Measurement Laboratory Jan 2016 – May 2018
Collected and verified data from Purdue's linear particle accelerator. Operated the accelerator during overnight shifts, participated in maintenance, and responded to emergency shutdowns.

Leadership

Whitewater Kayaking and Caving Consultant: Purdue Outing Club May 2016 – Dec 2019
Taught caving and whitewater kayaking skills from beginner through advanced levels. Organized and led expeditions. Ensured safe environment for all participants and practiced inclusive leadership within groups.

Facilitator, participant: EMV sophomore leadership retreat 2016, 2017, 2018
Participated in, and twice facilitated, a leadership retreat exploring inclusive leadership in the classroom and community.

Eagle Scout: BSA 2014