Isaiah Robert Grace

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Education

Purdue University, West Lafayette IN **GPA: 3.40**
Bachelor of Science in Computer Engineering, Minor in History Aug 2015 – Dec 2019

Relevant Coursework: Data Structures & Algorithms, Computer Architecture, Microcontrollers, Object Oriented Programming, Functional Programming, Artificial Intelligence, ASIC design

Technical Skills

C/C++	Assembly	Java	Regular Expressions	SystemVerilog	Cadence synthesis software
Python	Bash	Git	Questa-Sim	Linux	PowerPoint
LaTeX	Matlab	Scheme	FPGA Synthesis	Microsoft Office	KiCad PCB Layout

Research and Project Experience

SOCET Research Team, Senior design project Apr – Dec 2019

Coordinated the work of two teammates in creating a custom layout for two logic cells. Specified, documented, and implemented the digital logic design for an APB bus peripheral device. Integrated the team project into the larger System on a Chip for fabrication at MIT Lincoln Labs.

Design and test of MIPS dual core processor Sep – Dec 2019

Designed, tested, implemented, and synthesized a MIPS based processor design featuring a five stage pipeline, and two cores with independent coherent L1 Caches. Used SystemVerilog to implement RTL logic and testbench scripts to validate design. Synthesized design to target an Altera Cyclone FPGA.

Tetris hand-held game console Mar – May 2019

Planned and organized a team of four in developing an STM32 based handheld Tetris console. Created an SPI driver for the embedded display using embedded C++ and assembly.

ASIC Module design for USB to AHB bridge Nov 2018

Collaborated to design and test a USB interface module suitable for use on an SoC. Personally designed and wrote SystemVerilog code for the USB receiving/decoding submodule.

1st place in Data Structures – Big Data Challenge Oct 2017

Designed and optimized a Huffman encoding algorithm of an arbitrarily large input using a multi-threaded approach. Applied principals of data structures and algorithms to heavily optimize C code. Placed first of 83 students in fasted compression of 64GB of data.

Work Experience

Student Researcher: Purdue SOCET team, physical design group Jun – Aug 2019

Developed layout, place and route, and floorplanning workflows using Cadence software for the SOCET System on a Chip physical design

Grader: ECE369 Discrete Mathematics Jan – May 2019

Graded Discrete Mathematics course assignments covering theory of computation, formal logic, graph theory, mathematical induction, state machines, and regular expressions.

Raft Guide: Outdoor Adventure Rafting May – Aug 2018

Guided on class IV-V whitewater. Responsible for customer satisfaction and safety in demanding and dynamic workplace environment. Certified Wilderness First Responder.

Operator: Purdue Rare Isotope Measurement Laboratory Jan 2016 – May 2018

Collected and verified data from Purdue's linear particle accelerator. Operated the accelerator during overnight shifts and responded to emergency shutdowns due to sparking in the accelerator chamber.

Leadership

Whitewater Kayaking and Caving Consultant: Purdue Outing Club May 2016 – Dec 2019

Lead and organized caving and whitewater kayaking trips. Ensured safe environment for all participants and practiced inclusive leadership within groups.

Facilitator, participant: EMV sophomore leadership retreat 2016, 2017, 2018

Participated in, and twice facilitated, a leadership retreat exploring inclusive leadership in the classroom and workplace.

Eagle Scout: BSA 2014