Isaiah Grace

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Education

Purdue University Aug 2015 – Dec 2019
B.S. in Computer Engineering **Major GPA: 3.63**
Minor in History **Minor GPA: 3.93**

Relevant Coursework: Digital Signal Processing Data Structures & Algorithms, Computer Architecture, Microcontrollers, Object-oriented Programming, Functional Programming, Artificial Intelligence, ASIC Design, Leadership Development

Technical Skills

C & C++	Assembly	Embedded Systems	Git	Regular expressions	Rust
Python	AWS IoT	Linux	Zig	FPGA design & synthesis	Circuit design

Work Experience

Embedded Software Developer: ASML via Actalent Services Jul 2022–Present

Responsible for the implementation of high reliability and high performance C driver firmware, enabling next-gen semiconductor manufacturing. Designed, developed, and tested modular driver and subsystem components in a highly distributed and real-time environment.

Embedded Systems Engineer: Sestra Systems May 2021–Jun 2022

Responsible for the design and implementation of IoT embedded systems. Architected and implemented new subsystems in a multi-threaded and multi-process distributed system. Designed hardware drivers on extremely resource constrained bare-metal microcontroller boards. Reverse-engineered a BLE Bluetooth protocol to develop a custom driver and control system for off the shelf hardware. Integrated open source device drivers utilizing C and modern C++.

Student Researcher: Purdue SoCET team, physical design group Apr–Aug 2019

Developed layout, place and route, and floorplanning workflows for the physical design of an experimental research microcontroller eventually fabricated at MIT Lincoln Labs.

Grader: ECE369 Discrete Mathematics Jan–May 2019

Graded Discrete Mathematics course assignments covering theory of computation, formal logic, graph theory, mathematical induction, state machines, and regular expressions.

Operator: Purdue Rare Isotope Measurement Laboratory Jan 2016 – May 2018

Collected and verified data from Purdue's linear particle accelerator. Operated the accelerator during overnight shifts, participated in maintenance, and responded to emergency shutdowns.

Research and Project Experience

Senior design team: Polymorphic logic Aug–Dec 2019

Investigated the design and integration of experimental ambipolar transistors using CMOS as a proxy. Personally specified, documented, and implemented the digital control modules for custom logic cells. Integrated the team project into the larger SoCET system on a chip for fabrication at MIT Lincoln Labs.

Tetris hand-held game console – link Mar–May 2019

Developed an STM32-based handheld Tetris console as a member of a four-person team. Personally created an SPI driver for the embedded display using C++ and assembly.

MIPS dual-core processor – link Sep–Dec 2019

Designed, implemented, tested, and synthesized a MIPS-based processor featuring a five stage pipeline, and two cores with independent coherent L1 caches. Used SystemVerilog to implement RTL logic and testbench scripts for design validation. Synthesized design to target an Altera Cyclone FPGA.

First place in ECE368: Data Structures & Algorithms "big data challenge" Oct 2017

Designed and optimized a Huffman encoding algorithm of an arbitrarily-large input using a multi-threaded approach. Applied principals of data structures and algorithms to heavily optimize C code. Placed first of 83 students for fastest compression of 64GB of data.

Leadership

Whitewater Kayaking and Caving Consultant: Purdue Outing Club May 2016 – Dec 2019
Facilitator: E.M. Vogel Sophomore Leadership Retreat 2016, 2017, 2018
Eagle Scout: BSA 2014