

SSD202D PADTOP Module Description







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1. REGISTER DESCRIPTION

1.1. PADTOP Register (Bank = 103C)

PADTOP Re	gister (Bank = 103C)			
Index (Absolute)	Mnemonic	Bit	Description	
00h	REG103C00	7:0	Default: 0x20	Access: RO, R/W
(103C00h)	-	7:6	Reserved.	117
	GPIO_OEN_0	5		
	GPIO_OUT_0	4		XT.
	-	3:1	Reserved.	27
	GPIO_IN_0	0		
01h (103C02h)	REG103C02	7:0	Default : 0x20	Access: RO, R/W
	-	7:6	Reserved.	
	GPIO_OEN_1	5	(=X')	
	GPIO_OUT_1	4	14	
		3:1	Reserved.	
	GPIO_IN_1	0		T
02h	REG103C04	7:0	Default : 0x20	Access: RO, R/W
(103C04h)	-	7:6	Reserved.	
	GPIO_OEN_2	5		
	GPIO_OUT_2	4		
	-	3:1	Reserved.	
	GPIO_IN_2	0		T
03h	REG103C06	7:0	Default: 0x20	Access: RO, R/W
(103C06h)	- \ \ \ /	7:6	Reserved.	
	GPIO_OEN_3	5		
	GPIO_OUT_3	4		
	-	3:1	Reserved.	
	GPIO_IN_3	0		T
04h	REG103C08	7:0	Default: 0x20	Access: RO, R/W
(103C08h)	-	7:6	Reserved.	
	GPIO_OEN_4	5		



PADTOP Re	gister (Bank = 103C)		
Index (Absolute)	Mnemonic	Bit	Description
	GPIO_OUT_4	4	
	-	3:1	Reserved.
	GPIO_IN_4	0	• •
05h	REG103C0A	7:0	Default: 0x20 Access: RO, R/W
(103C0Ah)	-	7:6	Reserved.
	GPIO_OEN_5	5	
	GPIO_OUT_5	4	
	-	3:1	Reserved.
	GPIO_IN_5	0	
06h	REG103C0C	7:0	Default: 0x20 Access: RO, R/W
(103C0Ch)	-	7:6	Reserved.
	GPIO_OEN_6	5	
	GPIO_OUT_6	4	X Y
	- XX.O.	3:1	Reserved.
	GPIO_IN_6	0	
07h	REG103C0E	7:0	Default: 0x20 Access: RO, R/W
(103C0Eh)		7:6	Reserved.
	GPIO_OEN_7	5	
	GPIO_OUT_7	4	
	-	3:1	Reserved.
	GPIO_IN_7	0	
08h	REG103C10	7:0	Default: 0x20 Access: RO, R/W
(103C10h)	- [-]]	7:6	Reserved.
	GPIO_OEN_8	5	
	GPIO_OUT_8	4	
	- //	3:1	Reserved.
	GPIO_IN_8	0	
09h	REG103C12	7:0	Default: 0x20 Access: RO, R/W
(103C12h)	-	7:6	Reserved.
	GPIO_OEN_9	5	
	GPIO_OUT_9	4	
	-	3:1	Reserved.
	GPIO_IN_9	0	



PADTOP Reg	gister (Bank = 103C)			
Index (Absolute)	Mnemonic	Bit	Description	
OAh	REG103C14	7:0	Default: 0x20	Access: RO, R/W
(103C14h)	-	7:6	Reserved.	
	GPIO_OEN_10	5	• • •	
	GPIO_OUT_10	4	XIO	
	-	3:1	Reserved.	
	GPIO_IN_10	0	10)	//-
OBh	REG103C16	7:0	Default: 0x20	Access: RO, R/W
(103C16h)	-	7:6	Reserved.	
	GPIO_OEN_11	5		7 17
	GPIO_OUT_11	4	X	VI.
	-	3:1	Reserved.	2/0
	GPIO_IN_11	0	· X/>	
OCh	REG103C18	7:0	Default : 0x20	Access: RO, R/W
(103C18h)	- XYO	7:6	Reserved.	
	GPIO_OEN_12	5		
	GPIO_OUT_12	4	·X	
		3:1	Reserved.	
	GPIO_IN_12	0		
0Dh	REG103C1A	7:0	Default: 0x20	Access: RO, R/W
(103C1Ah)	-	7:6	Reserved.	1
	GPIO_OEN_13	5		
	GPIO_OUT_13	4		
	- [,	3:1	Reserved.	
	GPIO_IN_13	0		
0Eh	REG103C1C	7:0	Default: 0x20	Access: RO, R/W
(103C1Ch)	-	7:6	Reserved.	
	GPIO_OEN_14	5		
	GPIO_OUT_14	4		
	-	3:1	Reserved.	
	GPIO_IN_14	0		
14h	REG103C28	7:0	Default: 0x20	Access: RO, R/W
(103C28h)	-	7:6	Reserved.	
	FUART_GPIO_OEN_0	5		



PADTOP Re	gister (Bank = 103C)		
Index (Absolute)	Mnemonic	Bit	Description
	FUART_GPIO_OUT_0	4	
	-	3:1	Reserved.
	FUART_GPIO_IN_0	0	
15h	REG103C2A	7:0	Default: 0x20 Access: RO, R/W
(103C2Ah)	-	7:6	Reserved.
	FUART_GPIO_OEN_1	5	
	FUART_GPIO_OUT_1	4	
	-	3:1	Reserved.
	FUART_GPIO_IN_1	0	
16h	REG103C2C	7:0	Default: 0x20 Access: RO, R/W
(103C2Ch)	-	7:6	Reserved.
	FUART_GPIO_OEN_2	5	
	FUART_GPIO_OUT_2	4	X. Y.
	- XXO	3:1	Reserved.
	FUART_GPIO_IN_2	0	
17h	REG103C2E	7:0	Default: 0x20 Access: RO, R/W
(103C2Eh)		7:6	Reserved.
	FUART_GPIO_OEN_3	5	
~ '\C	FUART_GPIO_OUT_3	4	
5	-	3:1	Reserved.
	FUART_GPIO_IN_3	0	
18h	REG103C30	7:0	Default: 0x20 Access: RO, R/W
(103C30h)	- 1-	7:6	Reserved.
	UARTO_GPIO_OEN_0	5	
	UARTO_GPIO_OUT_0	4	
	-	3:1	Reserved.
	UARTO_GPIO_IN_0	0	
19h	REG103C32	7:0	Default: 0x20 Access: RO, R/W
(103C32h)	-	7:6	Reserved.
	UARTO_GPIO_OEN_1	5	
	UARTO_GPIO_OUT_1	4	
	-	3:1	Reserved.
	UARTO_GPIO_IN_1	0	



PADTOP Reg	gister (Bank = 103C)			
Index (Absolute)	Mnemonic	Bit	Description	
1Ah	REG103C34	7:0	Default: 0x20	Access: RO, R/W
(103C34h)	-	7:6	Reserved.	
	UART1_GPIO_OEN_0	5	• • •	
	UART1_GPIO_OUT_0	4	X/O	
	-	3:1	Reserved.	
	UART1_GPIO_IN_0	0		//-
1Bh	REG103C36	7:0	Default: 0x20	Access : RO, R/W
(103C36h)	-	7:6	Reserved.	
	UART1_GPIO_OEN_1	5		7 17
	UART1_GPIO_OUT_1	4	1	VI.
	-	3:1	Reserved.	2/0
	UART1_GPIO_IN_1	0		
20h	REG103C40	7:0	Default : 0x20	Access: RO, R/W
(103C40h)	- X O	7:6	Reserved.	
	TTL_GPIO_OEN_0	5		
	TTL_GPIO_OUT_0	4	·X	
		3:1	Reserved.	
	TTL_GPIO_IN_0	0		
21h	REG103C42	7:0	Default: 0x20	Access: RO, R/W
(103C42h)	-	7:6	Reserved.	1
	TTL_GPIO_OEN_1	5		
	TTL_GPIO_OUT_1	4		
	- (,	3:1	Reserved.	
	TTL_GPIO_IN_1	0		
22h	REG103C44	7:0	Default: 0x20	Access: RO, R/W
(103C44h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_2	5		
	TTL_GPIO_OUT_2	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_2	0		
23h	REG103C46	7:0	Default: 0x20	Access: RO, R/W
(103C46h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_3	5		



PADTOP Reg	gister (Bank = 103C)		
Index (Absolute)	Mnemonic	Bit	Description
	TTL_GPIO_OUT_3	4	
	=	3:1	Reserved.
	TTL_GPIO_IN_3	0	
24h	REG103C48	7:0	Default: 0x20 Access: RO, R/W
(103C48h)	=	7:6	Reserved.
	TTL_GPIO_OEN_4	5	
	TTL_GPIO_OUT_4	4	
	-	3:1	Reserved.
	TTL_GPIO_IN_4	0	
25h	REG103C4A	7:0	Default: 0x20 Access: RO, R/W
(103C4Ah)	-	7:6	Reserved.
	TTL_GPIO_OEN_5	5	
	TTL_GPIO_OUT_5	4	
	- X O	3:1	Reserved.
	TTL_GPIO_IN_5	0	
26h	REG103C4C	7:0	Default: 0x20 Access: RO, R/W
(103C4Ch)		7:6	Reserved.
	TTL_GPIO_OEN_6	5	F13 . O
	TTL_GPIO_OUT_6	4	
6	-	3:1	Reserved.
	TTL_GPIO_IN_6	0	
27h	REG103C4E	7:0	Default: 0x20 Access: RO, R/W
(103C4Eh)	-	7:6	Reserved.
	TTL_GPIO_OEN_7	5	
	TTL_GPIO_OUT_7	4	
	-	3:1	Reserved.
	TTL_GPIO_IN_7	0	
28h	REG103C50	7:0	Default: 0x20 Access: RO, R/W
(103C50h)	-	7:6	Reserved.
	TTL_GPIO_OEN_8	5	
	TTL_GPIO_OUT_8	4	
	-	3:1	Reserved.
	TTL_GPIO_IN_8	0	



PADTOP Re	gister (Bank = 103C)			
Index (Absolute)	Mnemonic	Bit	Description	
29h	REG103C52	7:0	Default: 0x20	Access: RO, R/W
(103C52h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_9	5	•.0	
	TTL_GPIO_OUT_9	4	X/O	
	-	3:1	Reserved.	
	TTL_GPIO_IN_9	0		//-
2Ah	REG103C54	7:0	Default: 0x20	Access: RO, R/W
(103C54h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_10	5		A 117
	TTL_GPIO_OUT_10	4	1	VI
	-	3:1	Reserved.	7/0
	TTL_GPIO_IN_10	0		
2Bh	REG103C56	7:0	Default : 0x20	Access: RO, R/W
(103C56h)	- XXO	7:6	Reserved.	
	TTL_GPIO_OEN_11	5		
	TTL_GPIO_OUT_11	4	X	
		3:1	Reserved.	
	TTL_GPIO_IN_11	0		
2Ch	REG103C58	7:0	Default: 0x20	Access: RO, R/W
(103C58h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_12	5		
	TTL_GPIO_OUT_12	4		
	- [-]]	3:1	Reserved.	
	TTL_GPIO_IN_12	0		
2Dh	REG103C5A	7:0	Default: 0x20	Access: RO, R/W
(103C5Ah)	-	7:6	Reserved.	
	TTL_GPIO_OEN_13	5		
	TTL_GPIO_OUT_13	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_13	0		
2Eh	REG103C5C	7:0	Default: 0x20	Access: RO, R/W
(103C5Ch)	-	7:6	Reserved.	
	TTL_GPIO_OEN_14	5		



PADTOP Re	gister (Bank = 103C)			
Index (Absolute)	Mnemonic	Bit	Description	
	TTL_GPIO_OUT_14	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_14	0		
2Fh	REG103C5E	7:0	Default : 0x20 Acc	cess : RO, R/W
(103C5Eh)	-	7:6	Reserved.	
	TTL_GPIO_OEN_15	5	10)	/
	TTL_GPIO_OUT_15	4	**	(())
	-	3:1	Reserved.	~
	TTL_GPIO_IN_15	0	\ \ \	
30h	REG103C60	7:0	Default : 0x20 Acc	cess: RO, R/W
(103C60h)	-	7:6	Reserved.	V \
	TTL_GPIO_OEN_16	5		
	TTL_GPIO_OUT_16	4	X X	
	- XO	3:1	Reserved.	
	TTL_GPIO_IN_16	0		
31h	REG103C62	7:0	Default: 0x20 Acc	cess: RO, R/W
(103C62h)		7:6	Reserved.	
	TTL_GPIO_OEN_17	5		
	TTL_GPIO_OUT_17	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_17	0		
32h	REG103C64	7:0	Default: 0x20 Acc	cess : RO, R/W
(103C64h)	- [////	7:6	Reserved.	
	TTL_GPIO_OEN_18	5		
	TTL_GPIO_OUT_18	4		
	- \/	3:1	Reserved.	
	TTL_GPIO_IN_18	0		
33h	REG103C66	7:0	Default : 0x20 Acc	cess : RO, R/W
(103C66h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_19	5		
	TTL_GPIO_OUT_19	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_19	0		



PADTOP Reg	gister (Bank = 103C)			
Index (Absolute)	Mnemonic	Bit	Description	
34h	REG103C68	7:0	Default: 0x20	Access: RO, R/W
(103C68h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_20	5	• • •	
	TTL_GPIO_OUT_20	4	X/O	
	-	3:1	Reserved.	
	TTL_GPIO_IN_20	0		//-
35h	REG103C6A	7:0	Default: 0x20	Access : RO, R/W
(103C6Ah)	-	7:6	Reserved.	
	TTL_GPIO_OEN_21	5		7 17
	TTL_GPIO_OUT_21	4	1	VI.
	-	3:1	Reserved.	1.1
	TTL_GPIO_IN_21	0	· X/>	
36h	REG103C6C	7:0	Default : 0x20	Access: RO, R/W
(103C6Ch)	- X O	7:6	Reserved.	
	TTL_GPIO_OEN_22	5		
	TTL_GPIO_OUT_22	4	·X	
		3:1	Reserved.	
	TTL_GPIO_IN_22	0		
37h	REG103C6E	7:0	Default: 0x20	Access: RO, R/W
(103C6Eh)	-	7:6	Reserved.	
	TTL_GPIO_OEN_23	5		
	TTL_GPIO_OUT_23	4		
	- (,)	3:1	Reserved.	
	TTL_GPIO_IN_23	0		
38h	REG103C70	7:0	Default: 0x20	Access: RO, R/W
(103C70h)	-	7:6	Reserved.	
	TTL_GPIO_OEN_24	5		
	TTL_GPIO_OUT_24	4		
	-	3:1	Reserved.	
	TTL_GPIO_IN_24	0		
39h	REG103C72	7:0	Default: 0x20	Access: RO, R/W
(103C72h)	-	7:6	Reserved.	
,	TTL_GPIO_OEN_25	5		



gister (Bank = 103C)		
Mnemonic	Bit	Description
TTL_GPIO_OUT_25	4	
-	3:1	Reserved.
TTL_GPIO_IN_25	0	. (1)
REG103C74	7:0	Default: 0x20 Access: RO, R/W
-	7:6	Reserved.
TTL_GPIO_OEN_26	5	//-
TTL_GPIO_OUT_26	4	4())
-	3:1	Reserved.
TTL_GPIO_IN_26	0	4 17
REG103C76	7:0	Default: 0x20 Access: RO, R/W
-		Reserved.
TTL GPIO OEN 27		
		V. Y.
- XO		Reserved.
TTL_GPIO_IN_27	0	
REG103C80	7:0	Default: 0x20 Access: RO, R/W
	7:6/	Reserved.
IDAC_GPIO_OEN_0	5	
-	4	
	3:1	Reserved.
IDAC GPIO IN 0	0	
		Default: 0x20 Access: RO, R/W
- ()		Reserved.
IDAC GPIO OEN 1		
-		Reserved.
IDAC GPIO IN 1		
		Default: 0x20 Access: RO, R/W
-		Reserved.
HDMI GPIO OEN 0		
	4	
HUMI GPIO OUT O	4	
HDMI_GPIO_OUT_0	3:1	Reserved.
	Mnemonic TTL_GPIO_OUT_25 - TTL_GPIO_IN_25 REG103C74 - TTL_GPIO_OEN_26 TTL_GPIO_OUT_26 - TTL_GPIO_IN_26 REG103C76 - TTL_GPIO_OEN_27 TTL_GPIO_OUT_27 - TTL_GPIO_OUT_27 - TTL_GPIO_IN_27	Mnemonic Bit TTL_GPIO_OUT_25 4 - 3:1 TTL_GPIO_IN_25 0 REG103C74 7:0 - 7:6 TTL_GPIO_OEN_26 5 TTL_GPIO_OUT_26 4 - 3:1 TTL_GPIO_IN_26 0 REG103C76 7:0 - 7:6 TTL_GPIO_OEN_27 5 TTL_GPIO_OUT_27 4 - 3:1 TTL_GPIO_IN_27 0 REG103C80 7:0 - 7:6 IDAC_GPIO_OEN_0 5 IDAC_GPIO_OUT_0 4 - 7:6 IDAC_GPIO_OEN_1 5 IDAC_GPIO_OEN_1 5 IDAC_GPIO_OUT_1 4 - 3:1 IDAC_GPIO_IN_1 0 REG103C84 7:0 - 7:6



PADTOP Re	gister (Bank = 103C)			
Index (Absolute)	Mnemonic	Bit	Description	
43h	REG103C86	7:0	Default: 0x20	Access : RO, R/W
(103C86h)	-	7:6	Reserved.	
	HDMI_GPIO_OEN_1	5	•.0	
	HDMI_GPIO_OUT_1	4	XIO	
	-	3:1	Reserved.	
	HDMI_GPIO_IN_1	0	10)	/_
44h	REG103C88	7:0	Default: 0x20	Access: RO, R/W
(103C88h)	-	7:6	Reserved.	
	HDMI_GPIO_OEN_2	5		117
	HDMI_GPIO_OUT_2	4	X	VI_V
	-	3:1	Reserved.	2/
	HDMI_GPIO_IN_2	0	\ \/\\	
50h	REG103CA0	7:0	Default: 0x20	Access: RO, R/W
(103CA0h)	- XYO	7:6	Reserved.	
	SD_GPIO_OEN_0	5		
	SD_GPIO_OUT_0	4	·XIX	
		3:1	Reserved.	
	SD_GPIO_IN_0	0-		
51h	REG103CA2	7:0	Default: 0x20	Access: RO, R/W
(103CA2h)	-	7:6	Reserved.	1
	SD_GPIO_OEN_1	5		
	SD_GPIO_OUT_1	4		
	- (////	3:1	Reserved.	
	SD_GPIO_IN_1	0		
52h	REG103CA4	7:0	Default: 0x20	Access: RO, R/W
(103CA4h)	-	7:6	Reserved.	
	SD_GPIO_OEN_2	5		
	SD_GPIO_OUT_2	4		
	-	3:1	Reserved.	
	SD_GPIO_IN_2	0		
53h	REG103CA6	7:0	Default: 0x20	Access: RO, R/W
(103CA6h)	-	7:6	Reserved.	<u>'</u>
	SD_GPIO_OEN_3	5		



PADTOP Re	gister (Bank = 103C)	r	
Index (Absolute)	Mnemonic	Bit	Description
	SD_GPIO_OUT_3	4	
	-	3:1	Reserved.
	SD_GPIO_IN_3	0	• • • • • • • • • • • • • • • • • • • •
54h	REG103CA8	7:0	Default: 0x20 Access: RO, R/W
(103CA8h)	-	7:6	Reserved.
	SD_GPIO_OEN_4	5	
	SD_GPIO_OUT_4	4	///>
	-	3:1	Reserved.
	SD_GPIO_IN_4	0	
55h	REG103CAA	7:0	Default: 0x20 Access: RO, R/W
(103CAAh)	-	7:6	Reserved.
	SD_GPIO_OEN_5	5	
	SD_GPIO_OUT_5	4	Y. Y.
	- X O	3:1	Reserved.
	SD_GPIO_IN_5	0	
56h	REG103CAC	7:0	Default: 0x20 Access: RO, R/W
(103CACh)		7:6	Reserved.
	SD_GPIO_OEN_6	5	-1 · . · ·
	SD_GPIO_OUT_6	4	
6)	-	3:1	Reserved.
	SD_GPIO_IN_6	0	