

SSD202D GPI_INT Module Description







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1. REGISTER DESCRIPTION

1.1. GPI_INT Register (Bank = 103D)

GPI_INT Register (Bank = 103D)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (103D00h)	REG103D00	7:0	Default : 0xFF	Access : R/W
	FIQ_MASK_0[7:0]	7:0	Fiq mask enable.	
00h	REG103D01	7:0	Default : 0xFF	Access : R/W
(103D01h)	FIQ_MASK_0[15:8]	7:0	See description of '103D00h'	XT.
01h	REG103D02	7:0	Default : 0xFF	Access : R/W
(103D02h)	FIQ_MASK_1[7:0]	7:0	Fig mask enable.	
01h	REG103D03	7:0	Default : 0xFF	Access: R/W
(103D03h)	FIQ_MASK_1[15:8]	7:0	See description of '103D02h'.	
02h	REG103D04	7:0	Default: 0xFF	Access : R/W
(103D04h)	FIQ_MASK_2[7:0]	7:0	Fiq mask enable.	
02h	REG103D05	7:0	Default : 0xFF	Access : R/W
(103D05h)	FIQ_MASK_2[15:8]	7:0	See description of '103D04h'.	
03h	REG103D06	7:0	Default: 0xFF	Access : R/W
(103D06h)	FIQ_MASK_3[7:0]	7:0	Fiq mask enable.	
03h	REG103D07	7:0	Default: 0xFF	Access : R/W
(103D07h)	FIQ_MASK_3[15:8]	7:0	See description of '103D06h'	
04h	REG103D08	7:0	Default : 0xFF	Access : R/W
(103D08h)	FIQ_MASK_4[7:0]	7:0	Fiq mask enable.	
04h	REG103D09	7:0	Default: 0x0F	Access : R/W
(103D09h)	- \ /	7:4	Reserved.	
	FIQ_MASK_4[11: 8]	3:0	See description of '103D08h'.	
05h	REG103D0A	7:0	Default: 0x00	Access : R/W
(103D0Ah)	FIQ_FORCE[7:0]	7:0	Fiq force enable.	<u>, </u>
05h	REG103D0B	7:0	Default: 0x00	Access : R/W
(103D0Bh)	FIQ_FORCE[15:8]	7:0	See description of '103D0Ah'.	
06h (103D0Ch)	REG103D0C	7:0	Default: 0x00	Access : R/W
	FIQ_FORCE[23:16]	7:0	See description of '103D0Ah'.	



GPI_INT Re	egister (Bank = 103D)			
Index (Absolute)	Mnemonic	Bit	Description	
06h (103D0Dh)	REG103D0D	7:0	Default: 0x00	Access : R/W
	FIQ_FORCE[31:24]	7:0	See description of '103D0Ah'	
07h (103D0Eh)	REG103D0E	7:0	Default: 0x00	Access : R/W
	FIQ_FORCE[39: 32]	7:0	See description of '103D0Ah'	
07h	REG103D0F	7:0	Default: 0x00	Access : R/W
(103D0Fh)	FIQ_FORCE[47:40]	7:0	See description of '103D0Ah'	. /
08h	REG103D10	7:0	Default: 0x00	Access : R/W
(103D10h)	FIQ_FORCE[55:48]	7:0	See description of '103D0Ah'	
08h	REG103D11	7:0	Default: 0x00	Access : R/W
(103D11h)	FIQ_FORCE[63: 56]	7:0	See description of '103D0Ah'	VI.
09h	REG103D12	7:0	Default: 0x00	Access : R/W
(103D12h)	FIQ_FORCE[71: 64]	7:0	See description of '103D0Ah'	
09h (103D13h)	REG103D13	7:0	Default : 0x00	Access : R/W
	- XO	7:4	Reserved.	
	FIQ_FORCE[75: 72]	3:0	See description of '103D0Ah'	
OAh	REG103D14	7:0	Default: 0x00	Access : WO
(103D14h)	FIQ_CLR[7:0]	7:0	Fiq clear.	
0Ah	REG103D15	7:0	Default: 0x00	Access : WO
(103D15h)	FIQ_CLR[15:8]	7:0	See description of '103D14h'	
0Bh	REG103D16	7:0	Default: 0x00	Access : WO
(103D16h)	FIQ_CLR[23:16]	7:0	See description of '103D14h'	
0Bh	REG103D17	7:0	Default: 0x00	Access : WO
(103D17h)	FIQ_CLR[31:24]	7:0	See description of '103D14h'	·
0Ch	REG103D18	7:0	Default: 0x00	Access : WO
(103D18h)	FIQ_CLR[39: 32]	7:0	See description of '103D14h'	·
0Ch	REG103D19	7:0	Default: 0x00	Access : WO
(103D19h)	FIQ_CLR[47:40]	7:0	See description of '103D14h'	·
0Dh	REG103D1A	7:0	Default: 0x00	Access : WO
(103D1Ah)	FIQ_CLR[55:48]	7:0	See description of '103D14h'	
0Dh (103D1Bh)	REG103D1B	7:0	Default: 0x00	Access : WO
	FIQ_CLR[63: 56]	7:0	See description of '103D14h'	
0Eh (103D1Ch)	REG103D1C	7:0	Default: 0x00	Access: WO
	FIQ_CLR[71: 64]	7:0	See description of '103D14h'	



GPI_INT Re	gister (Bank = 103D)			
Index (Absolute)	Mnemonic	Bit	Description	
0Eh (103D1Dh)	REG103D1D	7:0	Default: 0x00	Access : WO
	-	7:4	Reserved.	
	FIQ_CLR[75: 72]	3:0	See description of '103D14h'	
10h (103D20h)	REG103D20	7:0	Default : 0x00	Access : R/W
	FIQ_POL[7:0]	7:0	Fig polarity.	
10h	REG103D21	7:0	Default: 0x00	Access : R/W
(103D21h)	FIQ_POL[15:8]	7:0	See description of '103D20h'	
11h	REG103D22	7:0	Default: 0x00	Access : R/W
(103D22h)	FIQ_POL[23:16]	7:0	See description of '103D20h'	A 117
11h (103D23h)	REG103D23	7:0	Default: 0x00	Access : R/W
	FIQ_POL[31:24]	7:0	See description of '103D20h'	
12h (103D24h)	REG103D24	7:0	Default: 0x00	Access: R/W
	FIQ_POL[39: 32]	7:0	See description of '103D20h'	
12h	REG103D25	7:0	Default: 0x00	Access: R/W
(103D25h)	FIQ_POL[47:40]	7:0	See description of '103D20h'.	
13h	REG103D26	7:0	Default : 0x00	Access : R/W
(103D26h)	FIQ_POL[55:48]	7:0	See description of '103D20h'	
13h	REG103D27	7:0	Default: 0x00	Access : R/W
(103D27h)	FIQ_POL[63: 56]	7:0	See description of '103D20h'	
14h	REG103D28	7:0	Default: 0x00	Access : R/W
(103D28h)	FIQ_POL[71: 64]	7:0	See description of '103D20h'	
14h	REG103D29	7:0	Default: 0x00	Access : R/W
(103D29h)	- [-	7:4	Reserved.	
	FIQ_POL[75: 72]	3:0	See description of '103D20h'	
15h	REG103D2A	7:0	Default : 0x00	Access : R/W
(103D2Ah)	- //	7:1	Reserved.	
	FIQ_RAW_SEL	0	Fiq raw status select.	<u>, </u>
20h	REG103D40	7:0	Default : 0xFF	Access : R/W
(103D40h)	IRQ_MASK[7:0]	7:0	Irq mask enable.	
21h	REG103D42	7:0	Default : 0xFF	Access : R/W
(103D42h)	IRQ_FORCE[7:0]	7:0	Irq force enable.	
22h (103D44h)	REG103D44	7:0	Default : 0xFF	Access : R/W
	IRQ_POL[7:0]	7:0	Irq polarity.	



GPI_INT Register (Bank = 103D)					
Index (Absolute)	Mnemonic	Bit	Description		
30h	REG103D60	7:0	Default: 0x00	Access : RO	
(103D60h)	FIQ_FINAL_STATUS[7:0]	7:0	FIQ_FINAL_STATUS.		
30h (103D61h)	REG103D61	7:0	Default: 0x00	Access: RO	
	FIQ_FINAL_STATUS[15:8]	7:0	See description of '103D60h'.		
31h	REG103D62	7:0	Default: 0x00	Access : RO	
(103D62h)	FIQ_FINAL_STATUS[23:16]	7:0	See description of '103D60h'.	7-	
31h	REG103D63	7:0	Default: 0x00	Access : RO	
(103D63h)	FIQ_FINAL_STATUS[31:24]	7:0	See description of '103D60h'.		
32h	REG103D64	7:0	Default: 0x00	Access : RO	
(103D64h)	FIQ_FINAL_STATUS[39: 32]	7:0	See description of '103D60h'.		
32h (103D65h)	REG103D65	7:0	Default: 0x00	Access: RO	
	FIQ_FINAL_STATUS[47:40]	7:0	See description of '103D60h'.		
33h	REG103D66	7:0	Default: 0x00	Access: RO	
(103D66h)	FIQ_FINAL_STATUS[55:48]	7:0	See description of '103D60h'.		
33h	REG103D67	7:0	Default: 0x00	Access: RO	
(103D67h)	FIQ_FINAL_STATUS[63: 56]	7:0	See description of '103D60h'.		
34h	REG103D68	7:0	Default: 0x00	Access : RO	
(103D68h)	FIQ_FINAL_STATUS[71: 64]	7:0	See description of '103D60h'.		
34h	REG103D69	7:0	Default: 0x00	Access : RO	
(103D69h)	-	7:4	Reserved.		
	FIQ_FINAL_STATUS[75: 72]	3:0	See description of '103D60h'.		
35h	REG103D6A	7:0	Default: 0x00	Access : RO	
(103D6Ah)	FIQ_RAW_STATUS[7:0]	7:0	FIQ_RAW_STATUS.		
35h	REG103D6B	7:0	Default: 0x00	Access : RO	
(103D6Bh)	FIQ_RAW_STATUS[15:8]	7:0	See description of '103D6Ah'.		
36h	REG103D6C	7:0	Default: 0x00	Access: RO	
(103D6Ch)	FIQ_RAW_STATUS[23:16]	7:0	See description of '103D6Ah'.		
36h	REG103D6D	7:0	Default: 0x00	Access : RO	
(103D6Dh)	FIQ_RAW_STATUS[31:24]	7:0	See description of '103D6Ah'.		
37h	REG103D6E	7:0	Default: 0x00	Access : RO	



GPI_INT Register (Bank = 103D)				
Index (Absolute)	Mnemonic	Bit	Description	
(103D6Eh)	FIQ_RAW_STATUS[39: 32]	7:0	See description of '103D6Ah'.	
37h (103D6Fh)	REG103D6F	7:0	Default: 0x00	Access : RO
	FIQ_RAW_STATUS[47:40]	7:0	See description of '103D6Ah'	
38h (103D70h)	REG103D70	7:0	Default: 0x00	Access : RO
	FIQ_RAW_STATUS[55:48]	7:0	See description of '103D6Ah'	
38h	REG103D71	7:0	Default: 0x00	Access : RO
(103D71h)	FIQ_RAW_STATUS[63: 56]	7:0	See description of '103D6Ah'	
39h	REG103D72	7:0	Default: 0x00	Access : RO
(103D72h)	FIQ_RAW_STATUS[71: 64]	7:0	See description of '103D6Ah'	
39h	REG103D73	7:0	Default: 0x00	Access : RO
(103D73h)	-	7:4	Reserved.	
	FIQ_RAW_STATUS[75: 72]	3:0	See description of '103D6Ah'	
3Ah	REG103D74	7:0	Default: 0x00	Access: RO
(103D74h)	IRQ_FINAL_STATUS[7:0]	7:0	IRQ_FINAL_STATUS.	
3Bh	REG103D76	7:0	Default: 0x00	Access : RO
(103D76h)	IRQ_RAW_STATUS[7:0]	7:0	IRQ_RAW_STATUS.	
40h	REG103D80	7:0	Default: 0x00	Access : R/W
(103D80h)	GPI_GLHRM_EN[7:0]	7:0	Gpi glitch remove enable.	
40h	REG103D81	7:0	Default: 0x00	Access : R/W
(103D81h)	GPI_GLHRM_EN[15:8]	7:0	See description of '103D80h'.	
41h	REG103D82	7:0	Default: 0x00	Access : R/W
(103D82h)	GPI_GLHRM_EN[23:16]	7:0	See description of '103D80h'.	
41h	REG103D83	7:0	Default: 0x00	Access : R/W
(103D83h)	GPI_GLHRM_EN[31:24]	7:0	See description of '103D80h'.	
42h	REG103D84	7:0	Default : 0x00	Access : R/W
(103D84h)	GPI_GLHRM_EN[39: 32]	7:0	See description of '103D80h'.	
42h	REG103D85	7:0	Default : 0x00	Access : R/W
(103D85h)	GPI_GLHRM_EN[47:40]	7:0	See description of '103D80h'.	
43h	REG103D86	7:0	Default : 0x00	Access : R/W
(103D86h)	GPI_GLHRM_EN[55:48]	7:0	See description of '103D80h'.	
43h	REG103D87	7:0	Default: 0x00	Access : R/W
(103D87h)	GPI_GLHRM_EN[63: 56]	7:0	See description of '103D80h'.	
44h	REG103D88	7:0	Default : 0x00	Access : R/W



GPI_INT Register (Bank = 103D)					
Index (Absolute)	Mnemonic	Bit	Description		
(103D88h)	GPI_GLHRM_EN[71: 64]	7:0	See description of '103D80h'.		
44h	REG103D89	7:0	Default: 0x00	Access : R/W	
(103D89h)	-	7:4	Reserved.		
	GPI_GLHRM_EN[75: 72]	3:0	See description of '103D80h'.		
45h	REG103D8A	7:0	Default: 0x00	Access : R/W	
(103D8Ah)	GPI_GLHRM_NUM[7:0]	7:0	Gpi glitch remove number.		
45h	REG103D8B	7:0	Default: 0x00	Access : R/W	
(103D8Bh)	-	7:3	Reserved.		
	GPI_GLHRM_NUM[10: 8]	2:0	See description of '103D8Ah'		