Chittagong University of Engineering and Technology

Department of Electronics and Telecommunication Engineering

VLSI Technology Sessional

ETE 404

Lab Project

8x1 MUX schematic, ADE simulations, Power usage, Symbol and Stick Diagram
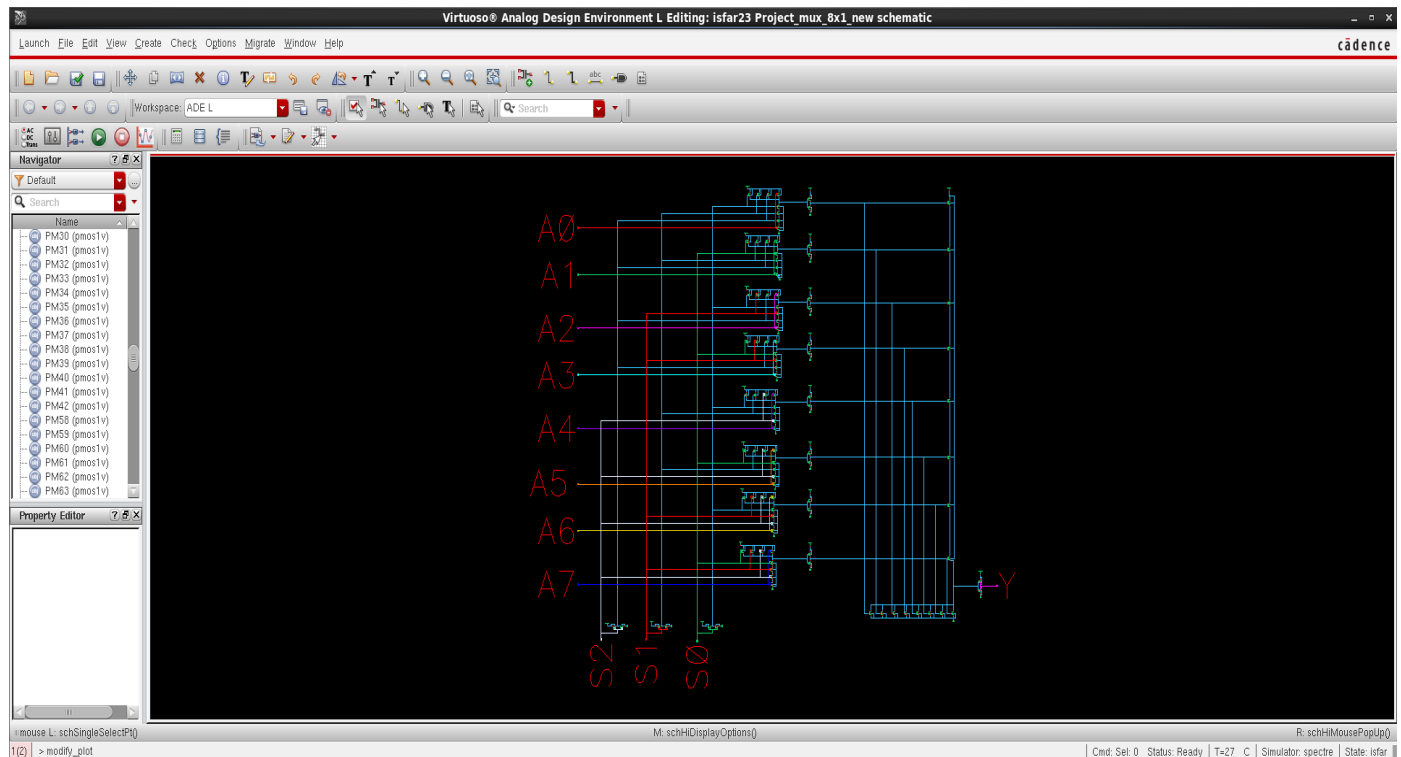

Name: Isfar Nayen
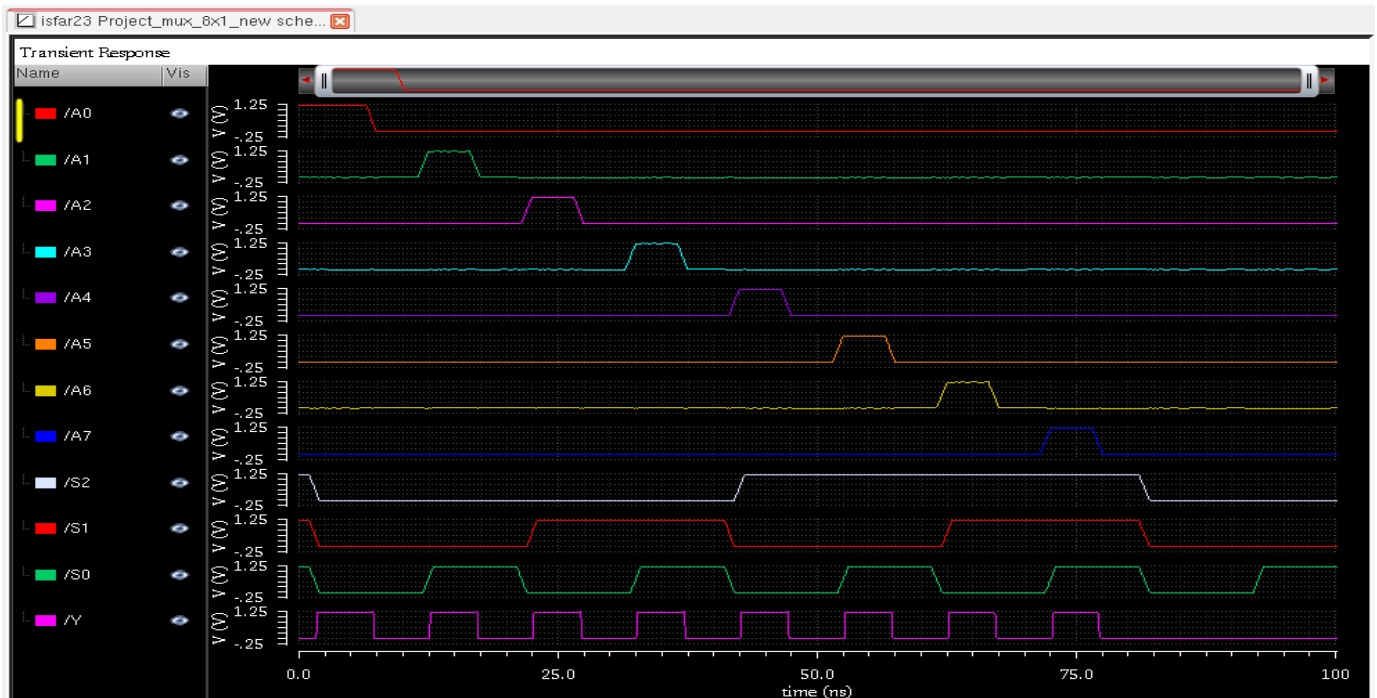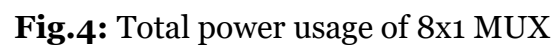ID: 1908023
Level: 04
Term: 01
Group: 01

Schematic:

Fig.1: Schematic of 8x1 MUX

ADE Simulations:

Fig.2: ADE simulation of 8x1 MUX

Power Usage:

Fig.3: Waveform of power usage of 8x1 MUX

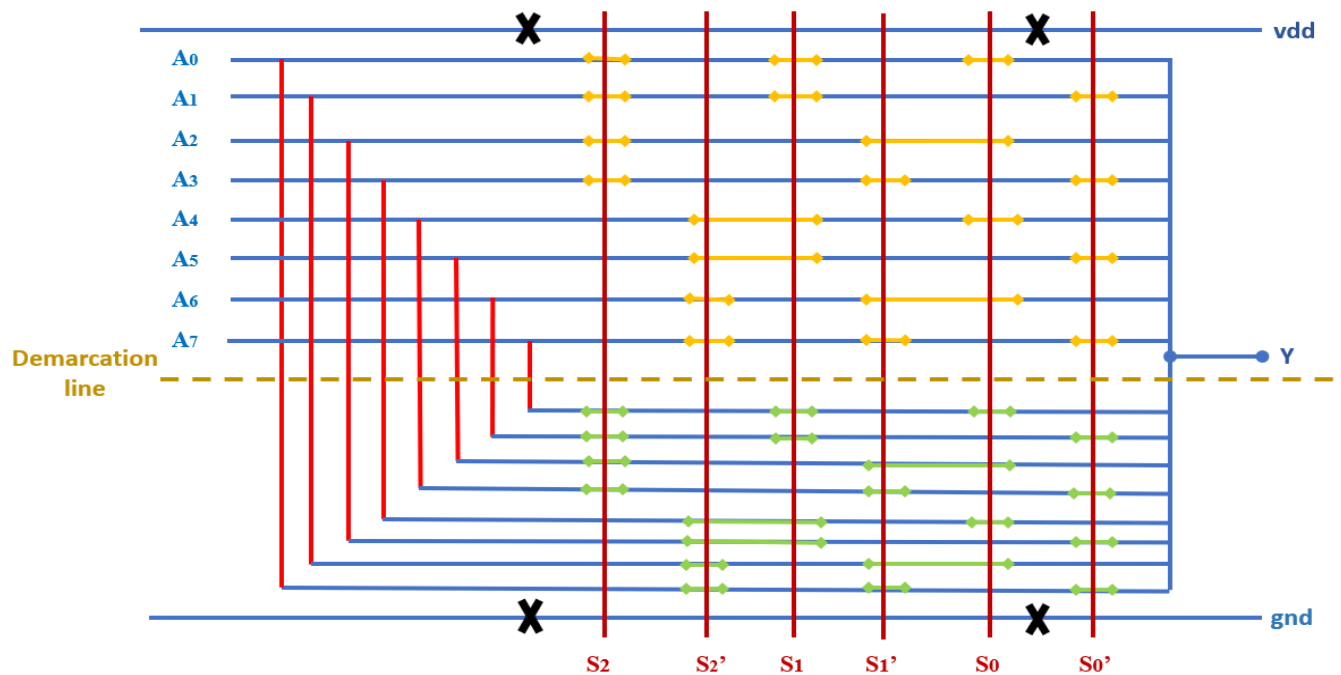**Fig.4:** Total power usage of 8x1 MUX

Symbol:
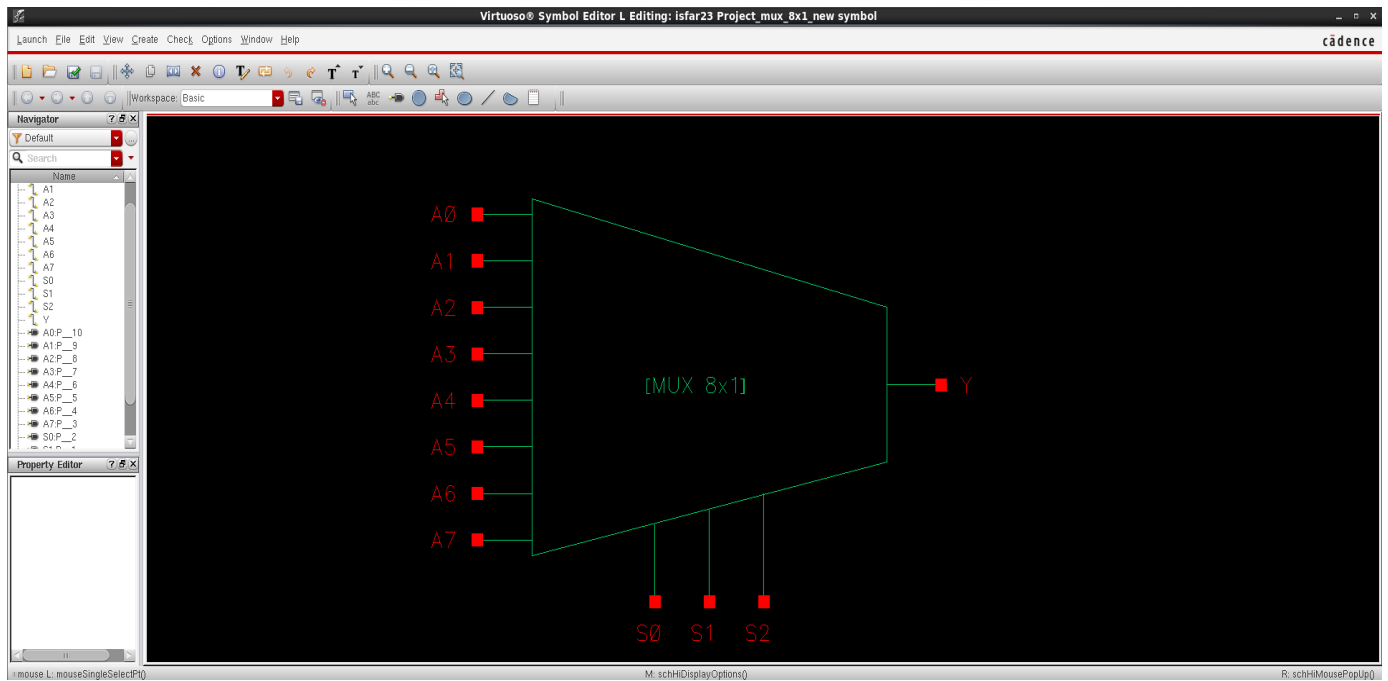
Fig.5: ADE simulation of 8x1 MUX

Stick Diagram:

Fig.6: Stick diagram of 8x1 MUX