Chittagong University of Engineering and Technology

Department of Electronics and Telecommunication Engineering

VLSI Technology Sessional

ETE 404

Experiment 07

Schematic Driven Layout Design of a NAND Gate Using Virtuoso Layout Suite Editor XL

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OBJECTIVES:

- To familiarize with schematic-driven layout design.
- To perform schematic-level verification, DRC and LVS.
- To perform post-layout simulation of NAND Gate.

DESIGN PROCEDURE:

To design the schematic for a 2-input NAND gate, named *nand2x1*, a new cell view was initiated from the CIW in Virtuoso Layout Editor XL. The design employed two NMOS transistors with a width of 240 nm and two PMOS transistors with a width of 480 nm. Inputs A and B were connected to the circuit, along with the output Y, properly interfaced with the ground (GND) and power supply (V_{dd}).

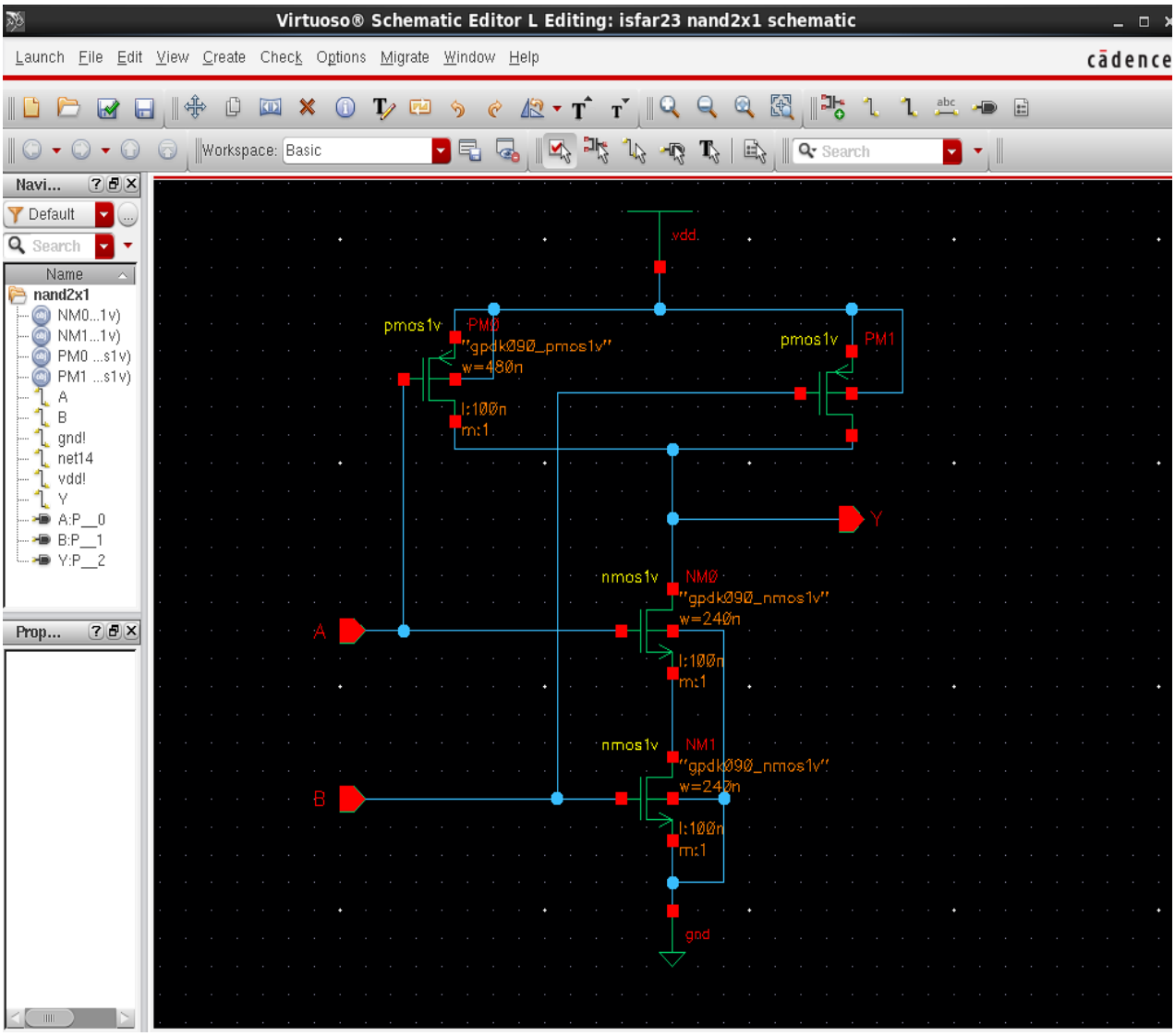

Figure 1: Schematic of NAND Gate

The design was simulated using ADE L to verify its functionality. After completing all necessary steps—such as configuring the model library, selecting the analysis type, and plotting the outputs as done in the previous lab—the output Y was successfully plotted based on the inputs A and B.

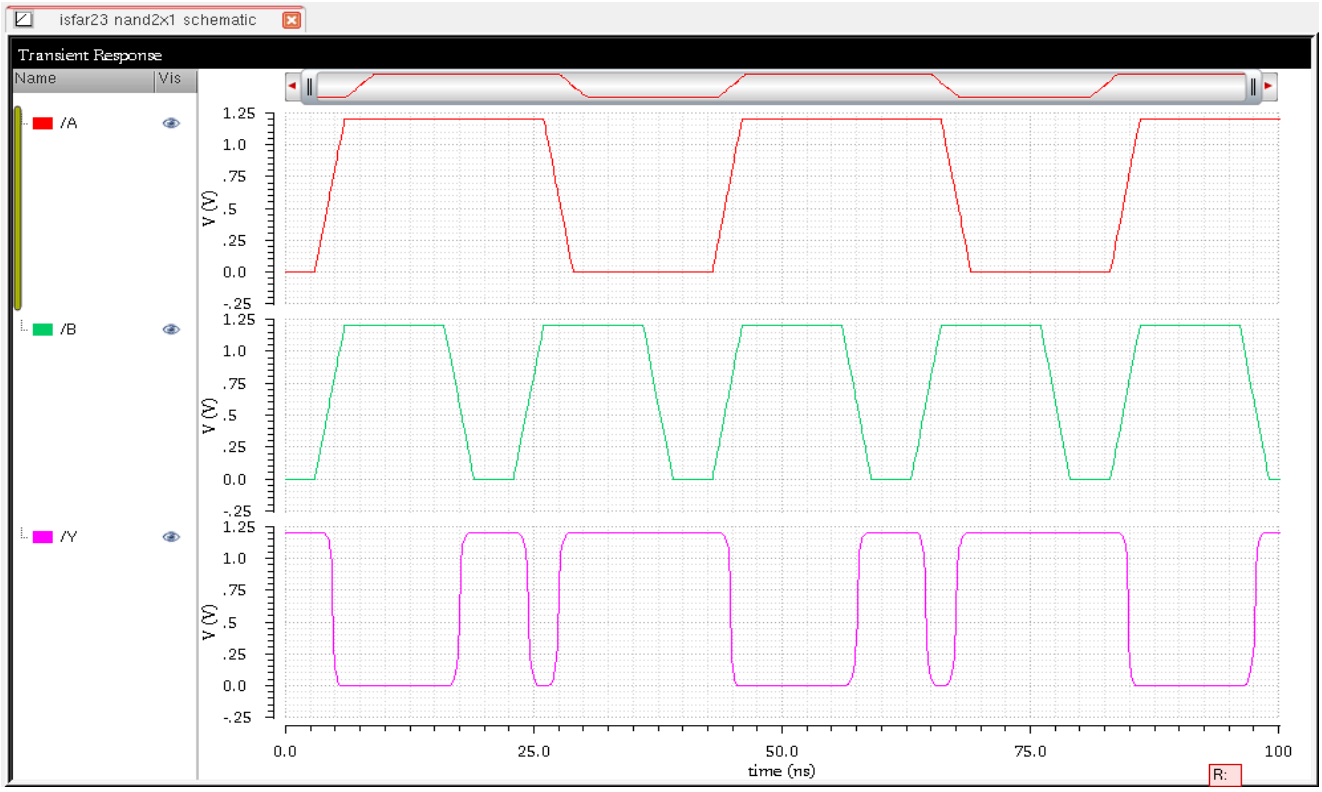

Figure 2: ADE L Output

After that, NAND gate symbol was created which is shown in Figure 3.

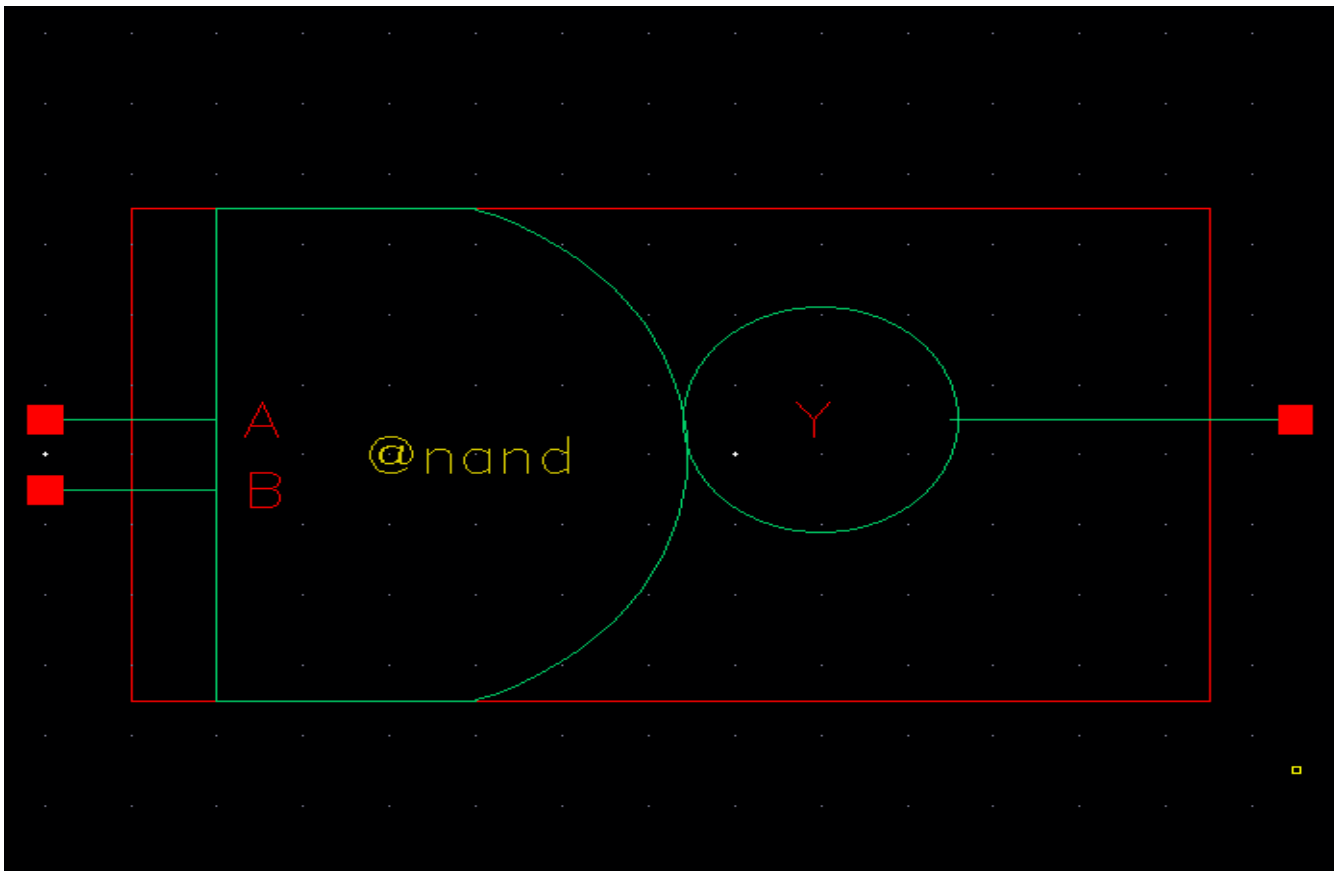

Figure 3: NAND Gate Symbol

Then Layout XL was launched from the schematic editor, the layout was created and wired up. The final layout is shown in Figure 4.

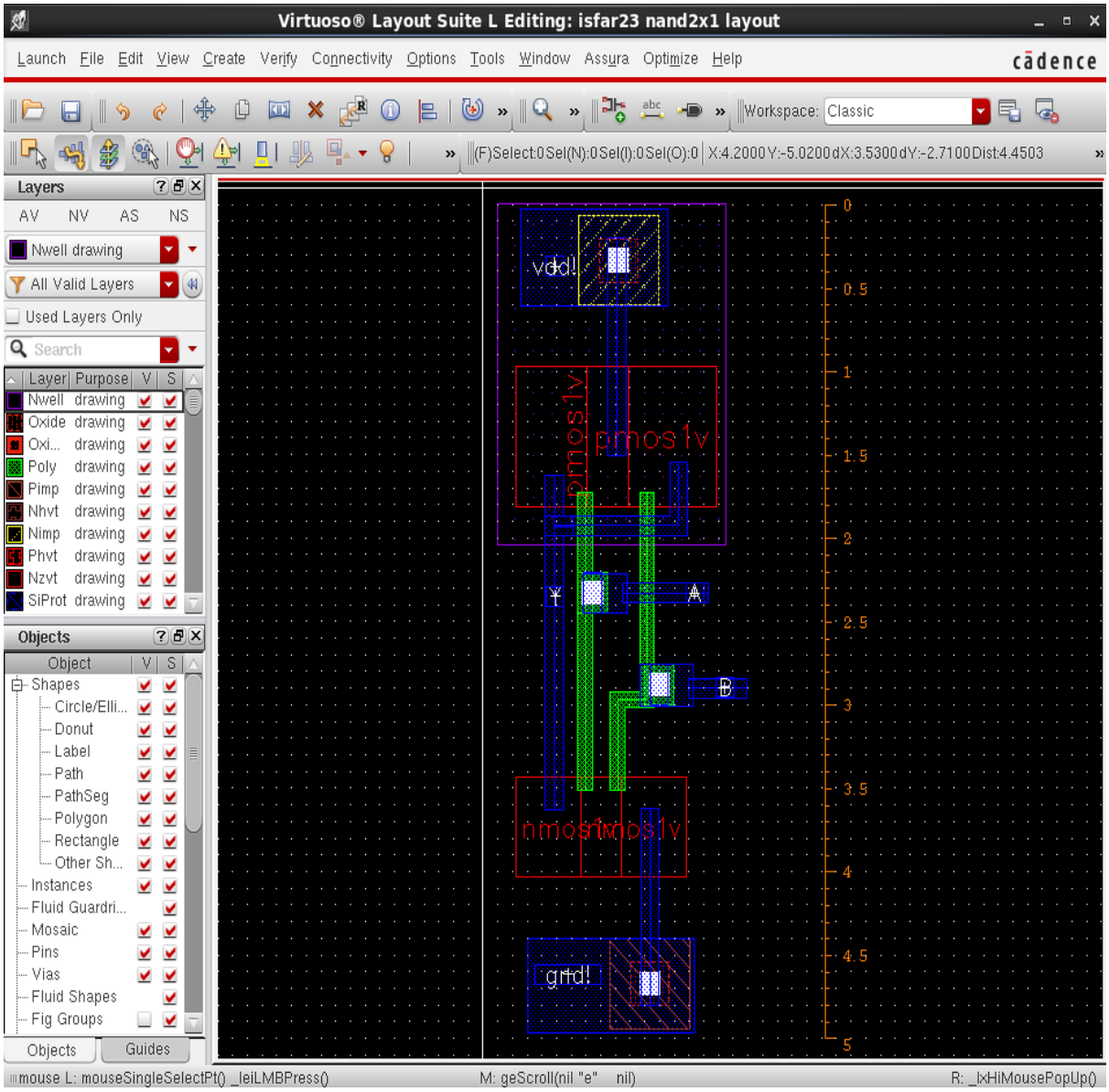

Figure 4: Final layout of NAND Gate

After that DRC and lvs were run and no error was found.

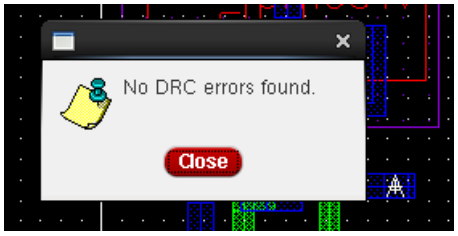

Figure 5: No DRC found

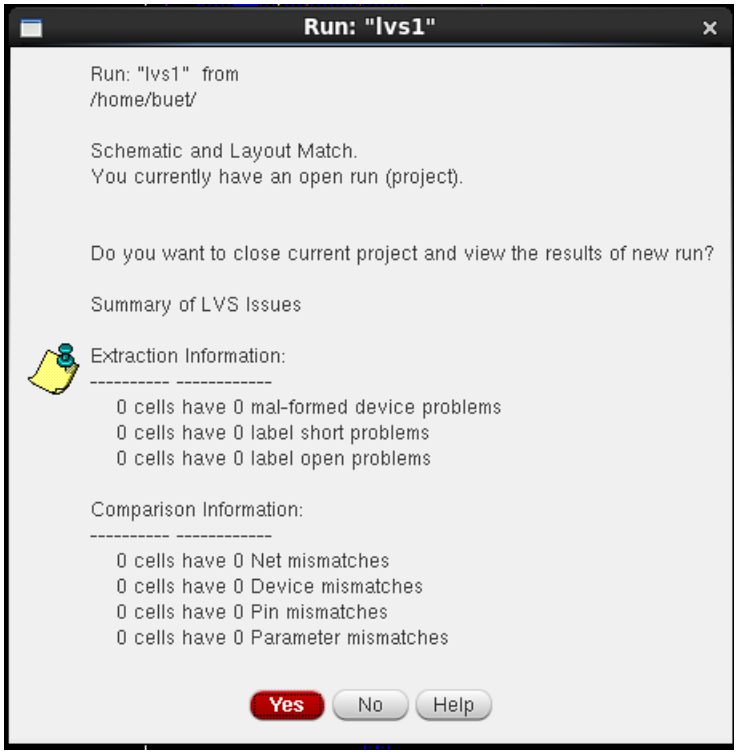

Figure 6: No error found in lvs run.

After performing RCX, av_extracted view was created which is shown in Figure 7.

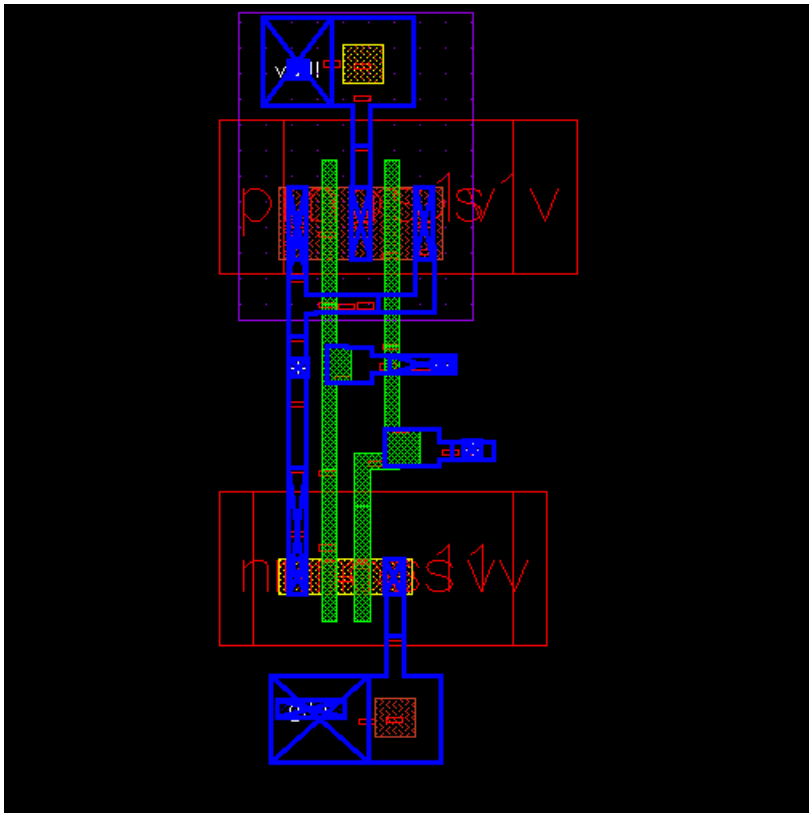

Figure 7: av_extracted view of NAND gate

After simulating the circuit to check its functionality, the intended output was obtained which is shown in Figure 8.

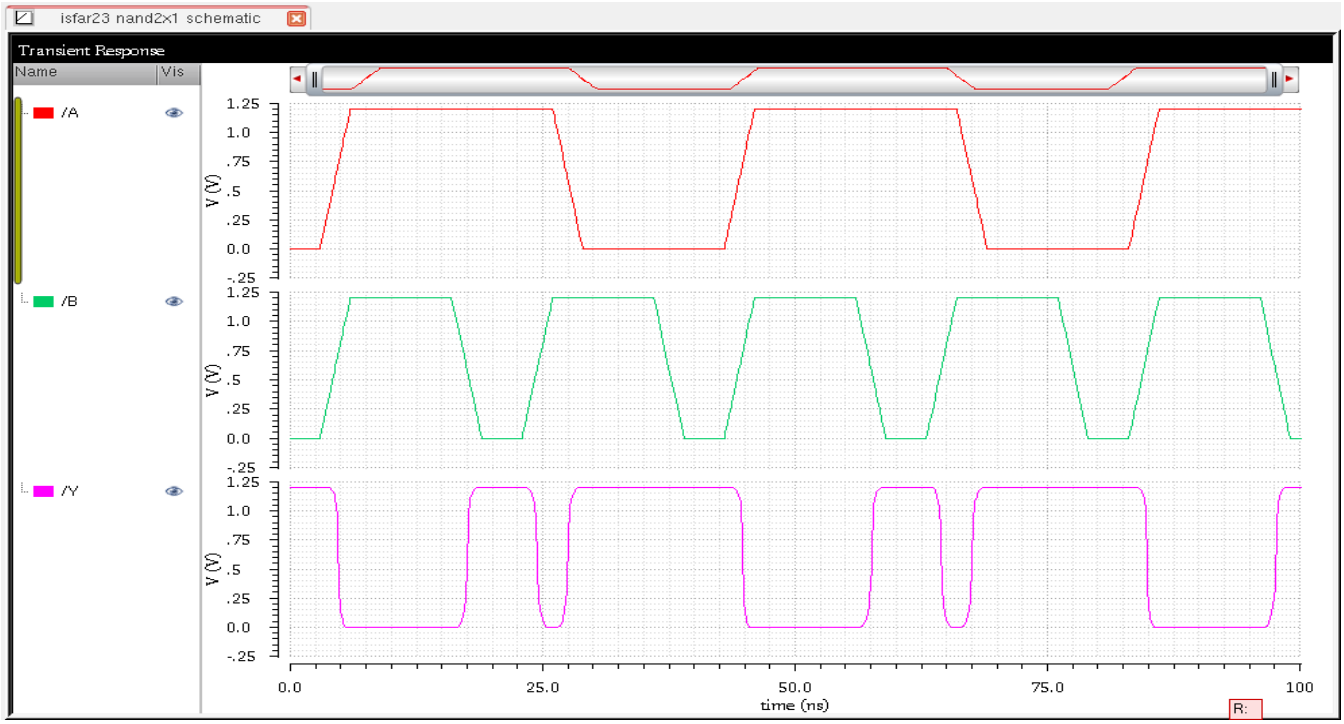

Figure 8: Transient response of av_extracted NAND gate

DISCUSSION:

- The NAND schematic, symbol, layout, and av_extracted views were produced using Virtuoso Layout Suite.
- A Design Rule Check (DRC) detected an error in the layout, prompting parameter adjustments.
- Layout versus Schematic (LVS) check was performed to establish the relationship between the schematic and the layout.
- After the adjustments, the intended output waveform was successfully displayed.