North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name:CSE231L

Section: 01

Experiment Number: 06

Experiment Name: Introduction to Multiplexers and Decoders

Experiment Date: 28/03/2021

Report Submission Date:4/04/2021

Group Number:

Student Name: Ishrat Jahan	Score
Student ID: 1921909042	
Remarks:	

Introduction to Multiplexers and Decoders

Objectives

- Understand the concept of multiplexing in the context of digital logic circuits.
- Learn about the internal logic of digital multiplexers.
- Implement digital logic functions using multiplexers.
- Observe and analyze the operations of the 3- 8 Line Decoder

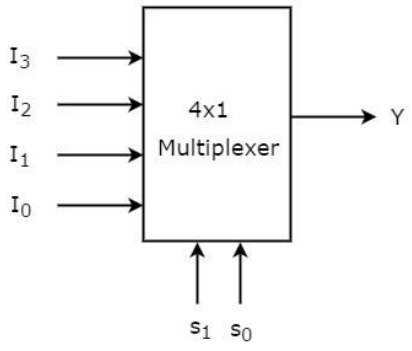
Theory

Multiplexer:

Multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination will select only one data input. Multiplexer is also known as Mux.

4x1 Multiplexer

4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0, two selection lines s_1 & s_0 and one output Y.



Block diagram of 4x1 Multiplexer

Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

From Truth table, we can directly write the Boolean function for output, Y as

$$Y=S1'S0'I0+S1'S0I1+S1S0'I2+S1S0I3$$

8x1 Multiplexer

We know that 4x1 Multiplexer has 4 data inputs, 2 selection lines and one output. Whereas, 8x1 Multiplexer has 8 data inputs, 3 selection lines and one output. 8x1 Multiplexer has eight data inputs I_7 to I_0, three selection lines S2, S1& S0 and one output Y.

Selection Inputs			Output
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

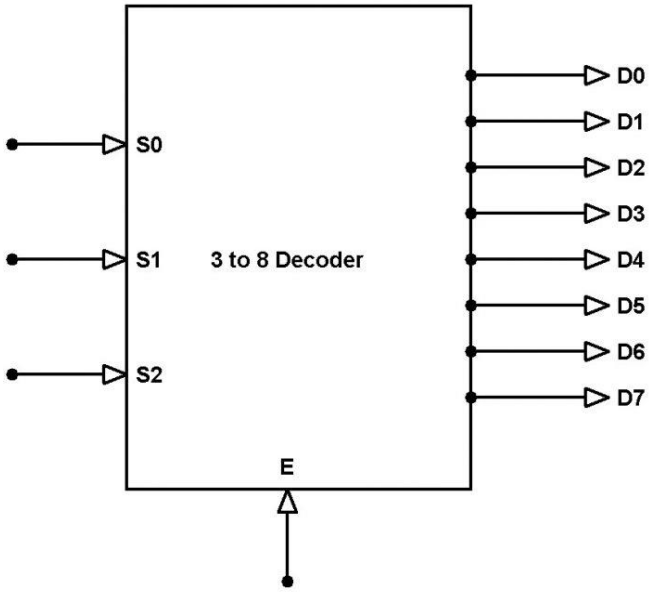
Truth table of 8x1 Multiplexer

From Truth table, we can directly write the Boolean function for output, Y as

$$Y= I0S2'S1'S0' + I1S2'S1'S0+ I2S2'S1S0'+ I3S2'S1S0+ I4S2S1'S0'+ I5S2S1'S0+ I6S2S1S0'+ I7S2S1S0$$

3 to 8 line Decoder

A decoder is a combinational circuit that is used to change the code into a set of signals. It takes multiple inputs and gives multiple outputs by converting binary information from n input lines to a maximum of 2^n output lines.



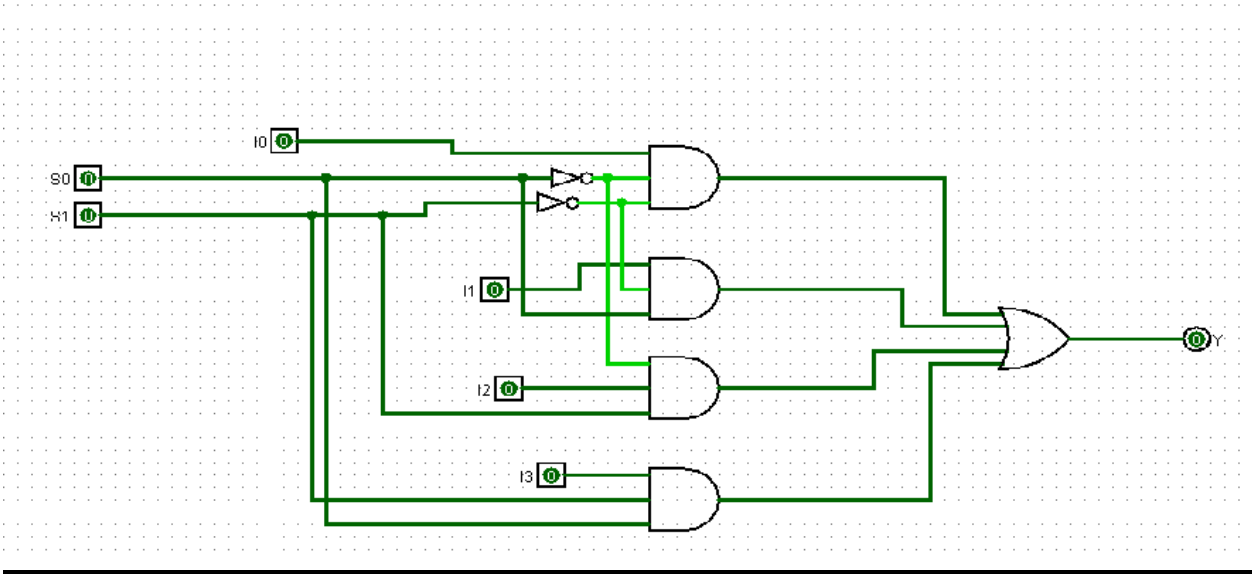
3 to 8 Decoder

It takes 3 binary inputs and activates one of the eight outputs. Here, S0, S1 and S2 are the inputs and the combination of their values determines which output line becomes active. Setting all the input values to zero activates the first output line (D0), setting x and y to zero and z to 1 activates the second

output line (D1) and this pattern continues till all the inputs are 1 at which point the eighth output line (D7) is activated.

Circuit Diagrams

Experiment 1: Constructing a 4:1 Multiplexer using basic Logic Gates



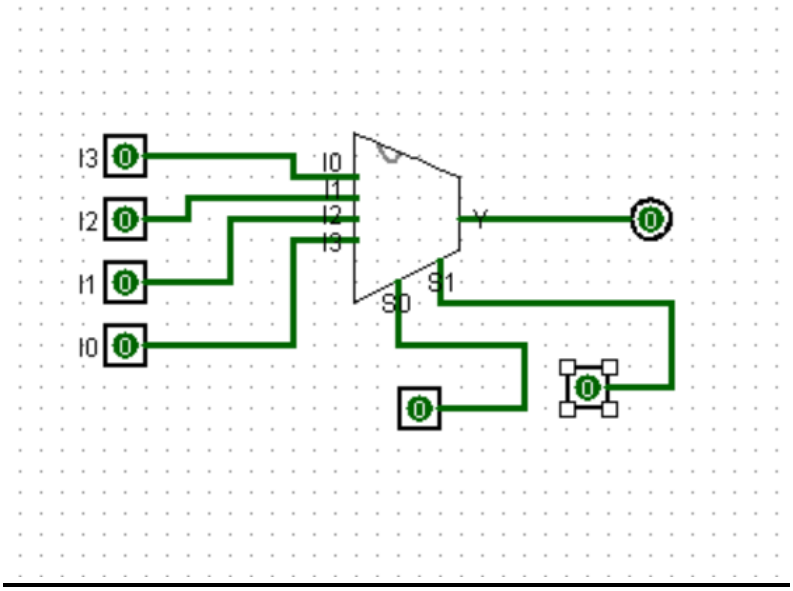
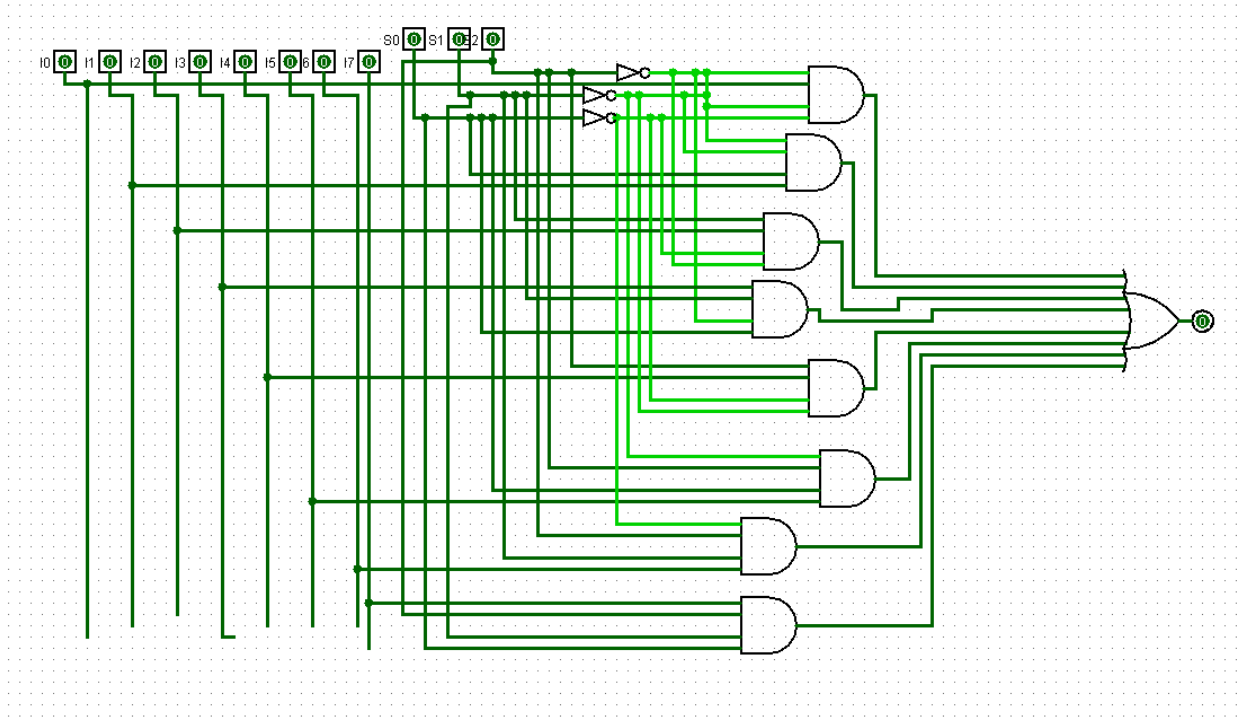


Figure D.1.1 4:1 Multiplexer

Experiment 2: Using an 8:1 Multiplexer to implement a Boolean function



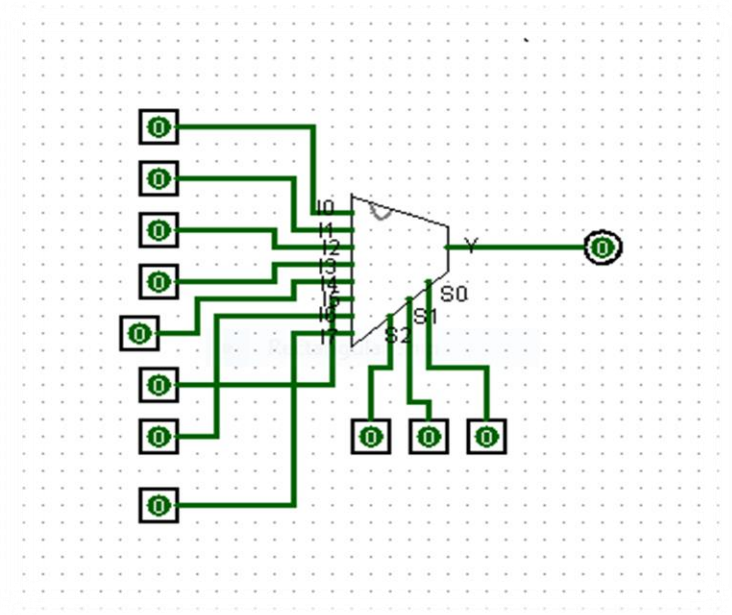
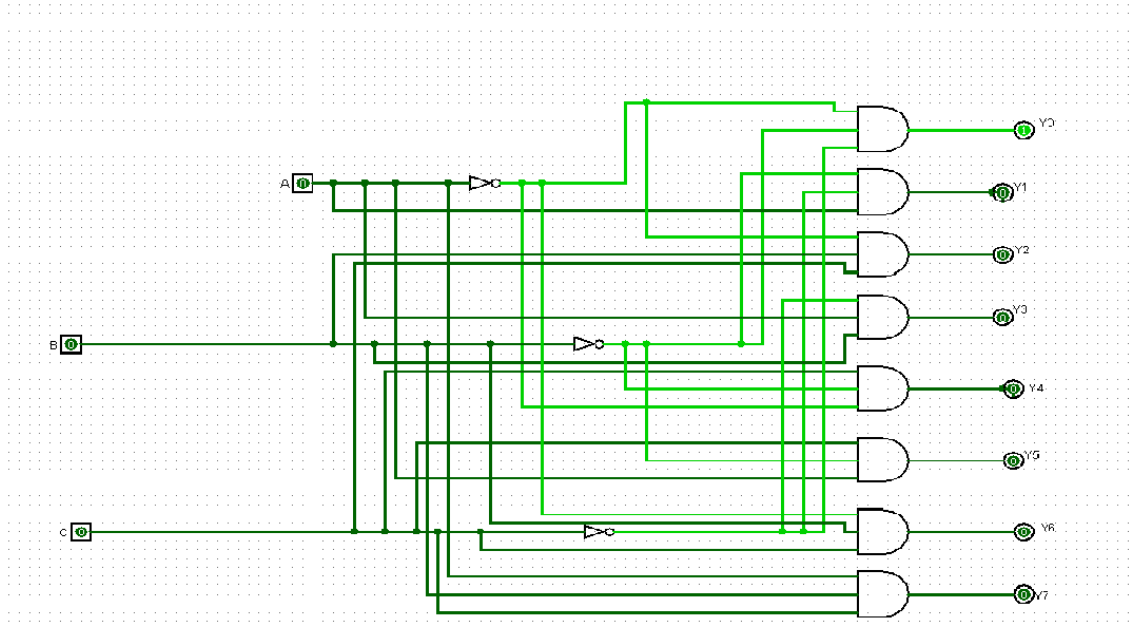
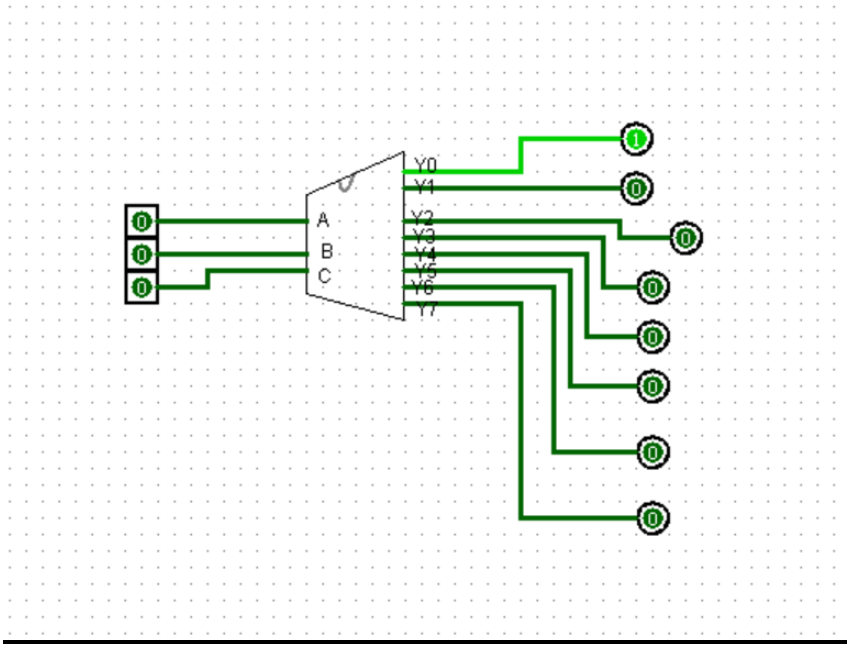


Figure F.2

Experiment 3: Implementing a 3 to 8 Line Decoder





Truth Table

F.1 Experimental Data: Implementing a Boolean function using a 4:1 MUX:

A	B	Data Inputs	F(Practical)
0	0	I0=A'B'	0
0	0		1
0	1	I1=A'B	0
0	1		1
1	0	I2=AB'	0
1	0		1
1	1	I3=AB	0
1	1		1

Table F.1.1

F.2 Experimental Data: Using an 8:1 MUX to implement a Boolean function:

A	B	C	Data Inputs	F(Practical)
0	0	0	I0=A'B'C'	0
0	0	0		1
0	0	1	I1=A'B'C	0
0	0	1		1
0	1	0	I2=A'BC'	0
0	1	0		1
0	1	1	I3=A'BC	0
0	1	1		1
1	0	0	I4=AB'C'	0
1	0	0		1
1	0	1	I5=AB'C	0
1	0	1		1
1	1	0	I6=ABC'	0
1	1	0		1
1	1	1	I7=ABC	0
1	1	1		1

Table F.2.1

F.3 Experimental Data: 3-8 Line Decoder:

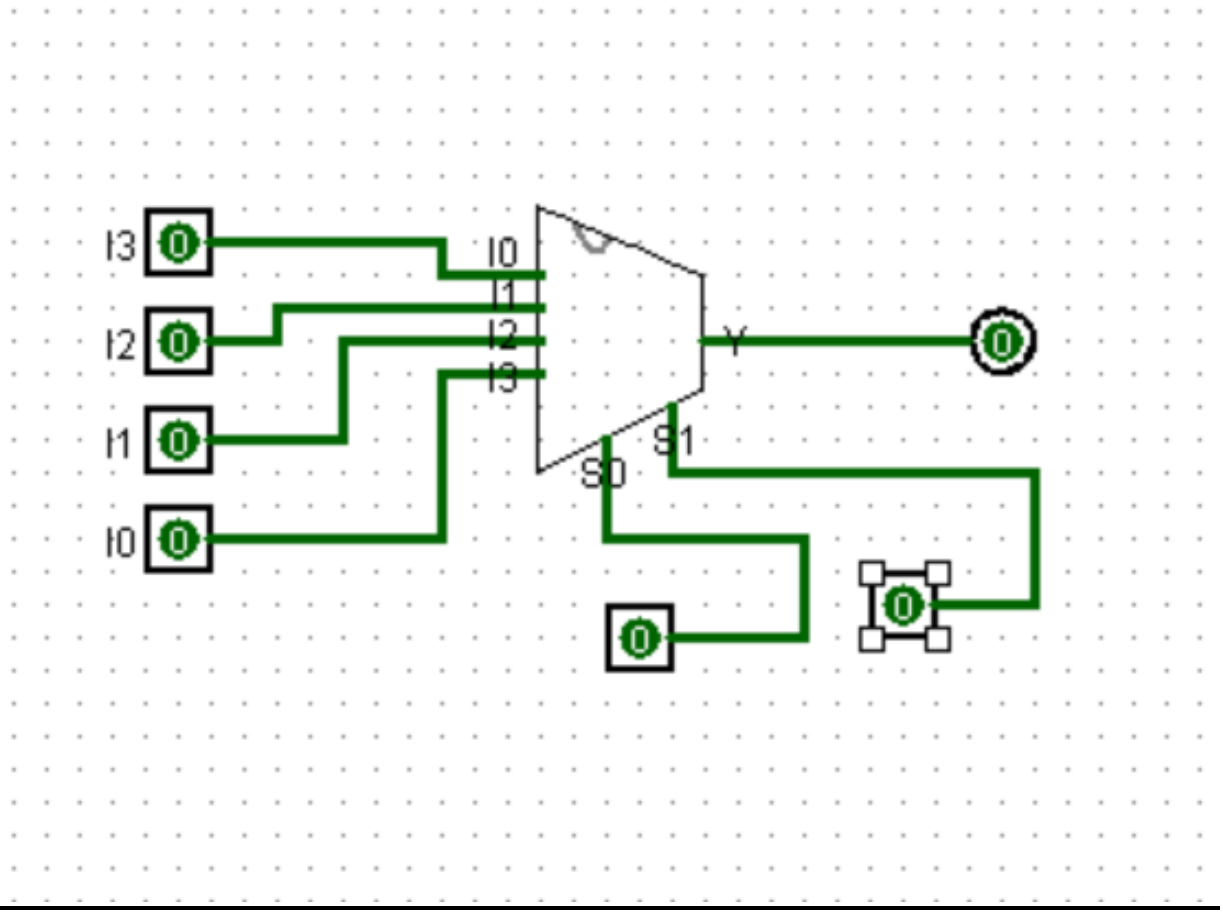
Enable Inputs		Select Inputs			Outputs							
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	1	0	0	0	0	0	0	0
H	L	L	L	H	0	1	0	0	0	0	0	0
H	L	L	H	L	0	0	1	0	0	0	0	0
H	L	L	H	H	0	0	0	1	0	0	0	0
H	L	H	L	L	0	0	0	0	1	0	0	0
H	L	H	L	H	0	0	0	0	0	1	0	0
H	L	H	H	L	0	0	0	0	0	0	1	0
H	L	H	H	H	0	0	0	0	0	0	0	1

Table F.3.1

Questions

E.1 Report

1)



4:1 Multiplexer

Discussion

The lecture was based on multiplexers and decoders. At first, we studied the concept of multiplexing in the context of digital logic. Firstly, the input, output and the selection bits in a 4:1 multiplexer was discussed. We learnt how the inputs will be on the left side and two inputs will be positioned below, which are known as the selection bits and how their values will control the output Y on the right side. We studied Figure: B1, a block diagram of a 4:1 multiplexer which will have 4 inputs, we used the formula Number of inputs=2^ (Number of selection bits) to find the number of selection bits which will be 2 selection bits (S0, S1) where the more significant one (S1) will be on the left side and the less significant one (S0) will be on the right side. Alongside that, we studied the truth table for the 4:1 multiplexer and how to derive the equation for a multiplexer using S0, S1 and the output. We also learned how we can vary the selection bits to get the desired outputs. For example: When both the selection bits are 0, we will get the first input as 1.We basically learnt how we can decide which of the output we want as 1.Following these, we conducted Experiment -1, where we drew the circuit of a 4:1 multiplexer using the sub-circuit knowledge. For drawing the sub-circuit of a multiplexer we went to the sub- circuit of the circuit and selected the plexer and took points to connect the lines. Then we completed the Data Inputs and F(Practical) column of the truth table F.1.1.Secondly, we conducted Experiment-2 where we drew an 8:1 mux. An 8:1 mux means it has eight inputs and 3 selection bits, which we worked out using Number of inputs=2^ (Number of selection bits)and then completed Table F.2.1 where we wrote down the values in the Data input column and the F(Practical) column. The last topic of the discussion was Decoder. We studied the 3x8 decoder. We saw how a decoder is different from a multiplexer in the area of inputs and outputs. A multiplexer has more inputs and only one output, whereas a decoder's number of output is more than its input and a decoder doesn't have any selection bits. For example, a 3x8 decoder has 3 inputs and 8 outputs. For an n input decoder we can have 2^n outputs. Then we studied Figure B2 and saw how setting all the input values to zero activates the first output line (0), and setting x and y to zero and z to 1 activates the second output line (1) and this pattern continues till all the inputs are 1 at which point the eighth output line (7) is

activated. Using these knowledge we carried out Experiment -3, where we had to draw a circuit of 3x8 decoder in Logisim.We changed the values of the selected inputs (C B A) to every combination from LLL where “L” was used to record a 0 and” to record a 1 and completed the truth table in Table F.3.1.