

North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No: 06

Experiment Title: Design of an ALU

Course Code: CSE332L

Course Name: Computer Organization & Architecture Lab

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Objective:

- 1: Building 1-bit ALU with specific set of instructions.
- 2: Building 16-bit ALU by connecting 16 one-bit ALU.
- 3. Designing the FLU to perform operations: Add, Sub, And, Or.
- 4. Incomponenting zero flag in the ALU.

Theory

FIN: An ALU stands for arithmetic-logical unit. It is a combinational circuit that can compute arithmetic operations like addition and subtraction as well as logical operations like FIND and OR. The MIPS word in an ALU refers to the bit width of the ALU. For example: Is the MIPS word is 32 bits wide, we need a 32-bit wide ALU. The input and output will be 32 bit each.

1-bit ALU: An 1-bit ALU have two 1-bit inputs Fland B and an 1-bit Output S(Sum). The 1-bit ALU performs Addition, Subtraction, AND and OR operations.

Operations: To pendorm the logical operations AND and OR, the 1-bit ALU uses AND gate and OR gate nespectively for each of them.

For performing the arithmetic operation:

For performing the arithmetic operation:

Add: An 1-bit adder is used. One input is same for both addition and subtraction, therefore it doesn't need varying.

Subtract: For subtraction we know: A + B + 1.

To change B we can keep a selection by using a change B we can keep a selection by using a Mux. The Mux will have two inputs, B and a Mux. The Mux will have two inputs, B and B and the selection is Binvert. When the Binvert is 1 and the Cin of the adder is 1, Binvert is 1 and the Mux is the Q's complement of the Mux is the Q's complement of the adder will carry out the B. Therefore, the adder will carry out the Subtraction Process.

Tok selecting which operation will be carried out.

there will be a second Mux to choose operations: Add, Subtract, AND, OR by varying the two bit's selection bit. It will have 4 inputs, one from AND gate, other Grom or gate and the last two from the Adder.

Herre, 00 personms AND operation. 01 performs OR operation 10 pendonms ADD operation. 11 Personms SUB operation.

16-bit ALU: By connecting 16 1-bit ALU, a 16-bit ALU can be designed. It will have two inputs each of 16 bits and an output (s) of 16-bit as mell. The 16-bit ALU will also have a zero flag.

Zerro flag. It is a single bit flag that is used to check the mesuit of an arithmetic operation. The Zero Slag is set (1) when the Kesult of an operation is zero. The zero flag will be I only is the entire result has all zeroe's. Otherwise the Zerro flag will be zerro in presence of 1.

For example: For a 4 bit-result

Sum = 0000, Zerro flag=1. Sum = 1000, Zeno flag=0.

The zero flag only considers the output sum and excludes the carry out. It doesn't matter is us. is the aarry out is \$10.

Advantage of using 1-bit ALU to construct n-bit ALU:

While using I - bit ALU to build a n-bit ALU, the change of things in the circuit is simple and easy. If we were to build a 16-bit ALU directly, it would have required IG AND gates, IG Adders and the whole circuit would have been messy and hard to sigure out is any there went wrong. Therefore, the approach of thing went wrong. Therefore, the approach of I-bit ALU to build n-bit ALU was used so that changes could be easily made. changes could be easily made.

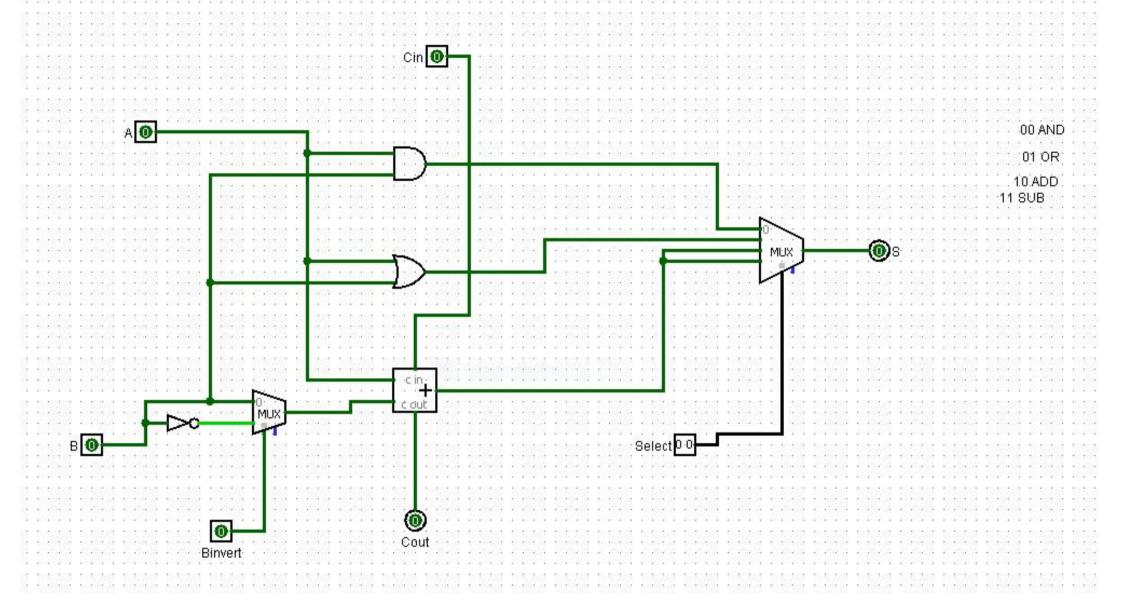


Figure:1-BIT ALU...

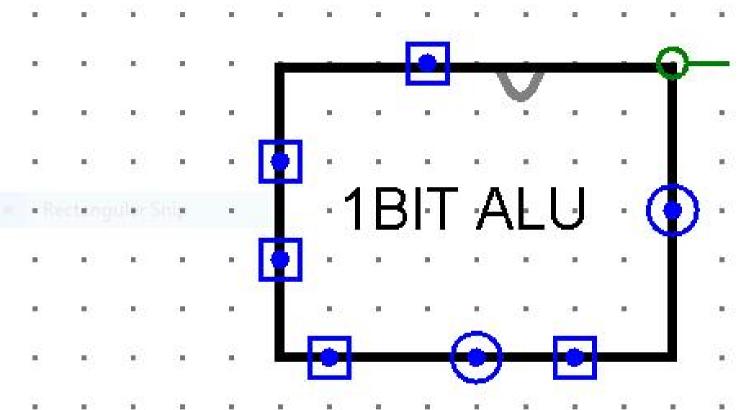
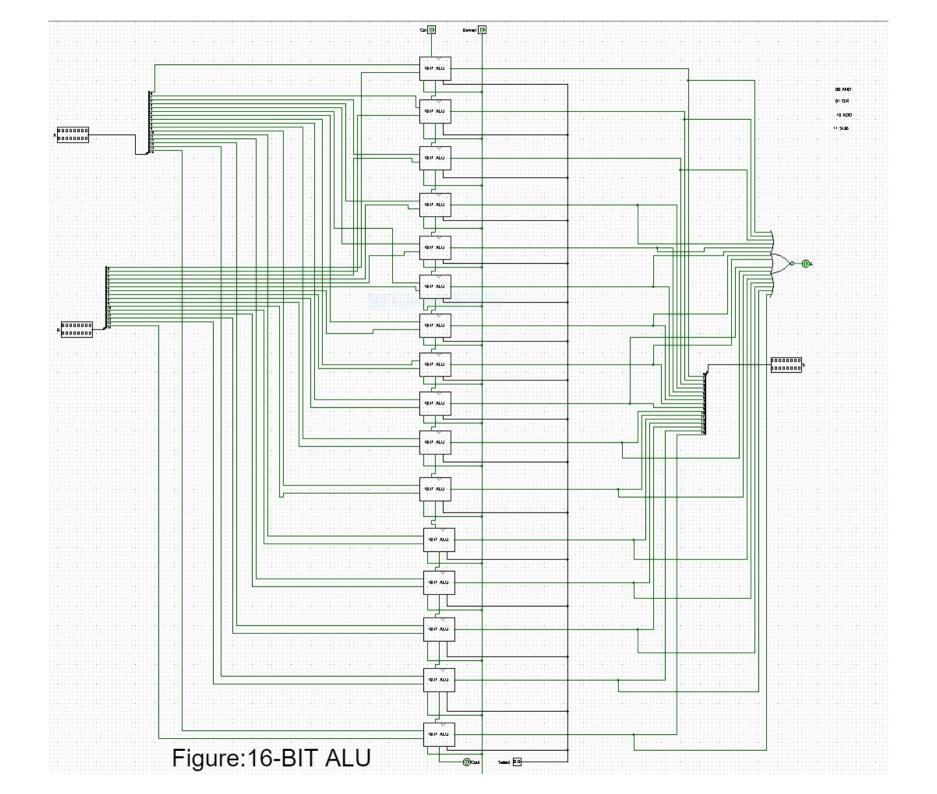


Figure:Subcircuit of 1-bit alu...



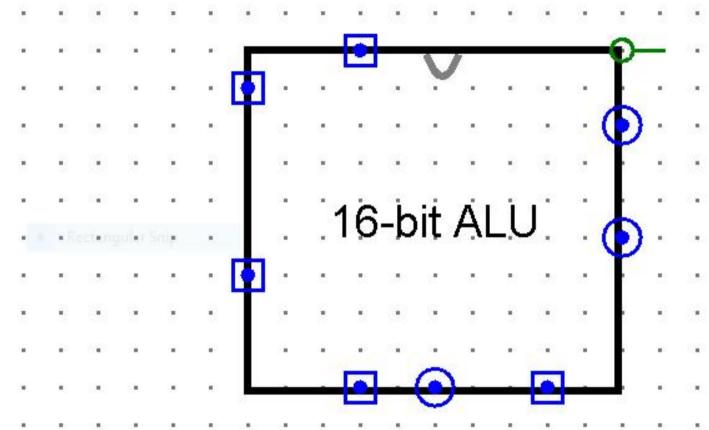


Figure:Subcircuit of 16-bit alu

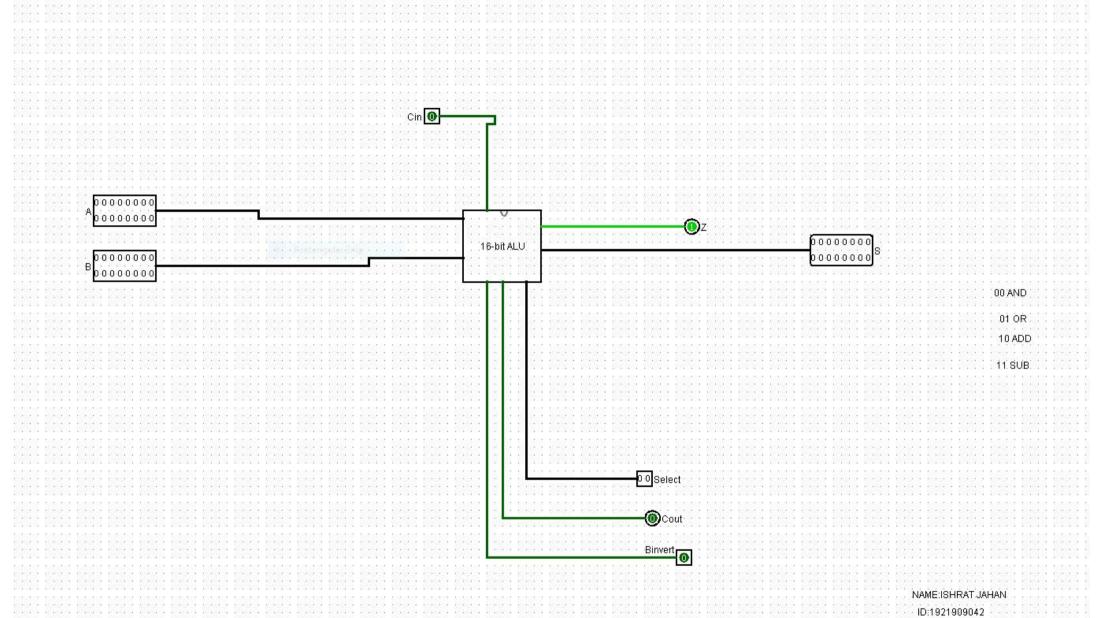


Figure:16 BIT-ALU(Final Circuit)

Discussion:

The experiment of Labob was based on "Design of an HLU". In this dab, we learned how to build an 1-bit FILU and by using it how we can design a 16-bit FILU.

Ht first we studied what an ALU is and how it works. We learn that ALU is a combinational circuit that can perform various of arithmetic and logical operations. The MIPS world refers to the bit width of an ALU. For example: Is the MIPS mond is 16-bits wide, we need a 16-bit wide ALU. His per the instructions in the lab manual, we were suggested to design a d-bit ALU and combine 16-d-bit ALU to design a d-bit ALU. The reason for doing so is build a 16-bit ALU. The reason for doing so is changes can be easily made to the circuit. If g changes can be easily made to the circuit. If g change enything in the d-bit ALU all other change enything in the delay updated. Horeover, if 1-bit ALU are automatically updated.

Then we studied the arithmetic and logical operations the FLU will perform. For the logical operations: the FLU will perform. For the logical operations: AND and OR, it can be done using AND gate and OR gales mespectively. For addition, we can use on Adder. For Subtraction we know the equation an Adder. The input TI will be same for both is:- A+B+1. The input TI will be same for both Addition and Subtraction but we need to change Addition and Subtraction it will be B and for B; that is for Addition it will be B and for authorized a Next Mux which will have input B and B' and a Next Mux which will have input B and B' and a Next Mux which will have input B and B' and a Selection known as Binvert which is turned a selection known as Binvert which is formed to the output of the Mux is the 2's complement of B and the subtraction operation will be ent of B and the subtraction operation will be

carried out. And for ahoosing between these four operations we will be using a 4x2 Mux where the select bits will control which operation will be carried out. Here, oo carries AND operation, of does OR, 10 does ADD and 11 does SUB. For SUB the carry in must be 1.

Then we discussed what a zero glag is and how to design it in the circuit. A zero glag is a single bit slag that is used to check is the output of an operation is zero or not. If the zero glag is I, the output consists of all zeroe's. Otherwise if it is 0, the output might be sil I or mixture of I and 0. To incomporate a zero flag in a circuit, we noticed for a two bit sum

(S, So)	Z	AND	OR	1
00	1		0	
0.1	0	0	1	
4 2	0	0	1	
1 1	0	1.	1	

that, zero flag is when the circuits works in the invert of OR, that is NOR. Therefore, if we connect a NOR gate with the circuit, the output will show the zero flag. The theoretical part of the lab ended after this.

To make it easier for us, our lab instructor showed us how a create a 4-bit Rep ALU. The sirest step was to design a 1-bit ALU. It has two input of 4-bits each and the 4-bit output. The rest of the circuit was constructed as per explained in circuit was constructed as per explained in the 4-bits each and these circuits were created the theory. The these circuits were created the theory. The these circuits were another lab.

Then we were taught to create seperate file's for the 4-bit ALU which was created using the sub-circuit of the 1-bit ALU. Aster showing the whole procedure we were asked to complete our lab task which was to design a 16-bit ALU.

The first-step in creating a 16-bit ALU, was to areate a 1-bit ALU. For creating 1-bit ALU, 9 opened the Lab-Sile that have the Register File, right clicked on the folder name in dogisim, selected the 'Add Circuit' option and named it as 1-bit ALU. To create 1-bit, 8inst 9 took two input Pin of 1-bit and labelled them H and B Force AND and OR operation, 4 took two gates from gates section, one AND gate and another or gate both of data bits 1. Then I connected input A and B to them. For addition, 9 took an adder from the arithmetic section of data bits 1, 2nd connected it to the adders one input porct. For the other input B, we need to select among B and B' so & took a Mux of select bit I and connect B and B' (B with NOT gate) to the Mux's second input poret. Then I took snothere two 1-bit input Pin and connected one of them with the Nux's select porch and labelled it as Binverd. Binverd will be used to control what will be the output of the Mux (Bore B'). The other input pin was labelled Cin and connected to the adder's Cin. For the Carry out, & took an output pin labelled it as Cout y out, I took un of Cout port 08 the Adder. As there was suppossed to be a choice, the MUX's output was imputted to the adders second output. Is we were going to control

which operation out of these 4 operations will be carried out, we needed another mux of Linpois and selection bit 2. The output from the AND gate, or gate and Adder was added to the Nux. The last input was also the output from the adder. That fore the selection bit, I took an input pin, changed it's data bit to 2, labelled it as select and connected it to the Mux. For displaying the output, I took an output pin, labelled it as 15 and connected with the Mux's output. Then I created the sub-circuit of the I-bit ALU using the sub-circuit of the I-bit ALU using the sub-circuit of the I-bit ALU using the sub-circuit of the input, output, select bit, Qin, Binvert, I placed the input, output, select bit, Qin, Binvert, Cout and S Is pere my convenience. With it, I completed the design of I-bit ALU.

The second step was to execute the 16 bit ALU with 16 1-bit ALU. For that, 9 again created another file, named it 16-bit ALU. Then I drag and dropped 16 1-bit ALU subcirrcuits. For the input, 9. took two input pin, changed there data bite to 16 and labelled them F and B respectively. Then I took two splitters's, changed their bit width and San out to 16 and connected to A and B. Then & connected the input's with the ALU'S in order, AoBo with the 1st ALU, A1B1 with the second, till the MSB's are connected with the last ALU Fore the Cin, 9 took an input Din of pin of 1-bit, and connected it with the Cin part of the FLU. The Cout of the first ALU will be the Cin of the second ALU and so on. So & connected 311 the Cin's and Cout's in that order. Then 9 took another input pin of data bit I, labelled it as Binvert and connected it with the Binneret Porct of the ALU. & did the

same with the select port. For that & took on input pin, changed it's data bit's to & and connected it to all the ALU's selection port. For displaying Cout, & took an output pin, labelled it as Cout and connected it to the last ALU's Cout port.

tor displaying the output, of took an output pin, changed it's data bits to 16 and labelled it as S. Then of took a splitter from the wiring section, changed it's bit width and fan out to 16 and connected it with the output pin. The 1st ALU is the LSB so it was connected with the splitter's O part. The second ALU was connected with the splitter's I part and so on. This way I connected all the ALU output to the splitter. The output 'S' was completed.

For displaying the zero flag, 9 took a Nor gate from the gates section and changed it's number of inputs to 16. Then 9 connected the ALU output with the inputs of the Nor gate in sequential order. The first ALU was connected with the 15th input and so on. The result was displayed by using an output pin. 9 took the output pin of data bit 1 and connected it to the Nor gate's data bit 1 and connected it as 2. The diagram of output and labelled it as 2. The diagram of output and labelled it as 2. Then 9 created the 16-bit ALU was completed. Then 9 created the sub-circuit of the 16-bit ALU with the inputs, outputs and select bits, binvert, Cin in specific

Aster that I oneated another Sile using (Add Circuit) and named it 16-bit ALU final. I dragged and dropped the sub-circuit of the 16-bit ALU in that Sile. Aster that I took two input pin, changed

there data bits to ±6 and connected it with the sub-circuits input ports. I took two input pins again with data bits & I and connected one of them with lin Ind the other with the Binvert port. For the select option, I took an input pin changed it's data bits to 2, labelled it as select All the inputs were labelled. For displaying lout, I took one output pin, labelled it Cout and connected it with the Cout port. For 12' (zerro flag, I did the same and labelled the output pin, changed as 2. For displaying 1s', I took an output pin, changed it's data bit's to ±6 and labelled it as s and it's data bit's to ±6 and labelled it as s and connected it with the output port. The circuit was connected it with the output port. The circuit was completed. Fifter completion, I checked the outputs.

The only problem & Saced in this experiment, is the circuit of 16-bit ALU was too big and congested. Morreover, there were very less space as there were were many components in the eircuit as well as many connections. So, I had to be very carreful while connecting everything. be very carreful while connecting everything. Overcall, it is easy to design if designed cautiously with enough time on hard.