File: C:/My_Designs/lab09/lab09/src/spi_tx_shifter_tb.vhd (/spi_tx_shifter_tb)

```
1    ------------------------------------------------------------------------
     -----
2    --
3    -- Title       : spi_tx_shifter_tb
4    -- Design      : spi_tx_shifter_tb
5    -- Author      : Ishabul Haque and Ken Ejinkonye
6    -- Company     : Stony Brook
7    --
8    ------------------------------------------------------------------------
     -----
9    --
10   -- File        : c:\My_Designs\Lab_09\SPI_Transmitter_and_Reciever\src\spi_tx_shifter_t
     d
11   -- Generated   : Sun May  3 10:51:17 2020
12   -- From        : interface description file
13   -- By          : Itf2Vhdl ver. 1.22
14   --
15   ------------------------------------------------------------------------
     -----
16   --
17   -- Description : Non-self checking testbench for spi_tx_shifter design
18   --
19   ------------------------------------------------------------------------
     -----
20
21
22   library ieee;
23   use ieee.std_logic_1164.all;
24   use ieee.numeric_std.all;
25   library work;
26   use work.all;
27
28
29   entity spi_tx_shifter_tb is
30   end spi_tx_shifter_tb;
31
32
33
34   architecture tx_shifter_tb of spi_tx_shifter_tb is
35      --stimulus signals
36       signal rst_bar : std_logic;
37       signal clk : std_logic;
38       signal send_en: std_logic;
39       signal cpha: std_logic;
40       signal cpol: std_logic;
41       signal dord: std_logic;
42       signal data_in: std_logic_vector(7 downto 0);
43       signal spi_rxen: std_logic;
44
45       --observed signals
46       signal txd: std_logic;
47       signal sck: std_logic;
48       signal ss_bar: std_logic;
49
50
51       constant period : time := 40ns;
52       signal end_sim : boolean := false;
```

```
53
54   begin
55       -- Unit Under Test port map
56       UUT: entity spi_tx_shifter
57       port map (
58           rst_bar => rst_bar,
59           clk => clk,
60           send_en => send_en,
61           cpha => cpha,
62           cpol => cpol,
63           dord => dord,
64           data_in => data_in,
65           txd => txd,
66           sck => sck,
67           ss_bar => ss_bar,
68           spi_rxen => spi_rxen
69           );
70
71        -- Process to generate value for input data_in
72        data_gen:process
73        begin
74            for i in 1 to 2 loop
75                wait until clk='0';
76           data_in<="11001010";
77           end loop;
78           wait;
79        end process;
80
81        -- Process to generate clock
82
83        clock_gen:process
84        begin
85            clk<='0';
86            loop
87                wait for period/2;
88                clk<=not clk;
89                exit when end_sim = true;
90           end loop;
91           wait;
92        end process;
93
94       -- Process to generate values for reset bar
95       reset: process
96       begin
97           -- Reset bar intially 0 for 60ns
98           rst_bar <='0';
99           for i in 1 to 2 loop
100              wait until clk = '1';
101          end loop;
102          rst_bar<='1';
103          wait;
104      end process;
105
106      -- Process to generate values for dord,cpol,cpha. The push button
107      -- is represented by design send_pos_edge and cpol and cpha are
108      -- not changed in the middle of a transmission. Value of dord
109      -- determines which bit position the data is shifted to.
```

```
110      push_button:process
111      begin
112          -- Initialized values
113          send_en <= '0';
114          cpol <= '0';
115          cpha <= '0';
116          dord <= '0';
117
118          wait for 4*period;
119          for i in 0 to 7 loop
120              -- Generates the different modes of operation
121              (dord, cpol, cpha) <= to_unsigned(i,3);
122              wait for 2*period;
123              send_en <= '1';
124              wait for 20*period;
125              send_en <= '0';
126              wait for 2*period;
127
128          end loop;
129          end_sim <= true;
130          wait;
131      end process;
132
133
134  end tx_shifter_tb;
135
```