1. How long is the send_en pulse generated by send_pos_edge_det? State this time duration as both number of clock pulses and as ns.
    a. The send_en pulse generated by the designs task is 80ns long and is the duration of two clock pulses
2. What is the frequency relationship between the SPI clock sck and the system clock clk?
    a. The frequency of SPI clock sck is half of system clock clk.
3. From the log file determine the default state assignment encoding used by the synthesizer for your FSMs.