File: C:/My_Designs/lab09/lab09/src/spi_rx_shifter_tb.vhd

```
1    ------------------------------------------------------------------------
     -----
2    --
3    -- Title       : spi_rx_shifter_tb
4    -- Design      : spi_rx_shifter_tb
5    -- Author      : Ishabul Haque and Ken Ejinkonye
6    -- Company     : Stony Brook University
7    --
8    ------------------------------------------------------------------------
     -----
9    --
10   -- File        : c:\My_Designs\Lab_09\SPI_Transmitter_and_Reciever\src\spi_rx_shifter_t
     d
11   -- Generated   : Tue May  5 10:55:14 2020
12   -- From        : interface description file
13   -- By          : Itf2Vhdl ver. 1.22
14   --
15   ------------------------------------------------------------------------
     -----
16   --
17   -- Description : Non self checking test bench for spi_rx_shifter design
18   --
19   ------------------------------------------------------------------------
     -----
20
21
22   library ieee;
23   use ieee.std_logic_1164.all;
24   use ieee.numeric_std.all;
25
26
27
28   entity spi_rx_shifter_tb is
29   end spi_rx_shifter_tb;
30
31
32
33   architecture rx_shifter_tb of spi_rx_shifter_tb is
34
35       --stimulus signals
36       signal rst_bar : std_logic;
37       signal clk : std_logic;
38       signal rxd : std_logic;
39       signal dord: std_logic;
40       signal spi_rxen: std_logic;
41
42       --observed signals
43       signal data_out: std_logic_vector(7 downto 0);
44
45       -- Constants
46       constant period : time := 20ns;
47       signal end_sim : boolean := false;
48   begin
49       -- Unit Under Test port map
50       UUT: entity spi_rx_shifter
51       port map (
52           rst_bar => rst_bar,
```

```
53          clk => clk,
54          rxd => rxd,
55          dord => dord,
56          data_out => data_out,
57          spi_rxen => spi_rxen
58          );
59
60          -- Process to generate value for clock
61          clock_gen:process
62
63          begin
64
65              clk<='0';
66              loop
67                  wait for period/2;
68                  clk<=not clk;
69                  exit when end_sim = true;
70              end loop;
71              wait;
72          end process;
73
74          -- Process to generate value for reset bar
75          reset: process
76          begin
77
78              rst_bar<='0';
79              for i in 1 to 2 loop
80                  wait until clk = '1';
81
82              end loop;
83              rst_bar<='1';
84              wait;
85
86          end process;
87
88          -- Process to generate dord, dord simply changes
89          -- from 0 to 1 for verification purposes of the design
90          dord_gen: process
91          begin
92              loop
93              dord <= '0';
94              wait for 400 ns;
95              dord <= '1';
96              exit when end_sim = true;
97              end loop;
98          end process;
99
100         -- Process to generate value for spi_rxen
101         -- A value of 0 is asserted to verify data
102         -- is only shifted when spi_rxen is asserted
103         spi_rxen_gen: process
104
105         begin
106
107             spi_rxen <= '0';
108
109             loop
```

```
110                 wait for 2*period;
111                 spi_rxen <= '1';
112                 wait for 20*period;
113                 spi_rxen <= '0';
114                 wait for 2*period;
115                 exit when end_sim = true;
116             end loop;
117 
118         end process;
119 
120         -- Proocess to generate value for rxd, data
121         -- being shifted in
122         rxd_gen : process
123         begin
124             rxd <= '1';
125             loop
126                 wait for period/2;
127                 rxd <= '1';
128                 wait for period/2 ;
129                 rxd <= '0';
130                 wait for period/2;
131                 exit when end_sim = true;
132             end loop;
133         end process;
134 
135 
136 
137 end rx_shifter_tb;
138 
```