c:/My\_Designs/lab09/lab09/src/wave.asdb untitled.awc 800 1600 2400 3200 4000 4800 5600 6400 7200 ns Signal name Value rst bar 1 0 лг clk √u send en 1 Mode 100 Mode 110 Mode 101 Previous mode was 000 Mode 111 **™** cpha 1 Mode 010 Mode 011 **™** cpol 0 Mode 001 **J** dord 0 CA **∄ J** data in CA 1 .ru txd 0 Each sequential value of sck corresponds to a different state. These 0 лгsck values are identified in the design description ss\_bar is only 1 when idle **™**ss\_bar 0 ₁ end sim false Next state after idle is ph1 | fter ph2 is ph3 when send en = 1bit adder is 0 ph1 **л** present state idle Next state af Next state after ph3 is is always sta ph4 and then afterward is idle next state ph2 idle bit adder is decremented by 1 only on the rising edge of clock during ph2 0 ⊕ **J** bit addr Cursor 1 1 615 979 ps