```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : latch_vs_flip_flop
4   -- Design      : task1
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : c:\My_Designs\lab7\task1\src\latch_vs_flip_flop.vhd
11  -- Generated   : Fri Apr 10 18:00:01 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Design to understand the differences between a latch and a
    flop flop.
18
19  -- This design maps the inputs and outputs to the the declared inputs and
    outputs in the
20
21  -- design entity to highlight the differences in the outputs of these two
    devices when
22
23  -- the same stimulator is applied to their data and clock inputs
24  --
25  ------------------------------------------------------------------------
    ----
26
27  --{{ Section below this comment is automatically maintained
28  --   and may be overwritten
29  --{entity {latch_vs_flip_flop} architecture {structural}}
30
31  library IEEE;
32  use IEEE.std_logic_1164.all;
33  library work;
34  use work.all;
35
36  entity latch_vs_flip_flop is
37       port(
38           d : in STD_LOGIC;
39           clk : in STD_LOGIC;
40           q1 : out STD_LOGIC;
41           qff : out STD_LOGIC
42           );
43  end latch_vs_flip_flop;
44
45  --}} End of automatically maintained section
46
47  architecture structural of latch_vs_flip_flop is
48  begin
49
50       u0 : entity d_latch port map (d,clk, q1);
```

```
51       u1 : entity d_flip_flop port map (d, clk, qff);
52
53  end structural;
54
```