Signal name	Value									
		200	400	600	800	1000	1200	1400		ns
rst_bar	1									
clk	1 t...									
send_en	1	240 ns								
cpha	1									
cpol	0									
dord	0									
⊞ data_in	CA			CA						
spi_rxen	1	260 ns								
txd	0									
sck	0		Each sequential value of sck corresponds to a different state. These values are identified in the design description							
ss_bar	0		ss_bar is only 1 when idle							
end_sim	fal...									
present_sta..	ph1		Next state after idle is ph1 when send_en = 1			Next state after ph2 is ph3 only when bit adder is 0				
		idle								
next_state	ph2		Next state after state 1 is always stage 2			Next state after ph3 is ph4 and then afterward is idle				
		idle								
⊞ bit_addr	0		bit adder is decremented by 1 only on the rising edge of clock during ph2							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1

Cursor 1

1 600 ns