File: C:/My_Designs/lab09/lab09/src/SPI_test_system_II.vhd *

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : SPI_test_system_II
4   -- Design      : SPI_Transmitter_and_Reciever
5   -- Author      : kenechukwu.ejinkonye@stonybrook.edu
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        :
    c:\My_Designs\Lab_09\SPI_Transmitter_and_Reciever\src\spi_tx_shifter_tb.vhd
11  -- Generated   : Sun May  3 10:51:17 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :  SPI Test System II Top Level
18  --
19  ------------------------------------------------------------------------
    ----
20
21  --{{ Section below this comment is automatically maintained
22  --   and may be overwritten
23  --{entity {spi_tx_shifter_tb} architecture {spi_tx_shifter_tb}}
24
25  library ieee;
26  use ieee.numeric_std.all;
27  use ieee.std_logic_1164.all;
28  library work;
29  use work.all;
30
31  entity SPI_test_system_II is
32      port(
33      rst_bar : in std_logic;     -- asynchronous system reset
34      clk : in std_logic;         -- system clock
35      send : in std_logic;        -- positive pulse to start transmission
36      cpol : in std_logic;        -- clock polarity setting
37      cpha : in std_logic;        -- clock phase setting
38      dord : in std_logic;        -- transmission data order 0 => msb first
39      miso : in std_logic;        -- master in slave out
40      spi_rxen : in std_logic;    -- signal to enable shift
41      data_in : in std_logic_vector(7 downto 0);      -- parallel input data
42      data_out : out std_logic_vector(7 downto 0);    -- parallel output
    data
43      mosi : out std_logic;       -- master out slave in SPI serial data
44      sck : out std_logic;        -- SPI shift clock to slave
45      ss_bar : out std_logic      -- slave select signal );
46      );
47
48
49
50
51  end SPI_test_system_II;
```

```
52
53  architecture structural of SPI_test_system_II is
54
55  signal temp_send_en : std_logic;
56  signal temp_spi_rxen : std_logic;
57
58
59
60
61
62  begin
63
64
65  -- Port Map for first two designs to structural design SPI_test_system
66  u0 : entity send_pos_edge_det port map(rst_bar => rst_bar, clk => clk,
67      send => send, send_en => temp_send_en);
68
69  u1: entity spi_tx_shifter port map(rst_bar => rst_bar, clk => clk,
70      cpol => cpol, cpha => cpha,send_en => temp_send_en, dord => dord,
71      data_in => data_in,txd => mosi,sck => sck, ss_bar => ss_bar,
72      spi_rxen  => temp_spi_rxen );
73
74
75  u2: entity spi_rx_shifter port map(rst_bar => rst_bar, clk => clk,
76      rxd => miso, dord => dord, data_out => data_out, spi_rxen  =>
    temp_spi_rxen);
77
78
79
80
81  end structural;
```