File: c:\My_Designs\lab_7_task_3\task3\src\counter.vhd *

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : counter
4   -- Design      : task3
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   --
9   ------------------------------------------------------------------------
    ----
10  --
11  -- File        : c:\My_Designs\lab_7_task_3\task3\src\counter.vhd
12  -- Generated   : Fri Apr 17 16:14:22 2020
13  -- From        : interface description file
14  -- By          : Itf2Vhdl ver. 1.22
15  --
16  ------------------------------------------------------------------------
    ----
17  --
18  -- Description : counter that iterates from 0 to 127 making a 7 bit
19  -- unsigned int, updates on rising edge of clk and when en is enabled or
    '1'
20  -- Inputs: en, rst_bar, clk
21  -- OOutput count
22  --
23  ------------------------------------------------------------------------
    ----
24
25  --{{ Section below this comment is automatically maintained
26  --   and may be overwritten
27  --{entity {counter} architecture {int_count}}
28
29  library IEEE;
30  use IEEE.std_logic_1164.all;
31  use ieee.numeric_std.all;
32
33  entity counter is
34       port(
35           en : in STD_LOGIC;
36           rst_bar : in STD_LOGIC;
37           clk : in STD_LOGIC;
38           count : out STD_LOGIC_VECTOR(6 downto 0)
39           );
40  end counter;
41
42  --}} End of automatically maintained section
43
44  architecture int_count of counter is
45
46
47  begin
48
49      cnt_int: process(clk, rst_bar)
50      variable count_int : integer range 0 to 127;
51      begin
52          if rst_bar = '0' then
```

```
53              count_int :=0;
54          elsif rising_edge(clk) and en='1' then
55              if count_int = 127 then
56                  count_int := 0;
57              else
58                  count_int := count_int + 1;
59              end if;
60          end if;
61          count <= std_logic_vector(to_unsigned(count_int,7));
62      end process;
63
64       -- enter your statements here --
65
66
67  end int_count;
68
```