```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : d_flip_flop
4   -- Design      : task1_2
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   -- Description : Design for D Flip Flop with input D and Clock and output
    Qff. If the data for
9   -- D changes state while the clock pulse is high, then output Qff follows
    input D.
10  -- The value of qff only changes on the rising edge of clock
11  ----------------------------------------------------------------------------
    ----
12
13  library IEEE;
14  use IEEE.std_logic_1164.all;
15
16  entity d_flip_flop is
17       port(
18           d : in STD_LOGIC;
19           clk : in STD_LOGIC;
20           qff : out STD_LOGIC
21           );
22  end d_flip_flop;
23
24  --}} End of automatically maintained section
25
26  architecture behavioral of d_flip_flop is
27  begin
28      process(clk)
29      begin
30          if clk'event and clk = '1' then
31              qff <= d;
32          end if;
33      end process;
34
35  end behavioral;
36
```