File: c:\My_Designs\lab_7_task_3\task3\src\mesmerize.vhd *

```
1                 ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : mesmirize
4   -- Design      : task1
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10
11  -- Generated   : Fri Apr 10 18:00:01 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :  connects
18  -- counter and pattern_gen to create the system
19  --
20  ------------------------------------------------------------------------
    ----
21
22  --{{ Section below this comment is automatically maintained
23  --   and may be overwritten
24  --{entity {latch_vs_flip_flop} architecture {structural}}
25
26  library IEEE;
27  use IEEE.std_logic_1164.all;
28  library work;
29  use work.all;
30
31  entity latch_vs_flip_flop is
32       port(
33           clk : in STD_LOGIC;
34           rst_bar : out STD_LOGIC;
35           led_array : out STD_LOGIC
36           );
37  end latch_vs_flip_flop;
38
39  --}} End of automatically maintained section
40
41  architecture structural of latch_vs_flip_flop is
42  begin
43
44      u0 : entity counter port map (clk,rst_bar);
45      u1 : entity pattern_gen port map (led_array);
46
47  end structural;
48
```