File: C:/My_Designs/Lab 8/lab8/task1/src/task2_tb.vhd *

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : task2_tb
4   -- Design      : task1_2
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   -- Description : Non-self checking testbench for spi_tx_shifter
9   ----------------------------------------------------------------------------
    ----
10
11
12  library ieee;
13  use ieee.std_logic_1164.all;
14  use ieee.numeric_std.all;
15  library work;
16  use work.all;
17
18
19  entity task2_tb is
20      -- Generic declarations of the tested unit
21
22
23
24
25  --}} End of automatically maintained section
26  end task2_tb;
27
28  architecture tb_architecture of task2_tb is
29
30
31         --stimulus signals
32      signal rst_bar : std_logic;
33      signal send : std_logic := '1';
34      signal clk : std_logic := '0';
35      signal cpha: std_logic :='0';
36      signal cpol: std_logic := '0';
37      signal data_in: std_logic_vector(7 downto 0);
38
39      --observed signals
40      signal send_en: std_logic;
41      signal txd: std_logic;
42      signal sck: std_logic;
43      signal ss_bar: std_logic;
44
45
46      constant period : time := 20ns; --need a much longer period
47                                      -- in actual hardware
48
49  begin
50      -- Unit Under Test port map
51      UUT: entity spi_tx_shifter
52      port map (
53          rst_bar => rst_bar,
54          clk => clk,
55          send_en => send_en,
```

```
56          cpha => cpha,
57          cpol => cpol,
58          data_in => data_in,
59          txd => txd,
60          sck => sck,
61          ss_bar => ss_bar
62          );
63
64      -- Port mapping for send_en from send_pos_edge_det
65      -- design to spi_tx_shifter design
66      u0 : entity send_pos_edge_det
67      port map(
68      rst_bar => rst_bar, clk => clk,
69      send_en => send_en,
70      send=>send);
71      rst_bar <= '0', '1' after period * 3;   -- reset
72
73      clock: process                      -- system clock
74      begin
75          -- clock starts at 0 for 0.5 clock periods
76          for i in 0 to 28 loop
77              wait for period;
78              clk <= not clk;             -- 28 rising edges
79              wait for period;
80          end loop;                       -- stop clock
81          std.env.finish;
82      end process;
83
84
85
86
87  end tb_architecture;
88
```