Lattice Mapping Report File for Design Module 'SPI_test_system_II'

Design Information

```
Command line:   map -a LatticeXP -p LFXP3C -t TQFP100 -s 4 -oc Commercial
     lab09_impl1.ngd -o lab09_impl1_map.ncd -pr lab09_impl1.prf -mp
     lab09_impl1.mrp -lpf
     C:/lscc/diamond/3.11_x64/bin/nt64/impl1/lab09_impl1_synplify.lpf -lpf
     C:/lscc/diamond/3.11_x64/bin/nt64/lab09.lpf -gui -msgset
     C:/lscc/diamond/3.11_x64/bin/nt64/promote.xml
Target Vendor:  LATTICE
Target Device:  LFXP3CTQFP100
Target Performance:   4
Mapper:  mg5g00,  version:  Diamond (64-bit) 3.11.2.446
Mapped on:  05/11/20  16:21:22
```

Design Summary

```
   Number of registers:     20 out of  3258 (1%)
      PFU registers:           20 out of  3072 (1%)
      PIO registers:            0 out of   186 (0%)
   Number of SLICEs:        17 out of  1536 (1%)
      SLICEs as Logic/ROM:     17 out of  1536 (1%)
      SLICEs as RAM:            0 out of   384 (0%)
      SLICEs as Carry:          0 out of  1536 (0%)
   Number of LUT4s:         25 out of  3072 (1%)
      Number used as logic LUTs:         25
      Number used as distributed RAM:     0
      Number used as ripple logic:        0
      Number used as shift registers:     0
   Number of PIO sites used: 25 out of 62 (40%)
   Number of PIO FIXEDDELAY:    0
   Number of DQSDLLs:  0 out of 2 (0%)
   Number of PLLs:  0 out of 2 (0%)
   Number of block RAMs:  0 out of 6 (0%)
   Number of GSRs:  1 out of 1 (100%)
   JTAG used :      No
   Readback used :  No
   Oscillator used :  No
   Startup used :   No
   Notes:-
      1. Total number of LUT4s = (Number of logic LUT4s) + 2*(Number of
     distributed RAMs) + 2*(Number of ripple logic)
      2. Number of logic LUT4s does not include count of distributed RAM and
     ripple logic.
   Number of clocks:  3
     Net u1.present_state[4]: 4 loads, 0 rising, 4 falling (Driver:
     u1/present_state[4] )
     Net clk_c: 8 loads, 8 rising, 0 falling (Driver: PIO clk )
     Net u1/N_52_lo: 2 loads, 2 rising, 0 falling (Driver:
     u1/present_state_RNIRO9D[0] )
   Number of Clock Enables:  0
   Number of local set/reset loads for net rst_bar_c merged into GSR:  15
   Number of LSRs:  1
     Net u1/un3_rst_bar: 2 loads, 2 LSLICEs
   Number of nets driven by tri-state buffers:  0
   Top 10 highest fanout non-clock nets:
     Net u1/bit_addr[2]: 9 loads

     Net dord_c: 8 loads
     Net u1/bit_addr[1]: 7 loads
     Net u1/bit_addr[0]: 6 loads
     Net u1/present_state[2]: 6 loads
     Net temp_send_en: 4 loads
     Net data_out_c[1]: 3 loads
     Net data_out_c[2]: 3 loads
     Net data_out_c[3]: 3 loads
     Net data_out_c[4]: 3 loads




   Number of warnings:  3
   Number of errors:    0
```

Design Errors/Warnings

```
WARNING - map: Using local reset signal 'rst_bar_c' to infer global GSR net.
WARNING - map: IO buffer missing for top level port cpha...logic will be
     discarded.
WARNING - map: IO buffer missing for top level port spi_rxen...logic will be
     discarded.
```

IO (PIO) Attributes

IO Name	Direction	Levelmode IO_TYPE	IO Register	FIXEDDELAY
data_out[0]	OUTPUT	LVCMOS25		
rst_bar	INPUT	LVCMOS25		
ss_bar	OUTPUT	LVCMOS25		
sck	OUTPUT	LVCMOS25		
mosi	OUTPUT	LVCMOS25		
data_out[7]	OUTPUT	LVCMOS25		
data_out[6]	OUTPUT	LVCMOS25		
data_out[5]	OUTPUT	LVCMOS25		

data_out[5]	OUTPUT	LVCMOS25		
data_out[4]	OUTPUT	LVCMOS25		
data_out[3]	OUTPUT	LVCMOS25		
data_out[2]	OUTPUT	LVCMOS25		
data_out[1]	OUTPUT	LVCMOS25		
data_in[7]	INPUT	LVCMOS25		
data_in[6]	INPUT	LVCMOS25		
data_in[5]	INPUT	LVCMOS25		
data_in[4]	INPUT	LVCMOS25		
data_in[3]	INPUT	LVCMOS25		
data_in[2]	INPUT	LVCMOS25		
data_in[1]	INPUT	LVCMOS25		
data_in[0]	INPUT	LVCMOS25		
miso	INPUT	LVCMOS25		
dord	INPUT	LVCMOS25		
cpol	INPUT	LVCMOS25		
send	INPUT	LVCMOS25		
clk	INPUT	LVCMOS25		

Removed logic

Block VCC undriven or does not drive anything - clipped.
Block GND undriven or does not drive anything - clipped.
Block u0/GND undriven or does not drive anything - clipped.
Block u0/VCC undriven or does not drive anything - clipped.
Block u1/GND undriven or does not drive anything - clipped.
Block u1/VCC undriven or does not drive anything - clipped.
Block u2/GND undriven or does not drive anything - clipped.
Block u2/VCC undriven or does not drive anything - clipped.
Signal rst_bar_c_i was merged into signal rst_bar_c
Signal u2/CN was merged into signal u1.present_state[4]
Signal VCC undriven or does not drive anything - clipped.
Block rst_bar_pad_RNI1JBB was optimized away.
Block u2/g_1_.CN was optimized away.

GSR Usage

GSR Component:
The local reset signal 'rst_bar_c' of the design has been inferred as Global Set Reset (GSR). The reset signal used for GSR control is 'rst_bar_c'.

GSR Property:
The design components with GSR property set to ENABLED will respond to global set reset while the components with GSR property set to DISABLED will not.

Run Time and Memory Usage

Total CPU Time: 0 secs
Total REAL Time: 0 secs
Peak Memory Usage: 27 MB