File: C:/My_Designs/Lab 8/lab8/task1/src/SPI_test_system_I.vhd *

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : SPI_test_system
4   -- Design      : task1_2
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   -- Description : The top-level structure simply combines the two previous
    entities
9   -- send_pos_edge_det and spi_tx_shifter.
10  -- List of Circuit Features to be verified:
11  -- Inputs: rst_bar, clk, send, cpol, cpha, data_in
12  -- Outputs: mosi, sck, ss_bar
13  -- Observant Stimulus: Presennt State, Next State
14  ------------------------------------------------------------------------
    ----
15
16  library IEEE;
17  use IEEE.std_logic_1164.all;
18  library work;
19  use work.all;
20
21  entity SPI_test_system_I is
22      port(
23      rst_bar : in std_logic;     -- asynnchronous system reset
24      clk : in std_logic;         -- system clock
25      send : in std_logic;        -- debounced send input
26      cpol : in std_logic;        -- clock poolarity settinng
27      cpha : in std_logic;        -- clock phase setting
28      data_in : in std_logic_vector(7 downto 0);  -- parallel input data
29      mosi: out std_logic;        -- master out slave in SPI serial data
30      sck: out std_logic;         -- SPI shift clock to slave
31      ss_bar : out std_logic      -- SPI shift clock to slave
32      );
33  end SPI_test_system_I;
34
35  architecture structural of SPI_test_system_I is
36
37  signal temp_send_en : std_logic;
38
39  begin
40
41
42  -- Port Map for first two designs to structural design SPI_test_system
43  u0 : entity send_pos_edge_det port map(rst_bar => rst_bar, clk => clk,
44      send => send, send_en => temp_send_en);
45
46  u1: entity spi_tx_shifter port map(rst_bar => rst_bar, clk => clk,
47      cpol => cpol, cpha => cpha, data_in => data_in, sck => sck,
48      ss_bar => ss_bar, send_en => temp_send_en, txd => mosi);
49
50
51
52
53  end structural;
```