Signal name	Value										
rst_bar	0										
clk	0	set by amending period									
cpol	0										
cpha	0										
data_in	AA				AA						
send	1										
mosi	1										
sck	0	sent to 0 due to send_en being 0									
presen...	idle									ends at 001 so it doesnt go back	
		idle	ph2	ph1	ph2	ph1	ph2	ph1	ph2	ph1	ph2	ph1	ph2
bit_addr	7	7	6	5	4	3	2	1
ss_bar	1										
next_st...	ph2	ph2	ph1	ph2	ph1	ph2	ph1	ph2	ph1	ph2	ph1	ph2	ph1
send_er	0										

Cursor 1   0 fs