File: c:\My_Designs\lab_7_task_3\task3\src\pattern_gen.vhd *

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : part2
4   -- Design      : Lab_07
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   --
9   ----------------------------------------------------------------------------
    ----
10  --
11  -- File        :
    C:\Users\kenej\OneDrive\Designs\Lab_07\Lab_07\src\part2.vhd
12  -- Generated   : Fri Apr 17 14:01:18 2020
13  -- From        : interface description file
14  -- By          : Itf2Vhdl ver. 1.22
15  --
16  ----------------------------------------------------------------------------
    ----
17  --
18  -- Description : table takes input data from the nubmer it grabs from the
    counter.
19  --it takes the number and turns it into unsigned vector and uses that for
    table lookup
20  --
21  -- Input: pat_num, b0,b1,b2,b3,b4,b5,b6
22  -- Output: led_array
23
24  ----------------------------------------------------------------------------
    ----
25
26  --{{ Section below this comment is automatically maintained
27  --   and may be overwritten
28  --{entity {part2} architecture {part2}}
29  library ieee;
30  use IEEE.std_logic_1164.all;
31  use  ieee.numeric_std.all;
32
33
34  entity pattern_gen is
35      port(
36      pat_num : in STD_LOGIC;
37      b0,b1,b2,b3,b4,b5,b6 : in STD_LOGIC;
38      led_array : out std_logic_vector(6 downto 0)
39      );
40  end pattern_gen;
41
42  --}} End of automatically maintained section
43
44  architecture table_lookup of pattern_gen is
45      signal place_holder: STD_LOGIC_VECTOR(6 downto 0);
46
47
48      type lookup_table is array (0 to 6) of std_logic_vector(6 downto 0);
49      constant table: lookup_table :=
50      ("1000001", "0100010", "0010100", "0001000", "0010100", "0100010",
    "1000001");
```

```
51
52  begin
53
54
55
56      p1: process (place_holder)
57
58      variable temp : integer;
59      begin
60
61          place_holder <= (b6,b5,b4,b3,b2,b1,b0);
62          temp := to_integer(unsigned(place_holder));
63          place_holder <= std_logic_vector(to_unsigned(temp,7));
64          led_array <= table(to_integer(unsigned(place_holder)));
65
66      end process;
67
68
69  end table_lookup;
70
```