File: C:\My_Designs\Lab 8\lab8\task1\src\task3_tb.vhd *

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : task3_tb
4   -- Design      : task1_2
5   -- Author      : Ishabul Haque and Ken Ejinkonye
6   -- Company     : Stony Brook
7   --
8   -- Description : Non self checking test bench for SPI_test_system
9   ------------------------------------------------------------------------
    ----
10
11
12  library ieee;
13  use ieee.std_logic_1164.all;
14  use ieee.numeric_std.all;
15  library work;
16  use work.all;
17
18
19
20  entity task3_tb is
21      -- Generic declarations of the tested unit
22
23
24
25
26  --}} End of automatically maintained section
27  end task3_tb;
28
29  architecture tb_architecture of task3_tb is
30
31
32         --stimulus signals
33      signal rst_bar : std_logic;
34      signal send : std_logic := '1';
35      signal cpha : std_logic;
36      signal cpol: std_logic;
37      signal clk : std_logic := '0';
38
39      signal data_in: std_logic_vector(7 downto 0);
40
41      --observed signals
42      signal send_en: std_logic;
43      signal txd: std_logic;
44      signal sck: std_logic;
45      signal ss_bar: std_logic;
46      signal present_state:std_logic;
47      signal next_state:std_logic;
48      signal mosi : std_logic;
49
50      constant period : time := 20ns; --need a much longer period
51                                      -- in actual hardware
52
53  begin
54      -- Unit Under Test port map
55
```

```
56      u0 : entity send_pos_edge_det port map(rst_bar => rst_bar, clk => clk,
57      send => send, send_en => send_en);
58
59      u1: entity spi_tx_shifter port map(rst_bar => rst_bar, clk => clk,
60      cpol => cpol, cpha => cpha, data_in => data_in, sck => sck,
61      ss_bar => ss_bar, send_en => send_en, txd => mosi);
62
63      rst_bar <= '0', '1' after period * 3;   -- reset
64
65      clock: process              -- system clock
66      begin
67                      -- clock starts at 0 for 0.5 clock periods
68          for i in 0 to 28 loop
69              wait for period;
70              clk <= not clk;     -- 15 rising edges
71              wait for period;
72          end loop;                   -- stop clock
73          std.env.finish;
74      end process;
75
76      snd: process
77      begin
78          for i in 0 to 28 loop      --28 rising edges
79              wait for 200ns;        -- Send pulse duration of 200ns
80              send <= not send;
81          end loop;                  --end pulse
82
83          std.env.finish;
84          end process;
85
86
87
88  end tb_architecture;
89
```