File: C:\My_Designs\task2\src\dff_en.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : dff_en
4   -- Design      : Design Task 2: D flip-flop with Enable Input
5   -- Author      : Ishabul Haque
6   -- Company     : Ken Ejinkonye
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : c:\My_Designs\task2\src\dff_en.vhd
11  -- Generated   : Fri Apr 10 18:16:18 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Design for D flip-flop with Enable Input. Input for the
    design are d, clk, en
18  -- and rst_bar. Output is q. When rst_bar is asserted, the flip-flop is
    cleared. When rst_bar
19  -- is not asserted and en is asserted, the flip-flop stores its input data
    on a rising clock edge.
20  -- When that condition is met, the output of the flip flop will be equal to
    the input data
21  -- which was stored by the flip flop earlier.
22  ------------------------------------------------------------------------
    ----
23
24  --{{ Section below this comment is automatically maintained
25  --   and may be overwritten
26  --{entity {dff_en} architecture {behavioral}}
27
28  library IEEE;
29  use IEEE.std_logic_1164.all;
30
31  entity dff_en is
32       port(
33           d : in STD_LOGIC;
34           clk : in STD_LOGIC;
35           en : in STD_LOGIC;
36           rst_bar : in STD_LOGIC;
37           q : out STD_LOGIC
38           );
39  end dff_en;
40
41  --}} End of automatically maintained section
42
43  architecture behavioral of dff_en is
44  begin
45
46       process(clk, rst_bar)
47      begin
48      if rst_bar = '1' then
49
```

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```
50              q <= '0';
51
52      elsif rst_bar = '0' then
53          if rising_edge(clk) then
54              if en = '1' then
55                  q <= d;
56              end if;
57          end if;
58          end if;
59          end process;
60
61  end behavioral;
62
```