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3  -- Title      : send_pos_edge_det_tb
4  -- Design     : task1_2
5  -- Author     : Ishabul Haque and Ken Ejinkonye
6  -- Company    : Stony Brook
7  --
8  -- Description : Non self checking testbench for send_pos_edge_det design.
9  --
10 -----
11 ---
12
13 library ieee;
14 use ieee.std_logic_1164.all;
15 use ieee.numeric_std.all;
16 library work;
17 use work.all;
18
19
20
21 entity send_pos_edge_det_TB is
22
23
24 end send_pos_edge_det_TB;
25
26 architecture tb_architecture of send_pos_edge_det_TB is
27
28
29     --stimulus signals
30     signal rst_bar : std_logic;
31     signal send : std_logic;
32     signal clk : std_logic;
33     --observed signals
34     signal send_en : std_logic;
35
36     constant period : time := 20ns; --need a much longer period
37                                     -- in actual hardware
38
39 begin
40     -- Unit Under Test port map
41     UUT: entity send_pos_edge_det
42     port map (
43         clk => clk,
44         rst_bar => rst_bar,
45         send => send,
46         send_en => send_en
47     );
48
49     rst_bar <= '0', '1' after period; -- reset
50
51     clock: process -- system clock
52     begin
53         -- clock starts at 0 for 0.5 clock periods
54         for i in 0 to 28 loop
55             wait for period;
```

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56         clk <= not clk;           -- 28 rising edges
57         wait for period;
58     end loop;                       -- stop clock
59     std.env.finish;
60 end process;
61
62 -- Duration of signal send is 200ns at a high value
63 snd: process
64 begin
65     for i in 0 to 28 loop          --28 rising edges
66         wait for 200ns;            -- Send pulse duration of 200ns
67         send <= not send;
68     end loop;                      --end pulse
69
70     std.env.finish;
71 end process;
72
73 end tb_architecture;
74
```