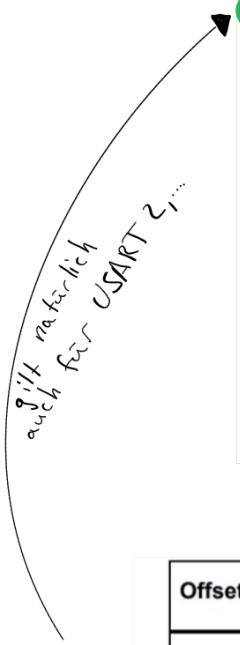
Table 1. Low and medium-density device register boundary addresses

Boundary address	Peripheral	Bus	Register map
0x4002 3000 - 0x4002 33FF	CRC	AHB	*Section 3.4.4 on page 49*
0x4002 2400 - 0x4002 2FFF	Reserved		-
0x4002 2000 - 0x4002 23FF	Flash memory interface		-
0x4002 1400 - 0x4002 1FFF	Reserved		-
0x4002 1000 - 0x4002 13FF	Reset and clock control RCC		*Section 6.3.12 on page 101*
0x4002 0400 - 0x4002 0FFF	Reserved		-
0x4002 0000 - 0x4002 03FF	DMA1		*Section 9.4.7 on page 159*
0x4001 4C00 - 0x4001 FFFF	Reserved	APB2	-
0x4001 4800 - 0x4001 4BFF	TIM17 timer		*Section 15.6.16 on page 454*
0x4001 4400 - 0x4001 47FF	TIM16 timer		*Section 15.6.16 on page 454*
0x4001 4000 - 0x4001 43FF	TIM15 timer		*Section 15.5.18 on page 434*
0x4001 3C00 - 0x4001 3FFF	Reserved		-
0x4001 3800 - 0x4001 3BFF	USART1		*Section 23.6.8 on page 646*
0x4001 3400 - 0x4001 37FF	Reserved		-
0x4001 3000 - 0x4001 33FF	SPI1		*Section 21.4.8 on page 565*
0x4001 2C00 - 0x4001 2FFF	TIM1 timer		*Section 12.4.21 on page 282*
0x4001 2800 - 0x4001 2BFF	Reserved		-
0x4001 2400 - 0x4001 27FF	ADC1		*Section 10.11.15 on page 188*
0x4001 1C00 - 0x4001 23FF	Reserved		-
0x4001 1800 - 0x4001 1BFF	GPIO Port E		*Section 7.5 on page 130*
0x4001 1400 - 0x4001 17FF	GPIO Port D		*Section 7.5 on page 130*
0x4001 1000 - 0x4001 13FF	GPIO Port C		*Section 7.5 on page 130*
0x4001 0C00 - 0x4001 0FFF	GPIO Port B		*Section 7.5 on page 130*
0x4001 0800 - 0x4001 0BFF	GPIO Port A		*Section 7.5 on page 130*
0x4001 0400 - 0x4001 07FF	EXTI		*Section 8.3.7 on page 143*
0x4001 0000 - 0x4001 03FF	AFIO		*Section 7.5 on page 130*



32 bit

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	USART_SR	Reserved																						CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NF	FE	PE
	Reset value																							0	0	1	1	0	0	0	0	0	0
0x04	USART_DR	Reserved																								DR[8:0]							
	Reset value																									0	0	0	0	0	0	0	0
0x08	USART_BRR	Reserved																DIV_Mantissa[15:4]												DIV_Fraction [3:0]			
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	USART_CR1	Reserved																						OVER8	Reserved	UE	M	WAKE	PCE	PS	PEIE	TXEIE	TCIE	RXNEIE	IDLEIE	TE	RE	RWU	SBK
	Reset value																							0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	USART_CR2	Reserved																							LINEN	STOP [1:0]		CLKEN	CPOL	CPHA	LBCL	Reserved	LBDIE	LBDL	Reserved	ADD[3:0]			
	Reset value																								0	0	0	0	0	0	0		0	0		0	0	0	0
0x14	USART_CR3	Reserved																										ONEBIT	CTSIE	CTSE	RTSE	DMAT	DMAR	SCEN	NACK	HDSEL	IRLP	IREN	EIE
	Reset value																											0	0	0	0	0	0	0	0	0	0	0	0
0x18	USART_GTPR	Reserved																						GT[7:0]								PSC[7:0]						
	Reset value																							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

relativ zur Basisadresse

default value
"volatile"

name of a group of bits

32bit-Architektur → 2^{32} Adressraum

kleinste adressierbare Adresse

0x 0000 0000	8-bit Daten
0x 0000 0001	8-bit Daten
0x 0000 0002	8-bit Daten
0x 0000 0003	8-bit Daten
0x 0000 0004	...

32bit