Tisha Mudgal

CSCI 3130

Homework 9

Due: Apr. 4, 10:00 PM

1. (1 point) Will your RSC's Control Unit be **hardwired** or **microprogrammed**?

   hardwired

2. (2 points) What is the **key principle** that cache memory utilizes to increase CPU throughput?

   locality of reference

3. (2 points) A system with a 1K x 8 **main memory** has a 32 x 4 **cache**, therefore each address contains __5__ -bits for specifying the cache block, __3__ -bits for specifying the tag, and 2-bits for specifying the offset.

4. (2 points) A system with a 64M x 32 **main memory** has a 2K x 64 **cache**, therefore each address contains 11-bits for specifying the cache block, __9__ -bits for specifying the tag, and __6__ -bits for specifying the offset.

5. (2 points) A system with a 16K x 64 **main memory** has a 1K x 2 **cache**, therefore each address contains __10__ -bits for specifying the cache block, 3-bits for specifying the tag, and __1__ -bits for specifying the offset.

6. (1 point each) Determine if the following CPU address requests are cache **hits** or **misses**. If it is a hit, then provide the **value** stored at that location as well.

   a. 10110010 Miss

   b. 11110111 Hit 8

   c. 11111010 Miss

   d. 10010000 Miss

   e. 00001011 hit 3

   f. 01100001 hit 35

8 x 2 Cache

Block	Tag	$Word_0$	$Word_1$
000	0110	102	35
001	1001	25	21
010	1110	87	67
011	1111	8	8
100	1111	11	25
101	0000	108	3
110	0101	65	66
111	1001	0	0