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CSCI 3130

Homework 8

Due: Mar. 23, 10:00 PM

1. (2 points) Which register is wired directly (not using the bus) to the memory module in the RSC?

   AR

2. (2 points) What 3 values will the sequence counter (SC) cycle through during the FETCH portion of the RSC instruction cycle?

   t_0 t_1 t_2

3. (2 points each) The Z register is never mentioned in the RTL Microcode specification, which brings up the following questions:
   a. Under what condition is the Z register updated?

      when ACC is changed

   b. When Z is updated, under what condition would it be set to zero?

      when ACC is 1

   c. When Z is updated, under what condition would it be set to one?

      when ACC = 0

4. (5 points) Draw a simple circuit that implements the following RTL instruction assuming right hand side variables refer to 4-bit registers.

   A: X ← Y, Z ← Y

   A': Y ← X

a