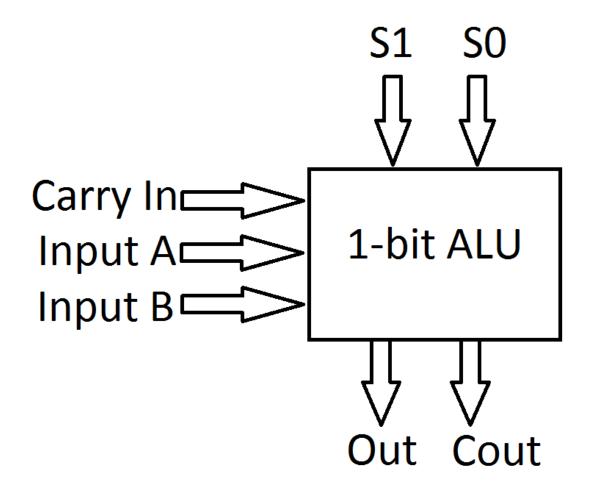
# ECE 451 LAB REPORT

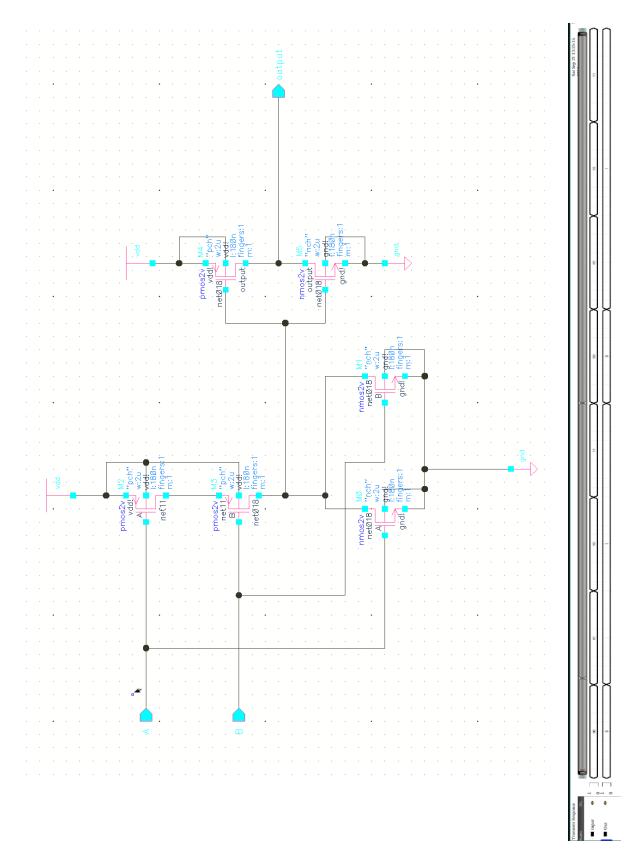
Digital System Design

#### Design Of 1-Bit ALU slice:

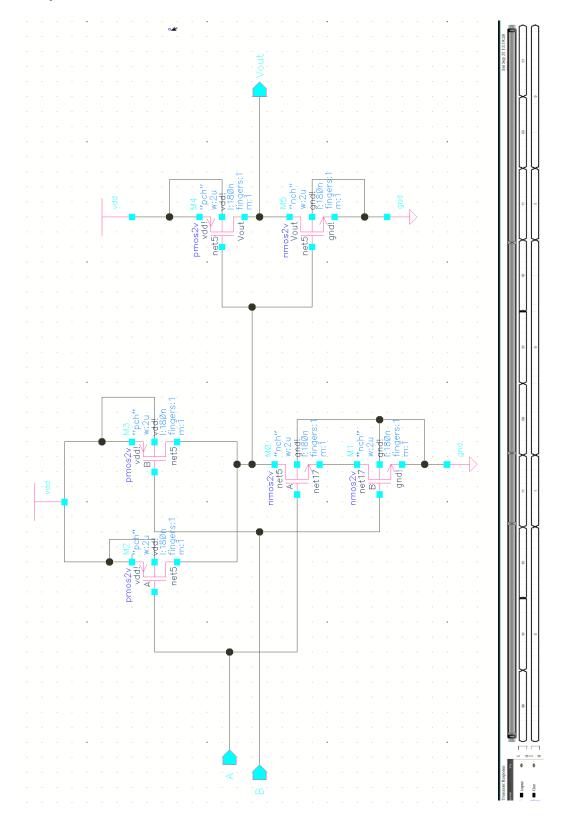


| <b>S1</b> | S0 | Function   |
|-----------|----|------------|
| 0         | 0  | ADD        |
| 0         | 1  | SUBTRACT   |
| 1         | 0  | XOR        |
| 1         | 1  | Left Shift |

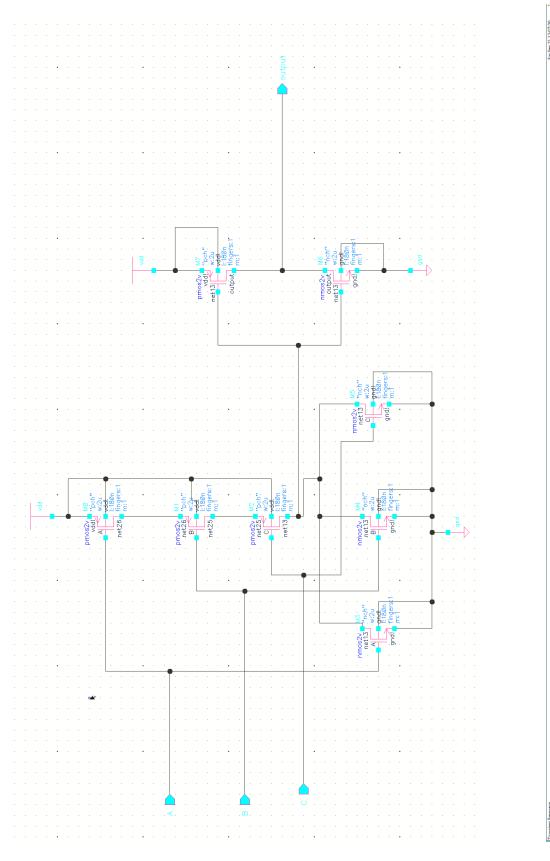
# 2 Input OR schematic with Waveform



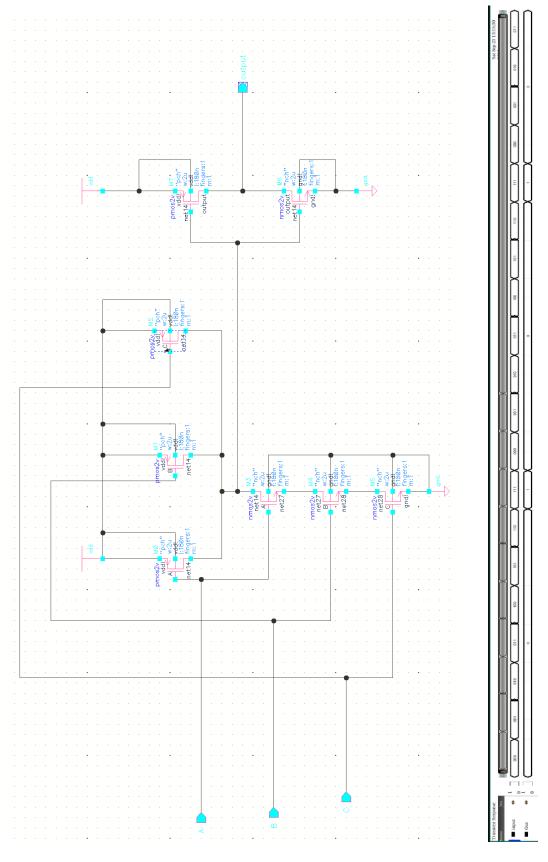
# 2 Input AND schematic with Waveform



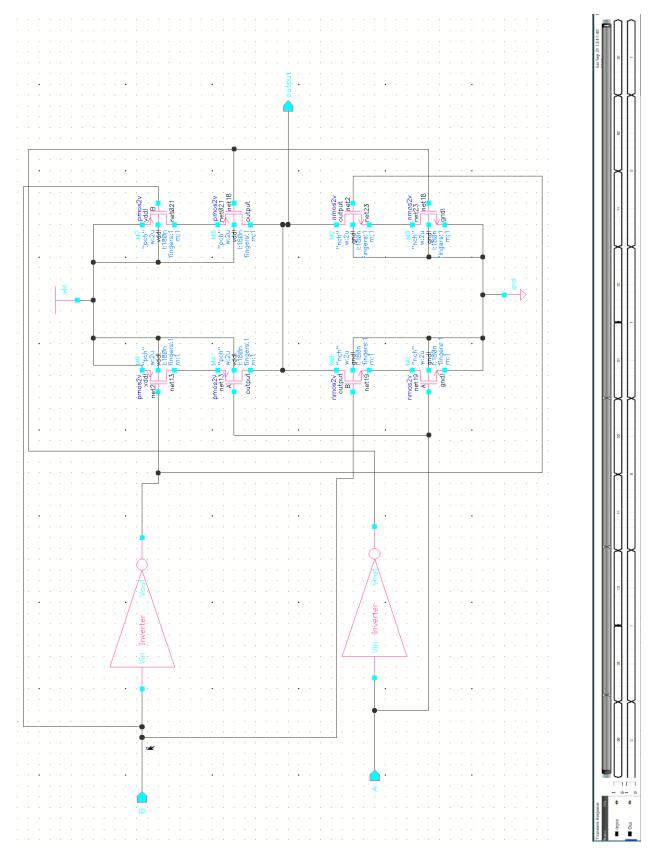
## 3 Input OR schematic with Waveform



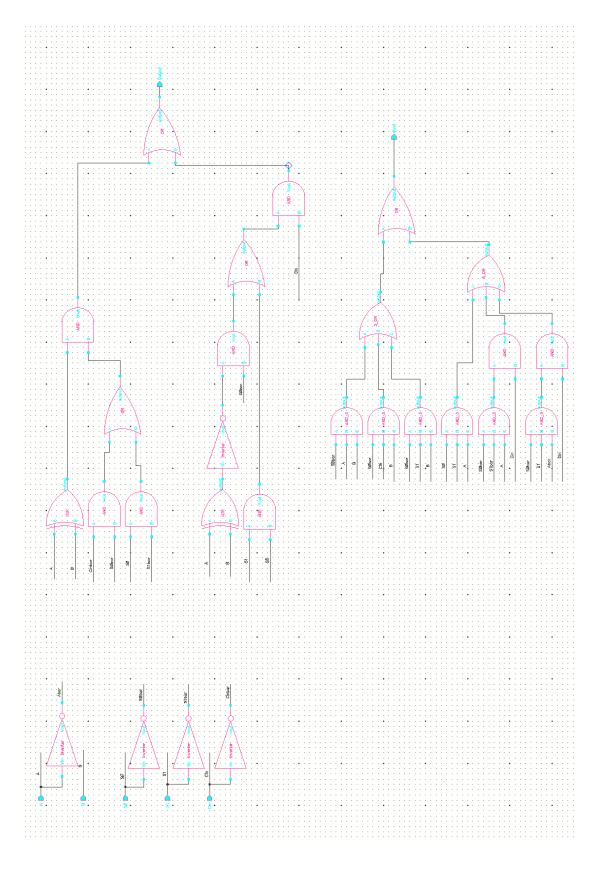
# **3 Input AND schematic with Waveform**



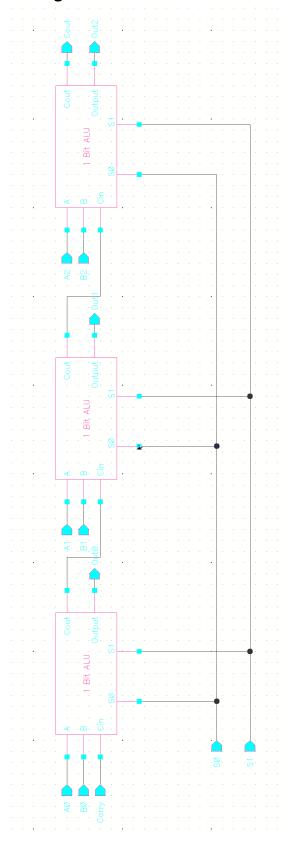
## 2 Input XOR schematic with Waveform



# **Schematic of 1-Bit ALU slice using Cadence**



Design of 3-Bit ALU using 1-Bit slice



### 3 bit ALU Waveforms

| Transient Response  |      | \$41.540.00 1   |
|---|------|---|
| Input A • Input B • Input |      |   |
| od.   |      |   |
| Carry In Carry Out Output   |      | 0 11 10 00 00 110 00 00 111   |
| Transfert Response  Vis  Input A  Input B  Select  Carry in   |      | Company   Comp    |
| □ Carry Out   |      | 000   100   011   111   101   000   111   111   101   010   111   1 |
| Transient Response  Vis  Input A  Input B  Select  Carry in   |      | Coop       |
| Output •  | <br> |   |

#### **Conclusion:**

Hence, I have implemented 3 bit ALU using 1 bit ALU slices in Cadence.

#### **Questions:**

- 1. Hierarchical design is basically dividing a design into multiple blocks (sometimes referred to as sub-chips, sub-blocks, modules, hierarchical blocks, etc.
- 2. Advantages of a hierarchical design:
  - a. The hierarchical design helps us to work on blocks separately and in parallel from RTL through physical implementations.
  - b. Working with smaller blocks results in the tool run time being shorter and less complex.
  - c. In case of any timing issue, we can fix individual blocks relatively easily.