LAB #1: THREE-BIT ALU (Cadence)

Due: at the beginning of your registered lab section between Sep 16 and Sep 20

Objective:

- The objective of this lab is to design a bit slice 3-bit Arithmetic Logic Unit (ALU) using Cadence as well as using hierarchical design principles.

Lab Description and Specs:

- **Function:**
  - Three-bit addition, subtraction, XOR (bitwise between A and B), and 3-bit shift-left (on A; shift in zero at the least significant bit).

- **Inputs:**
  - *fun_sel0* and *fun_sel1*: Selects one of the four functions.
    ain[2:0] and *bin[2:0]*: Inputs for the two 3-bit numbers or one 3-bit number.
- **Outputs:**
  - *out[2:0]*: The three-bit number that is the result of the ALU operation.

Recommended Procedures:

- For this lab you will use logic synthesis to design a *1-bit* ALU block that performs the *four functions* on two one-bit inputs. You will then *cascade* three of these blocks together to form the 3-bit ALU along with the control decoding logic and the output decoding block.

  a. Write out the truth table to perform the 1-bit ALU and perform the logic minimization process to obtain the minimum Boolean equations.
  b. Map the Boolean equations to a schematic sheet using CADENCE.
  c. Run Cadence to verify the functionality of the 1-bit ALU block by applying every combination of inputs like those in the truth table.
  d. Check the sheet prior to making a symbol. Make a symbol for the 1-bit ALU using CADENCE.
  e. Open a new schematic sheet. Cascade three 1-bit ALUs to form a 3-bit ALU.
  f. Check the sheet prior to making a symbol. Make a new symbol for the 3-bit ALU. Note that the data ports should now be 3-bit wide bus.

Prelab:

- Truth table and equations for 1-bit ALU.
- Paper Logic Schematic of 1-bit ALU.
- Paper Schematic of 3-bit ALU, using 1-bit slices.

Questions:

- Discuss what is a hierarchical design.
- Discuss the advantages of a hierarchical design such as what was accomplished in this lab.