LAB #4: Blinkenlights (Cadence and Verilog)

Due: at the beginning of your registered lab section between 28 OCT and 1NOV

Objective:

- Use hierarchical design to create complex circuits
- Understand the design and function of a ROM and Decoder
- blinkenlights!

Lab Description and Specs:

Cadence:

Use a 7xN ROM to write an English word or phrase at least 5 ASCII characters long to the output.

Inputs:

char_select[$\log_2$(N)-1:0]: Selects the character to output

Outputs:

char_out [6:0]: The character output

Verilog:

Use a ROM to display a sequence of frames to an 8x8 LED matrix. You must use at least 4 different frames. You will be provided with a clock divider module to help with timing. The frame rate should be 0.25 Hz at the slowest. (4 seconds per frame). You may make the frame rate as fast as necessary, so long as it is apparent that you are using multiple frames. As a guideline, 8-15 Hz should be sufficient for a simple animation.

Inputs:

clock50MHz: The internal 50MHz clock

run: If run is high, the frames should cycle normally. If run is low, the cycle should be paused, but continue displaying the current frame.

reset: Reset the sequence to the first frame.

Outputs:

row[7:0]: Row select for the display unit

column[7:0]: Column select for the display unit

The LED Matrix is common Cathode, meaning to rows are connected to the cathode of a group of LEDs, and the columns are connected to the anode of a group of LEDs. This means that rows are active low and columns are active high. For example, applying 0b00011000 to the column input and 0b11100111 to the row input will illuminate the 4 central diodes, as shown in Figure 1.

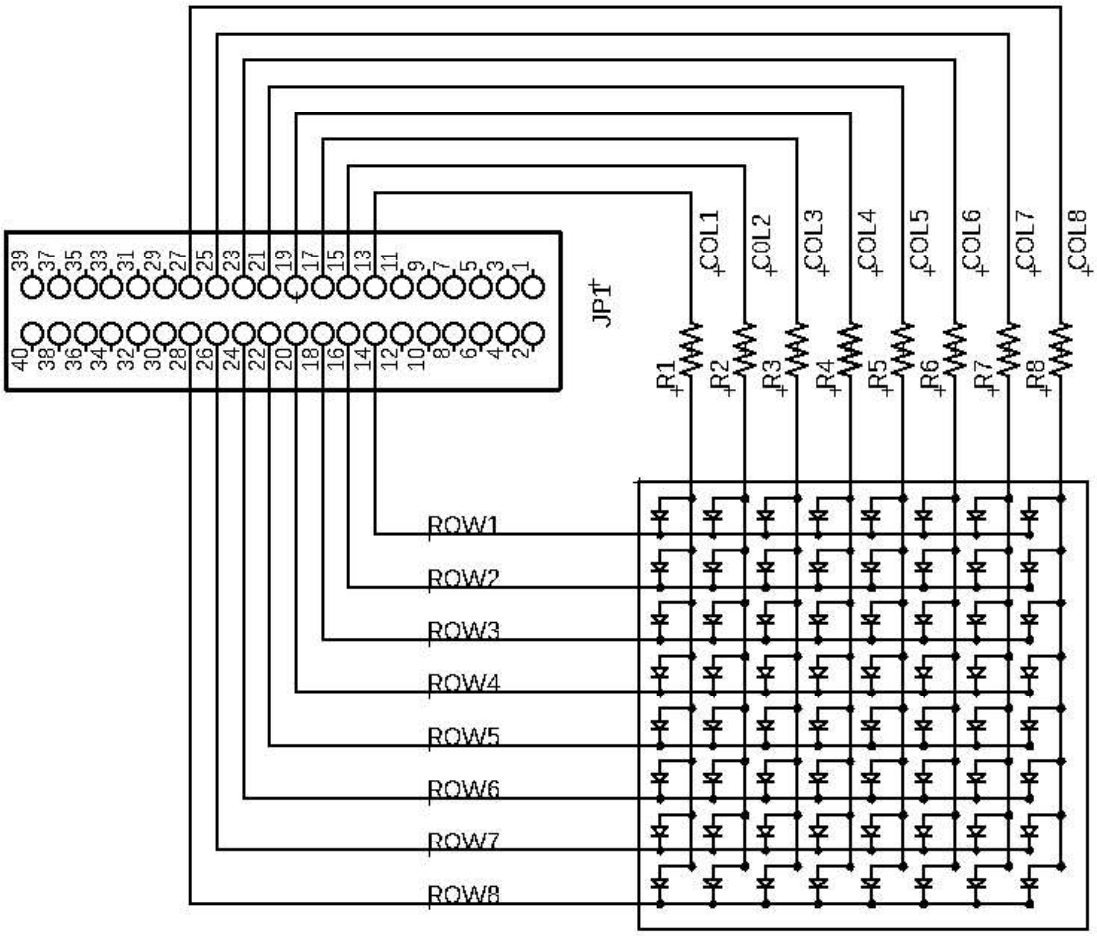

Figure 1: LED Grid example

It is impossible to individually address an arbitrary set of pixels on the whole display at once. To display a single frame, you must quickly cycle through individual rows and take advantage persistence of vision. This is a phenomenon where an image is still perceived even after the source of the image no longer exists. This is commonly used in televisions and monitors, though not implemented exactly as will be done in this lab.
To create a sequence of frames, you simply need to cycle through a sequence of frames stored in the ROM.

Connect the LED display to GPIO 1. With the switches facing you, pin 1 is the top left pin on the DE0 CV board. Pin 1 of the LED grid is marked with a small box around the pin.

Number	1	2	3	4	5	6	7	8
Row	PIN_R22	PIN_T22	PIN_N19	PIN_P19	PIN_P17	PIN_M18	PIN_L17	PIN_K17
Column	PIN_N21	PIN_R21	PIN_N20	PIN_M22	PIN_L22	PIN_P16	PIN_L18	PIN_L19

Recommended Procedures:

Cadence

1) Create a 7-bit ROM. Each word line is a single printable ASCII character (see http://www.asciitable.com).
2) Create a 1:2 decoder.
3) Use hierarchical design starting with the 1:2 decoder to create a $\lceil \log_2 N \rceil - 1 : N$ decoder, able to address each line your ROM.
4) Connect the decoder and ROM.
5) Simulate the circuit to verify the message is correctly generated at the output.

Verilog:

1) Create a ROM module containing the frames you will display
2) Use the provided clock divider module to create a clock for selecting rows
3) Use the provided clock divider module to create a clock for selecting frames
4) Use the frame clock to select the current frame in the ROM
5) Use the row clock to select the current row in the ROM
6) Use the output of the ROM for the column output
7) Use the row number to generate the row output (remember rows are active low)
8) Assign pins and program the board.
9) Enjoy the fruits of your labor

Prelab:

Week 1 (Cadence):

- Truth table for 1:2 decoder
- CMOS design for 1:2 decoder
- Modular design for 3:8 decoder consisting of multiple 1:2 decoders

Week 2 (Verilog):

- 8x8 image to be written to the LED matrix

Questions:

- Discuss the concept and advantages of hierarchical design.
- How was hierarchical design utilized in this lab?