LAB #5: GREY CODE COUNTER(Cadence)

Due: at the beginning of your registered lab section between Nov 4 and Nov 8

Objective:

- The objective of this lab is to learn simple sequential logic circuit design and verification using schematic capture and digital simulation tools.

Lab Description and Specs:

- **Function:**
  - Design a 3-bit grey code counter. The counting sequence for grey code is 000, 001, 011, 010, 110, 111, 101, 100. Use D-FFs to implement the counter.

- **Inputs:**
  - *clock*: Clock signal

- **Outputs:**
  - *o[2:0]*: Grey code outputs

Recommended Procedures:

a. Draw the state transition diagram for the grey code counter.
b. Map unused states to the initial count of 000.
c. Translate the state transition diagram into a state transition table.
d. Generate a truth table for each D-FF input.
e. Obtain the Boolean equations from the truth table.
f. Draw the corresponding schematic diagram in Cadence.
g. Run Cadence to simulate and verify the functionality of the counter.

Prelab:

a. State Transition Diagram
b. State Transition Table
c. Truth Tables
d. Boolean Equations
e. Paper Schematic Drawing

Questions:

- What is Moore Finite State Machine (FSM)?
- What is Mealy FSM?