ECE 451 LAB 5

Gray Code Counter

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Objective:

The objective of this lab is to learn simple sequential logic circuit design and verification using schematic capture and digital simulation tools.

Lab Description and Specs:

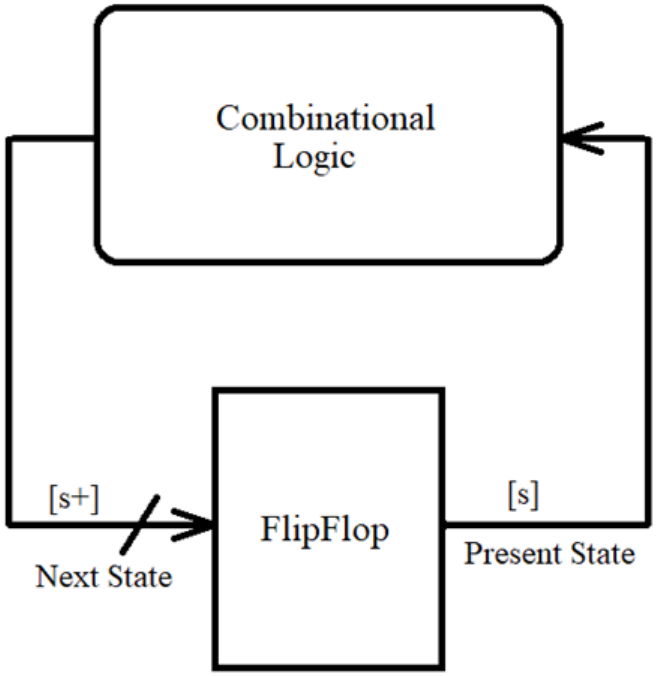
- Function:
  Design a 3 bit grey code counter. The counting sequence for grey code is 000, 001, 011, 010, 110, 111, 101, and 100.
  Use D-FFs to implement the counter.
- Inputs: clock: Clock signal
- Outputs: [2:0]: Grey code outputs

Introduction:

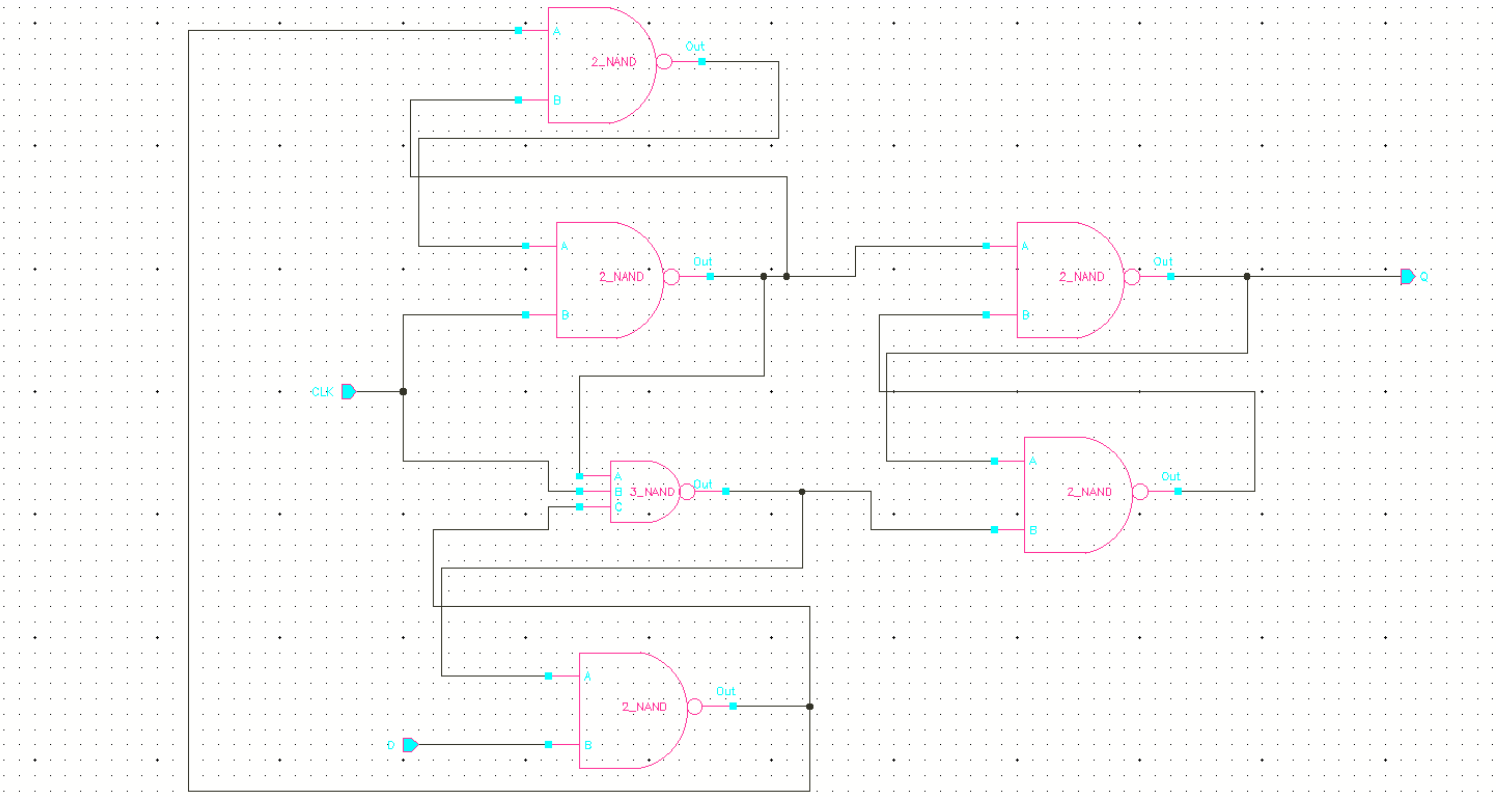
A gray code is encoding of numbers in binary values, such that the adjacent numbers have a difference of a single digit, i.e. they differ by 1.

BINARY	GREY CODE
000	001
001	011
011	010
010	110
110	111
111	101
101	100
100	000

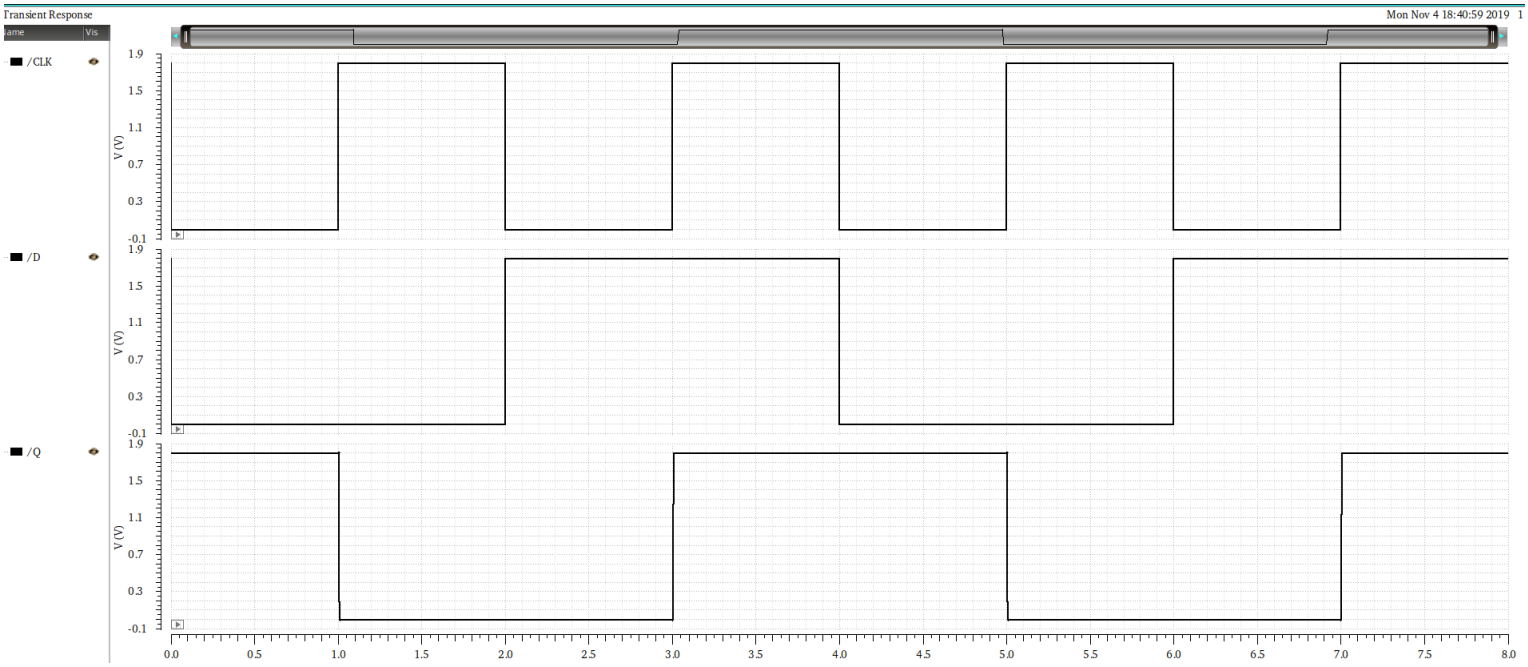
The basic design is as follows:



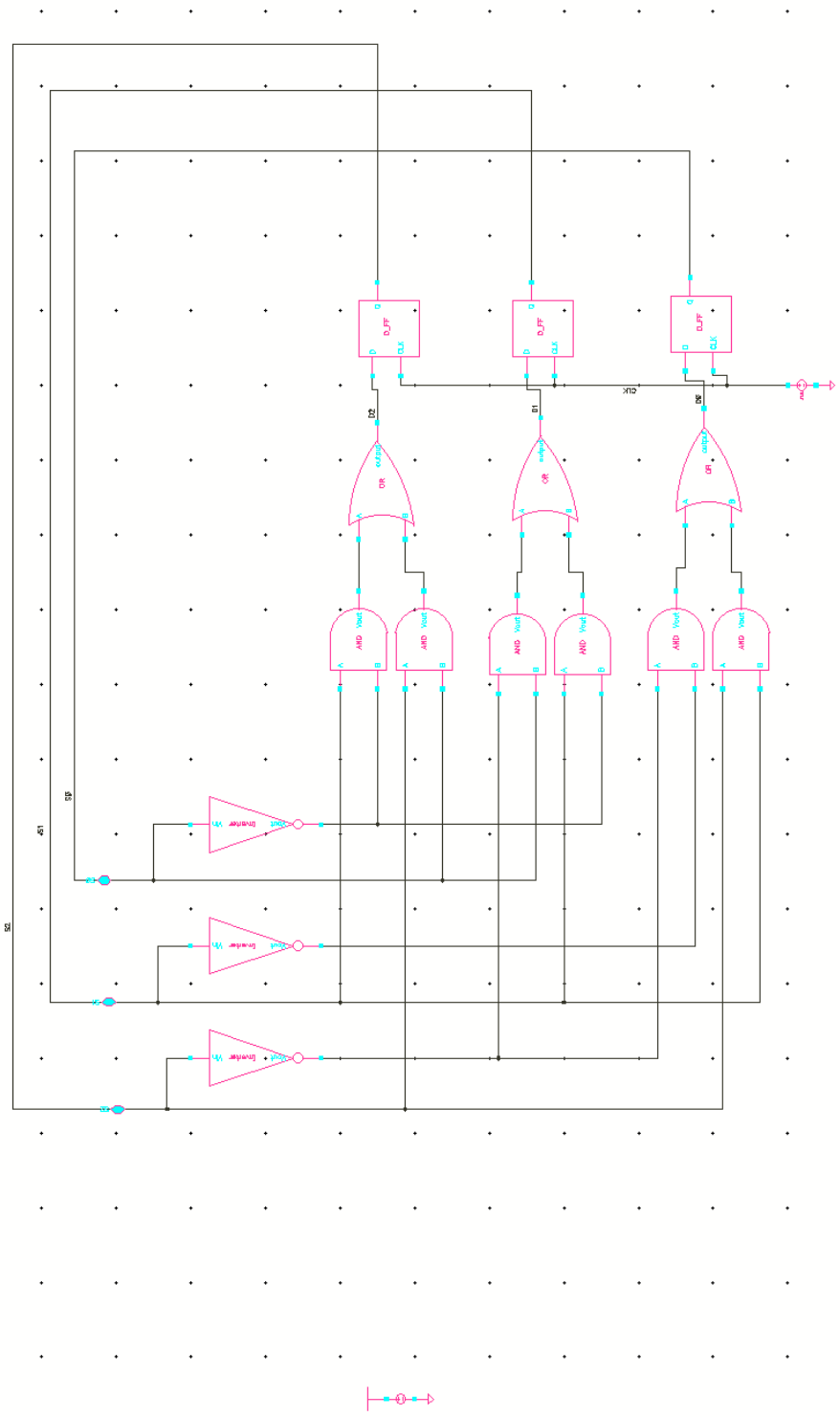
D-Flip flop Design:



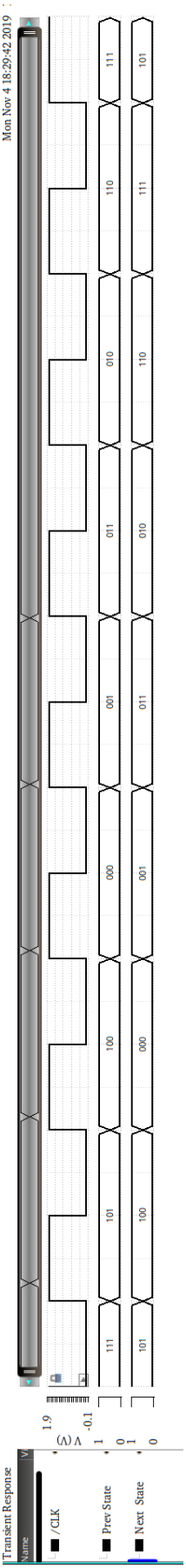
D-Flip flop Output:



Gray Code Counter:



Gray Code Counter Output:



Conclusion:

The lab was successfully implemented on the Cadence. A gray code counter is an example of Moore machine since its output is only determined by the present state. At every clock cycle this counter counts the gray code values for its corresponding binary equivalent.

Questions:

What is Moore Finite State Machine (FSM)?

- A Moore machine is a finite-state machine whose outputs depend only on its present state, and not the present state inputs. The example of Moore machine is the Gray Code counter.

What is Mealy FSM?

- A Mealy machine is a finite-state machine whose outputs depend on both, its current state as well as the current inputs.