Department of Computer Engineering
Faculty of Engineering, University of Peradeniya

CO221: Digital Design | Lab 06 (with Proteus)

Deadline - 26/05/2020

Instructions for Completing Online Labs:

- You're required to implement the lab tasks using Proteus software.
- You should create a separate Proteus project for each lab task and each project should be placed inside a separate folder with the name LabXX_TaskYY where XX is the lab number and YY is the task number (e.g. if Lab 05 contains 4 tasks, you should have 4 Proteus projects in 4 folders named Lab05_Task01, Lab05_Task02, Lab05_Task03, Lab05_Task04).
- You should put all the above folders containing lab tasks into a single folder named E17XXX_LabYY where XXX is your E-number and YY is the lab number (e.g. if your E-number is E/17/001 and the lab is Lab 05, the folder should be named E17001_Lab05).
- Finally, you should create a .zip file by compressing the above lab folder E17XXX_LabYY and submit it via the link in FEeLS before the deadline mentioned in the lab sheet above.
- Note that any form of plagiarism will result in zero marks for the entire lab.

Lab Tasks:

Note: When you are implementing the following circuits in Proteus, make sure you use physically available devices to build them. That is, you should use LEDs for outputs, ICs you've been using in physical labs, etc. in your designs. Further, make sure you do a good hardware design keeping safety issues in mind (e.g. use proper resistors where necessary to limit current).

1. Storage Elements: Latches

a. Implement an SR latch using two input NAND gates and verify its functionality. (10 marks)
b. Extend the SR latch circuit into a gated D latch and verify its functionality. (15 marks)

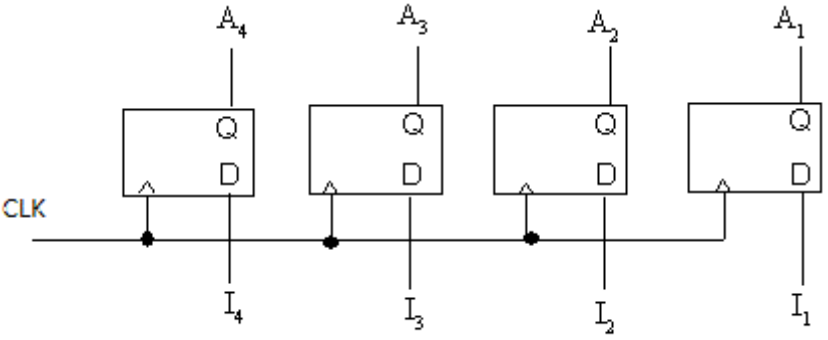
2. Storage Elements: Flip - flops

a. Implement a master-slave D flip-flop (negative edge triggered) using two gated D latches and verify its functionality. You may use a push button in place of the clock signal. (20 marks)
b. Extend the D flip-flop into a T flip-flop using an XOR gate and verify its functionality. You may use 74LS86 IC for the XOR gate. (10 marks)

3. Sequential circuits

A register is a group of flip-flops. Each flip-flop is capable of storing one bit of information. An n-bit register consists of a group of n flip -flops capable of storing n bits of binary information.

There are various types of registers which perform different functionalities. The simplest type of register can be constructed using D flip flops. Figure below shows such a register. Implement this register using 4 positive edge triggered D-flip flops. Use 74LS74 IC for the implementation. (20 marks)



Bonus marks exercise

Design and construct a JK flip-flop using a 2-to-1 line multiplexer and an inverter. Include your design and Proteus project inside a folder named Lab06_Bonus.