Department of Computer Engineering
Faculty of Engineering, University of Peradeniya

CO221 : Digital Design
Lab 6: Pre-lab

THEORY

Digital circuits we constructed so far have been combinational, where outputs are entirely dependent on current inputs. Although many logic functions can be performed using combinational circuits, them alone are not very useful in practical situations. The reason for this being many practical scenarios require some storage elements to store data. Hence, most of the circuits are implemented using combinational logic to which storage elements are connected, giving rise to sequential logic.

Storage elements are devices capable of storing binary information. Binary information stored in the element at a given time is given by the *state* of the circuit at the given time. Inputs, together with the present state determines the outputs of the circuit.

In this lab session, we will be focussing on two types of storage elements, namely latches and flip-flops.

Latches (gated) are asynchronous elements, where the state of the latch will change as long as the trigger inputs are active. In other words, a latch is level-triggered. On the other hand, a flip-flop works synchronously with the clock. That is, it changes state only when a transition in the clock signal occurs. Hence, a flip-flop is edge triggered.

QUESTIONS

- Each individual should have a written/printed pre-report.
- If you have any questions or you need help, put a post in the forum for CO221 in FEeLS rather than copying from someone else.
- If you are caught copying you get 0 for the prelab and also the marks for the rest of the lab would be reduced by 50%.

1. **Storage Elements: Latches**

    a. Draw the circuit diagram and the function table of the SR latch using NAND gates.

    b. Show how the gated D latch can be obtained using the above SR latch. Draw the circuit diagram. Give the function table of a gated D latch.

2. **Storage Elements: Flip - flops**

    a. Draw state diagrams of SR, D, JK and T flip-flops.

    b. Draw the circuit diagram of a master-slave D flip-flop using the above gated D latch and give the characteristic table.

    c. Draw the circuit diagram of the positive edge triggered D flip-flop using three SR latches.

    d. Show how the JK flip-flop can be obtained using a D flip-flop. Draw the circuit diagram. (You may use the graphic symbol of D flip-flop). Give the characteristic table of a JK flip-flop.

    e. Show how the T flip-flop can be obtained using a D flip-flop. Draw the circuit diagram (You may use the graphic symbol of D flip-flop). Give the characteristic table of a T flip-flop.