Department of Computer Engineering
Faculty of Engineering, University of Peradeniya

CO221: Digital Design | Lab 07 (with Proteus)

Deadline - 14/06/2020

Instructions for Completing Online Labs:

- You're required to implement the lab tasks using Proteus software.
- You should create a separate Proteus project for each lab task and each project should be placed inside a separate folder with the name LabXX_TaskYY where XX is the lab number and YY is the task number (e.g. if Lab 05 contains 4 tasks, you should have 4 Proteus projects in 4 folders named Lab05_Task01, Lab05_Task02, Lab05_Task03, Lab05_Task04).
- Include the prelab answers in a folder named LabXX_Prelab
- You should put all the above folders containing lab tasks and the prelab answers into a single folder named E17XXX_LabYY where XXX is your E-number and YY is the lab number (e.g. if your E-number is E/17/001 and the lab is Lab 05, the folder should be named E17001_Lab05).
- Finally, you should create a .zip file by compressing the above lab folder E17XXX_LabYY and submit it via the link in FEeLS before the deadline mentioned in the lab sheet above.
- Note that any form of plagiarism will result in zero marks for the entire lab.

Lab Tasks:

Note: When you are implementing the following circuits in Proteus, make sure you use physically available devices to build them. That is, you should use LEDs for outputs, ICs you've been using in physical labs, etc. in your designs. Further, make sure you do a good hardware design keeping safety issues in mind (e.g. use proper resistors where necessary to limit current).

1. Parity bits are the simplest form of error checking mechanism used in digital communication systems.

Implement an Even parity checker which takes a stream of bits and asserts the output when the number of 1 bits received is an even number using,

a. Mealy model
b. Moore model

Use D flip-flops and combinational logic for the implementation. (30 marks)

2. Combinations of bit patterns are used as passcodes or passwords when locking doors and safe boxes. A pattern detector which detects a given pattern can be implemented using sequential logic.

Implement a sequential circuit which detects the pattern '011' in an input bit stream. The circuit should be in the Moore model. Use D flip-flop as the type of flip-flop. (35 marks)

3. Implement a 3-bit synchronous binary counter with D flip-flops and combinational logic. Use Moore model. (35 marks)