Date:

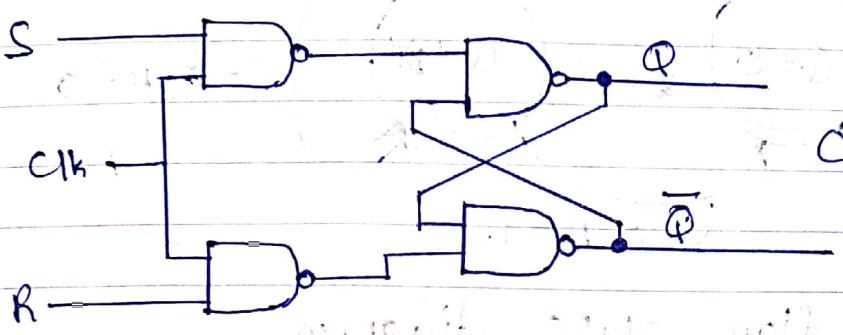
No.

Pre Lab. - Lab 6.

E/17/219

Nawarathna K.G.I.S.

1.a)

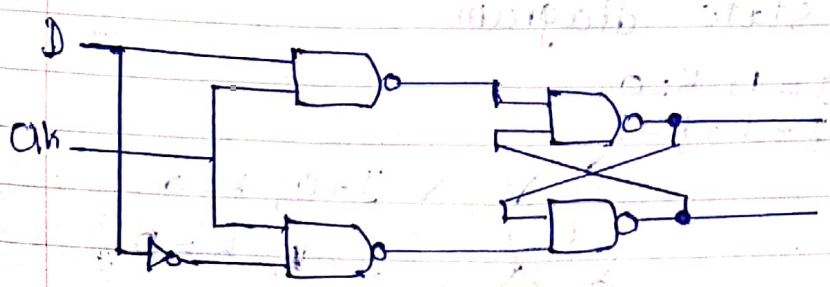


Circuit diagram.

Characteristic Table. (Clk is 1.)

S	R	Q	$\overline{Q}$	
0	0	0/1	1/0	memory state.
0	1	0	1	
1	0	1	0	
1	1	Uncertain.		

b). In the above SR latch If S = R = 1 then the results would be uncertain. Therefore D ~~flip~~ latch is desgined such a way that the same input doesn't occur to ~~the~~ both S and R. (S an R both cannot have the same input value: ie⇒ if S is 1 the R is definetely 0 and rise versa.)



Circuit Diagram.

Clock	D	Q(t+1)
0	X	Q(t). memory
1	0	0
1	1	1

Characteristic Table.

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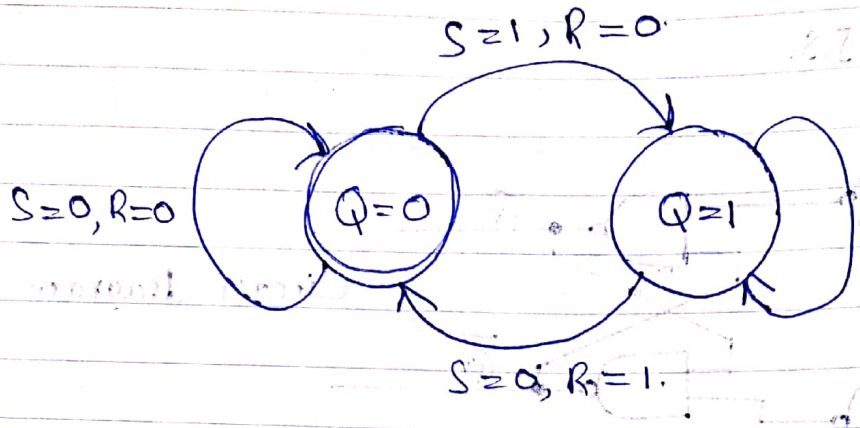
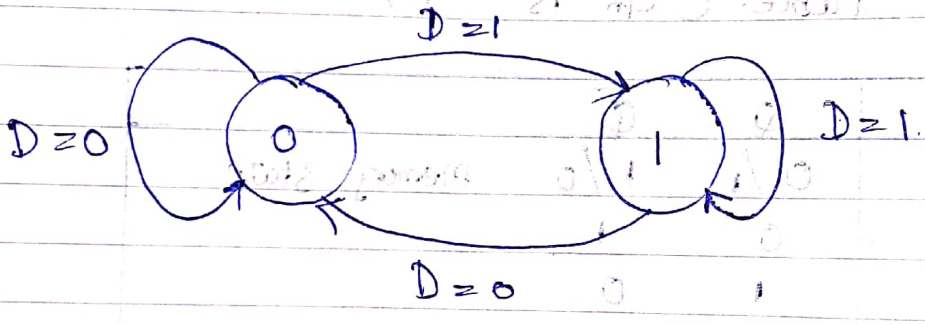
No.

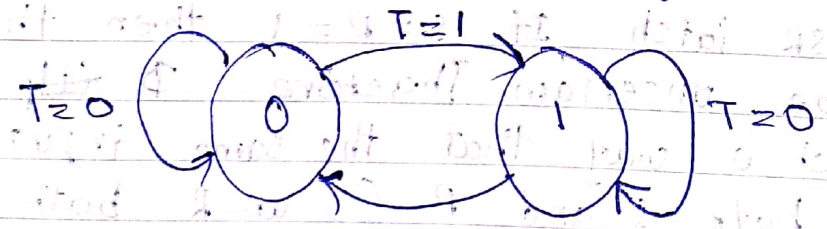
② a). SR flip flop state diagram:



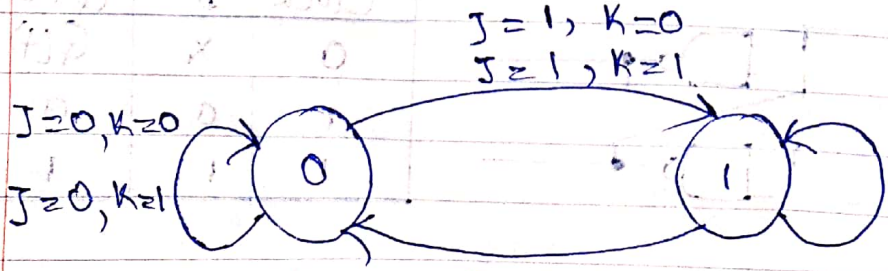
D flip flop state diagram.



T flip flop state diagram.



JK flip flop state diagram.



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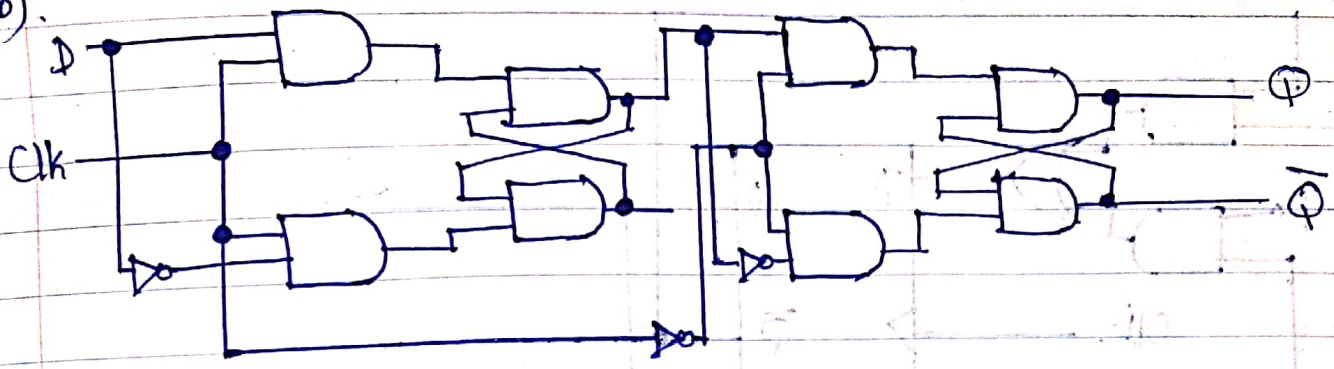
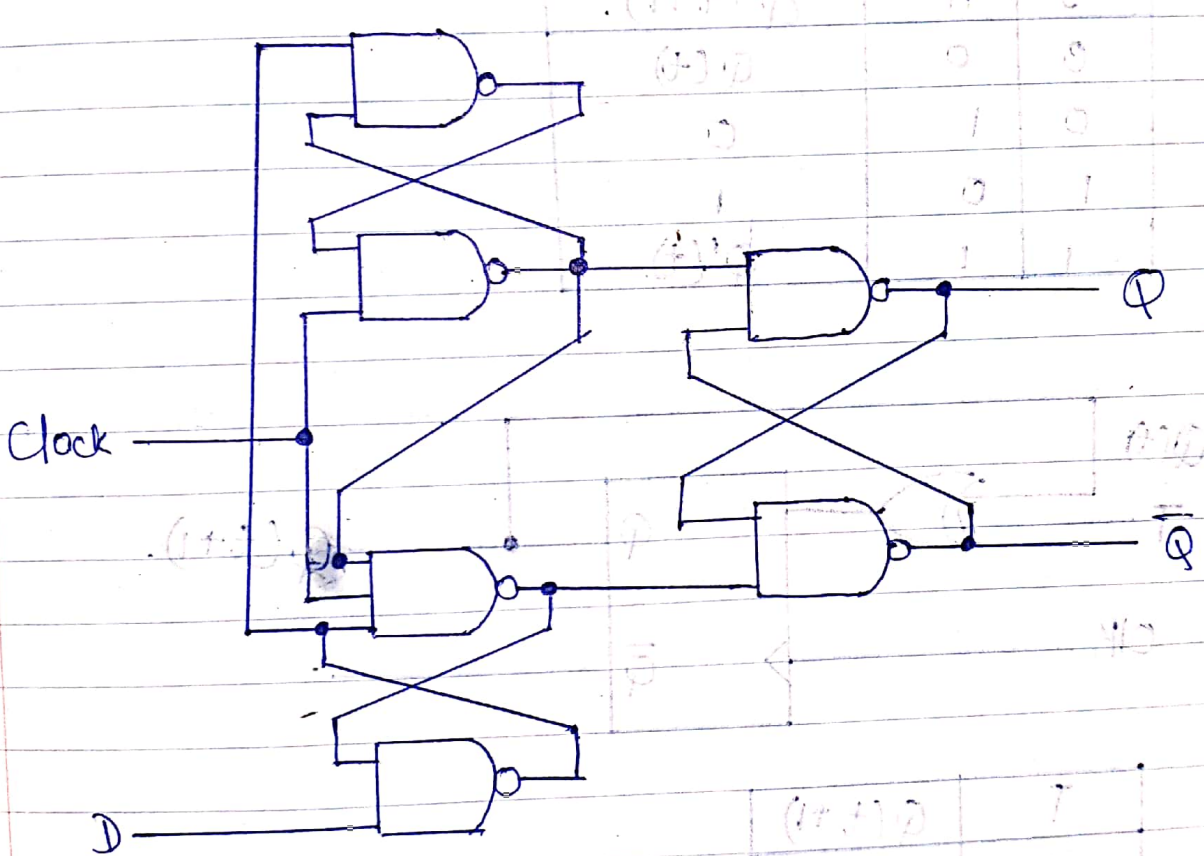
b).



Characteristic table.

c).



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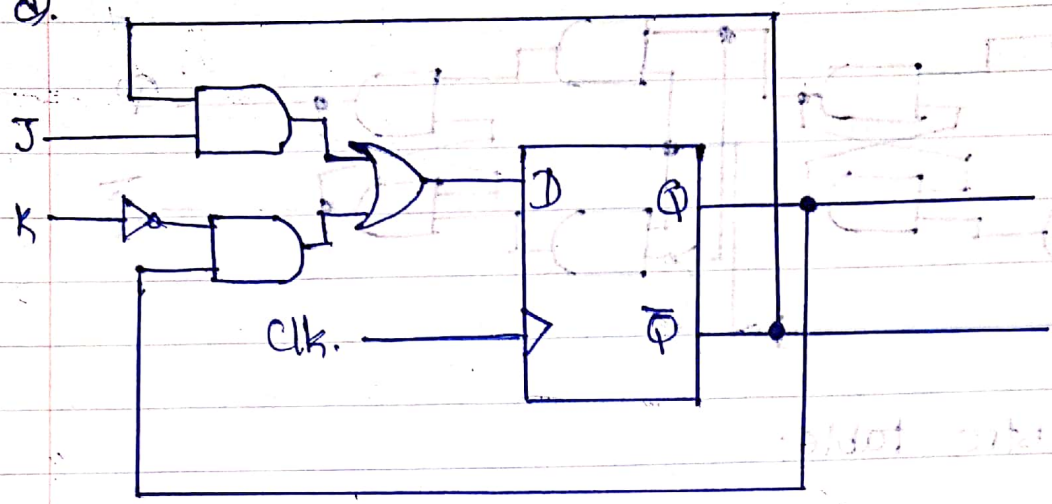
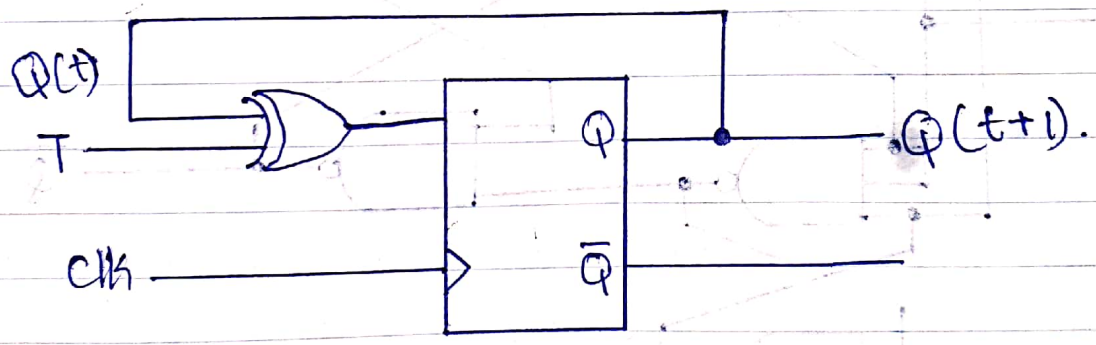
d).



J	K	Q (t+1).
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t).

e).



T	Q(t+1)
0	Q(t)
1	Q'(t)