CO224 Computer Architecture - 2020

Lab 6 - Building a Memory Hierarchy – Lab report

Comparison of the system's performance using the data memory with and without the data cache memory:

Observation 1:

Register file values of the Cache-less Data memory (Part 1):

time	reg0	reg1	reg2	reg3	reg4	reg5	reg6	reg7
5	0	0	0	0	0	0	0	0
13	9	0	0	0	0	0	0	0
21	9	1	0	0	0	0	0	0
165	9	1	9	0	0	0	0	0
213	9	1	9	9	0	0	0	0
221	9	1	9	9	8	0	0	0
317	9	1	9	9	8	8	0	0
413	9	1	9	9	8	8	8	0

Register file values of the Cache Data memory (Part 2):

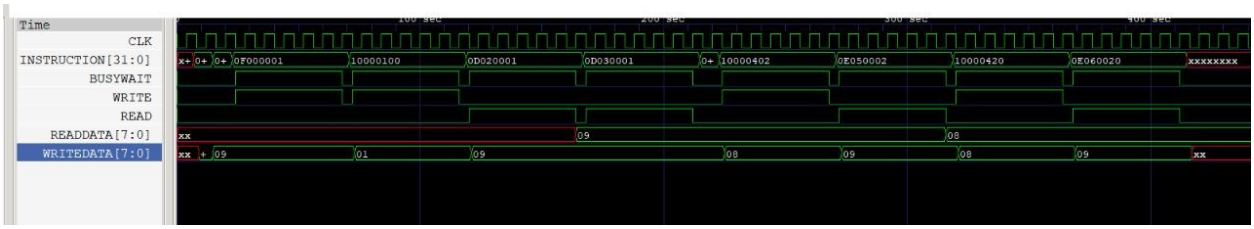
time	reg0	reg1	reg2	reg3	reg4	reg5	reg6	reg7
5	0	0	0	0	0	0	0	0
13	9	0	0	0	0	0	0	0
21	9	1	0	0	0	0	0	0
221	9	1	0	0	0	0	0	0
229	9	1	0	9	0	0	0	0
237	9	1	0	9	8	0	0	0
253	9	1	0	9	8	8	0	0
613	9	1	0	9	8	8	0	0

Conclusion:

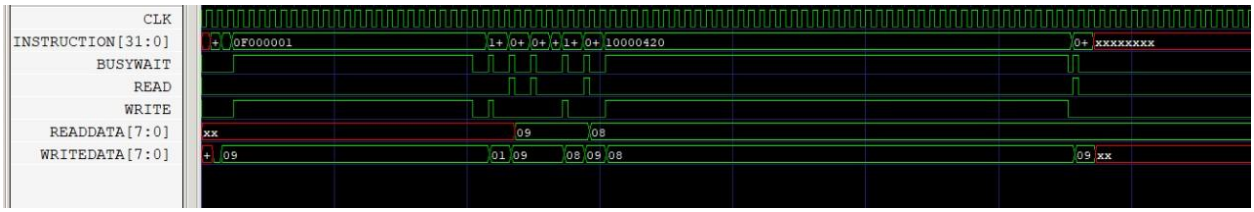
Cache-less Data memory takes less clock cycles (32 clock cycles less) than the other to complete the task. This is because the cache memory accesses the Data memory according to the Write Back method.

Observation 2:

Timing diagram (GTKWave file) of the Cache-less Data memory (Part 1):



Timing diagram (GTKWave file) of the Cache Data memory (Part 2):



Conclusion:

In the first diagram we can see, accessing the Data memory depends on the instruction. But in the second diagram we can see, the Cache memory accesses the Data memory according to the state changing. Therefore, in the Part 2 the Data memory is accessed only two times.

ite Back method.