NATIONAL INSTITUTE OF BUSINESS MANAGEMENT

DIPLOMA IN SOFTWARE ENGINEERING 17.2F

COMPUTER TECHNOLOGY DSE-2-4-05

21st May 2018

9.00 am – 12.00 noon

Answer ***all*** questions.

Electronic calculators are allowed. Time: THREE hours.

PART A-DIGITAL ELECTRONICS

Question 1

i. Simplify the following expressions using De Morgan's Law.

a. $Z = \overline{\bar{A}.\bar{B} + \overline{A.\bar{B}.C}}$

b. $Z = \overline{A + \overline{\overline{B.\bar{C}}} + C.D} + \overline{\overline{\overline{B.C}}}$

c. $Z = \overline{(A.B + \overline{\overline{B.\bar{C}}})}.\overline{(\overline{\overline{A.\bar{B}}} + \overline{A.B.C} + ABC)}$

(06 Marks)

ii. Z = f (A, B, C, D)

Z =1 for the minterms (0, 2, 5, 7, 8, 13)

Z= don't care for the minterms (10, 15)

Z = 0 for the remaining minterms.

Simplify Z using:

i) K- map method (02 Marks)

ii) Tabular method (04 Marks)

iii. Explain the importance of Boolean expression simplification in Digital Circuit Designing.

(02 Marks)

Question 2

i. Draw the truth table of Full Adder and implement the circuit using basic logic gates.

(04 Marks)

ii. An assembly line has 3 failsafe sensors and 1 emergency shutdown switch. The assembly line will be deactivated by switching off the emergency shutdown switch if anyone of the following conditions occur.

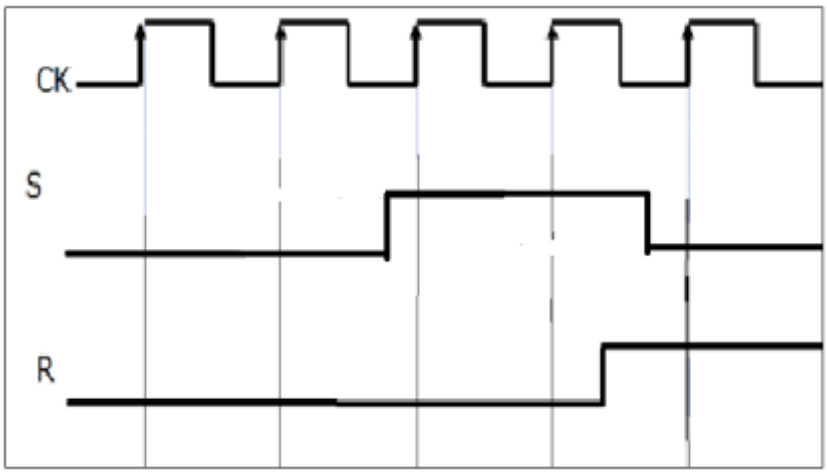
- If the emergency switch is pressed, the system shuts down.
- If sensor 1 and sensor 2 are activated at the same time, the system shuts down
- If sensor 2 and sensor 3 are activated at the same time, the system shuts down.
- If all three sensors are activated at the same time, the system shuts down.

a. Determine the truth table for the circuit. (02 Marks)
b. Obtain the simplified
    i. SOP expression (02 Marks)
    ii. POS expression (02 Marks)
c. Implement the circuit using
    i. **NAND** gates only. (03 Marks)
    ii. 4:1 Multiplexer. (03 Marks)

iii. Explain the operation of 1:4 De multiplexer using a diagram. (04 Marks)

Question 3

i. Draw the output waveform Q of a positive edge triggered SR flip flop. Assume that the initial value of the flip flop is 0. (02 Marks)



ii. Complete the truth table of J-K flip flop and derive its excitation table. (04 Marks)

iii. Design a 3-bit counter to count the bit sequence 0,2,4,6. Use positive edge triggered J-K flip flops. (06 Marks)

iv. Three edge-triggered JK flip flops in a synchronous circuit have the following input conditions:

$J_A = Q_C$ $K_A = 1$

$J_B = 1$ $K_B = \bar{Q}_A.Q_C$

$J_C = Q_B$ $K_C = 1$

Assume that the initial state is $Q_A = 0$ $Q_B = 1$ $Q_C = 1$. Find the count sequence. (04 Marks)

PART B- PHYSICAL ELECTRONICS

Question 4

i. Briefly explain how N-Type semi-conductors are formed using its crystal structure. (03 Marks)

ii. Explain the reversed biased mode of the P-N junction. (03 Marks)

iii. Draw the Volt-Ampere characteristics of a practical diode and mark I_s (Reverse Saturation Current), PIV (Peak Inverse Voltage) and V_b (Forward Biased Voltage) on the curve.

(02 Marks)

iv. Draw the circuit diagram of Half Wave Rectifier and explain the operation of it. (04 Marks)

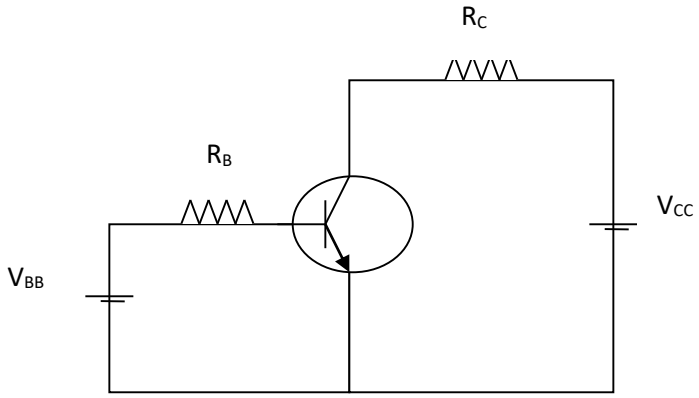
Question 5

i. Draw the graph of input characteristics of a transistor. (03 Marks)

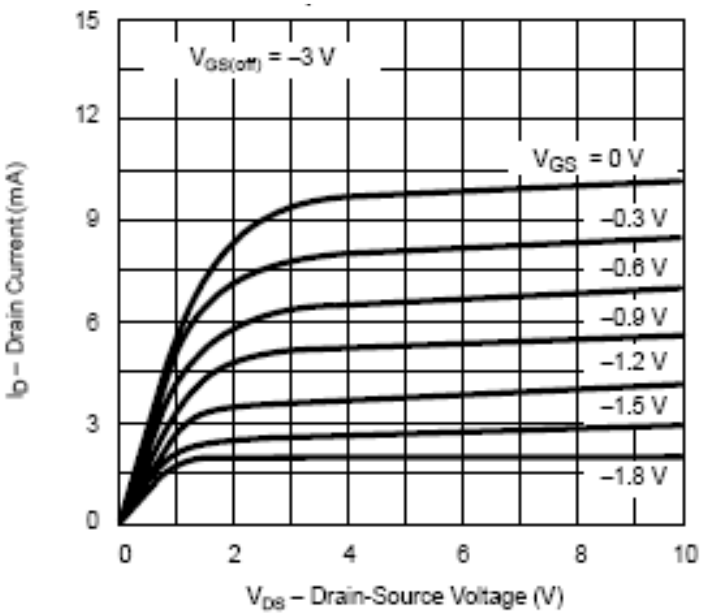
ii. Consider the following circuit and obtain the operating mode of the transistor. Hence calculate **I_B, I_C and V_{CE}**. Assume that the transistor is made out of Silicon. (12 Marks)

Material	**V_{CE}(sat)**	**V_{BE}(sat)**	**V_{BE}(act)**	**V_{BE}(cut in)**
Si	0.2V	0.8V	0.7V	0.5V
Ge	0.1V	0.3V	0.2V	0.1V

β	**R_B**	**R_C**	**Vcc**	**V_{BB}**
100	200kΩ	2kΩ	10V	5V



6. Consider the circuit in figure 2 and the characteristic curve of the JFET in figure 3 .If VDD = 12V, VGG = 1.2V, RG = 2kΩ, RD = 2kΩ.



i. What is the type of the given JFET? (01 Mark)

ii. Indicate the three regions of the characteristic curve. (01 Mark)

iii. Calculate Gate-Source voltage. (03 Marks)

iv. Obtain an equation for the load line of the circuit and plot it over the given characteristic curve. (03 Marks)

v. Hence identify the operating mode of the JFET and find the coordinate of the operating point. (02 Marks)

There are many digital logic families.

a. Explain two important characteristics of Digital Logic Families briefly. (02 Marks)

b. Consider the following digital logic circuit. Then identify its logic family and show that it is an AND gate by using a suitable truth table. (03 Marks)