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Ishika Kanakath

OBJECTIVE

Seeking a Ph.D. research position in electrical and computer engineering with emphasis on digital design and verification of AI based hardware, software systems, robotics, and neural interfaces design

EDUCATION

MS Computer Engineering, Case Western Reserve University, 2024-2025, 3.9

Master's Project: "Design of laser scanner for 3D printers Wire Additive Manufacturing Machines to detect vision, temperature, and measurement of material layers for a
NASA Funded project**"**

BS Computer Engineering, Case Western Reserve University, 2021-2024, 3.5

Senior Project: "Develop a cost-effective RADAR velocity measurement device for Cleveland Big Wheels Relay"

HONORS and AWARDS

SOURCE STEM Scholarship (May 2024)
This scholarship is for conducting research using Human Fusion Institute Baxter Robot and aims to generate insights that will inform the development of more effective and socially aware robotic systems, a crucial aspect as robots become increasingly integrated into various aspects of human life.

Robert L. Shurter Prize (April 2024)
The Prize recognizes outstanding achievement and leadership in extracurricular activities at the Electrical and Computer Engineering department of Case Western Reserve University.

Dean's Honors List (2021-2024)
I was in the Dean's honor list for 5 Semesters. The Dean's Honors Lists consist of the names of those undergraduate students who have distinguished themselves by achieving during the previous semester the grade point averages of at least 3.5 required with a minimum of twelve credit hours.

University Merit Scholarship (Aug 2021-May 2025)
I received CWRU Merit Scholarship as an incoming student based upon my admission application, including academic achievement, performance on standardized tests, leadership, artistic talent, and other personal qualities that distinguish students from others in the applicant pool.

Experian College Scholarship Award (2021-2022)
Received Merit-based scholarship based on academic, athletic, or artistic performance provided by company Experian.

Jerry P Lind Prize (2024-2025)
Awarded to a senior in Science and Engineering that made a significant contribution to campus life.

ISAAC Scholarship (2024-2025)
Scholarship awarded to a masters student in the ECSE department pursuing the project or thesis based masters program. Project was funded by NASA.

RESEARCH EXPERIENCE

Case Western University, Cleveland. Research Intern, Material Science and Engineering Department (2023-2025)

- Working on integrating laser and temperature sensors to scan printed layers and adjusting subsequent layers based on deviation, improving print accuracy as part of Masters Project which was NASA funded.
- Design a process for continuous layer scanning and data processing to ensure uniformity, leveraging laser feedback to inform next layer planning and reduce distortion.
- Document hardware and architecture components for the relay switch, temperature, duet 3d boards, and vision sensors for the WAAM machine.
- Conducting comprehensive literature review on: Current wire additive manufacturing techniques, Process control strategies in WAAM, Hardware integration methods, Software control systems, Limitations and opportunities in existing systems.
- Assisted with Engineering custom G-code generation system for Wire Arc Additive Manufacturing (WAAM) by developing post-processing scripts integrated with Ultimaker Cura, enabling automated translation of 3D models to machine-compatible instructions for Duet 3D controller board.

Case Western University, Cleveland. Research Intern, Human Fusion Institute (2024) • Design and implement hand gestures, movement, text to speech features in Baxter robot using ROS and Python.

- Worked on a laser device to communicate with ROS which helped the Baxter Robot move close and far distances.
- Worked on integrating object detection into the Kinect camera on the robot and built the user design study to evaluate users.

Case Western University, Cleveland. Research Intern, Neural Engineering Center (2022-2023) • Developed MATLAB algorithms to analyze temporal relationships between neural stimulation and cognitive responses in upper-limb amputees.

- Quantified neural feedback mechanisms and response patterns to improve proprioceptive sensation in neuroprosthetic devices.
- Processed experimental data to characterize both functional and affective touch responses,

contributing to enhanced prosthetic sensory feedback systems.

- Assisted with development of multi-input/output Universal Electronic Control Unit (UECU) switchboard designed for neural stimulation experiments in proprioceptive and affective touch research.
- Engineered precision control systems for neuroprosthetic feedback, enabling complex stimulation patterns crucial for restoring natural sensory perception in amputees. • Implemented hardware fabrication and testing protocols for neural interface electronics, including PCB assembly and validation of stimulation circuits.

TEACHING EXPERIENCE

Case Western University, Cleveland. Teaching Assistant, Digital Logic Lab, ECSE department (2024)

- Organized lab kits and demo lab assignments.
- Held Office hours for reviewing results and discussions.
- Graded lab reports and demonstrations of experiments

Case Western University, Cleveland. Peer Tutor (2024)

- Tutored Peer Students in Thermodynamics, Multivariable Calculus, Statistics and Strength of materials, and Chemistry of materials

PROFESSIONAL INTERNSHIPS

Cadence Design Systems, Sanjose, CA Application Engineering Intern (2023)

- Performed the RTL to post route implementation of Sous Vide chip being migrated from GPDK45 to the SKY130 node.
- Synthesized RTL using Genus and then took the gate level netlist through the entire implementation flow such as Floor planning, Place & Route implementation using Innovus towards the best achievable power, performance, and area.
- Static timing analysis of post routed netlist was done using Innovus.

Experian, Costa Mesa, CA, Software Engineering Intern (2022)

- Designed interfaces between hardware and software to meet the operational performance requirements.
- Participated in agile ceremonies, learned about the project lifecycle, and partnered with different cross-functional teams.
- Learned Amazon web services – Amazon S3, Amazon EC2

Experian, Technical Contractor, Costa Mesta, CA (2025)

- I worked part time as a technical contractor under the employer verification services software team working on applications using generative AI, Amazon Web Services, Data Analytics, APIS, and Microservices.

MACOM, Digital Circuit and Digital Signaling Processing Intern, CA (2025)

- I am currently working as an electrical engineering intern under the Digital circuit Design and

signal processing team. Skills include a strong mathematical knowledge, computer architecture, VlSI, Verilog, and Digital Signal Processing

ACADEMIC PROJECTS

Radar Sensor Design

- Developed a cost-effective RADAR velocity measurement device using the HB100 Microwave Motion Sensor and ESP32 microcontroller for the Cleveland Big Wheels Relay.
- The system captured and transmitted real-time velocity data of racers, enhancing audience engagement and supporting fundraising efforts for the Cleveland Hearing and Speech Center.
- Led research on RADAR modules, prototyping, signal processing, and Bluetooth communication to relay data to spectators.

Laser Sensor Integration WAAM

- Development of an advanced closed-loop control system for Wire Arc Additive Manufacturing (WAAM) that integrates real-time laser scanning with adaptive process control.
- The system ensured consistent layer height and quality through continuous monitoring and adjustment of process parameters.

Our closed loop system included:

- Real-time height measurement and analysis system.
- Integration with ARC Mini control system.
- Automated adjustment of process parameters based on scan data.
- Layer-by-layer validation and correction.
- Position-aware scanning: (50,0) to (50,100) gantry movement.

Comparative Analysis of Attention Mechanisms: Implementing Flash Attention for Enhanced GPU Performance

- Developed CUDA-based implementations of both standard and Flash Attention algorithms, incorporating shared memory tiling and warp-level parallelism optimization techniques. • Conducted comprehensive performance analysis across varying sequence lengths (128-1024), demonstrating linear vs. quadratic memory scaling benefits.
- Implemented memory-efficient attention computation using GPU shared memory and tile based processing, reducing memory bandwidth usage while maintaining mathematical accuracy.
- Utilized NVIDIA CUDA for parallel computing optimization, achieving significant speedup in attention computation through efficient memory hierarchy utilization.

Image Processing & Neural Network Research project in Quantum Computing • Focused on a fundamental operator in image processing and convolutional neural networks, the convolution operator, or more precisely, cross-correlation.

- Explored the feasibility and efficiency of implementing convolution in quantum computing, particularly examining how it can be adapted or redefined for quantum information processing.

• Designed quantum image encoding and quantum convolution using quantum gates, and my goal was to determine efficient and optimal criteria for selecting quantum gates.

Finite State Machine (FSM) design and FPGA Implementation

- Designed and implemented a finite state machine (FSM) in VHDL to monitor cars entering and exiting a parking lot.
- Used Synopsys tools to synthesis and simulate the FSM into a gate-level sequential circuit. • Deployed the design on a Xilinx VIRTEX II FPGA board, utilizing input switches and LEDs to validate the system's behavior in real-time.
- Demonstrated proficiency in hardware description languages, FPGA implementation, and digital system design.

Arduino Uno and Raspberry Pi 3 Integration for Microcontroller Programming and LED Control • I familiarized myself with the Arduino Uno microcontroller and Arduino IDE on Raspberry Pi 3 by executing example sketches, including 'Blink' with both built-in and external LEDs. • Compiled and uploaded the tested code for microcontroller functionality, and successfully interfaced external components.

Microseconds Response driver for Raspberry Pi

- Developed a microseconds response driver as a kernel module for Raspberry Pi, integrating real-time processing for a temperature sensor.
- Designed the driver by adapting previous application-level code into a kernel module, utilizing GPIO pin interrupts for real-time response.
- Compiled and evaluated the module using Linux kernel utilities and compared its performance with previous implementations in terms of accuracy and response time.

RISC Processor Architecture Design | Digital Hardware Project

- Designed and implemented a 32-bit RISC processor with a 16-bit ALU in Verilog HDL, featuring comprehensive instruction set execution.
- Developed processor components including ALU, Program Counter, Status Register, and 16-register file with memory interface.
- Created and validated test programs demonstrating arithmetic operations, two's complement conversion, and binary multiplication.

Traffic Light Controller Design Project | VHDL

- Designed and implemented an intelligent traffic control system in VHDL for two-street intersection with priority management.
- Developed real-time vehicle detection system using sensor inputs for adaptive signal timing control.
- Implemented Moore state machine architecture with precise timing control (10-second clock periods, 50-60 second cycles).
- Created multi-output controller managing six traffic signals with priority-based street handling.
- Verified functionality through Model Sim simulation with comprehensive test scenarios.

Designed and implemented three distinct 16-bit adder Architectures

- Ripple Carry Adder with propagation path optimization.
- Uniform Carry Select Adder with optimized 4-bit blocks.

- Variable-size Carry Select Adder for enhanced performance.
- Conducted comparative timing analysis using unit-delay gate model. Developed comprehensive test vectors for functional verification.
- Optimized critical path delay through strategic block sizing and architecture selection.

CPU Design

- Designed and implemented a complete 16-bit CPU architecture with instruction set support for arithmetic, logic, and control operations.
- Developed multi-cycle instruction execution unit using finite state machine architecture with 50+ states.
- Implemented comprehensive memory system including register file (4K × 16-bit) and RAM (256 × 16-bit).
- Created complete instruction fetch and decode unit supporting ten distinct instructions.

Digital Circuit Simulation and Analysis Project | ISCAS Benchmark Implementation • Developed comprehensive circuit simulation software for analyzing ISCAS benchmark circuits with three-valued logic.

- Implemented sophisticated data structures for circuit representation including gate records, fanout lists, and level-based organization.

Direct-Mapped Cache Memory System Implementation | VHDL

- Designed and implemented a direct-mapped cache controller system supporting 32-bit data paths and 16-bit addressing.

Engineered comprehensive memory hierarchy including:

- 8-entry cache system with tag RAM and efficient lookup mechanisms.
- Write-through policy implementation with coherency management.
- 4-cycle memory access control with parallel operation support.

PET Image Reconstruction Case Study:

- Was given a set of coincidence measurements from detector pairs, the goal was to reconstruct the spatial distribution of radioactive emissions within the body
- The case study implemented and analyzed the relationship between the emission and the measurements and was described by a system of equations
- Mathematically modeled the PET emission and detection process using poisson statistics and convex optimization principles
- Derived necessary mathematical components (objective function, gradient, hessian)
- Implement and compare both an efficient interior point algorithm of a fixed point method with non negativity constraints
- Evaluated the reconstructed image quality and algorithm performance for both methods

Emergency Vehicle Vibrotactile Device

- Worked on development and evaluation of a wearable haptic device designed to enhance environmental awareness for individuals with hearing impairments

- Used 4 degrees of freedom and provided kinesthetic force feedback to the user as an object is detected to get closer in proximity to them in
- The system used an ultrasonic distance sensor and three vibration motors arranged linearly on a wearable arm sleeve which then translates accurate proximity and directional information into intuitive vibration patterns by implementing the skin to imitate an oncoming vehicle
- The results from tests demonstrated the potential for haptic feedback to serve as an effective alternative sensory channel to detect approaching objects

COURSEWORK

Undergraduate Courses (2021-2024): Logic Design and Computer Organization, Computer Architecture (Assembly MIPS), Introduction to Programming in Java, Digital Logic Lab (Verilog), VLSI CAD (Verilog / VHDL), Introduction to Circuits,Physics 2: Electricity and Magnetism, Physics 1 : Mechanics, Embedded System Design, FPGA Programming, Quantum Computing, Differential Equations, Discrete, Statistics, Statics & Strength of Materials, Chemistry of Materials, Chemistry for Engineering, Multivariable Calculus,Thermodynamics/Mass fluid Heat Transfer, Data Structures and Algorithms (Python), and Digital Systems Design

Graduate Courses (2024-2025): Human Robotic Design (ROS, Python), High Performance Computing , Computer Systems Architecture , Masters Project (1 year long), Quantum Computing, FPGA Design, Haptics and kinematics design, Convex Optimization for Engineering, Embedded Systems Design, and Quantum Computing Information and Devices

Certifications : Innovus Implementation System V22.1 Exam (Cadence Design Systems), Introduction to Programming in Matlab Coursera, Digital Signal processing 1 Coursera : Basic Concepts and Algorithms, Digital Signal Processing 2 : Filtering, Digital Signal Processing 3 : Analog vs Digital, and Digital Logic Design for VLSI Coursera

SKILLS

Languages: Python, Java, TCL, MATLAB, Verilog, VHDL, MIPS, ROS, System Verilog , C

EDA Tools: Synplicity, VCS, ModelSim, Genus, Innovus, KiCAD, Xcelium Cadence

Technical & Other: Linux/Unix Operating Systems, Microsoft Office, Agile Methodology, Linear Algebra, Multivariable Calculus, Differential Equations, Digital Signal Processing