

ATME COLLEGE OF ENGINEERING

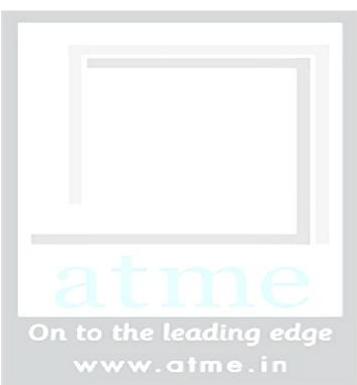
MYSURU-570028

BASIC ELECTRONICS

NOTES FOR 1st SEMESTER

SUBJECT CODE: 18ELN14

A T M E
College of Engineering



Vision

To develop highly skilled and globally competent professionals in the field of Electronics and Communication Engineering to meet industrial and social requirements with ethical responsibility.

Mission

- To provide State-of-art technical education in Electronics and Communication at undergraduate and post-graduate levels, to meet the needs of the profession and society and achieve excellence in teaching-learning and research.
- To develop talented and committed human resource, by providing an opportunity for innovation, creativity and entrepreneurial leadership with high standards of professional ethics, transparency and accountability.
- To function collaboratively with technical Institutes/Universities/Industries, offer opportunities for interaction among faculty-students and promote networking with alumni, industries and other stake-holders.

Program outcomes (POs)

Engineering Graduates will be able to:

PO1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

At the end of graduation the student will be able,

- To comprehend the fundamental ideas in Electronics and Communication Engineering and apply them to identify, formulate and effectively solve complex engineering problems using latest tools and techniques.
- To work successfully as an individual pioneer, team member and as a leader in assorted groups, having the capacity to grasp any requirement and compose viable solutions.
- To be articulate, write cogent reports and make proficient presentations while yearning for continuous self improvement.
- To exhibit honesty, integrity and conduct oneself responsibly, ethically and legally; holding the safety and welfare of the society paramount.

Program Educational Objectives (PEOs)

- Graduates will have a successful professional career and will be able to pursue higher education and research globally in the field of Electronics and Communication Engineering thereby engaging in lifelong learning.
- Graduates will be able to analyse, design and create innovative products by adapting to the current and emerging technologies while developing a conscience for environmental/ societal impact.
- Graduates with strong character backed with professional attitude and ethical values will have the ability to work as a member and as a leader in a team.
- Graduates with effective communication skills and multidisciplinary approach will be able to redefine problems beyond boundaries and develop solutions to complex problems of today's society.

Ripple Counter (refer 10.1-10.7 of Text 1).

Basic Communication system, Principle of operations of Mobile phone (refer 18.2 and 18.18 of Text 1).

List of Text Books

1. D.P. Kothari, I.J. Nagarath, "Basic Electronics", 2nd edition, Mc Graw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

List of Reference Books

1. D.P. Kothari, I.J. Nagarath, "Basic Electronics", 1st edn, McGraw Hill, 2014.
2. Boylestad, Nashelskey, "Electronic Devices and Circuit Theory", Pearson Education, 9th Edition, 2007/11th edition, 2013.
3. David A. Bell, "Electronic Devices and Circuits", Oxford University Press, 5th Edition, 2008.
4. Muhammad H. Rashid, "Electronics Devices and Circuits", Cengage Learning, 2014.

List of URLs, Text Books, Notes, Multimedia Content, etc

1. K A Navas, T A Suhail, "Basic Electronics" Rajath publishers
2. <http://nptel.ac.in/courses/117103063/>
3. <http://engineering.nyu.edu/gk12/amps-cbri/pdf/Basic%20Electronics.pdf>

Course Outcome s	After studying this course, students will be able to:
	1. Describe the operation of diodes, BJT, FET and Operational Amplifiers.
	2. Design and explain the construction of rectifiers, regulators, amplifiers and oscillators.
	3. Describe general operating principles of SCRs and its application.
	4. Explain the working and design of fixed voltage IC regulator using 7805 and Astable oscillator using Timer IC 555.
	5. Explain the different number system and their conversions and construct simple combinational and sequential logic circuits using Flip-Flops.
	6. Describe the basic principle of operation of communication system and mobile phones.

Internal Assessment Marks: 40 (3 Session Tests are conducted during the semester and marks allotted based on average of best performances).

MODULE 1

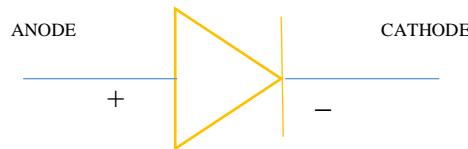
SEMICONDUCTOR DIODE AND APPLICATIONS

Structure

- 1.1 Introduction
- 1.2 P-N Junction Diode
 - 1.2.1 Diode Characteristics
 - 1.2.2. Diode Relationship
- 1.3 Equivalent circuit of Diode
- 1.4 Zener Diode
- 1.5 Zener Diode as a Voltage Regulator
- 1.6 Complement of Binary Numbers
 - 1.6.1. Half wave rectifier
 - 1.6.2 Full wave rectifier
 - 1.6.3 Bridge rectifier
 - 1.6.4. Capacitor filter Circuit
- 1.7 Photo Diode
- 1.8 LED
- 1.9 Photo Coupler
- 1.10 78XX series and 7805 Fixed IC voltage regulator

1.1 INTRODUCTION

Diode is an electrical component that allows the flow of current in only one direction. In circuit diagrams, a diode is represented by a triangle with a line across one vertex.



Diode has a wide range of applications like rectification (converting ac to dc), voltage regulation, protection against high voltage and wave shaping.

There are special purpose diodes like Zener diode, LED- light emitting diode and several other.

1.2 P-N JUNCTION DIODE

When P-type and N-type silicon are placed in contact with one another it forms a PN junction. At this junction an interesting phenomenon occurs, one that is the foundation of solid-state electronics.

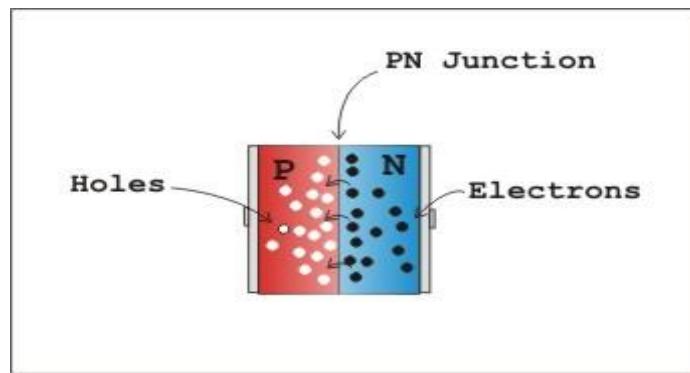


Fig 1

A basic PN junction creates a diode that allows electricity to flow in one direction. We can see in the fig 1 that the N type material has free electrons shown as black dots and the P type material has holes shown as white dots.

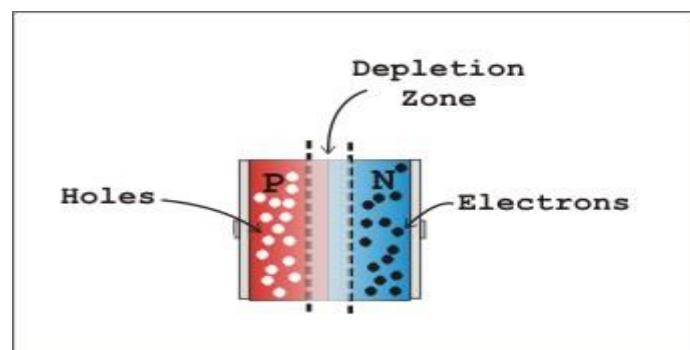


Fig 2

Near the PN junction the electrons diffuse into the vacant holes in the P material causing a depletion zone. This depletion zone acts like an insulator preventing other free electrons in the N-type silicon and holes in the P-type silicon from combining as shown in fig 2.

In addition, this leaves a small electrical imbalance inside the crystal. Since the N region is missing some electrons it has obtained a positive charge. And the extra electrons that filled the holes in the P region, have given it a negative charge. Unfortunately, one cannot generate power from this electrical imbalance. However, the stage is set to see how the PN junction functions as a diode.

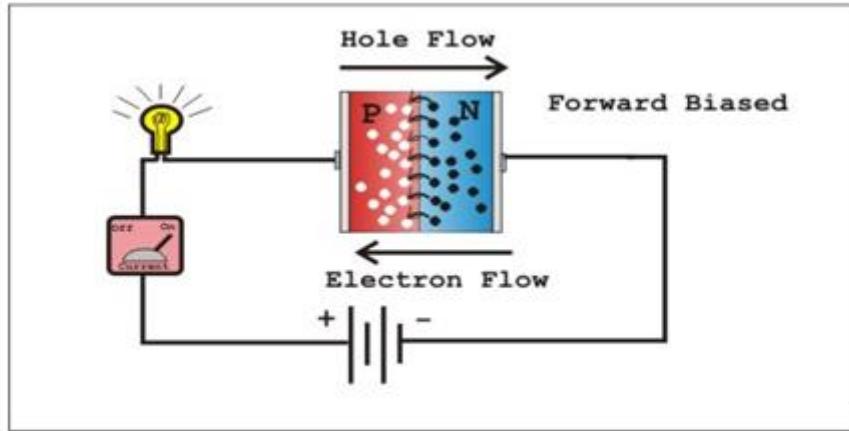


Fig 3

In the fig 3 we have connected an external power source; a battery with a light and current meter that indicate current flow. The negative terminal of the battery is connected to the N-type silicon. Like charges repel, so the free electrons are pushed toward the PN junction. Similarly, the holes are repelled by the positive terminal of the battery toward the PN junction. If the voltage pushing the electrons and holes has sufficient strength to overcome the depletion zone (approximately 0.7 V for typical silicon diode) the electrons and holes combine at the junction and current passes through the diode. When a diode is arranged this way with a power supply it is said to be forward-biased.

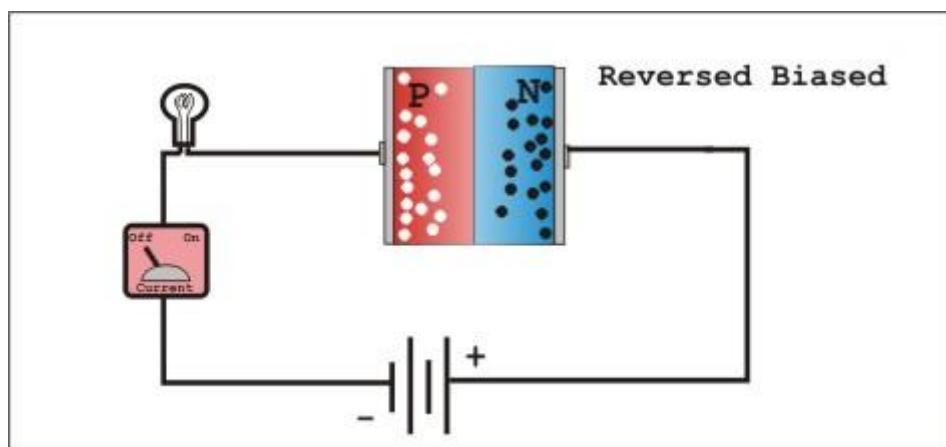


Fig 4

In the fig 4 the battery is connected to the diode so that the negative terminal of the battery connects to the P-type silicon and the positive terminal of the battery connects to the N-type silicon. The negative terminal attracts the positive holes in the P-type silicon and the positive terminal of the battery attracts the free electrons in the N-type silicon. All the charge carriers are pulled away from the PN junction which essentially creates a larger depletion region and no current flows. When a diode is arranged this way with a power supply it is said to be reverse-biased.

1.2.1. DIODE CHARACTERISTICS

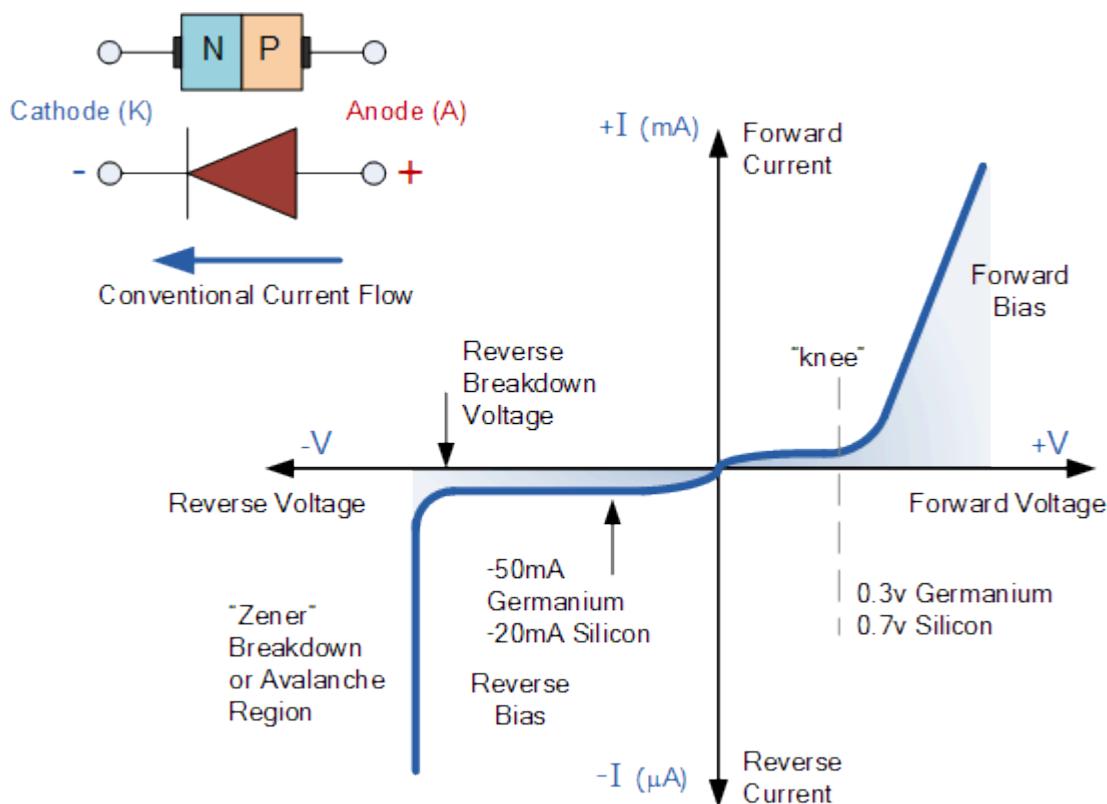


Fig 5

There are two operating regions and three possible “biasing” conditions for the standard Junction Diode as shown in fig 5 and these are:

1. Zero Bias – No external voltage potential is applied to the PN junction diode.
2. Reverse Bias – The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of Increasing the PN junction diode's width.
3. Forward Bias – The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of Decreasing the PN junction diodes width.

1.2.2. DIODE RELATIONSHIP

$$I_D = I_S (e^{kVd/Tk} - 1) \quad \text{Eq ----- 1}$$

where I_S = reverse saturation current

$k = 11600/\eta$; $\eta=1$ for Ge and $\eta=2$ for Si for low current, below the knee of the curve

$\eta = 1$ for both Ge and Si for higher level of current beyond the knee.

$T_K = T_C + 273^0$ where T_C = operating temperature (25°C).

The plots of equation 1 for Ge and Si diodes are as shown in fig 6. The sharply rising part of the curve extended downward meets the V_D axis, which is indicated as V_T = offset, threshold or firing potential.

It is quite accurate to assume that $I_D=0$ up to V_T and then increases almost linearly at a sharp slope. The value of V_T is 0.7V for Silicon diode and 0.3V for Germanium diode.

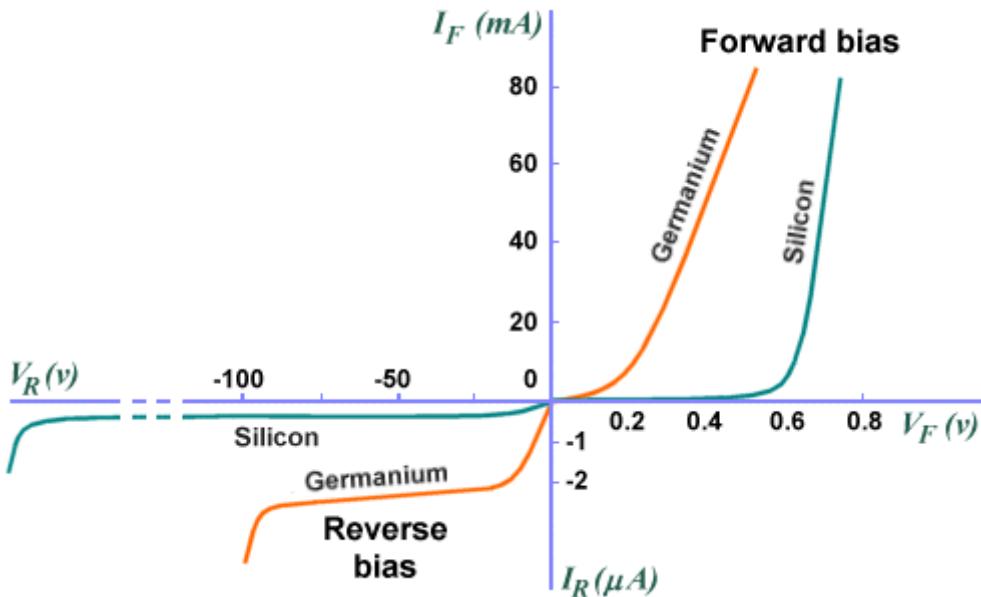


Fig 6 Diode Characteristics

NOTE:

- **ZENER REGION:** When the diode is in the reverse bias condition at some point the reverse bias voltage is so large that diode breaks down and the reverse current increases dramatically. This maximum voltage is called avalanche breakdown voltage and the current is called avalanche current. The maximum negative voltage that a diode can withstand is at Peak Inverse Voltage (PIV rating).
- **ZENER BREAKDOWN:** By heavily doping the N and P Regions, the breakdown voltage V_z can be brought as low as -10V , -5V . this mechanism of breakdown is different from avalanche.

This type of diode is called ZENER diode. When connected at a point in an electronic circuit, it does not allow the potential there to exceed the diode rated voltage.

1.3 EQUIVALENT CIRCUIT OF DIODE

1. Ideal diode

It conducts when $V_D > 0$ as shown below

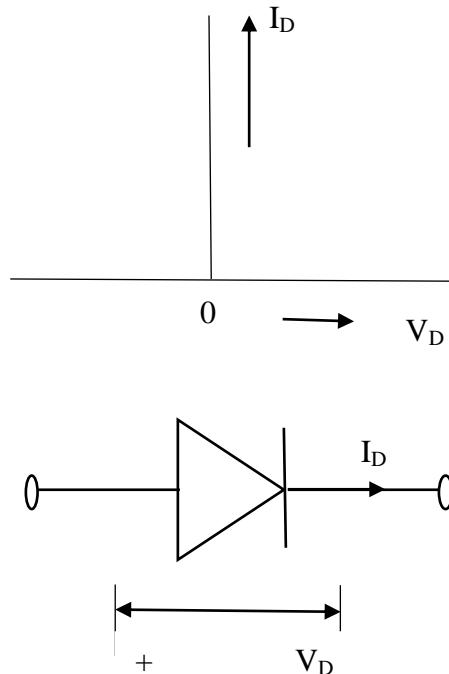


Fig 7

2. Piecewise Linear diode

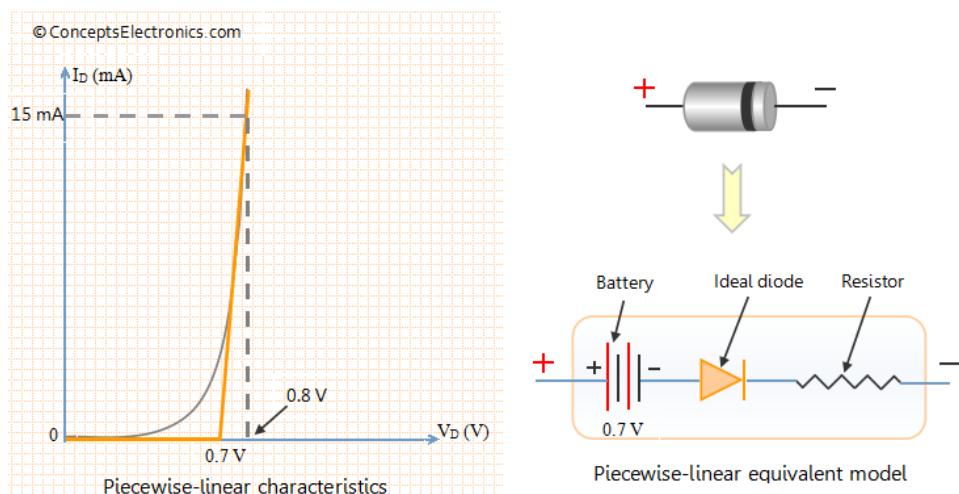


Fig 8

3. Dynamic Resistance

$$R_D = dV_D / dI \text{ (average)}$$

It can be proved that dynamic resistance on any point of the actual IV characteristics of a diode is given by $R_D = 26\text{mV} / dI$ (mA). The dynamic resistance of R_D is quite small and order of few ohms.

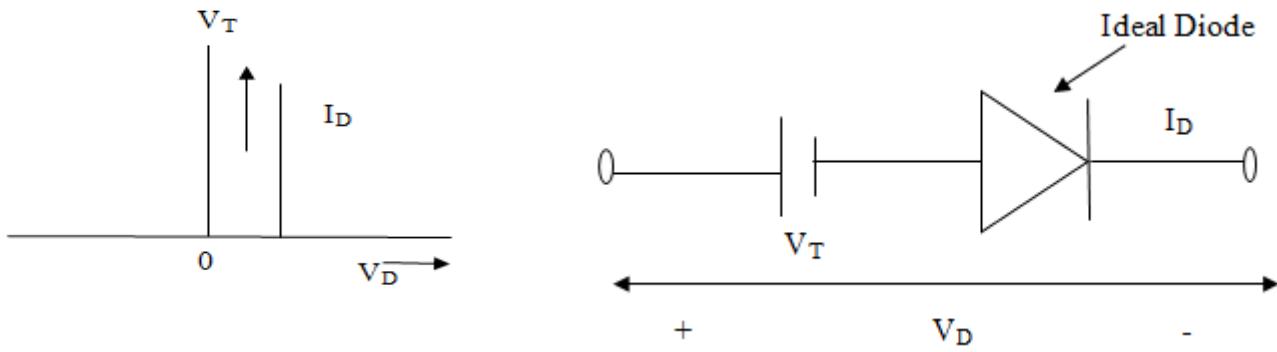


Fig 9

1.4 ZENER DIODE

A Zener diode has Zener breakdown in reverse bias as shown in IV characteristics of fig below. The symbol of Zener diode is also shown.

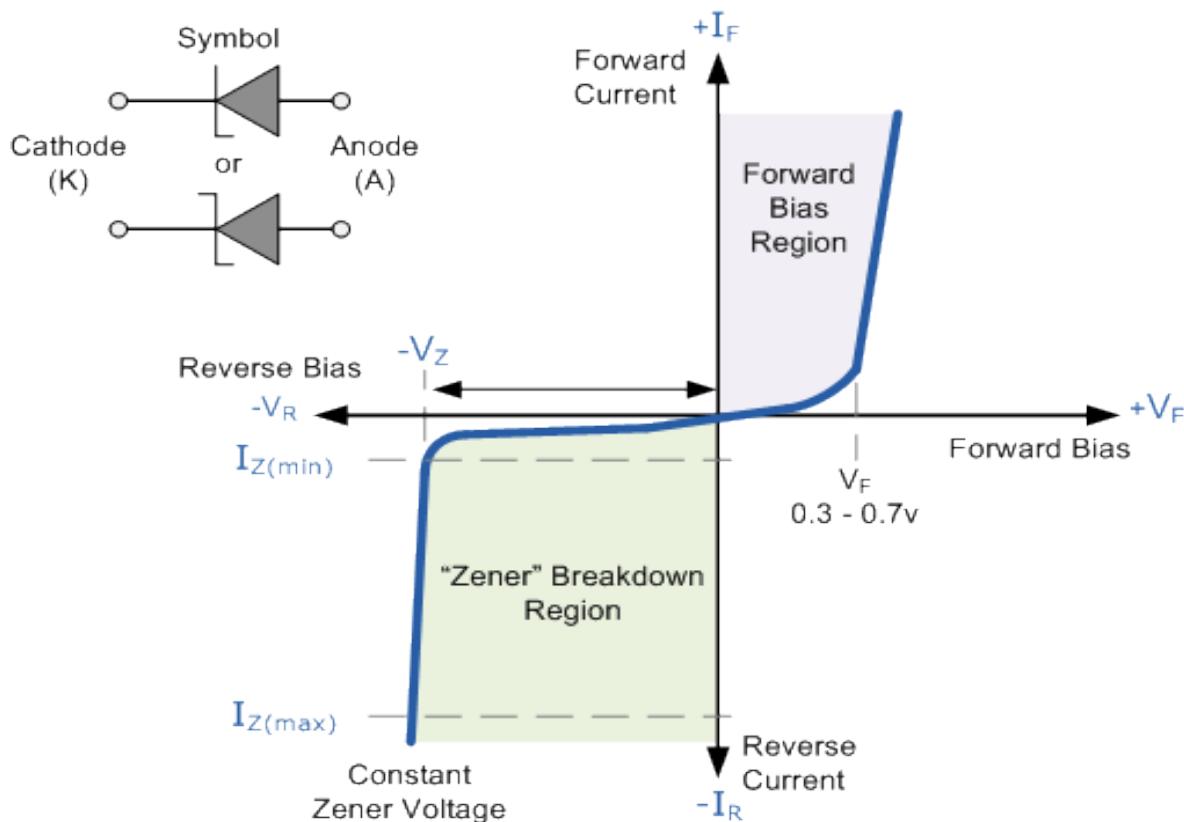


Fig 10

1.5. ZENER DIODE AS A VOLTAGE REGULATOR

Zener Diodes can be used to produce a stabilized voltage output with low ripple under varying load current conditions. By passing a small current through the diode from a voltage source, via a suitable current limiting resistor (R_S), the Zener diode will conduct sufficient current to maintain a voltage drop of V_{out} .

We remember from the previous tutorials that the DC output voltage from the half or full-wave rectifiers contains ripple superimposed onto the DC voltage and that as the load value changes so does the average output voltage. By connecting a simple Zener stabilizer circuit as shown below across the output of the rectifier, a more stable output voltage can be produced.

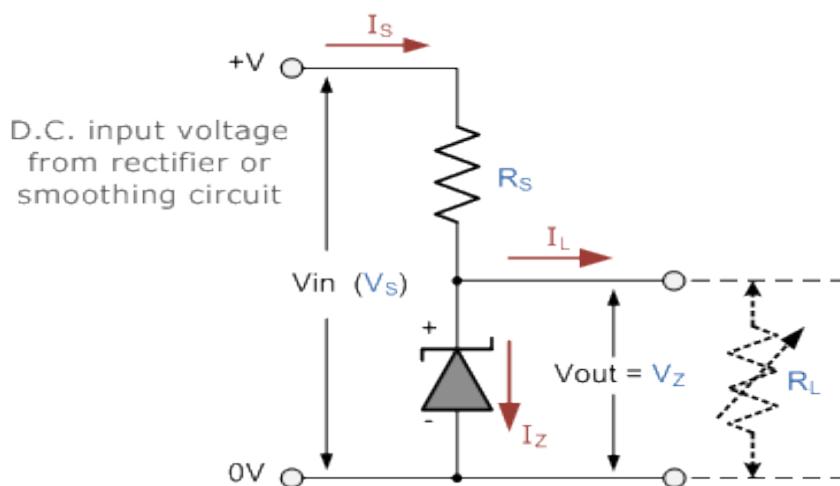


Fig 11

The resistor, R_S is connected in series with the Zener diode to limit the current flow through the diode with the voltage source, V_S being connected across the combination. The stabilised output voltage V_{out} is taken from across the Zener diode. The Zener diode is connected with its cathode terminal connected to the positive rail of the DC supply so it is reverse biased and will be operating in its breakdown condition. Resistor R_S is selected so to limit the maximum current flowing in the circuit.

With no load connected to the circuit, the load current will be zero, ($I_L = 0$), and all the circuit current passes through the Zener diode which in turn dissipates its maximum power. Also a small value of the series resistor R_S will result in a greater diode current when the load resistance R_L is connected and large as this will increase the power dissipation requirement of the diode so care must be taken when selecting the appropriate value of series resistance so that the Zener's maximum power rating is not exceeded under this no-load or high-impedance condition.

The load is connected in parallel with the Zener diode, so the voltage across R_L is always the same as the Zener voltage, ($V_R = V_Z$). There is a minimum Zener current for which the stabilization of the voltage is

effective and the Zener current must stay above this value operating under load within its breakdown region at all times. The upper limit of current is of course dependent upon the power rating of the device.

The supply voltage V_S must be greater than V_Z .

One small problem with Zener diode stabilizer circuits is that the diode can sometimes generate electrical noise on top of the DC supply as it tries to stabilize the voltage. Normally this is not a problem for most applications but the addition of a large value decoupling capacitor across the Zener's output may be required to give additional smoothing.

Then to summarize a little. A Zener diode is always operated in its reverse biased condition. A voltage regulator circuit can be designed using a Zener diode to maintain a constant DC output voltage across the load in spite of variations in the input voltage or changes in the load current. The Zener voltage regulator consists of a current limiting resistor R_S connected in series with the input voltage V_S with the Zener diode connected in parallel with the load R_L in this reverse biased condition. The stabilized output voltage is always selected to be the same as the breakdown voltage V_Z of the diode.

1.6. RECTIFICATION

"Rectifiers are the circuit which converts ac to dc". Rectifiers are grouped into two categories depending on the period of conductions.

1. Half-wave rectifier
2. Full- wave rectifier.

1.6.1. HALF-WAVE RECTIFIER

The circuit diagram of a half-wave rectifier is shown in Figure 1. 22 below along with the I/P and O/P waveforms.

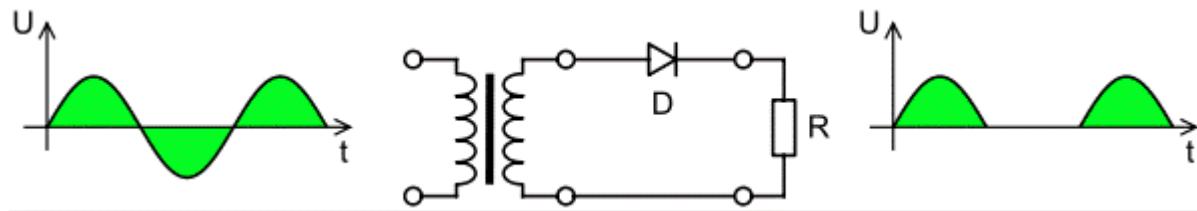


Figure 12 Half wave rectifier and its input output waveforms

The transformer is employed in order to step-down the supply voltage and also to prevent from shocks.

The diode is used to rectify AC signal while, the pulsating DC is taken across the load resistor R_L .

During the +ve half cycle, the end X of the secondary is +ve and end Y is -ve. Thus, forward biasing the diode. As the diode is forward biased, the current flows through the load R_L and a voltage is developed across it.

During the –ve half-cycle the end Y is +ve and end X is –ve thus, reverse biasing the diode. As the diode is reverse biased there is no flow of current through RL thereby the output voltage is zero.

1.6.2. THE FULL WAVE RECTIFIER

In the previous Power Diodes tutorial we discussed ways of reducing the ripple or voltage variations on a direct DC voltage by connecting capacitors across the load resistance. While this method may be suitable for low power applications it is unsuitable to applications which need a “steady and smooth” DC supply voltage. One method to improve on this is to use every half-cycle of the input voltage instead of every other half-cycle. The circuit which allows us to do this is called a Full Wave Rectifier.

Like the half wave circuit, a Full Wave Rectifier Circuit produces an output voltage or current which is purely DC or has some specified DC component. Full wave rectifiers have some fundamental advantages over their half wave rectifier counterparts. The average (DC) output voltage is higher than for half wave, the output of the full wave rectifier has much less ripple than that of the half wave rectifier producing a smoother output waveform. In a Full Wave Rectifier circuit two diodes are now used, one for each half of the cycle. A multiple winding transformer is used whose secondary winding is split equally into two halves with a common centre tapped connection, (C). This configuration results in each diode conducting in turn when its anode terminal is positive with respect to the transformer centre point C producing an output during both half-cycles, twice that for the half wave rectifier so it is 100% efficient as shown below.

Full Wave Rectifier Circuit

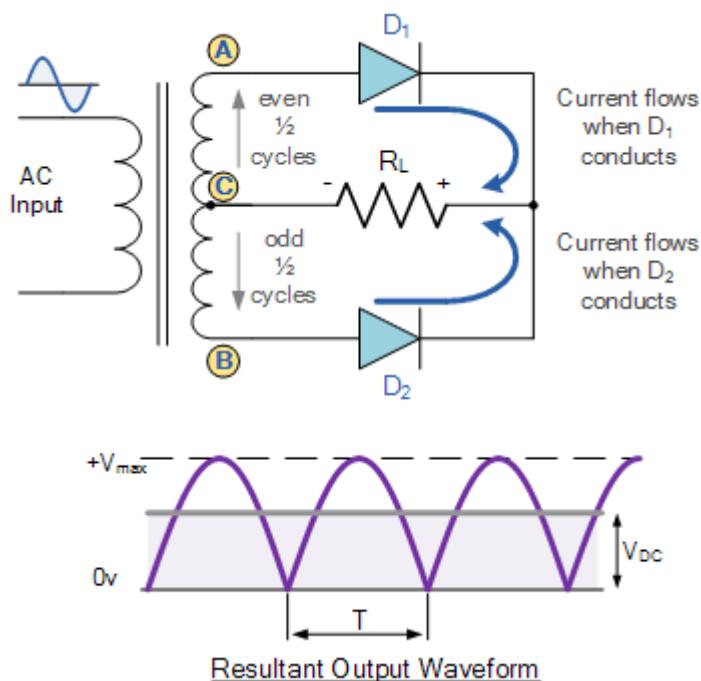


Figure 13. Center tap full wave rectifier and its input output waveforms

The full wave rectifier circuit consists of two *power diodes* connected to a single load resistance (RL) with each diode taking it in turn to supply current to the load. When point A of the transformer is positive with respect to point C, diode D1 conducts in the forward direction as indicated by the arrows.

When point B is positive (in the negative half of the cycle) with respect to point C, diode D2 conducts in the forward direction and the current flowing through resistor R is in the same direction for both half-cycles. As the output voltage across the resistor R is the phasor sum of the two waveforms combined, this type of full wave rectifier circuit is also known as a “bi-phase” circuit.

As the spaces between each half-wave developed by each diode is now being filled in by the other diode the average DC output voltage across the load resistor is now double that of the single half-wave rectifier circuit and is about 0.637V_{max} of the peak voltage, assuming no losses.

$$V_{d.c.} = \frac{2V_{\max}}{\pi} = 0.637V_{\max} = 0.9V_{RMS}$$

Where: VMAX is the maximum peak value in one half of the secondary winding and VRMS is the rms value.

The peak voltage of the output waveform is the same as before for the half-wave rectifier provided each half of the transformer windings have the same rms voltage value. To obtain a different DC voltage output different transformer ratios can be used. The main disadvantage of this type of full wave rectifier circuit is that a larger transformer for a given power output is required with two separate but identical secondary windings making this type of full wave rectifying circuit costly compared to the “Full Wave Bridge Rectifier” circuit equivalent.

1.6.3. THE FULL WAVE BRIDGE RECTIFIER

Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the Full Wave Bridge Rectifier. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop “bridge” configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

The Diode Bridge Rectifier

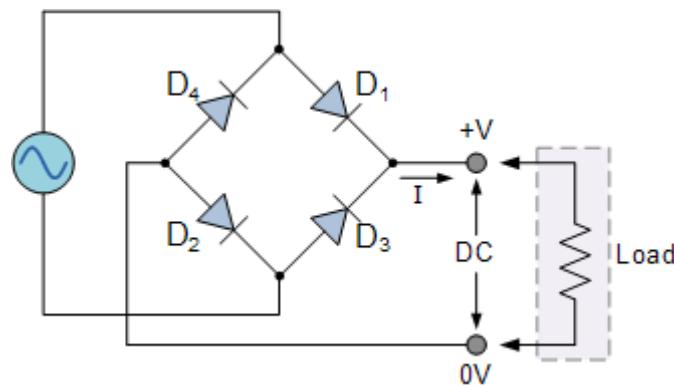


Figure 14 Full wave bridge rectifier and its input output waveforms

The four diodes labelled D1 to D4 are arranged in “series pairs” with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below.

The Positive Half-cycle

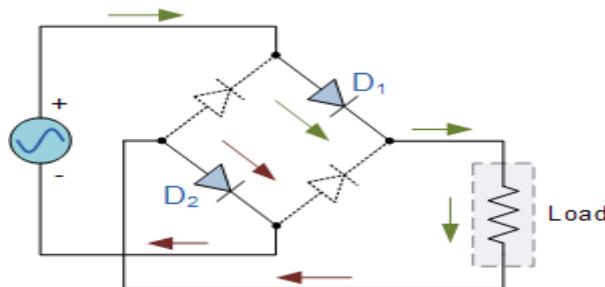


Fig 15

During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2 switch “OFF” as they are now reverse biased. The current flowing through the load is the same direction as before.

The Negative Half-cycle

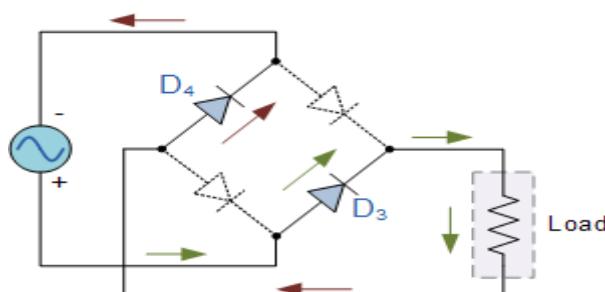


Fig 16

As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is $0.637V_{max}$.



Fig 17

Typical Bridge Rectifier

However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops ($2 \times 0.7 = 1.4V$) less than the input VMAX amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply or 120Hz for a 60Hz supply).

Although we can use four individual power diodes to make a full wave bridge rectifier, pre-made bridge rectifier components are available “off-the-shelf” in a range of different voltage and current sizes that can be soldered directly into a PCB circuit board or be connected by spade connectors.

The image to the right shows a typical single phase bridge rectifier with one corner cut off. This cut-off corner indicates that the terminal nearest to the corner is the positive or +ve output terminal or lead with the opposite (diagonal) lead being the negative or -ve output lead. The other two connecting leads are for the input alternating voltage from a transformer secondary winding.

1.6.4. THE CAPACITOR FILTER CIRCUIT

The Smoothing Capacitor

We saw in the previous section that the single phase half-wave rectifier produces an output wave every half cycle and that it was not practical to use this type of circuit to produce a steady DC supply. The full-wave bridge rectifier however, gives us a greater mean DC value ($0.637 V_{max}$) with less superimposed ripple while the output waveform is twice that of the frequency of the input supply frequency. We can therefore increase its average DC output level even higher by connecting a suitable smoothing capacitor across the output of the bridge circuit as shown below.

Full-wave Rectifier with Smoothing Capacitor

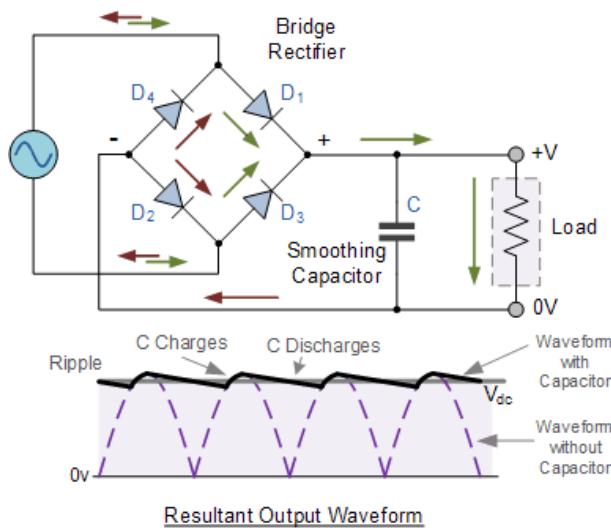


Figure 18. Bridge rectifier with capacitor filter and its input output waveforms

The smoothing capacitor converts the full-wave rippled output of the rectifier into a smooth DC output voltage. Generally, for DC power supply circuits the smoothing capacitor is an Aluminum Electrolytic type that has a capacitance value of 100μF or more with repeated DC voltage pulses from the rectifier charging up the capacitor to peak voltage.

However, there are two important parameters to consider when choosing a suitable smoothing capacitor and these are its *Working Voltage*, which must be higher than the no-load output value of the rectifier and its *Capacitance Value*, which determines the amount of ripple that will appear superimposed on top of the DC voltage.

Too low a capacitance value and the capacitor has little effect on the output waveform. But if the smoothing capacitor is sufficiently large enough (parallel capacitors can be used) and the load current is not too large, the output voltage will be almost as smooth as pure DC. As a general rule of thumb, we are looking to have a ripple voltage of less than 100mV peak to peak.

The maximum ripple voltage present for a Full Wave Rectifier circuit is not only determined by the value of the smoothing capacitor but by the frequency and load current, and is calculated as:

Bridge Rectifier Ripple Voltage

$$V_{(\text{ripple})} = \frac{I_{(\text{load})}}{f \times C}, \text{ Volts}$$

Where: I is the DC load current in amps, f is the frequency of the ripple or twice the input frequency in Hertz, and C is the capacitance in Farads.

The main advantages of a full-wave bridge rectifier is that it has a smaller AC ripple value for a given load and a smaller reservoir or smoothing capacitor than an equivalent half-wave rectifier. Therefore, the fundamental frequency of the ripple voltage is twice that of the AC supply frequency (100Hz) where for the half-wave rectifier it is exactly equal to the supply frequency (50Hz).

The amount of ripple voltage that is superimposed on top of the DC supply voltage by the diodes can be virtually eliminated by adding a much improved π -filter (pi-filter) to the output terminals of the bridge rectifier. This type of low-pass filter consists of two smoothing capacitors, usually of the same value and a choke or inductance across them to introduce a high impedance path to the alternating ripple component

Another more practical and cheaper alternative is to use an off the shelf 3-terminal voltage regulator IC, such as a LM78xx (where “xx” stands for the output voltage rating) for a positive output voltage or its inverse equivalent the LM79xx for a negative output voltage which can reduce the ripple by more than 70dB (Datasheet) while delivering a constant output current of over 1 amp.

In the next tutorial about diodes, we will look at the Zener Diode which takes advantage of its reverse breakdown voltage characteristic to produce a constant and fixed output voltage across itself.

1.7. PHOTODIODE

The field of photoelectrons has quite a variety of applications and has been attracting deep research interest. Here, we will study two types of devices- one in which light controls diode current and the other in which diode emits light when carrying current.

A photodiode is a p-n junction or PIN structure. When a photon of sufficient energy strikes the diode, it creates an electron-hole pair. This mechanism is also known as the inner photoelectric effect. If the absorption occurs in the junction's depletion region, or one diffusion length away from it, these carriers are swept from the junction by the built-in electric field of the depletion region. Thus holes move toward the anode, and electrons toward the cathode, and a photocurrent is produced. The total current through the photodiode is the sum of the dark current (current that is generated in the absence of light) and the photocurrent, so the dark current must be minimized to maximize the sensitivity of the device. It operates in reverse bias region as shown in fig below.

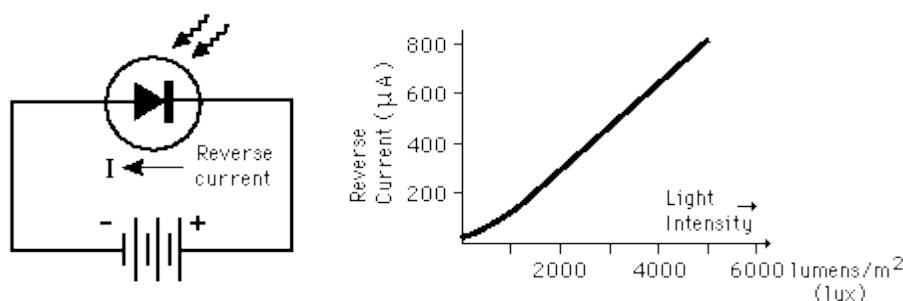


Fig 19. The IV characteristics of a photodiode is as shown in fig below.

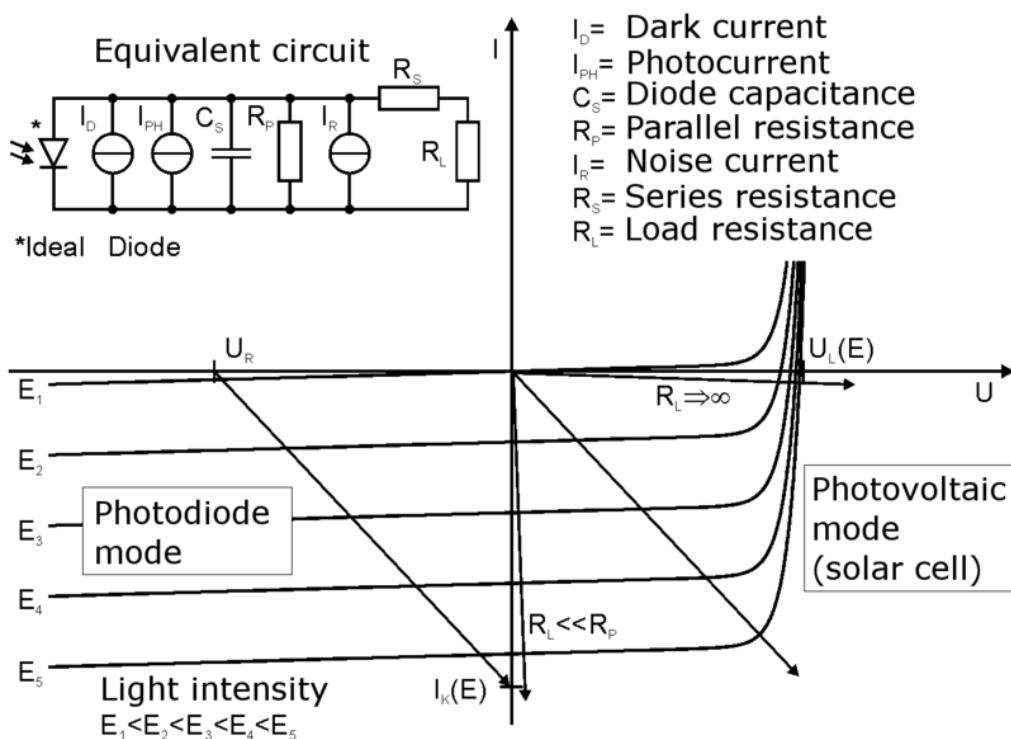


Fig 20. I-V characteristic of a photodiode.

The linear load lines represent the response of the external circuit: $I = (\text{Applied bias voltage-Diode voltage})/\text{Total resistance}$. The points of intersection with the curves represent the actual current and voltage for a given bias, resistance and illumination.

1.8. LIGHT EMITTING DIODE (LED)

Light Emitting Diodes or simply LED's, are among the most widely used of all the different types of semiconductor diodes available today and are commonly used in TV's and colour displays.

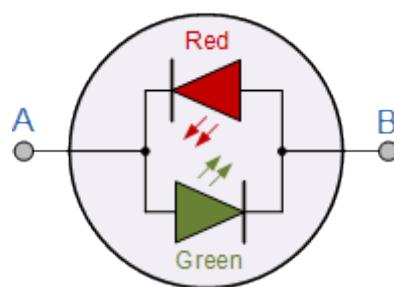


Fig 21

The “Light Emitting Diode” or LED as it is more commonly called, is basically just a specialised type of diode as they have very similar electrical characteristics to a PN junction diode. This means that an LED will pass current in its forward direction but block the flow of current in the reverse direction.

Light emitting diodes are made from a very thin layer of fairly heavily doped semiconductor material and depending on the semiconductor material used and the amount of doping, when forward biased an LED will emit a coloured light at a particular spectral wavelength.

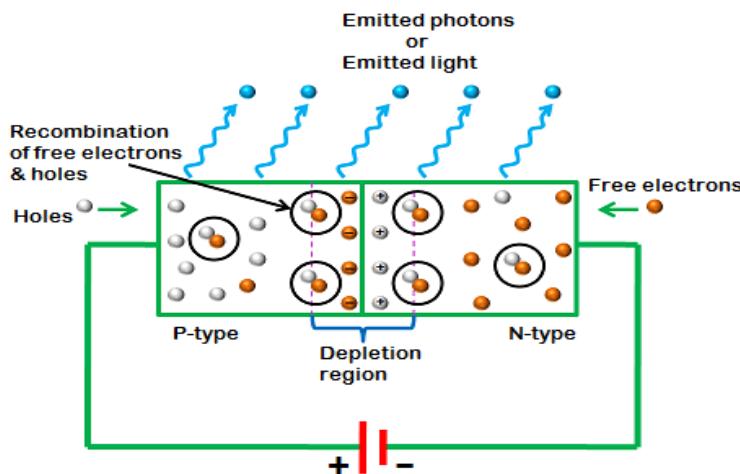
When the diode is forward biased, electrons from the semiconductors conduction band recombine with holes from the valence band releasing sufficient energy to produce photons which emit a monochromatic (single colour) of light. Because of this thin layer a reasonable number of these photons can leave the junction and radiate away producing a coloured light output.



Fig 22 LED Construction

Then we can say that when operated in a forward biased direction Light Emitting Diodes are semiconductor devices that convert electrical energy into light energy.

The construction of a Light Emitting Diode is very different from that of a normal signal diode. The PN junction of an LED is surrounded by a transparent, hard plastic epoxy resin hemispherical shaped shell or body which protects the LED from both vibration and shock. Surprisingly, an LED junction does not



Light Emitting Diode (LED)

Physics and Radio-Electronics

Fig 23

actually emit that much light so the epoxy resin body is constructed in such a way that the photons of light emitted by the junction are reflected away from the surrounding substrate base to which the diode is attached and are focused upwards through the domed top of the LED, which itself acts like a lens concentrating the amount of light. This is why the emitted light appears to be brightest at the top of the LED. However, not all LEDs are made with a hemispherical shaped dome for their epoxy shell. Some indication LEDs have a rectangular or cylindrical shaped construction that has a flat surface on top or their body is shaped into a bar or arrow. Generally, all LED's are manufactured with two legs protruding from the bottom of the body. Also, nearly all modern light emitting diodes have their cathode, (-) terminal identified by either a notch or flat spot on the body or by the cathode lead being shorter than the other as the anode (+) lead is longer than the cathode (k). Unlike normal incandescent lamps and bulbs which generate large amounts of heat when illuminated, the light emitting diode produces a "cold" generation of light which leads to high efficiencies than the normal "light bulb" because most of the generated energy radiates away within the visible spectrum. Because LEDs are solid-state devices, they can be extremely small and durable and provide much longer lamp life than normal light sources. Light Emitting Diode (LED) works only in forward bias condition. When Light Emitting Diode (LED) is forward biased, the free electrons from n-side and the holes from p-side are pushed towards the junction.

When free electrons reach the junction or depletion region, some of the free electrons recombine with the holes in the positive ions. We know that positive ions have less number of electrons than protons. Therefore, they are ready to accept electrons. Thus, free electrons recombine with holes in the depletion region. In the similar way, holes from p-side recombine with electrons in the depletion region. Because of the recombination of free electrons and holes in the depletion region, the width of depletion region decreases. As a result, more charge carriers will cross the p-n junction.

Some of the charge carriers from p-side and n-side will cross the p-n junction before they recombine in the depletion region. For example, some free electrons from n-type semiconductor cross the p-n junction and recombines with holes in p-type semiconductor. In the similar way, holes from p-type semiconductor cross the p-n junction and recombines with free electrons in the n-type semiconductor. Thus, recombination takes place in depletion region as well as in p-type and n-type semiconductor. The free electrons in the conduction band releases energy in the form of light before they recombine with holes in the valence band. In silicon and germanium diodes, most of the energy is released in the form of heat and emitted light is too small. However, in materials like gallium arsenide and gallium phosphide the emitted photons have sufficient energy to produce intense visible light.

1.9. PHOTOCOUPLED

Photo coupler generate light by using a light emitting diode (LED) to generate a current which is conducted through a phototransistor.

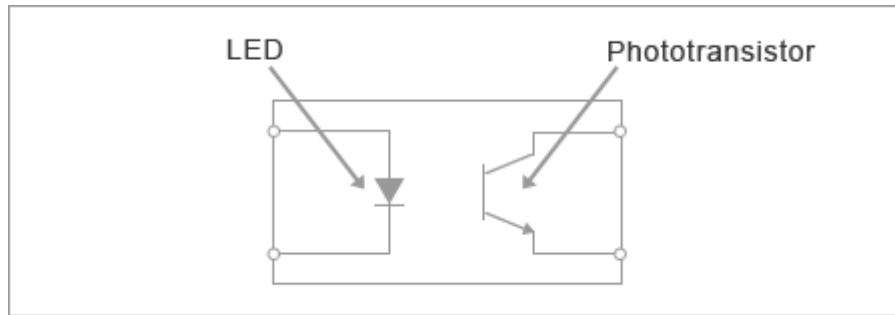


Figure 24 Internal Equivalence Circuit

Here we will describe how a general-purpose Photocoupler with this basic structure is used. Photocoupler are mainly used for the following:

1. As a switching device to transfer pulse signals.
2. To transfer feedback error signals in analog switching regulators
3. The operation of Photocoupler when used as switching devices is more basic, so we will start by describing this operation.

The key advantage of the photocoupler is the electrical isolation between two circuits. It is employed to couple circuits whose voltage level may differ by several thousand volts.

1.10. 78XX series and 7805 Fixed IC voltage regulator

The LM78XX series is typical of the 3-terminal voltage regulators. The 7805 produces an output of +5V, 7806 produces an output of +6V, and 7808 produces an output of + 8V, and so on, up to 7824, which produces an output of + 24V.

Figure 25 shows the functional block diagram for the 78XX series.

VOLTAGE REGULATOR IC - BLOCK DIAGRAM

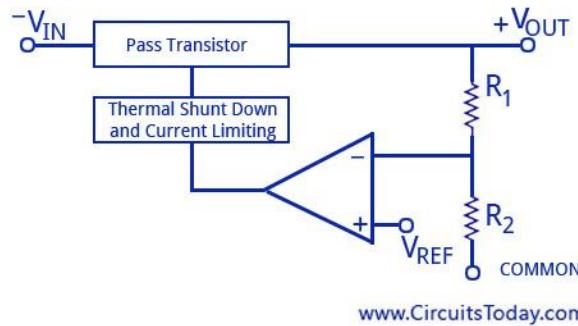


Fig 25

As shown in the block diagram above, the built-in reference voltage. V_{REF} drives the non-inverting input of the operational amplifier. There are many stages of voltage gain for the op-amp used here. This

high gain helps the op-amp to make the error voltage between the inverting and non-inverting terminals to be almost zero. Thus, the inverting input terminal value will also be the same as the non-inverting terminal, V_{REF} . Thus, the current flowing through the potential divider can be written as

$$I = V_{REF}/R_2$$

The resistor R_2 shown in the figure is not an external component connected to the IC, but an internal resistor that is built inside the IC during manufacture. Due to the conditions above, the same current flows through R_1 . Thus the output voltage can be written as

$$V_{OUT} = V_{REF}/R_2 (R_1 + R_2)$$

This shows that the output of the regulator can be controlled by putting desired values for R_1 and R_2 . The IC has a series pass transistor that can handle more than 1.5 A of load current provided that enough heat sinking is provided along with it. Like other IC's, this IC also has thermal shutdown and current limiting options. Thermal shutdown is a feature that will turn off the IC as soon as the internal temperature of the IC rises above its preset value. This rise in temperature may mostly be due to excessive external voltage, ambient temperature, or even heat sinking.

Fixed IC Voltage Regulator

The voltage regulator IC 7805 is actually a member of 78xx series of voltage regulator ICs. It is a fixed linear voltage regulator. The xx present in 78xx represents the value of the fixed output voltage that the particular IC provides. For 7805 IC, it is +5V DC regulated power supply. This regulator IC also adds

a provision for a heat sink. The input voltage to this voltage regulator can be up to 35V, and this IC can give a constant 5V for any value of input less than or equal to 35V which is the threshold limit.

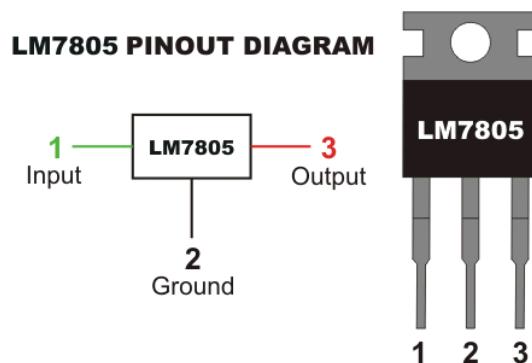


Fig 26

PIN 1-INPUT: The function of this pin is to give the input voltage. It should be in the range of 7V to 35V. An unregulated voltage is applied to this pin for regulation. For 7.2V input, the PIN achieves a maximum efficiency.

PIN 2-GROUND: The ground is connected to this pin. For output and input, this pin is equally neutral (0V).

PIN 3-OUTPUT: This pin is used to take the regulated output.

It has an output voltage of +5 volts and a maximum load current over 1A. The typical load regulation is 10mV for a load current between 5mA and 1.5 A.

The typical line regulation is 3 mV for an input voltage of 7 to 25 V. it also has a ripple rejection of 80 dB.

Applications of Voltage Regulator 7805 IC

1. Current regulator
2. Regulated dual supply
3. Building circuits for Phone charger, UPS power supply circuits, portable CD player etc
4. Fixed output regulator
5. Adjustable output regulator etc.

Module -2

FET and SCR

Structure:

- 2.1 Introduction,
- 2.2 JFET: Construction and operation,
- 2.3 JFET Drain Characteristics and Parameters,
- 2.4 JFET Transfer Characteristic, Square law expression for ID , input resistance,
- 2.5 MOSFET: Depletion and Enhancement type MOSFET- Construction,
- 2.6 Operation, Characteristics and Symbols,
- 2.7 CMOS
- 2.8 Silicon Controlled Rectifier (SCR) – Two-transistor model, switching action, Characteristics,
- 2.9 Phase control application
(Refer 3.4 up to 3.4.5 of Text 1) & (4.5 of Text 1).
(Refer 7.1, 7.2, 7.4 and 7.5 of Text 2),

2.1 INTRODUCTION

The JFET (junction field-effect transistor) is a type of FET that operates with a reverse-biased pn junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, n channel or p channel.

Basic Structure Figure 1(a) shows the basic structure of an n-channel JFET (junction field-effect transistor). Wire leads are connected to each end of the n-channel; the drain is at the upper end, and the source is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the p regions. A p-channel JFET is shown in Figure 1(b).

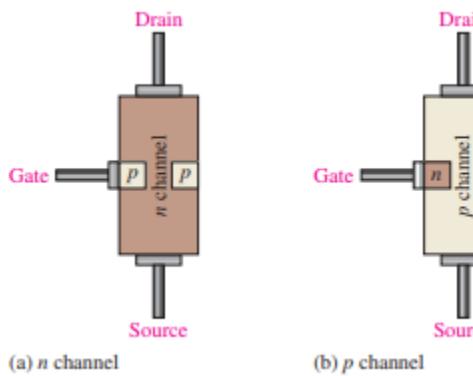


Figure : 1 A representation of the basic structure of the two types of JFET.

To illustrate the operation of a JFET, Figure 2 shows dc bias voltages applied to an n-channel device. V_{DD} provides a drain-to-source voltage and supplies current from drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source, as shown.

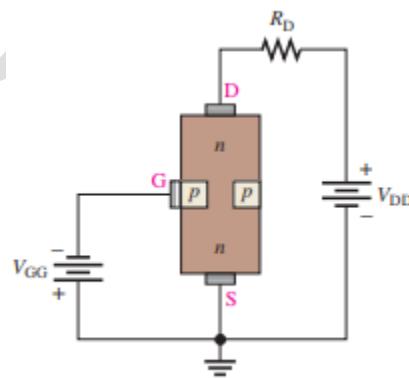
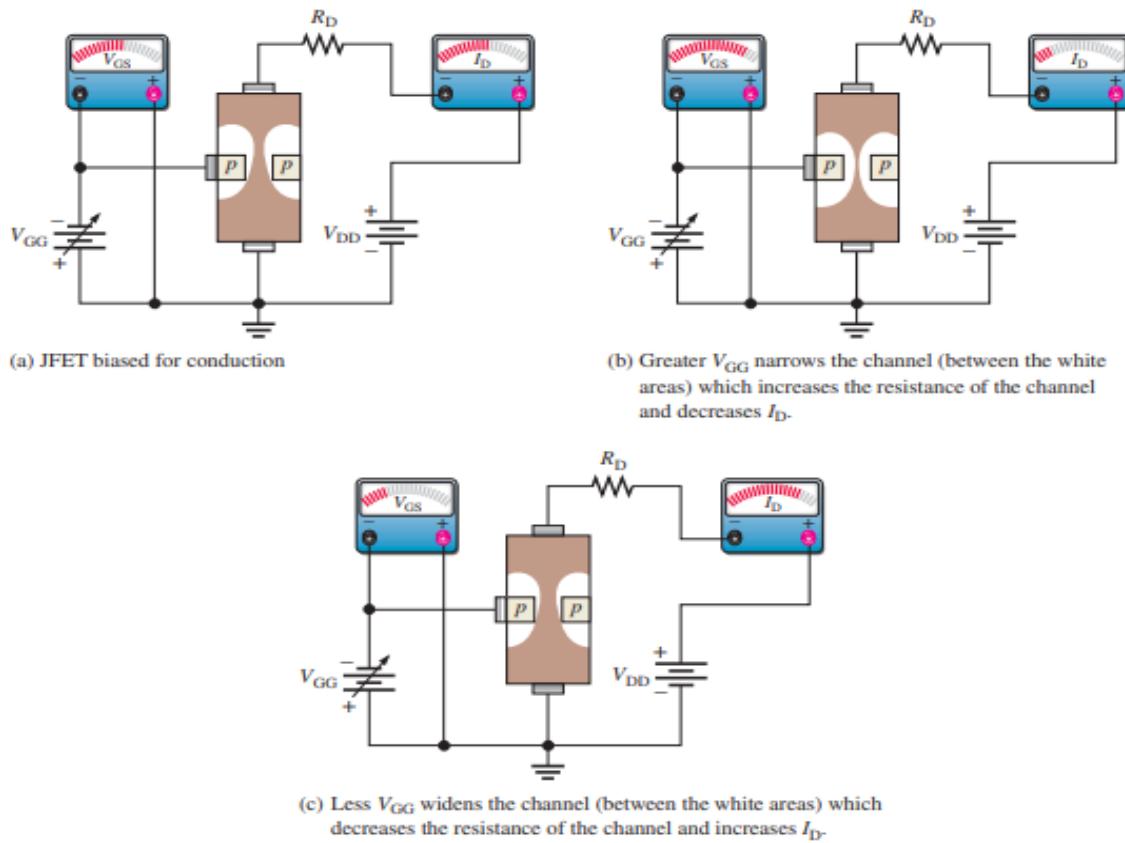


Figure: 2 A biased n-channel JFET.

The JFET is always operated with the gate-source pn junction reverse-biased. Reverse biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn junction, which extends into the n channel and thus increases its resistance by restricting the

channel width. The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, I_D . Figure 3 illustrates this concept.

The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.



2.2 JFET: Construction and operation

JFET Symbols The schematic symbols for both n-channel and p-channel JFETs are shown in Figure 4. Notice that the arrow on the gate points “in” for n channel and “out” for p channel.

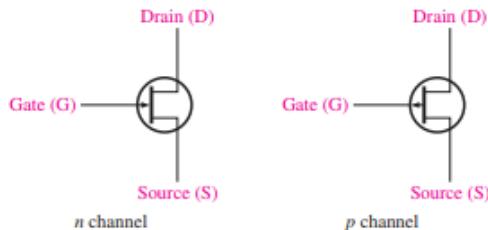


Figure 4 : JFET schematic symbols.

Drain Characteristic Curve Consider the case when the gate-to-source voltage is zero ($V_{GS} 0 \text{ V}$). This is produced by shorting the gate to the source, as in Figure 5(a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from 0 V, I_D will increase proportionally, as shown in the graph of Figure 5(b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ohmic region because V_{DS} and I_D are related by Ohm's law. At point B in Figure 5(b), the curve levels off and enters the active region where I_D becomes essentially constant. As V_{DS} increases from point B to point C, the reverse-bias.

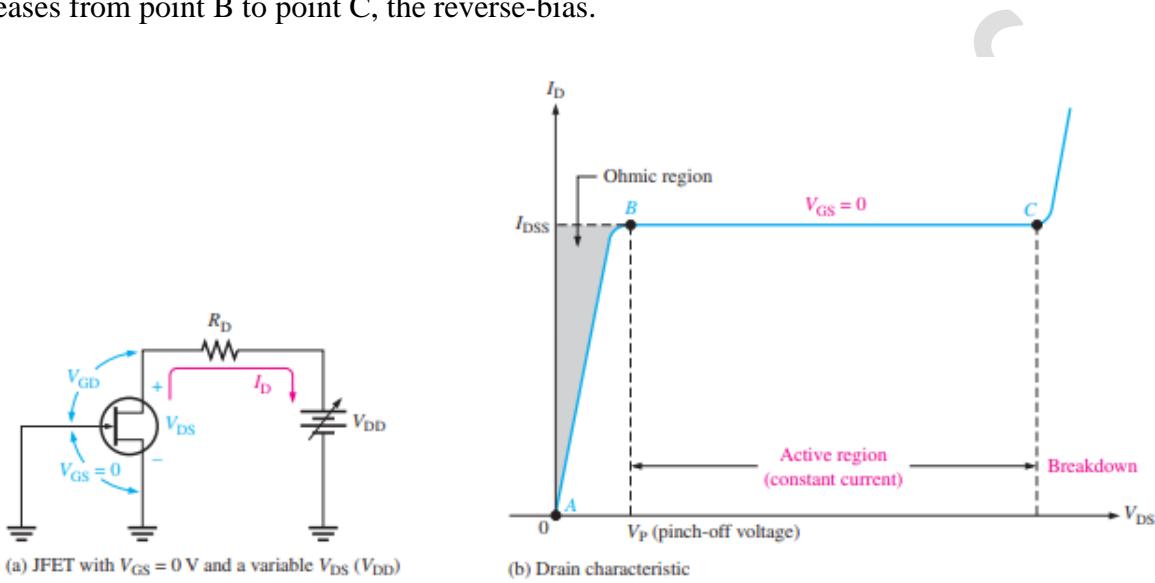


Figure 5 : The drain characteristic curve of a JFET for $V_{GS} 0 \text{ V}$ showing pinch-off voltage.

voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS} , thus keeping I_D relatively constant.

Pinch-Off Voltage

For $V_{GS} 0 \text{ V}$, the value of V_{DS} at which I_D becomes essentially constant (point B on the curve in Figure 5(b)) is the pinch-off voltage, V_P . For a given JFET, V_P has a fixed value. As you can see, a continued increase in V_{DS} above the pinch off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (Drain to Source current with gate Shorted) and is always specified on JFET datasheets. I_{DSS} is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} 0 \text{ V}$.

Breakdown As shown in the graph in Figure 5(b), breakdown occurs at point C when I_D begins to increase very rapidly with any further increase in V_{DS} . Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points B and C on the graph).

2.3 JFET Drain Characteristics and Parameters,

The JFET action that produces the drain characteristic curve to the point of breakdown for VGS 0 V is illustrated in Figure 6.

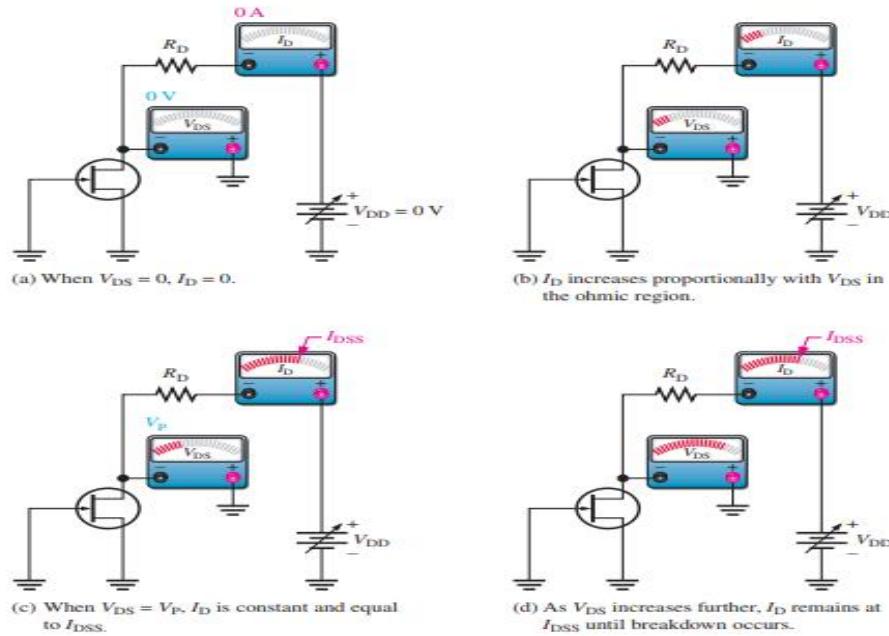


Figure 6 : JFET action that produces the characteristic curve for VGS 0 V.

VGS Controls ID

Let's connect a bias voltage, V_{GG} , from gate to source as shown in Figure 7(a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG} , a family of drain characteristic curves is produced, as shown in Figure 7(b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS} , the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_p . The term pinch-off is not the same as pinchoff voltage, V_p . Therefore, the amount of drain current is controlled by V_{GS} , as illustrated in Figure 8.

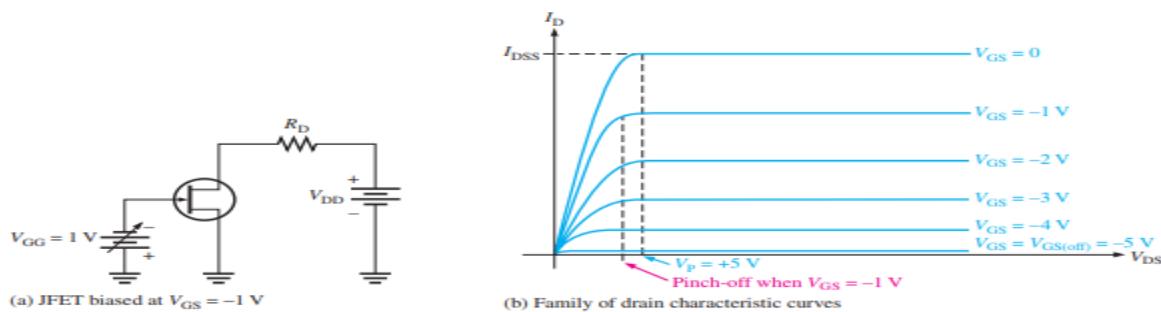


Figure 7 : Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values.

Cutoff Voltage The value of V_{GS} that makes I_D approximately zero is the cutoff voltage, $V_{GS(off)}$, as shown in Figure 8(d). The JFET must be operated between $V_{GS} 0 \text{ V}$ and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

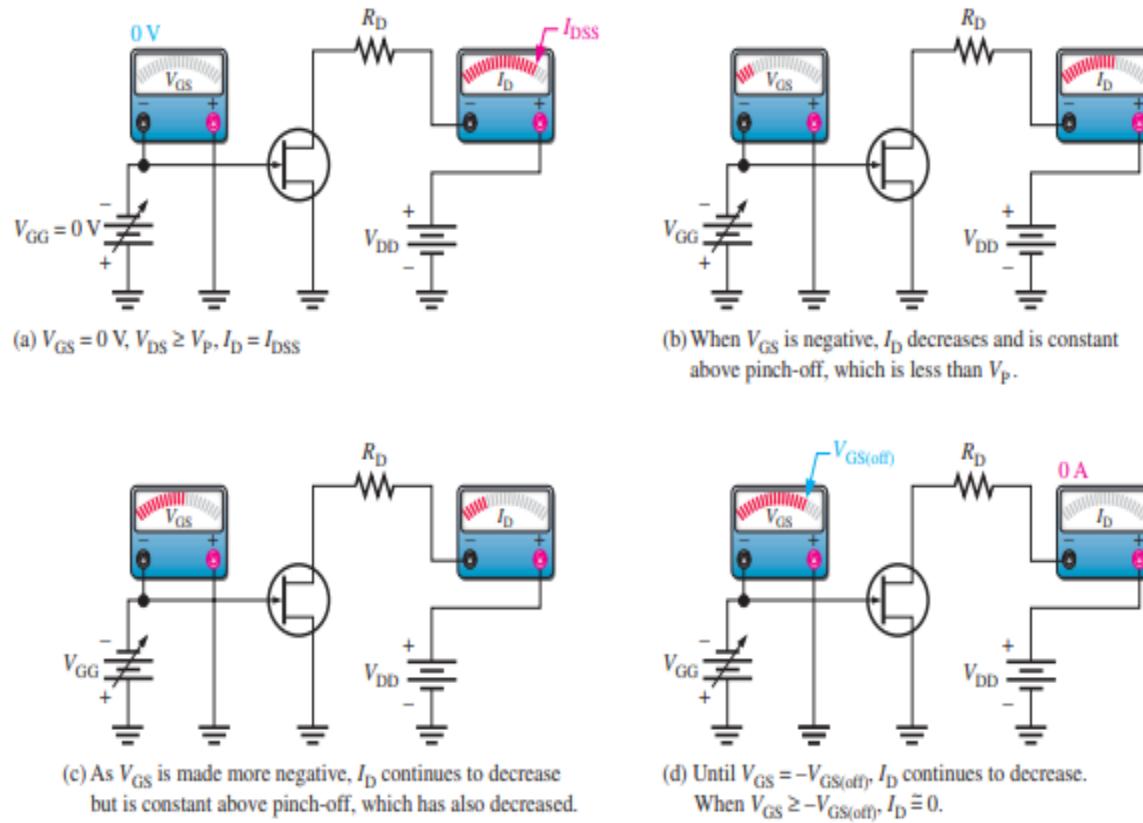
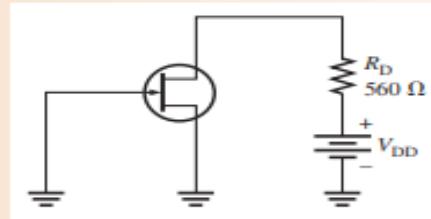


Figure 8 : VGS controls ID.

For the JFET in Figure 8–11, $V_{GS(off)} = -4 \text{ V}$ and $I_{DSS} = 12 \text{ mA}$. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation when $V_{GS} = 0 \text{ V}$.

► FIGURE 8-11



Solution Since $V_{GS(off)} = -4 \text{ V}$, $V_P = 4 \text{ V}$. The minimum value of V_{DS} for the JFET to be in its constant-current region is

$$V_{DS} = V_P = 4 \text{ V}$$

In the constant-current region with $V_{GS} = 0 \text{ V}$,

$$I_D = I_{DSS} = 12 \text{ mA}$$

The drop across the drain resistor is

$$V_{R_D} = I_D R_D = (12 \text{ mA})(560 \Omega) = 6.72 \text{ V}$$

Apply Kirchhoff's law around the drain circuit.

$$V_{DD} = V_{DS} + V_{R_D} = 4 \text{ V} + 6.72 \text{ V} = 10.7 \text{ V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

2.4 JFET Transfer Characteristic, Square law expression for I_D , input resistance,

A range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current. For an n-channel JFET, $V_{GS(off)}$ is negative, and for a p-channel JFET, $V_{GS(off)}$ is positive. Because V_{GS} does control I_D , the relationship between these two quantities is very important. Figure 8–12 is a general transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D . This curve is also known as a transconductance curve.

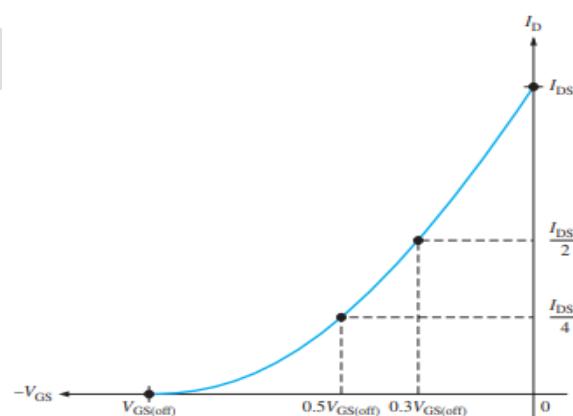


Figure 9 : Transfer Characteristic

Notice that the bottom end of the curve is at a point on the VGS axis equal to VGS(off), and the top end of the curve is at a point on the ID axis equal to IDSS. This curve shows that and The transfer

$$I_D = 0 \quad \text{when } V_{GS} = V_{GS(\text{off})}$$

$$I_D = \frac{I_{DSS}}{4} \quad \text{when } V_{GS} = 0.5V_{GS(\text{off})}$$

$$I_D = \frac{I_{DSS}}{2} \quad \text{when } V_{GS} = 0.3V_{GS(\text{off})}$$

$$I_D = I_{DSS} \quad \text{when } V_{GS} = 0$$

Characteristic curve can also be developed from the drain characteristic curves by plotting values of ID for the values of VGS taken from the family of drain curves at pinch-off, as illustrated in Figure 10 for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of VGS and ID on the drain curves.

For example, when Also, for this specific JFET, $V_{GS(\text{off})} = -5 \text{ V}$ and $I_{DSS} = 12 \text{ mA}$. $V_{GS} = -2 \text{ V}$, $ID = 4.32 \text{ mA}$. $ID = I_{DSS}$ when $V_{GS} = 0$ $ID = I_{DSS}/2$ when $V_{GS} = 0.3V_{GS(\text{off})}$ $ID = I_{DSS}/4$ when $V_{GS} = 0.5V_{GS(\text{off})}$ $ID = 0$ when $V_{GS} = V_{GS(\text{off})}$

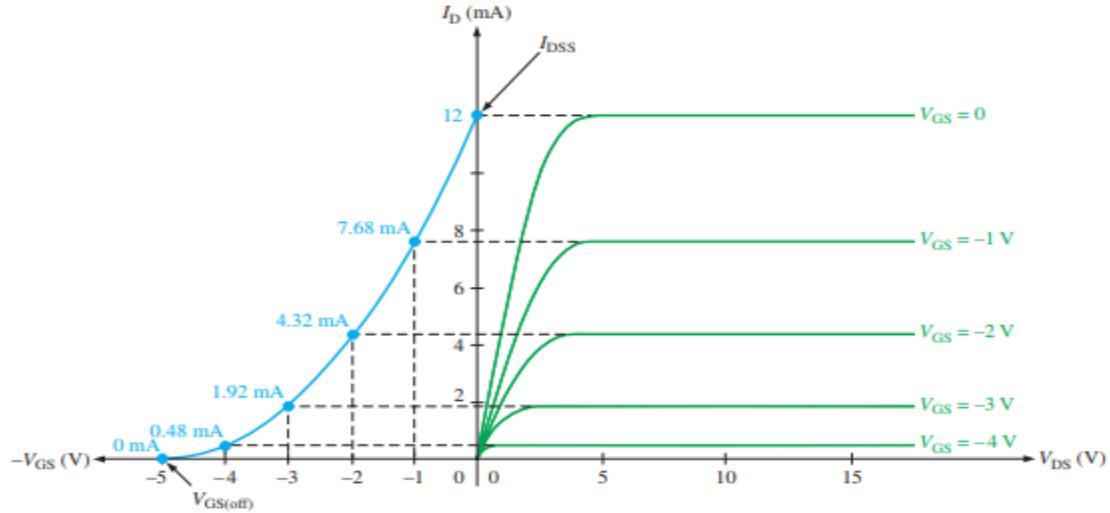


Figure 10 : n-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

A JFET transfer characteristic curve is expressed approximately as

$$I_D \cong I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

ID can be determined for any VGS if VGS(off) and IDSS are known. These quantities are usually available from the datasheet for a given JFET. Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a square law

The partial datasheet in Figure 8–14 for a 2N5459 JFET indicates that typically $I_{DSS} = 9 \text{ mA}$ and $V_{GS(\text{off})} = -8 \text{ V}$ (maximum). Using these values, determine the drain current for $V_{GS} = 0 \text{ V}$, -1 V , and -4 V .

Solution For $V_{GS} = 0 \text{ V}$,

$$I_D = I_{DSS} = 9 \text{ mA}$$

For $V_{GS} = -1 \text{ V}$, use Equation 8–1.

$$\begin{aligned} I_D &\approx I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2 = (9 \text{ mA}) \left(1 - \frac{-1 \text{ V}}{-8 \text{ V}} \right)^2 \\ &= (9 \text{ mA})(1 - 0.125)^2 = (9 \text{ mA})(0.766) = 6.89 \text{ mA} \end{aligned}$$

For $V_{GS} = -4 \text{ V}$,

$$I_D \approx (9 \text{ mA}) \left(1 - \frac{-4 \text{ V}}{-8 \text{ V}} \right)^2 = (9 \text{ mA})(1 - 0.5)^2 = (9 \text{ mA})(0.25) = 2.25 \text{ mA}$$

JFET Forward Transconductance

The forward transconductance (transfer conductance), g_m , is the change in drain current for a given change in gate-to-source voltage with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Other common designations for this parameter are gfs and yfs (forward transfer admittance). As you will see in Chapter 9, g_m is an important factor in determining the voltage gain of a FET amplifier. Because the transfer characteristic curve for a JFET is nonlinear, g_m varies in value depending on the location on the curve as set by VGS. The value for g_m is greater near the top of the curve (near $V_{GS} 0$) than it is near the bottom (near $V_{GS(\text{off})}$), as illustrated in Figure 11.

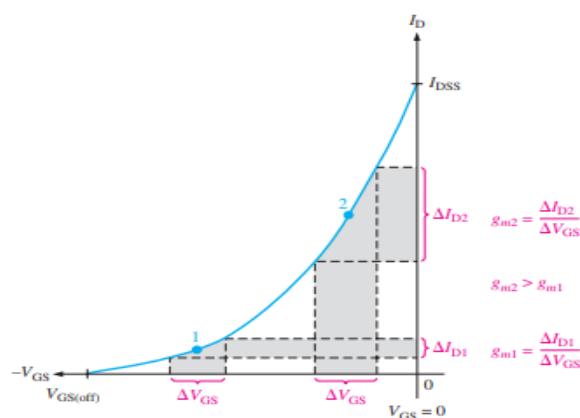


Figure 11: g_m varies depending on the bias point (V_{GS}).

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

The following information is included on the datasheet in Figure 8–14 for a 2N5457 JFET: typically, $I_{DSS} = 3.0 \text{ mA}$, $V_{GS(off)} = -6 \text{ V}$ maximum, and $g_{fs(max)} = 5000 \mu\text{S}$. Using these values, determine the forward transconductance for $V_{GS} = -4 \text{ V}$, and find I_D at this point.

Solution $g_{m0} = g_{fs} = 5000 \mu\text{S}$. Use Equation 8–2 to calculate g_m

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right) = (5000 \mu\text{S}) \left(1 - \frac{-4 \text{ V}}{-6 \text{ V}} \right) = 1667 \mu\text{S}$$

Next, use Equation 8–1 to calculate I_D at $V_{GS} = -4 \text{ V}$.

$$I_D \cong I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 = (3.0 \text{ mA}) \left(1 - \frac{-4 \text{ V}}{-6 \text{ V}} \right)^2 = 333 \mu\text{A}$$

MOSFET

The MOSFET (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor. The MOSFET, different from the JFET, has no pn junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. The two basic types of MOSFETs are enhancement (E) and depletion (D). Of the two types, the enhancement MOSFET is more widely used. Because polycrystalline silicon is now used for the gate material instead of metal, these devices are sometimes called IGFETs (insulated-gate FETs).

Enhancement MOSFET (E-MOSFET)

The E-MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET, which is discussed next, in that it has no structural channel. Notice in Figure 12(a) that the substrate extends completely to the SiO_2 layer. For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure 12 (b). The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area. For any gate voltage below the threshold value, there is no channel.

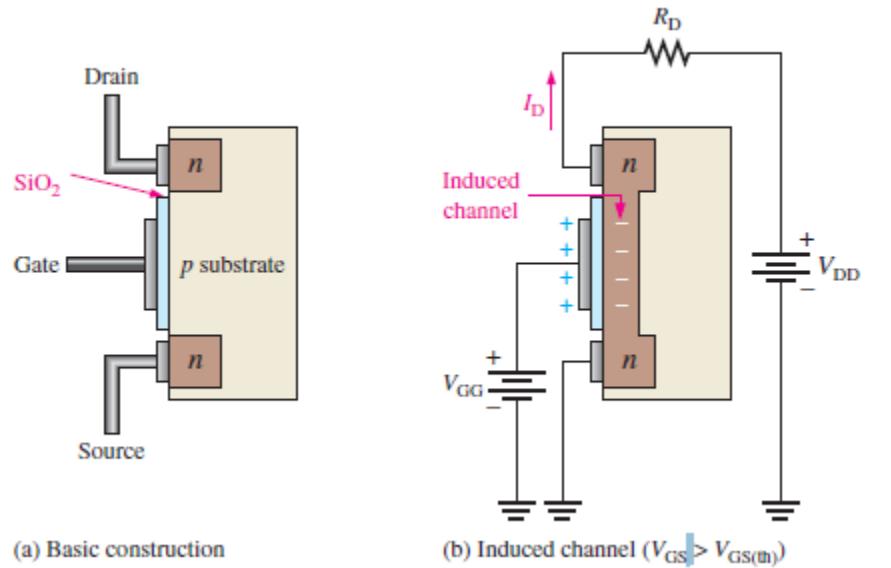


Figure12 : Representation of the basic E-MOSFET construction and operation (n-channel).

The schematic symbols for the n-channel and p-channel E-MOSFETs are shown in Figure 13. The broken lines symbolize the absence of a physical channel. An inward pointing substrate arrow is for n channel, and an outward-pointing arrow is for p channel. Some E-MOSFET devices have a separate substrate connection.

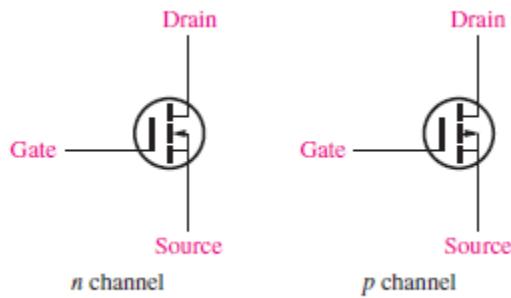


Figure13: E-MOSFET schematic symbols.

Depletion MOSFET (D-MOSFET)

Another type of MOSFET is the depletion MOSFET (D-MOSFET), and Figure 14 illustrates its basic structure. The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. Both n-channel and p-channel devices are shown in the figure. We will use the n-channel device to describe the basic operation. The p-channel operation is the same, except the voltage polarities are opposite those of the n-channel.

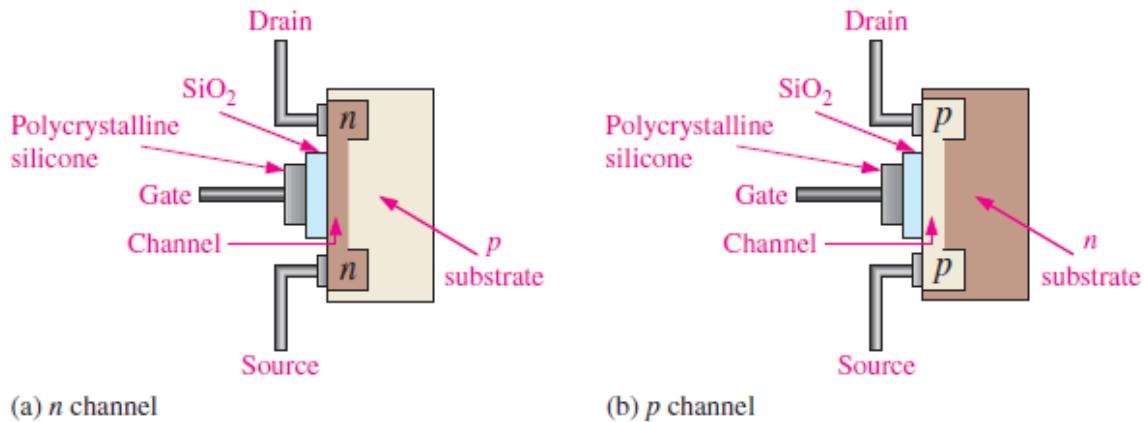
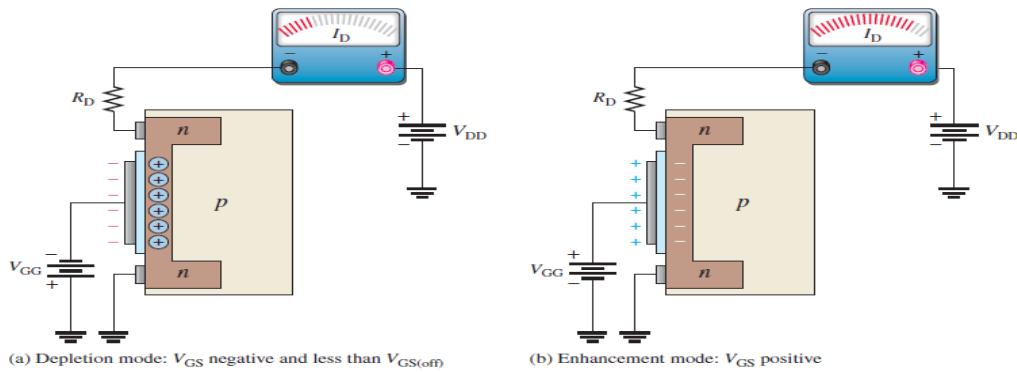


Figure 14: Representation of the basic structure of D-MOSFETs.

The D-MOSFET can be operated in either of two modes—the depletion mode or the enhancement mode—and is sometimes called a depletion/enhancement MOSFET. Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied. The n-channel MOSFET operates in the depletion mode when a negative gate-to-source voltage is applied and in the enhancement mode when a positive gate-to-source voltage is applied. These devices are generally operated in the depletion mode.

Depletion Mode Visualize the gate as one plate of a parallel-plate capacitor and the channel as the other plate. The silicon dioxide insulating layer is the dielectric. With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel conductivity.

The greater the negative voltage on the gate, the greater the depletion of n-channel electrons. At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure 15(a). Like the n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero. In addition, the D-MOSFET conducts for values of V_{GS} above zero.

Figure 15: Operation of *n*-channel

D-MOSFET. Enhancement Mode With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure 15(b).

2.8 Silicon Controlled Rectifier (SCR) – Two-transistor model, switching action, Characteristics,

An **SCR** (silicon-controlled rectifier) is a 4-layer *pnpn* device similar to the 4-layer diode except with three terminals: anode, cathode, and gate. The basic structure of an SCR is shown in Figure 16 (a), and the schematic symbol is shown in Figure 16(b). Typical SCR packages are shown in Figure 16 (c). Other types of thyristors are found in the same or similar packages.

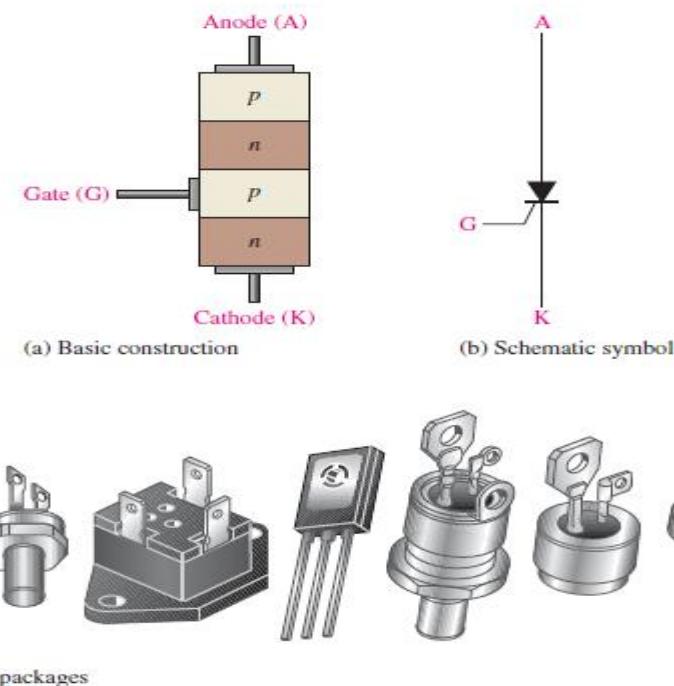


Figure 16 : The silicon-controlled rectifier (SCR).

SCR Equivalent Circuit

Like the 4-layer diode operation, the SCR operation can best be understood by thinking of its internal pnpn structure as a two-transistor arrangement, as shown in Figure 17. This structure is like that of the 4-layer diode except for the gate connection. The upper pnp layers act as a transistor, , and the lower npn layers act as a transistor, . Again, notice that the two middle layers are “shared.”

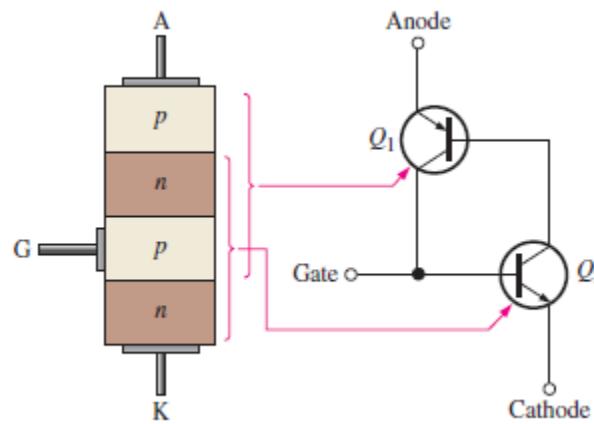


Figure 17 : SCR Equivalent Circuit

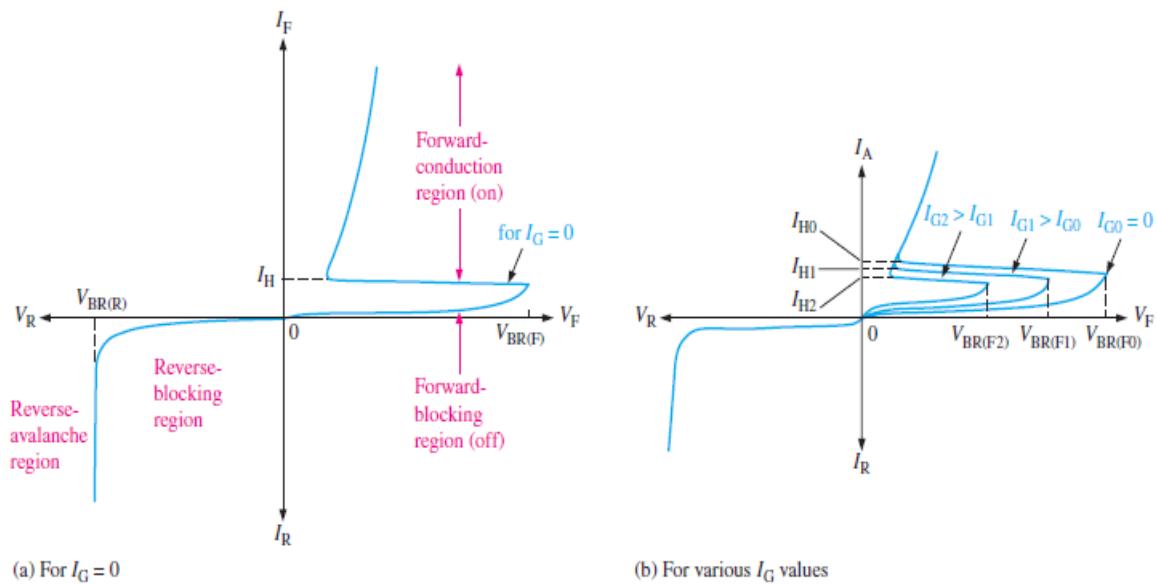


Figure 18 : SCR characteristic curves.

2.9 Phase control application

The SCR is used in many applications, including motor controls, time-delay circuits, heater controls, phase controls, relay controls, and sawtooth generators.

A common application of SCRs is in the control of ac power for lamp dimmers, electric heaters, and electric motors. A half-wave, variable-resistance, phase-control circuit is shown in Figure 19, 120 V ac are applied across terminals A and B; represents the resistance of the load (for example, a heating element or lamp filament). Resistor limits the current, and potentiometer R2 sets the trigger level for the SCR.

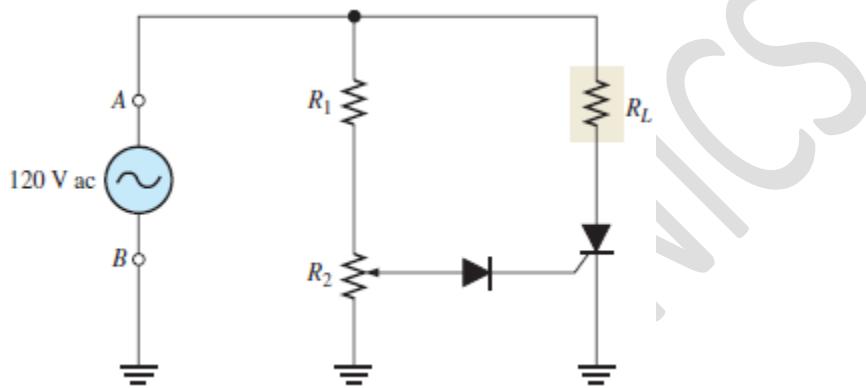


Figure 19 : Half-wave, variable-resistance, phase control circuit.

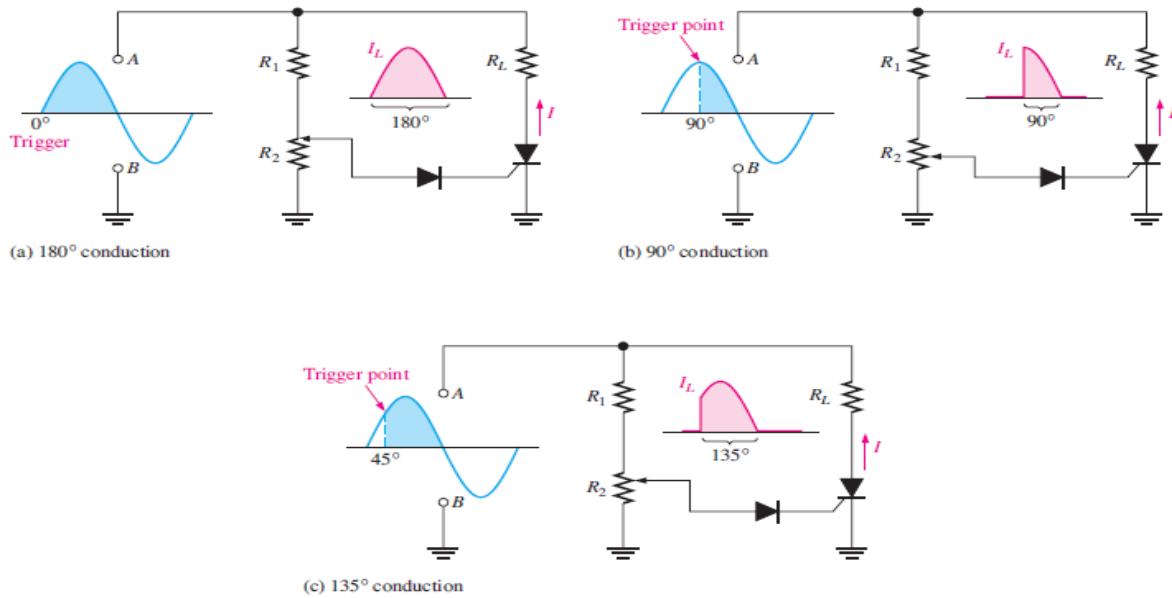


Figure 19: Operation of the phase-control circuit.

Module -3

Operational Amplifiers and Applications

Structure:

3.1 Introduction to Op-Amp, Op-Amp Input Modes

3.2 Op-Amp Parameters-CMRR, Input Offset Voltage and Current, Input Bias Current, Input and Output Impedance, Slew Rate

3.3 Applications of Op-Amp –

- Inverting amplifier,
- Non-Inverting amplifier,
- Summer,
- Voltage follower,
- Integrator,
- Differentiator and
- Comparator

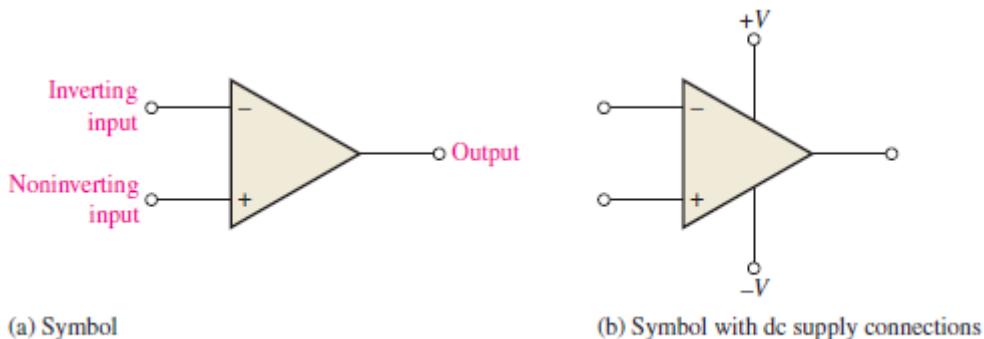
3.4 Outcomes

3.1 Introduction to Op-Amp

As well as resistors and capacitors, **Operational Amplifiers**, or **Op-amps** as they are more commonly called, are one of the basic building blocks of Analogue Electronic Circuits. *Operational amplifiers* are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation.

An **Operational Amplifier**, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or “operation” of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of “Operational Amplifier”.

An *Operational Amplifier* is basically a three-terminal device which consists of two high impedance inputs, one called the **Inverting Input**, marked with a negative or “minus” sign, (-) and the other one called the **Non-inverting Input**, marked with a positive or “plus” sign (+).



The Ideal Op-Amp

To illustrate what an op-amp is, let's consider its ideal characteristics. A practical op-amp, of course, falls short of these ideal standards, but it is much easier to understand and analyze the device from an ideal point of view. First, the ideal op-amp has *infinite voltage gain* and *infinite bandwidth*. Also, it has an *infinite input impedance* (open) so that it does not load the driving source. Finally, it has a *zero output impedance*. Op-amp characteristics are illustrated in Figure 1(a). The input voltage, V_{in} , appears between the two input terminals, and the

output voltage is $A_v V_{in}$, as indicated by the internal voltage source symbol. The concept of infinite input impedance is

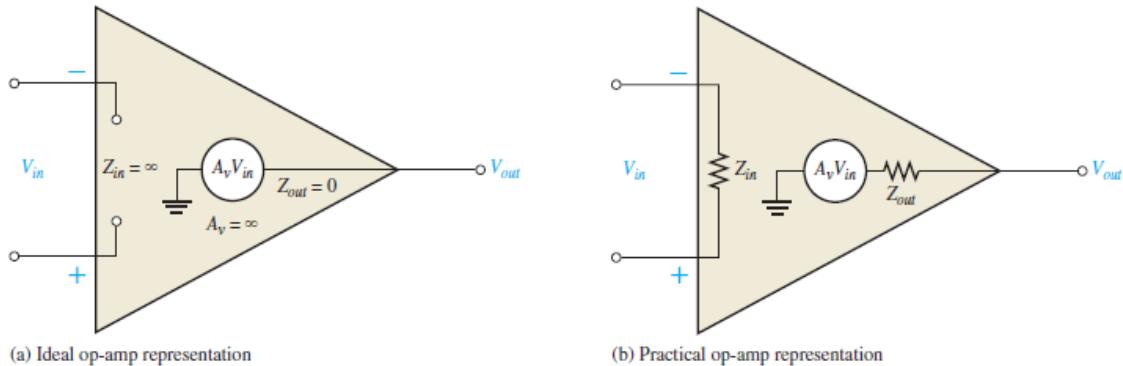


Figure 1: Basic op-amp representations

The Practical Op-Amp

Although integrated circuit (IC) op-amps approach parameter values that can be treated as ideal in many cases, the ideal device can never be made. Any device has limitations, and the IC op-amp is no exception. Op-amps have both voltage and current limitations. Peak-to-peak output voltage, for example, is usually limited to slightly less than the two supply voltages. Output current is also limited by internal restrictions such as power dissipation and component ratings. Characteristics of a practical op-amp are very high voltage gain, very high input impedance, and very low output impedance. These are labelled in Figure 1(b).

Another practical

consideration is that there is always noise generated within the op-amp. Noise is an undesired signal that affects the quality of a desired signal. Today, circuit designers are using smaller voltages that require high accuracy, so low-noise components are in greater demand. All circuits generate noise; op-amps are no exception, but the amount can be minimized.

Internal Block Diagram of an Op-Amp A typical op-amp is made up of three types of amplifier circuits: a differential amplifier, a voltage amplifier, and a push-pull amplifier, as shown in Figure 2. The differential amplifier is the input stage for the op-amp. It provides amplification of the difference voltage between the two inputs. The second stage is usually a class A amplifier that provides additional gain. Some op-amps may have more than one voltage amplifier stage. A push-pull class B amplifier is typically used for the output stage.

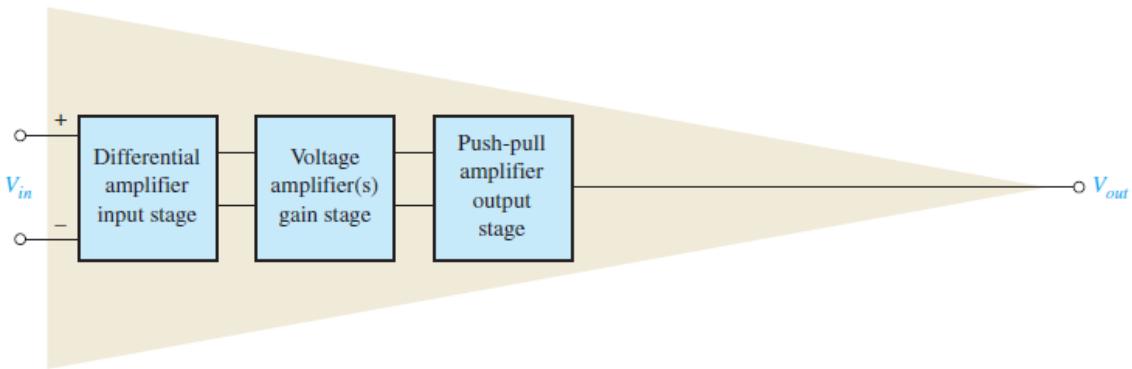


Figure 3: Basic internal arrangement of an op-amp.

Op-amp input modes

Input Signal Modes

Recall that the input signal modes are determined by the differential amplifier input stage of the op-amp. Differential Mode In the differential mode, either one signal is applied to an input with the other input grounded or two opposite-polarity signals are applied to the inputs. When an op-amp is operated in the single-ended differential mode, one input is grounded and a signal voltage is applied to the other input, as shown in Figure 4(a). In the case where the signal voltage is applied to the inverting input as in part (a), an inverted, amplified signal voltage appears at the output. In the case where the signal is applied to the noninverting input with the inverting input grounded, as in Figure 4(b), a noninverted, amplified signal voltage appears at the output

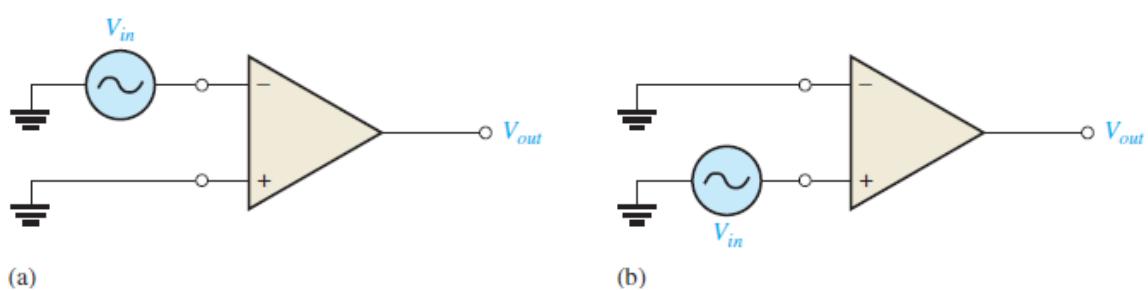


Figure 4: Single-ended differential mode.

In the double-ended differential mode, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure 5(a). The amplified difference between the two inputs appears on the output. Equivalently, the double-ended differential mode can be represented by a single source connected between the two inputs, as shown in Figure 5(b).

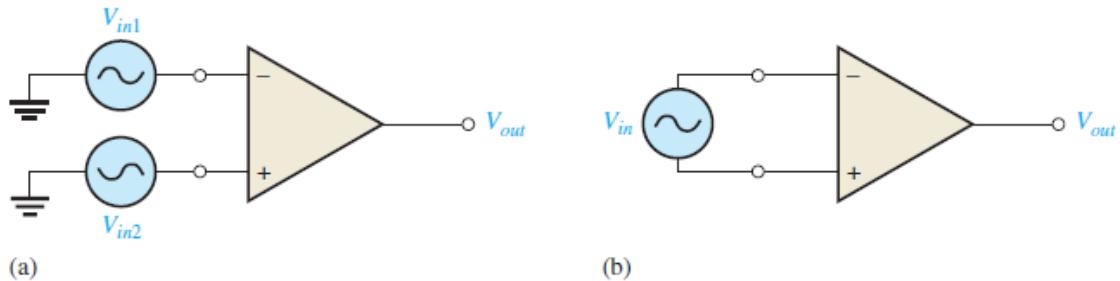
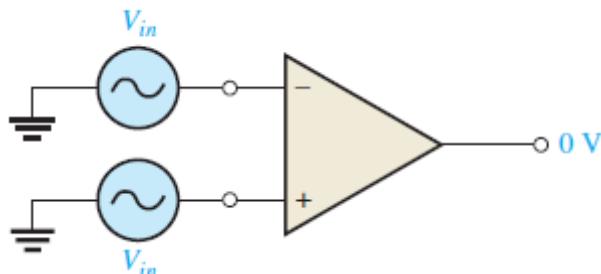


Figure 5: Double-ended differential mode.

Common Mode In the common mode, two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure 6. When equal input signals are applied to both inputs, they tend to cancel, resulting in a zero output voltage.



This action is called common-mode rejection. Its importance lies in the situation where an unwanted signal appears commonly on both op-amp inputs. Common-mode rejection means that this unwanted signal will not appear on the output and distort the desired signal. Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines, from adjacent lines, the 60 Hz power line, or other sources.

Op-Amp Parameters

Common-Mode Rejection Ratio Desired signals can appear on only one input or with opposite polarities on both input lines. These desired signals are amplified and appear on the output as previously discussed. Unwanted signals (noise) appearing with the same polarity on

both input lines are essentially cancelled by the op-amp and do not appear on the output. The measure of an amplifier's ability to reject common-mode signals is a parameter called the CMRR (common-mode rejection ratio). Ideally, an op-amp provides a very high gain for differential-mode signals and zero gain for common-mode signals. Practical op-amps, however, do exhibit a very small common-mode gain (usually much less than 1), while providing a high open-loop differential voltage gain (usually several thousand). The higher the open-loop gain with respect to the common-mode gain, the better the performance of the op-amp in terms of rejection of common-mode signals.

This suggests that a good measure of the op-amp's performance in rejecting unwanted common-mode signals is the ratio of the open-loop differential voltage gain, A_{ol} , to the common-mode gain, A_{cm} . This ratio is the common-mode rejection ratio, CMRR.

$$\text{CMRR} = \frac{A_{ol}}{A_{cm}}$$

The higher the CMRR, the better. A very high value of CMRR means that the open-loop gain, A_{ol} , is high and the common-mode gain, A_{cm} , is low.

The CMRR is often expressed in decibels (dB) as

$$\text{CMRR} = 20 \log \left(\frac{A_{ol}}{A_{cm}} \right)$$

A certain op-amp has an open-loop differential voltage gain of 100,000 and a common-mode gain of 0.2. Determine the CMRR and express it in decibels.

$A_{ol} = 100,000$, and $A_{cm} = 0.2$. Therefore,

$$\text{CMRR} = \frac{A_{ol}}{A_{cm}} = \frac{100,000}{0.2} = 500,000$$

Expressed in decibels,

$$\text{CMRR} = 20 \log (500,000) = 114 \text{ dB}$$

Determine the CMRR and express it in dB for an op-amp with an open-loop differential voltage gain of 85,000 and a common-mode gain of 0.25.

Input Offset Voltage The ideal op-amp produces zero volts out for zero volts in. In a practical op-amp, however, a small dc voltage, $V_{OUT}(\text{error})$, appears at the output when no differential input voltage is applied. Its primary cause is a slight mismatch of the baseemitter voltages of the differential amplifier input stage of an op-amp. As specified on an op-amp datasheet, the input offset voltage, V_{OS} , is the differential dc voltage required between the inputs to force the output to zero volts. Typical values of input offset voltage are in the range of 2 mV or less. In the ideal case, it is 0 V. The input offset voltage drift is a parameter related to V_{OS} that specifies how much change occurs in the input offset voltage for each degree change in temperature. Typical values range anywhere from about per degree Celsius to about per degree Celsius. Usually, an op-amp with a higher nominal value of input offset voltage exhibits a higher drift.

Input Bias Current You have seen that the input terminals of a bipolar differential amplifier are the transistor bases and, therefore, the input currents are the base currents. The input bias current is the dc current required by the inputs of the amplifier to properly operate the first stage. By definition, the input bias current is the average of both input currents and is calculated as follows:

$$I_{BIAS} = \frac{I_1 + I_2}{2}$$

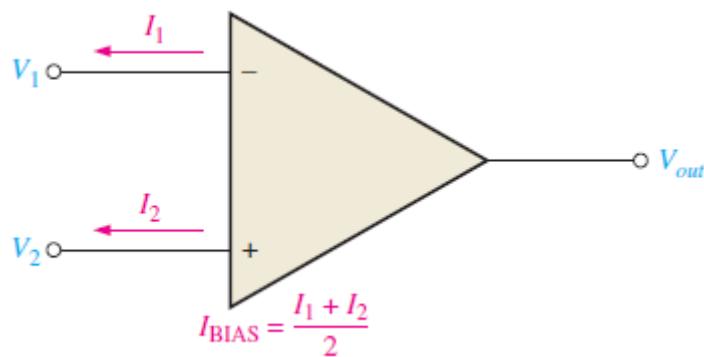


Figure 6: Input bias current is the average of the two op-amp input currents.

Input Impedance Two basic ways of specifying the input impedance of an op-amp are the differential and the common mode. The differential input impedance is the total resistance between the inverting and the noninverting inputs, as illustrated in Figure 7(a). Differential impedance is measured by determining the change in bias current for a given change in

differential input voltage. The common-mode input impedance is the resistance between each input and ground and is measured by determining the change in bias current for a given change in common-mode input voltage. It is depicted in Figure 7(b).

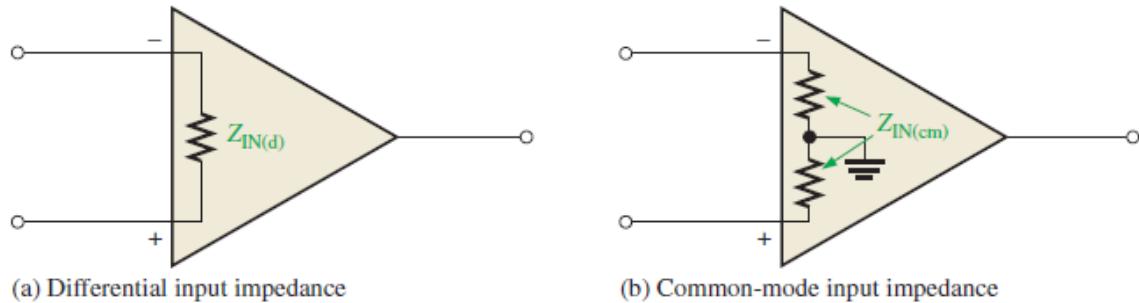


Figure 7: Op-amp input impedance.

Input Offset Current Ideally, the two input bias currents are equal, and thus their difference is zero. In a practical op-amp, however, the bias currents are not exactly equal. The input offset current, IOS, is the difference of the input bias currents, expressed as an absolute value.

$$I_{OS} = |I_1 - I_2|$$

Actual magnitudes of offset current are usually at least an order of magnitude (ten times) less than the bias current. In many applications, the offset current can be neglected. However, high-gain, high-input impedance amplifiers should have as little IOS as possible because the difference in currents through large input resistances develops a substantial offset voltage, as shown in Figure 8.

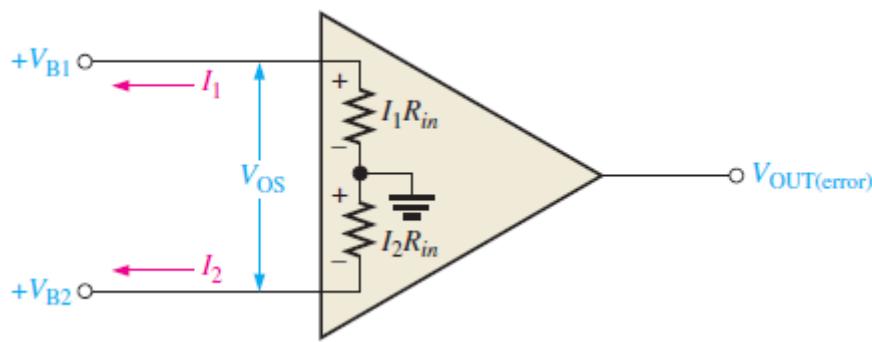


Figure 8: Effect of input offset current.

Output Impedance The output impedance is the resistance viewed from the output terminal of the op-amp, as indicated in Figure 9.

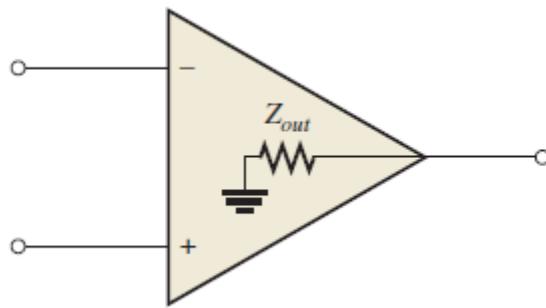


Figure 9: Output Impedance

Slew Rate The maximum rate of change of the output voltage in response to a step input voltage is the slew rate of an op-amp. The slew rate is dependent upon the high-frequency response of the amplifier stages within the op-amp. Slew rate is measured with an op-amp connected as shown in Figure 10(a). This particular op-amp connection is a unity-gain, non inverting configuration. It gives a worst-case (slowest) slew rate. Recall that the high frequency components of a voltage step are contained in the rising edge and that the upper critical frequency of an amplifier limits its response to a step input. For a step input, the slope on the output is inversely proportional to the upper critical frequency. Slope increases as upper critical frequency decreases.

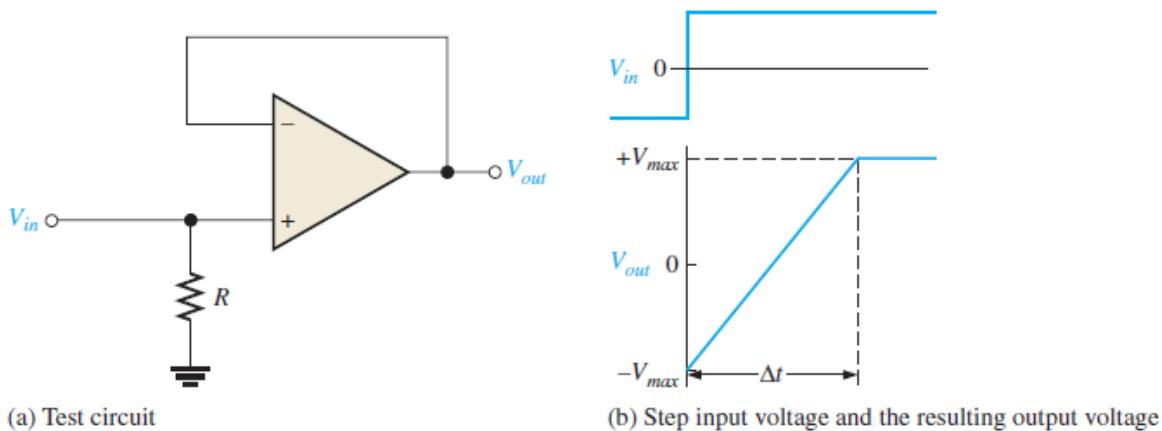
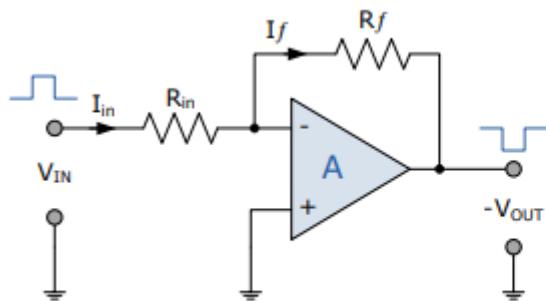


Figure 10 : Slew-rate measurement.

$$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

3.3 Applications of Op-Amp

- Inverting Amplifier



$$A_v = \frac{V_{OUT}}{V_{IN}} = -\frac{R_f}{R_{IN}}$$

$$V_{OUT} = -V_{IN} \left(\frac{R_f}{R_{IN}} \right)$$

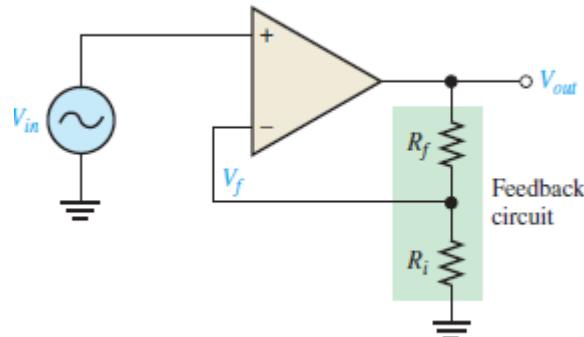
$$Z_{IN} = R_{IN}$$

An op-amp connected in a closed-loop configuration as a noninverting amplifier with a controlled amount of voltage gain is shown in Figure . The input signal is applied to the noninverting (+) input. The output is applied back to the inverting input through the feedback circuit (closed loop) formed by the input resistor R_i and the feedback resistor R_f . This creates negative feedback as follows. Resistors R_i and R_f form a voltage-divider circuit, which reduces V_{out} and connects the reduced voltage V_f to the inverting input. The feedback voltage is expressed as

$$A_v = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_f}{R_{IN}}$$

$$V_{OUT} = V_{IN}(A_v)$$

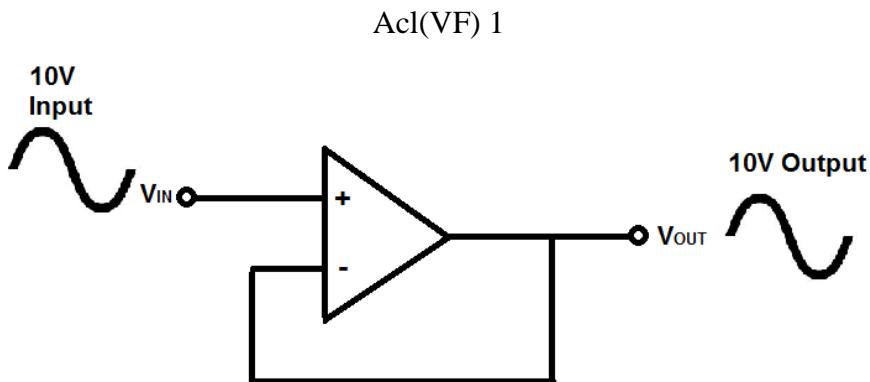
$$Z_{IN} = \infty$$



Voltage-Follower

The voltage-follower configuration is a special case of the noninverting amplifier where all of the output voltage is fed back to the inverting input by a straight connection, as shown in Figure . As you can see, the straight feedback connection has a voltage gain of 1 (which means there is no gain). The closed-loop voltage gain of a noninverting amplifier is as previously derived. Since B

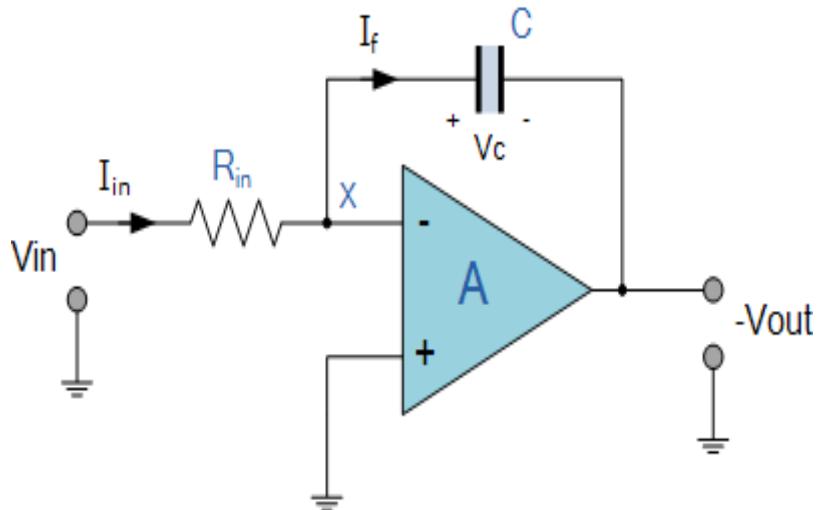
1 for a voltage-follower, the closed-loop voltage gain of the voltage-follower is $1/B$ (-)



Integrator Circuit

As its name implies, the **Op-amp Integrator** is an Operational Amplifier circuit that performs the mathematical operation of **Integration**, that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an *output voltage which is proportional to the integral of the input voltage*.

In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.



We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C . Then the voltage across the capacitor is $-V_{out}$ therefore: $-V_{out} = Q/C$. If the capacitor is charging and discharging, the rate of change of voltage across the capacitor is given as:

$$V_c = \frac{Q}{C}, \quad V_c = V_x - V_{out} = 0 - V_{out}$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{C dt} = \frac{1}{C} \frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, $X = 0$, the input current I_{in} flowing through the input resistor, R_{in} is given as:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$I_f = C \frac{dV_{out}}{dt} = C \frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out} \cdot C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out} \cdot C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in} C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

$$V_{out} = -\frac{1}{R_{in} C} \int_0^t V_{in} dt = -\int_0^t V_{in} \frac{dt}{R_{in} \cdot C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{j\omega RC} V_{in}$$

Differentiator Circuit

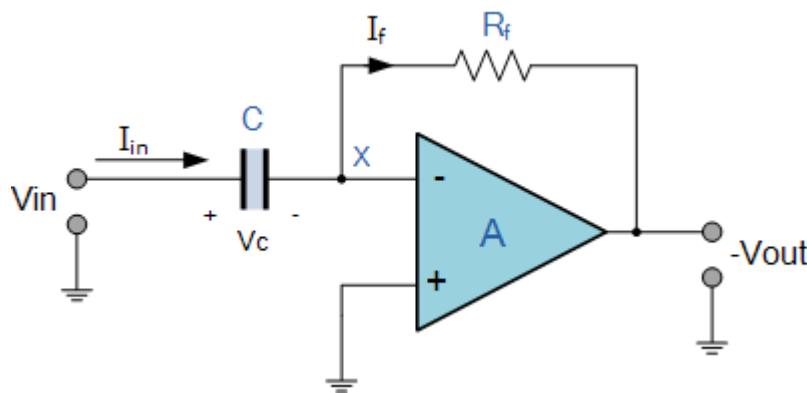


Figure.2.20 Opamp differentiator

The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is “High” resulting in a low gain (R_f/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R_f .

Ok, some math's to explain what's going on!. Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C \frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current i

$$I_{IN} = C \frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C \frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C \frac{dV_{IN}}{dt}$$

Therefore, the output voltage V_{out} is a constant $-R_f.C$ times the derivative of the input voltage V_{in} with respect to time. The minus sign indicates a 180° phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

3.4 OUTCOMES

- Design simple circuits like amplifiers (inverting and non inverting), comparators, adders, integrator and differentiator using OPAMPS.
- Compile the different building blocks in digital electronics using logic gates and implement

MODULE-4

BJT APPLICATIONS, FEEDBACK AMPLIFIERS AND OSCILLATORS

Structure:

- 4.1 BJT as an amplifier,
 - 4.2 BJT as a switch,
 - 4.3 Transistor switch circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay
 - 4.4 Feedback Amplifiers – Principle, Properties and advantages of Negative Feedback,
 - 4.5 Types of feedback, Voltage series feedback, Gain stability with feedback
 - 4.6 Oscillators – Barkhaunsen's criteria for oscillation,
 - 4.7 RC Phase Shift oscillator, Wien Bridge oscillator
 - 4.8 IC 555 Timer and Astable Oscillator using IC 555
- (refer 7.1-7.3 of Text 1).
(refer 7.7-7.9 of Text 1).
(refer 4.4 and 4.5 of Text 2).
(refer 17.2 and 17.3 of Text 1).

INTRODUCTION

DC and AC Quantities

Before discussing the concept of transistor amplification, the designations that we will use for the circuit quantities of current, voltage, and resistance must be explained because amplifier circuits have both dc and ac quantities.

In this text, italic capital letters are used for both dc and ac currents (I) and voltages (V). This rule applies to rms, average, peak, and peak-to-peak ac values. AC current and voltage values are always rms unless stated otherwise. Although some texts use lowercase I and v for ac current and voltage, we reserve the use of lowercase i and v only for instantaneous values. In this text, the distinction between a dc current or voltage and an ac current or voltage is in the subscript.

DC quantities always carry an uppercase roman (nonitalic) subscript. For example, I_B , I_C , and I_E are the dc transistor currents. V_{BE} , V_{CB} , and V_{CE} are the dc voltages from one transistor terminal to another. Single subscripted voltages such as V_B , V_C , and V_E are dc voltages from the transistor terminals to ground.

AC and all time-varying quantities always carry a lowercase italic subscript. For example, I_b , I_c , and I_e are the ac transistor currents. V_{be} , V_{cb} , and V_{ce} are the ac voltages from one transistor terminal to another. Single subscripted voltages such as V_b , V_c , and V_e are ac voltages from the transistor terminals to ground. The rule is different for internal transistor resistances. As you will see later, transistors have internal ac resistances that are designated by lowercase with an appropriate subscript. For example, the internal ac emitter resistance is designated as r_e . Circuit resistances external to the transistor itself use the standard italic capital R with a subscript that identifies the resistance as dc or ac (when applicable), just as for current and voltage. For example R_E is an external dc emitter resistance and r_e is an external ac emitter resistance.

4.1 BJT as an amplifier

As you have learned, a transistor amplifies current because the collector current is equal to the base current multiplied by the current gain, b . The base current in a transistor is very small compared to the collector and emitter currents. Because of this, the collector current is approximately equal to the emitter current. With this in mind, let's look at the circuit in

Figure 1. An ac voltage, V_s , is superimposed on the dc bias voltage V_{BB} by capacitive coupling as shown. The dc bias voltage V_{CC} is connected to the collector through the collector resistor, R_C .

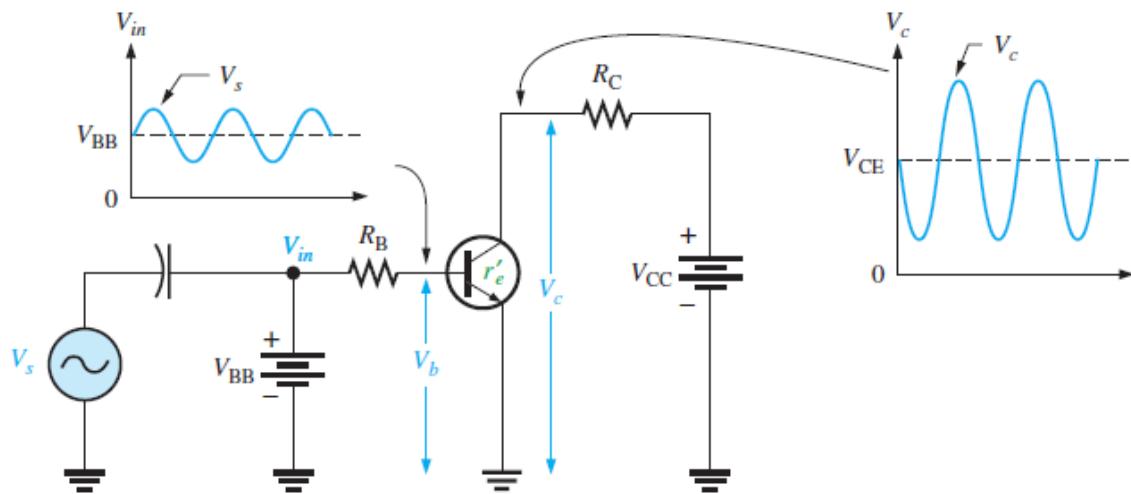


Figure 1: Basic transistor amplifier circuit with ac source voltage V_s and dc bias voltage V_{BB} superimposed.

The ac input voltage produces an ac base current, which results in a much larger ac collector current. The ac collector current produces an ac voltage across R_C , thus producing an amplified, but inverted, reproduction of the ac input voltage in the active region of operation, as illustrated in Figure 1.

The forward-biased base-emitter junction presents a very low resistance to the ac signal. This internal ac emitter resistance is designated in Figure 1 and appears in series with R_B . The ac base voltage is

$$V_b = I_e r'_e$$

The ac collector voltage, V_c , equals the ac voltage drop across R_C .

$$V_c = I_c R_C$$

Since $I_c \approx I_e$, the ac collector voltage is

$$V_c \approx I_e R_C$$

V_b can be considered the transistor ac input voltage where $V_b = V_s - I_b R_B$. V_c can be considered the transistor ac output voltage. Since *voltage gain* is defined as the ratio of the output voltage to the input voltage, the ratio of V_c to V_b is the ac voltage gain, A_v , of the transistor.

$$A_v = \frac{V_c}{V_b}$$

Substituting $I_e R_C$ for V_c and $I_e r'_e$ for V_b yields

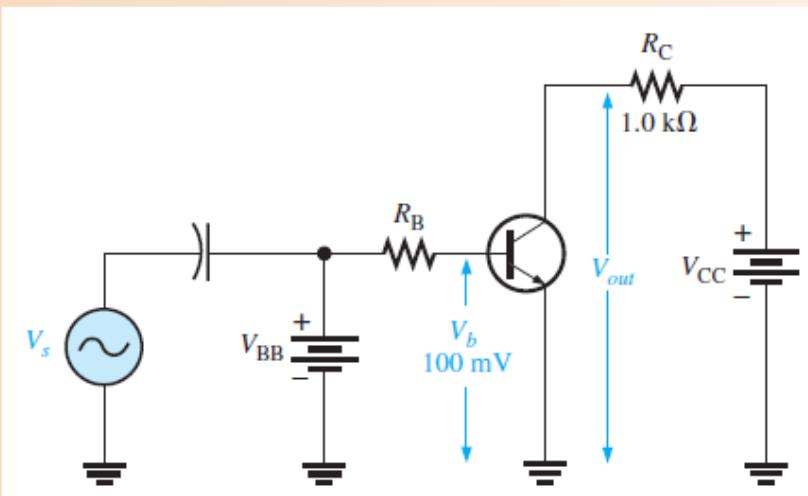
$$A_v = \frac{V_c}{V_b} \cong \frac{I_e R_C}{I_e r'_e}$$

The I_e terms cancel; therefore,

$$A_v \cong \frac{R_C}{r'_e}$$

Since R_C is always considerably larger in value than r'_e , the output voltage for this configuration is greater than the input voltage.

Determine the voltage gain and the ac output voltage in Figure 4–22 if $r'_e = 50 \Omega$.



The voltage gain is

$$A_v \cong \frac{R_C}{r'_e} = \frac{1.0 \text{ k}\Omega}{50 \Omega} = 20$$

Therefore, the ac output voltage is

$$V_{out} = A_v V_b = (20)(100 \text{ mV}) = 2 \text{ V rms}$$

4.2 BJT as a switch

Switching Operation

Figure 2 illustrates the basic operation of a BJT as a switching device. In part (a), the transistor is in the cutoff region because the base-emitter junction is not forward-biased. In this condition, there is, ideally, an open between collector and emitter, as indicated by the switch equivalent. In part (b), the transistor is in the saturation region because the base-emitter

junction and the base-collector junction are forward-biased and the base current is made large enough to cause the collector current to reach its saturation value. In this condition, there is, ideally, a short between collector and emitter, as indicated by the switch equivalent. Actually, a small voltage drop across the transistor of up to a few tenths of a volt normally occurs, which is the saturation voltage, $V_{CE(sat)}$.

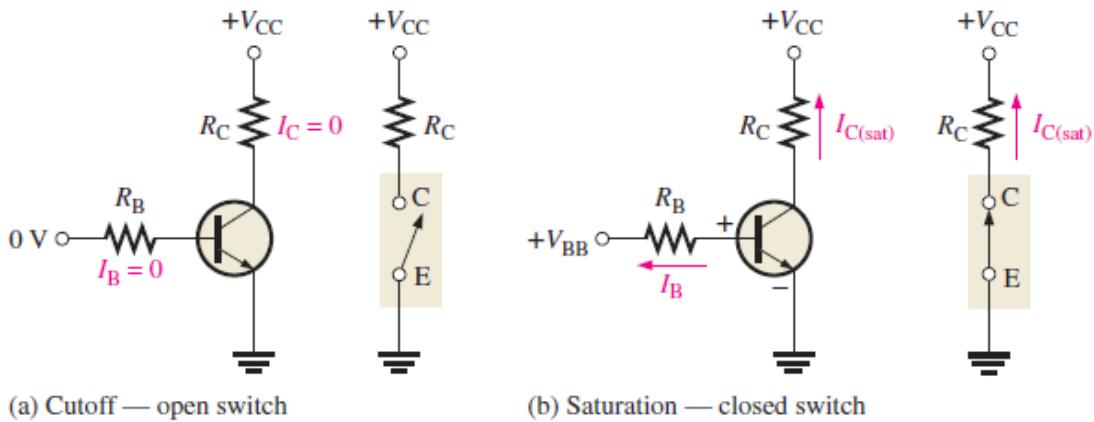


Figure: 2 Switching action of an ideal transistor.

Conditions in Cutoff As mentioned before, a transistor is in the cutoff region when the base-emitter junction is not forward-biased. Neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC} .

$$V_{CE(\text{cutoff})} = V_{CC}$$

Conditions in Saturation As you have learned, when the base-emitter junction is forward-biased and there is enough base current to produce a maximum collector current, the transistor is saturated. The formula for collector saturation current is

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

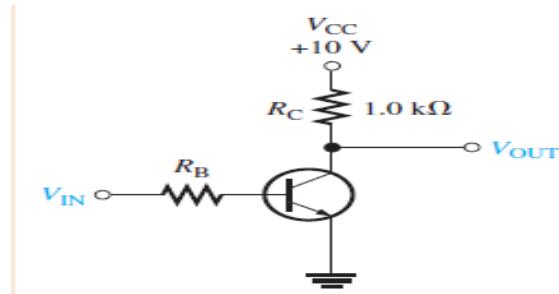
Since $V_{CE(\text{sat})}$ is very small compared to V_{CC} , it can usually be neglected.

The minimum value of base current needed to produce saturation is

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}}$$

Normally, I_B should be significantly greater than $I_{B(\text{min})}$ to ensure that the transistor is saturated.

Example: (a) For the transistor circuit in Figure 4–24, what is VCE when VIN = 0 V? (b) What minimum value of IB is required to saturate this transistor if β_{DC} is 200? Neglect VCE(sat). (c) Calculate the maximum value of RB when VIN = 5 V.



(a) When $V_{IN} = 0$ V, the transistor is in cutoff (acts like an open switch) and

$$V_{CE} = V_{CC} = 10 \text{ V}$$

(b) Since $V_{CE(sat)}$ is neglected (assumed to be 0 V),

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10 \text{ V}}{1.0 \text{ k}\Omega} = 10 \text{ mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{10 \text{ mA}}{200} = 50 \mu\text{A}$$

This is the value of I_B necessary to drive the transistor to the point of saturation. Any further increase in I_B will ensure the transistor remains in saturation but there cannot be any further increase in I_C .

(c) When the transistor is on, $V_{BE} \approx 0.7$ V. The voltage across R_B is

$$V_{R_B} = V_{IN} - V_{BE} \approx 5 \text{ V} - 0.7 \text{ V} = 4.3 \text{ V}$$

Calculate the maximum value of R_B needed to allow a minimum I_B of 50 μA using Ohm's law as follows:

$$R_{B(max)} = \frac{V_{R_B}}{I_{B(min)}} = \frac{4.3 \text{ V}}{50 \mu\text{A}} = 86 \text{ k}\Omega$$

4.3 Transistor switch circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay

A Simple Application of a Transistor Switch

The transistor in Figure 3 is used as a switch to turn the LED on and off. For example, a square wave input voltage with a period of 2 s is applied to the input as indicated. When

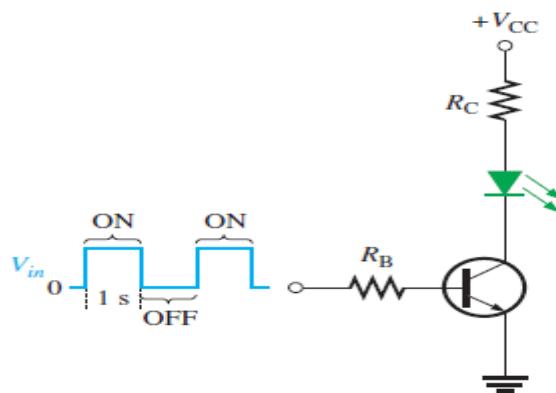


Figure 3: A transistor used to switch an LED

on and off.

the square wave is at 0 V, the transistor is in cutoff; and since there is no collector current, the LED does not emit light. When the square wave goes to its high level, the transistor saturates. This forward-biases the LED, and the resulting collector current through the LED causes it to emit light. Thus, the LED is on for 1 second and off for 1 second.

The LED in Figure 4–25 requires 30 mA to emit a sufficient level of light. Therefore, the collector current should be approximately 30 mA. For the following circuit values, determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the minimum value of base current as a safety margin to ensure saturation. $V_{CC} = 9\text{ V}$, $V_{CE(\text{sat})} = 0.3\text{ V}$, $R_C = 220\ \Omega$, $R_B = 3.3\text{ k}\Omega$, $\beta_{DC} = 50$, and $V_{LED} = 1.6\text{ V}$.

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{LED} - V_{CE(\text{sat})}}{R_C} = \frac{9\text{ V} - 1.6\text{ V} - 0.3\text{ V}}{220\ \Omega} = 32.3\text{ mA}$$

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}} = \frac{32.3\text{ mA}}{50} = 646\ \mu\text{A}$$

To ensure saturation, use twice the value of $I_{B(\text{min})}$, which is 1.29 mA. Use Ohm's law to solve for V_{in} .

$$I_B = \frac{V_{R_B}}{R_B} = \frac{V_{in} - V_{BE}}{R_B} = \frac{V_{in} - 0.7\text{ V}}{3.3\text{ k}\Omega}$$

$$V_{in} - 0.7\text{ V} = 2I_{B(\text{min})}R_B = (1.29\text{ mA})(3.3\text{ k}\Omega)$$

$$V_{in} = (1.29\text{ mA})(3.3\text{ k}\Omega) + 0.7\text{ V} = 4.96\text{ V}$$

4.6 Oscillators – Barkhaunsen's criteria for oscillation

An oscillator is a circuit that produces a periodic waveform on its output with only the dc supply voltage as an input. A repetitive input signal is not required except to synchronize oscillations in some applications. The output voltage can be either sinusoidal or nonsinusoidal, depending on the type of oscillator. Two major classifications for oscillators are **feedback oscillators and relaxation oscillators**.

Principles of Oscillator

With exception such as relaxation oscillator, the operation of oscillator is based on principle of positive feedback where portion of the output signal is feedback into input without phase change. Thus, it reinforces the input and sustains the continuous sinusoidal output. Beside this, the phase shift of feedback signal must be either 0° or 360° . The last requirement is the loop gain T of amplifier must be equal to one, which is also named as Barkhausen criterion. Thus mathematically, the loop gain T is

$$T = AV_b = 1$$

where A_V is the voltage gain of the amplifier and $\beta = \frac{V_f}{V_{out}}$ is the feedback portion of output voltage. If A_V is equal to 10 then the feedback portion β should be $1/10$. The principles of the oscillator are illustrated in Fig. 16.1. The transfer function of the circuit shall be $A_f = \frac{A_v}{1 - A_v\beta}$.

Conditions for Oscillation

Two conditions, illustrated in Figure 4, are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be effectively
2. The voltage gain, A_{cl} , around the closed feedback loop (loop gain) must equal 1 (unity).

The voltage gain around the closed feedback loop, is the product of the amplifier gain, and the attenuation, B , of the feedback circuit. If a sinusoidal wave is the desired output, a loop gain greater than 1 will rapidly cause the output to saturate at both peaks of the waveform, producing unacceptable distortion. To avoid this, some form of gain control must be used to keep the loop gain at exactly 1 once oscillations have started. For example, if the attenuation of the feedback circuit is 0.01, the amplifier must have a gain of exactly 100 to overcome this attenuation and not create unacceptable distortion. An amplifier gain of greater than 100 will cause the oscillator to limit both peaks of the waveform.

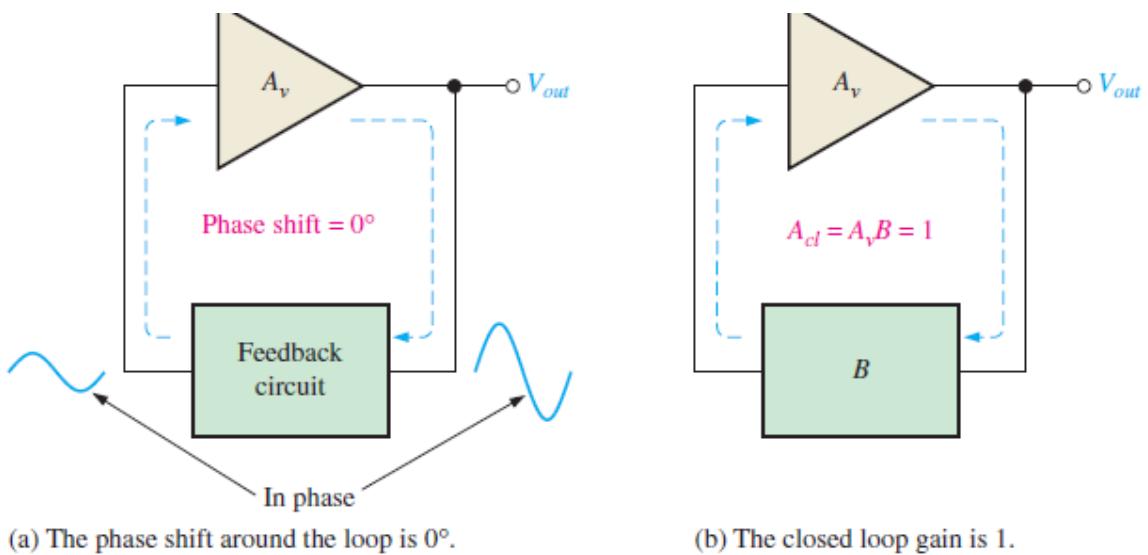
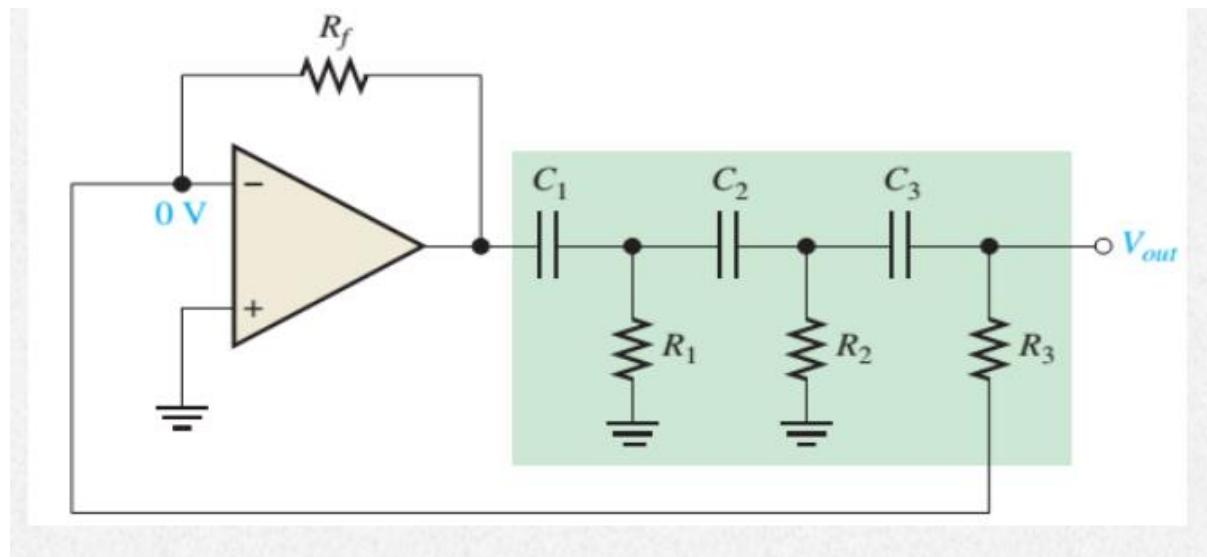


Figure 4: General conditions to sustain oscillation.

4.7 RC Phase Shift oscillator, Wien Bridge oscillator

RC Phase Shift oscillator

Three types of feedback oscillators that use RC circuits to produce sinusoidal outputs are the Wien-bridge oscillator, the phase-shift oscillator, and the twin-T oscillator. Generally, RC feedback oscillators are used for frequencies up to about 1 MHz. The Wien-bridge is by far the most widely used type of RC feedback oscillator for this range of frequencies.



$$f_r \doteq \frac{1}{2\pi\sqrt{6}RC}$$

Wien-Bridge Oscillator

Wien-Bridge oscillator is an oscillator that meets the principle of oscillator. Its circuit is shown in Figure 5

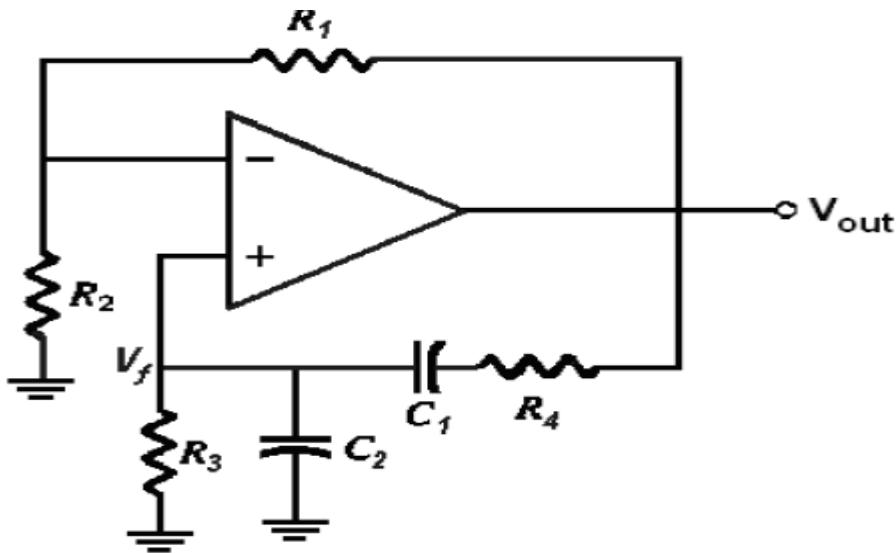
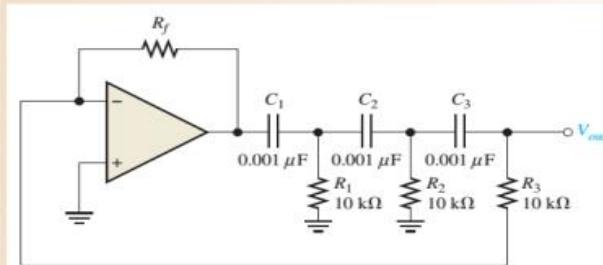


Figure 5 : Wien-Bridge Oscillator

There is a lead-lag RC network whereby C_1 and R_3 leads and R_4 and C_2 lags. Reactance χ_{C_1} of capacitance C_1 is significantly affecting the V_{IN+} at low frequency, whilst reactance χ_{C_2} of capacitor C_2 equal to $1/j\omega C_2$ is significant affecting at high frequency. If $C_1 = C_2$ and $R_4 = R_3$, there will be no phase-shift because the phase lead is compensated by phase lag. From the analysis of the circuit, the portion of the output feedback to input

(a) Determine the value of R_f necessary for the circuit in Figure 16–14 to operate as an oscillator.

(b) Determine the frequency of oscillation.



Solution (a) $A_{cl} = 29$, and $B = 1/29 = R_3/R_f$. Therefore,

$$\frac{R_f}{R_3} = 29$$

$$R_f = 29R_3 = 29(10 \text{ k}\Omega) = 290 \text{ k}\Omega$$

(b) $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$. Therefore,

$$f_r = \frac{1}{2\pi\sqrt{6RC}} = \frac{1}{2\pi\sqrt{6}(10 \text{ k}\Omega)(0.001 \mu\text{F})} \cong 6.5 \text{ kHz}$$

4.8 IC 555 Timer and Astable Oscillator using IC 555

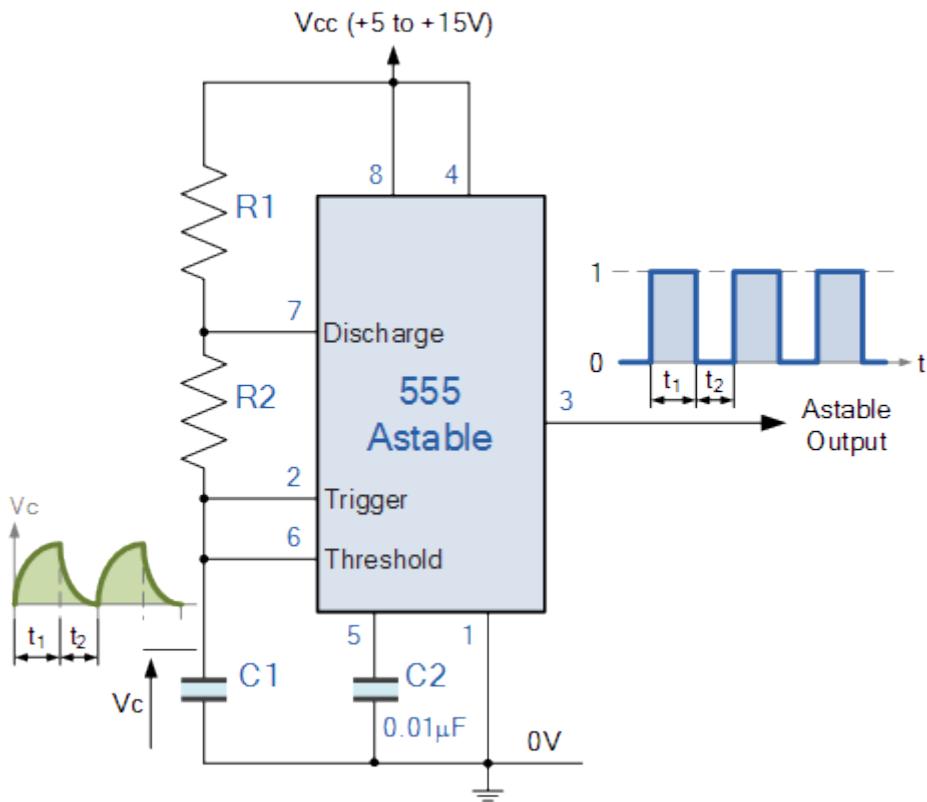
The **555 Timer IC** can be connected either in its Monostable mode thereby producing a precision timer of a fixed time duration, or in its Bistable mode to produce a flip-flop type switching action. But we can also connect the 555 timer IC in an Astable mode to produce a very stable **555 Oscillator** circuit for generating highly accurate free running waveforms whose output frequency can be adjusted by means of an externally connected RC tank circuit consisting of just two resistors and a capacitor.

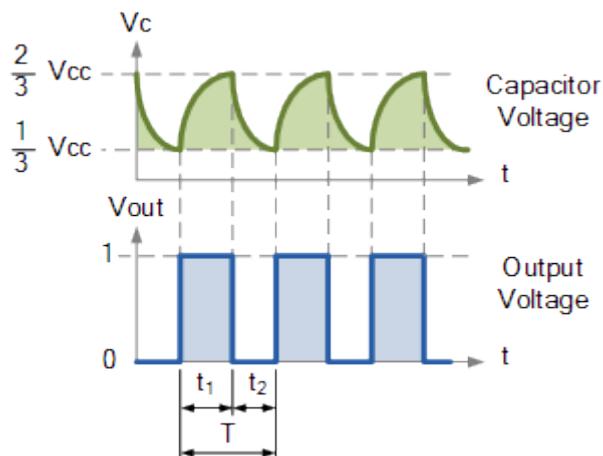
The **555 Oscillator** is another type of relaxation oscillator for generating stabilized square wave output waveforms of either a fixed frequency of up to 500kHz or of varying duty cycles from 50 to 100%. In the previous 555 Timer tutorial we saw that the Monostable circuit produces a single output one-shot pulse when triggered on its pin 2 trigger input.

Whereas the 555 monostable circuit stopped after a preset time waiting for the next trigger pulse to start over again, in order to get the 555 Oscillator to operate as an astable multivibrator it is necessary to continuously re-trigger the 555 IC after each and every timing cycle.

This re-triggering is basically achieved by connecting the *trigger* input (pin 2) and the *threshold* input (pin 6) together, thereby allowing the device to act as an astable oscillator. Then the 555 Oscillator has no stable states as it continuously switches from one state to the other. Also the single timing resistor of the previous monostable multivibrator circuit has been split into two separate resistors, R1 and R2 with their junction connected to the *discharge* input (pin 7) as shown below.

Basic Astable 555 Oscillator Circuit





In the **555 Oscillator** circuit above, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator. During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the *discharge* terminal, pin 7.

Then the capacitor charges up to $2/3 V_{cc}$ (the upper comparator limit) which is determined by the $0.693(R_1+R_2)C$ combination and discharges itself down to $1/3 V_{cc}$ (the lower comparator limit) determined by the $0.693(R_2 \cdot C)$ combination. This results in an output waveform whose voltage level is approximately equal to $V_{cc} - 1.5V$ and whose output “ON” and “OFF” time periods are determined by the capacitor and resistors combinations. The individual times required to complete one charge and discharge cycle of the output is therefore given as:

Astable 555 Oscillator Charge and Discharge Times

$$t_1 = 0.693(R_1 + R_2) \cdot C$$

and

$$t_2 = 0.693 \times R_2 \times C$$

Where, R is in Ω and C in Farads.

When connected as an astable multivibrator, the output from the **555 Oscillator** will continue indefinitely charging and discharging between $2/3 V_{cc}$ and $1/3 V_{cc}$ until the power supply is removed. As with the monostable multivibrator these charge and discharge times and therefore the frequency are independent on the supply voltage.

The duration of one full timing cycle is therefore equal to the sum of the two individual times that the capacitor charges and discharges added together and is given as:

555 Oscillator Cycle Time

$$T = t_1 + t_2 = 0.693(R_1 + 2R_2) \cdot C$$

The output frequency of oscillations can be found by inverting the equation above for the total cycle time giving a final equation for the output frequency of an Astable 555 Oscillator as:

555 Oscillator Frequency Equation

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C}$$

By altering the time constant of just one of the RC combinations, the **Duty Cycle** better known as the “Mark-to-Space” ratio of the output waveform can be accurately set and is given as the ratio of resistor R2 to resistor R1. The Duty Cycle for the 555 Oscillator, which is the ratio of the “ON” time divided by the “OFF” time is given by:

555 Oscillator Duty Cycle

$$\text{Duty Cycle} = \frac{T_{\text{ON}}}{T_{\text{OFF}} + T_{\text{ON}}} = \frac{R_1 + R_2}{(R_1 + 2R_2)} \%$$

The duty cycle has no units as it is a ratio but can be expressed as a percentage (%). If both timing resistors, R1 and R2 are equal in value, then the output duty cycle will be 2:1 that is, 66% ON time and 33% OFF time with respect to the period.

555 Oscillator Example No1

An **Astable 555 Oscillator** is constructed using the following components, R1 = 1kΩ, R2 = 2kΩ and capacitor C = 10uF. Calculate the output frequency from the 555 oscillator and the duty cycle of the output waveform.

t_1 – capacitor charge “ON” time is calculated as:

$$\begin{aligned} t_1 &= 0.693(R_1 + R_2)C \\ &= 0.693(1000 + 2000) \times 10 \times 10^{-6} \\ &= 0.021\text{s} = 21\text{ms} \end{aligned}$$

t_2 – capacitor discharge “OFF” time is calculated as:

$$\begin{aligned} t_2 &= 0.693 R_2 C \\ &= 0.693 \times 2000 \times 10 \times 10^{-6} \\ &= 0.014\text{s} = 14\text{ms} \end{aligned}$$

Total periodic time (T) is therefore calculated as:

$$T = t_1 + t_2 = 21\text{ms} + 14\text{ms} = 35\text{ms}$$

The output frequency, f is therefore given as:

$$f = \frac{1}{T} = \frac{1}{35\text{ms}} = 28.6\text{Hz}$$

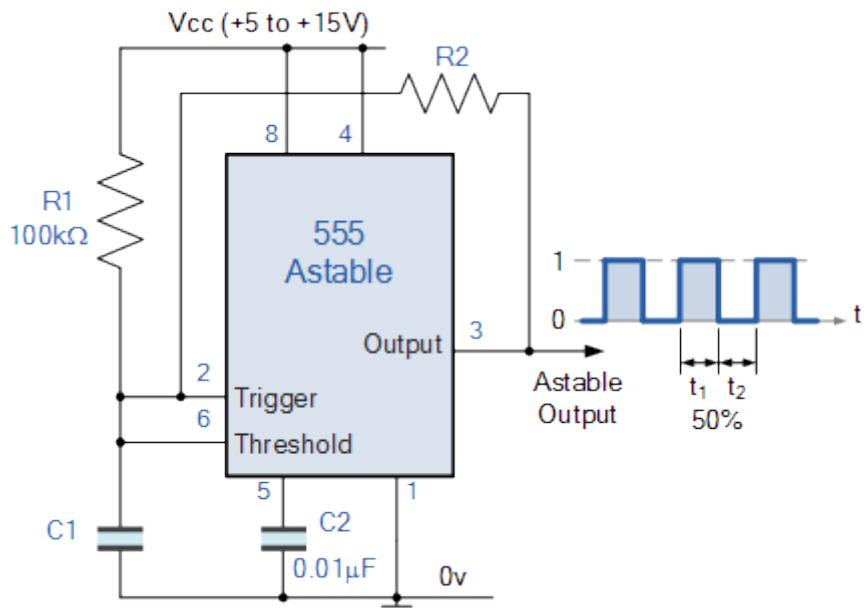
Giving a duty cycle value of:

$$\text{Duty Cycle} = \frac{R_1 + R_2}{(R_1 + 2R_2)} = \frac{1000 + 2000}{(1000 + 2 \times 2000)} = 0.6 \text{ or } 60\%$$

As the timing capacitor, C charges through resistors R1 and R2 but only discharges through resistor R2 the output duty cycle can be varied between 50 and 100% by changing the value of resistor R2. By decreasing the value of R2 the duty cycle increases towards 100% and by increasing R2 the duty cycle reduces towards 50%. If resistor, R2 is very large relative to resistor R1 the output frequency of the 555 astable circuit will be determined by $R2 \times C$ only.

The problem with this basic astable 555 oscillator configuration is that the duty cycle, the “mark to-space” ratio will never go below 50% as the presence of resistor R2 prevents this. In other words we cannot make the outputs “ON” time shorter than the “OFF” time, as $(R1 + R2)C$ will always be greater than the value of $R1 \times C$. One way to overcome this problem is to connect a signal bypassing diode in parallel with resistor R2 as shown below.

50% Duty Cycle Astable Oscillator



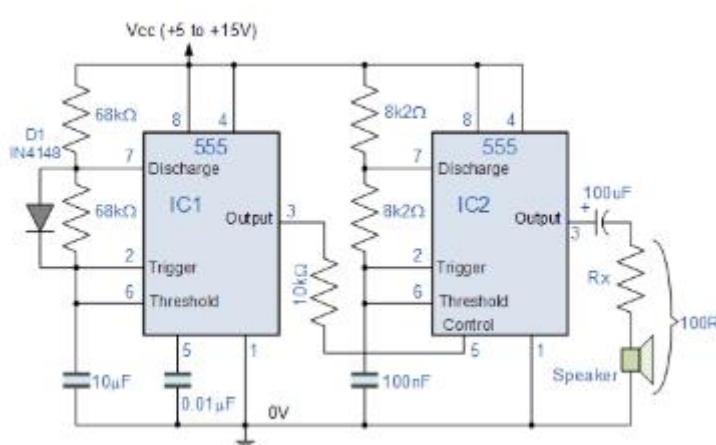
The 555 oscillator now produces a 50% duty cycle as the timing capacitor, C1 is now charging and discharging through the same resistor, R2 rather than discharging through the timers discharge pin 7 as before. When the output from the 555 oscillator is HIGH, the capacitor charges up through R2 and when the output is LOW, it discharges through R2. Resistor R1 is used to ensure that the capacitor charges up fully to the same value as the supply voltage.

However, as the capacitor charges and discharges through the same resistor, the above equation for the output frequency of oscillations has to be modified a little to reflect this circuit change. Then the new equation for the 50% Astable 555 Oscillator is given as:

50% Duty Cycle Frequency Equation

$$f = \frac{1}{0.693(2R_2)C} \text{ Hz}$$

Note that resistor R1 needs to be sufficiently high enough to ensure it does not interfere with the charging of the capacitor to produce the required 50% duty cycle. Also changing the value of the timing capacitor, C1 changes the oscillation frequency of the astable circuit.



MODULE 5 : FUNDAMENTALS OF DIGITAL ELECTRONICS

Structure

- 5.0 Introduction
- 5.1 Objectives
- 5.2 Switching and Logic Levels
- 5.3 Digital Waveform
- 5.4 Number Systems:
 - 5.4.1 Decimal Number System,
 - 5.4.2 Binary Number System,
 - 5.4.3 Converting Decimal to Binary
 - 5.4.4 Hexadecimal Number System
 - 5.4.5 Converting Binary to Hexadecimal & Vice versa
 - 5.4.6 Converting Hexadecimal to Decimal & Vice versa
 - 5.4.7 Octal Number System
 - 5.4.8 Octal to Binary & Binary to octal Conversion
- 5.5 Complement of Binary Numbers
- 5.6 Boolean Algebra Theorems
- 5.7 Digital Circuits
 - 5.7.1 Logic gates
 - 5.7.2 Algebraic Simplification
 - 5.7.3 NAND and NOR Implementation
 - 5.7.4 Half adder & Full adder
- 5.8 Flip Flops
 - 5.8.1 S R Flip Flop
 - 5.8.2 J K Flip Flop
 - 5.8.3 Shift Register
 - 5.8.4 Binary Counter
- 5.9 Principle of Communication system
- Course outcome
- 5.11 Further Reading

5.0 INTRODUCTION:

Definitions of Analog vs Digital signals

An **Analog signal** is any continuous signal for which the time varying feature (variable) of the signal is a representation of some other time varying quantity, i.e., analogous to another time varying signal. It differs from a digital signal in terms of small fluctuations in the signal which are meaningful.

A **digital signal** uses discrete (discontinuous) values. By contrast, non-digital (or analog) systems use a continuous range of values to represent information. Although digital representations are discrete, the information represented can be either discrete, such as numbers or letters, or continuous, such as sounds, images, and other measurements of continuous systems.

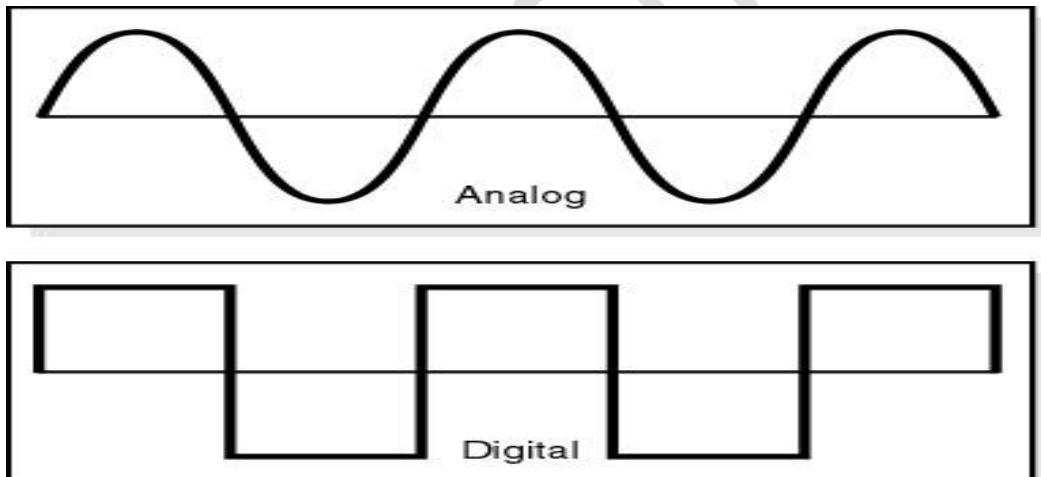


Figure. 3.0 Analog and digital signal

5.1 OBJECTIVES

1. To Understand the Number systems and conversion of one Number system to other
2. To define a Logic gate and understand the different types of Logic Gates
3. To state different laws of Boolean Algebra
4. Simplify the Logical expressions using Boolean algebra and implement using Universal

Gates

5. Design and implementation of Half adder and Full adder

5.2 SWITCHING AND LOGIC LEVELS

In digital circuits, a **logic level** is one of a finite number of states that a signal can have. Logic levels are usually represented by the voltage difference between the signal and ground (or some other common reference point), although other standards exist. The range of voltage levels that represents each state depends on the logic family being used.

In binary logic the two levels are logical high and logical low, which generally correspond to a binary 1 and 0 respectively. Signals with one of these two levels can be used in boolean logic for digital circuit design or analysis.

In three-state logic, an output device can also be high impedance. This is not a logic level, but means that the output is not controlling the state of the connected circuit.

5.3 DIGITAL WAVEFORMS

In computer architecture and other digital systems, a waveform that switches between two voltage levels representing the two states of a Boolean value (0 and 1) is referred to as a *digital signal*, even though it is an analog voltage waveform, since it is interpreted in terms of only two levels.

The clock signal is a special digital signal that is used to synchronize digital circuits. The image shown can be considered the waveform of a clock signal. Logic changes are triggered either by the rising edge or the falling edge.

The given diagram is an example of the practical pulse and therefore we have introduced two new terms that are:

- Rising edge: the transition from a low voltage (level 1 in the diagram) to a high voltage (level 2).
- Falling edge: the transition from a high voltage to a low one.

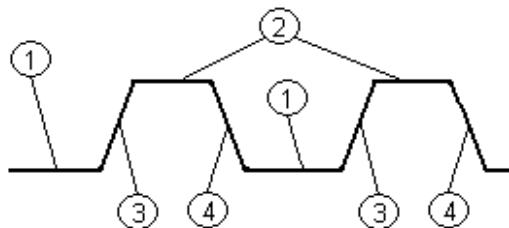


Figure 3.1 Digital Waveforms

5.4 NUMBER SYSTEMS

The human need to count things goes back to the dawn of civilization. To answer the questions like -how much||, or -how many||, people invented number system. A number system is any scheme used to count things. The decimal number system succeeded because very large numbers can be expressed using relatively short series of easily memorized numerals. Decimal or base 10 number system's origin: can be traced to, counting on the fingers with digits. -Digit|| taken from the Latin word *digitus* meaning -finger|| In any number system, the important terms to be known are :

Base or radix, numerals, positional value, absolute value, radix point and the prevalent number systems of interest for study.

Base: Base is the number of different digits or symbols or numerals used to represent the number system including zero in the number system. It is also called the **radix** of the number system. **Numerals :** Numeral is the symbols used to represent the number system

Each digit in the number system has two values: a) *Absolute value*

b) *Positional value*

The **absolute value** is the value of the digit itself, representing the no. system. The **positional value** is the value it possesses by virtue of its position in the no. system

The different number systems of interest for study, from the point of view of application to computers are:

Examples of commonly used number systems : **Decimal,Binary,Hexadecimal.**

Important properties of these systems need to be studied.

Polynomial Notation (Series Representation) :Any number system can be represented by the following polynomial.

$$N = a_{n-1} \times r^{n-1} + a_{n-2} \times r^{n-2} + \dots + a_0 \times r^0 + a_{-1} \times r^{-1} \dots + a_{-m} \times r^{-m}$$

Where r

= radix or base

n = number of integer digits to the left of the radix point

m = number of fractional digits to the right of the radix point

a_{n-1} = most significant digit (MSD)

a_{-m} = least significant digit (LSD)

Example:

$$N = (251.41)_{10} = 2 \times 10^2 + 5 \times 10^1 + 1 \times 10^0 + 4 \times 10^{-1} + 1 \times 10^{-2}$$

5.4.1 DECIMAL NUMBER SYSTEMS

The decimal system is composed of 10 numerals or symbols. These 10 symbols are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. Using these symbols as digits of a number, we can express any quantity. The decimal system is also called the base-10 system because it has 10 digits.

In decimal system, the no. 1000.111 is represented as:

□□	Integer part				□□□□□□□□□□	Fractional part	□
10³	10²	10¹	10⁰	10⁻¹	10⁻²	10⁻³	
=1000	=100	=10	=1	.	=0.1	=0.01	=0.001
Most Significant Digit				Least Significant Digit			
Decimal point							

Example : Multiply the value of the **symbol** by the value of the **position**, then add In decimal, 1954.89means

1 times 1,000 plus 9 times 100 plus 5 times 10 plus 4 times 1 plus 8 times 1/10

plus 9 times 1/100 = The number is 1954.89 in decimal. and is represented by **(1954.89)₁₀**. The digits are separated by a point “.” called the radix point.

Examples of decimal numbers

$$14_{10} \ 52_{10} \ 1024_{10} \ 64000_{10}$$

5.4.2 BINARY NUMBER SYSTEMS

In the binary system, there are only two symbols or possible digit values, 0 and 1. This base-2 system can be used to represent any quantity that can be represented in decimal or other

base system.

Integer part				Fractional part			
2^3	2^2	2^1	2^0	.	2^{-1}	2^{-2}	2^{-3}
=8	=4	=2	=1	.	=0.5	=0.25	=0.125
Most Significant Digit				Binary point			
				Least Significant Digit			

Binary Counting

The Binary counting sequence to represent decimal numbers is shown in the table below :

2^3	2^2	2^1	2^0	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Representing Binary Quantities

In digital systems the information that is being processed is usually presented in binary form. Any device that has only two operating states or possible conditions can represent binary quantities. E.g.. a switch which can be either be only open or closed. We arbitrarily (as we define them) let an open switch represent binary 1 and a closed switch represent binary 0. Thus we can represent any binary number by using series of switches

Typical Voltage Assignment

Binary 1: Any voltage between 2V to 5V

Binary 0: Any voltage between 0V to 0.8V

Not used: Voltage between 0.8V to 2V in 5 Volt CMOS and TTL Logic is not used as it may cause error in a digital circuit

We can see another significant difference between digital and analog systems. In digital systems, the exact voltage value is not important; eg, a voltage of 3.6V means the same as a voltage of 4.3V. In analog systems, the exact voltage value is important

Binary addition and subtraction: Examples of addition and subtraction in this number system is shown below:

The addition of binary numbers is done as follows:

- a) $1 + 1 = 0$ with a carry of 1, and can be represented as $(10)_2$, with 0 taking LSD position and 1 taking MSD.
- b) $1 + 0 = 1$ c) $0 + 1 = 1$ d) $0 + 0 = 0$

Example: Add the binary numbers 101011 and 11001 Sol: The binary addition process is indicated below,

Addition

111011 Carries the carries generated during addition is indicated here.

101011 Augend

+1001 Addend

1000100

The answer is : $(101011)_2 + (11001)_2 = (1000100)_2$

The subtraction of binary numbers is done as follows:

- e) $1 - 1 = 0$ f) $1 - 0 = 1$
- g) $0 - 1 = 0$ with a borrow of 1 from previous stage
- h) $0 - 0 = 0$

Example: Subtract the binary numbers 11011 from 100101. Sol: The binary subtraction process is

indicated below,

The answer is : $(100101)_2 - (11011)_2 = (01010)_2$

5.4.3 BINARY TO DECIMAL & DECIMAL TO BINARY CONVERSION

Binary to Decimal Conversion

The binary number system is the most important one in digital systems, but several others are also important. The decimal system is important because it is universally used to represent quantities outside a digital system. This means that there will be situations where decimal values have to be converted to binary values before they are entered into the digital system.

Any binary number can be converted to its decimal equivalent simply by summing together the weights of the various positions in the binary number which contain a 1 together the weights of the various positions in the binary number which contain a 1. **Technique**

Multiply each bit by 2^n , where n is the “weight” of the bit

The weight is the position of the bit, starting from 0 on the right Add the results

Example:

Binary	Decimal
10110101_2	
$2^7 + 0^6 + 2^5 + 2^4 + 0^3 + 2^2 + 0^1 + 2^0$	$= 128 + 0 + 32 + 16 + 0 + 4 + 0 + 1$
Result	181_{10}

You should have noticed that the method is to find the weights (i.e., powers of 2) for each bit position that contains a 1, and then to add them up.

Binary to decimal Fractions:

Example :

10.1011 =>

$$1 \times 2^{-4} = 0.0625 \quad 1 \times 2^{-3} = 0.125 \quad 0 \times 2^{-2} = 0.0$$

$$1 \times 2^{-1} = 0.5$$

$$0 \times 2^0 = 0.0$$

$$1 \times 2^1 = 2.0 = 2.6875$$

Procedure: Same principles with following exception ;.

Use negative powers of the base to the right of the radix point. (Only call it a decimal point in the decimal number system.)

Decimal-To-Binary Conversion There are 2 methods:

- Reverse of Binary-To-Decimal Method
- Repeat Division

Reverse of Binary-To-Decimal Method

Example :

Decimal	Binary
45_{10}	$=32 + 0 + 8 + 4 + 0 + 1$
	$=2^5 + 0 + 2^3 + 2^2 + 0 + 2^0$
Result	$=101101_2$

Repeat Division-Convert decimal to binary

This method uses repeated division by 2.

Example :

Conversion of 27_{10} to binary

Division	Remainder	Binary
$25/2$	$= 12 + \text{remainder of } 1$	1 (Least Significant Bit)
$12/2$	$= 6 + \text{remainder of } 0$	0
$6/2$	$= 3 + \text{remainder of } 0$	0
$3/2$	$= 1 + \text{remainder of } 1$	1
$1/2$	$= 0 + \text{remainder of } 1$	1 (Most Significant Bit)
Result	25_{10}	$= 11001_2$

Procedure :

- Divide by two, keep track of the remainder
- Group the remainders in the following order
- First remainder is bit LSB (least-significant bit)
- Last remainder is bit MSB (Most-significant bit)

5.4.4 HEXA DECIMAL NUMBER SYSTEM

The hexadecimal system uses base 16. Thus, it has 16 possible digit symbols. It uses the digits 0 through

9 plus the letters A, B, C, D, E, and F ,to represent 10 through 16, as the 16 digit symbols **Digits = {0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F}**

$$(B65F)_{16} = 11 \times 16^3 + 6 \times 16^2 + 5 \times 16^1 + 15 \times 16^0 = (46,687)_{10}$$

Sometimes, it is necessary to use a numbering system that has more than ten base digits One such numbering system is hexadecimal number system, useful in computer application. Hexadecimal number, is widely used in micro processors and micro controllers in assembly programming, and in embedded system development.

Hexadecimal addition and subtraction: Examples of addition and subtraction in this number system is shown below:

Addition

$$\begin{array}{r}
 1011 \quad \text{Carries} \\
 5BA9 \quad \text{Augend} \\
 + D058 \quad \text{Addend} \quad 12C0 \\
 \hline
 1 \quad \text{Sum}
 \end{array}$$

Subtraction

$$\begin{array}{r}
 910A10 \quad \text{Borrows} \\
 A5B9 \quad \text{Minuend} \\
 + 580D \quad \text{Subtrahend} \\
 \hline
 1DACA \quad \text{Difference}
 \end{array}$$

5.4.5 BINARY-TO-HEXADECIMAL /HEXADECIMAL-TO-BINARY CONVERSION

Hexadecimal Digit	0	1	2	3	4	5	6	7
Binary Equivalent	0000	0001	0010	0011	0100	0101	0110	0111

Hexadecimal Digit	8	9	A	B	C	D	E	F
Binary Equivalent	1000	1001	1010	1011	1100	1101	1110	1111

Each Hexadecimal digit is represented by **four** bits of binary digit

5.4.5 HEXADECIMAL TO DECIMAL/DECIMAL TO HEXADECIMAL CONVERSION

$$\text{Example: } 2AF_{16} = 2 \times (16^2) + 10 \times (16^1) + 15 \times (16^0) = 687_{10}$$

Hexadecimal to Decimal Conversion Technique

- Multiply each bit by 16^n , where n is the “weight” of the bit
- The weight is the position of the bit, starting from 0 on the right
- Add the results

Example:

$$\text{ABC.6D}_{16} \Rightarrow C \times 16^0 = 12 \times 1 = 12 \quad B \times 16^1 = 11 \times 16 = 176$$

$$A \times 16^2 = 10 \times 256 = 2560 \quad 6 \times 1/16 = 6 \times .0625$$

$$D \times 1/16^2 = 13 \times .0039 = 2748.0664_{10}$$

$$\text{Ans: ABC}_{16} = 2748.0664_{10}$$

Decimal To Hexadecimal

Repeat Division- Convert decimal to hexadecimal - This method uses repeated division by 16.

Example: convert 378_{10} to hexadecimal and binary:

Division	Result	Hexadecimal
$378/16$	= 23 + remainder of 10	A (Least Significant Bit)23
$23/16$	= 1 + remainder of 7	7
$1/16$	= 0 + remainder of 1	1 (Most Significant Bit)
Result	378_{10}	$= 17A_{16}$
Binary		$= 0001\ 0111\ 1010_2$

5.4.6 OCTAL NUMBER SYSTEM

The octal number system has a base of eight, meaning that it has eight possible digits: 0,1,2,3,4,5,6,7.

8^3	8^2	8^1	8^0	8^{-1}	8^{-2}	8^{-3}
=512	=64	=8	=1	.	=1/8	=1/64

The octal numbering system includes eight base digits (0-7). After 7, the next placeholder to the right begins with a “1”

0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13 ...

Octal to Decimal Conversion

$$237_8 = 2 \times (8^2) + 3 \times (8^1) + 7 \times (8^0) = 159_{10}$$

$$24.6_8 = 2 \times (8^1) + 4 \times (8^0) + 6 \times (8^{-1}) = 20.75_{10}$$

$$11.1_8 = 1 \times (8^1) + 1 \times (8^0) + 1 \times (8^{-1}) = 9.125_{10}$$

$$12.3_8 = 1 \times (8^1) + 2 \times (8^0) + 3 \times (8^{-1}) = 10.375_{10}$$

Octal addition and subtraction:

Examples of addition and subtraction in this number system is shown below:

Example: Add the octal numbers 5471 and 3754

Sol : The addition process with procedure is shown below :

Addition

1 1 1 Carries □ the carries generated during addition is indicated here.

5 4 7 1 Augend

+ 3 7 5 4 Addend

1 1 4 4 5 Sum

Procedure :

Addition of first column $1+4=5$

Addition of second column $7+5=12$ and $12-8=4$, with a carry of 1 to left
Addition of third column $1+4+7=12$ and $12-8=4$, with a carry of 1 to left

Addition of fourth column $1+5+3=9$ and $9-8=1$, with a carry of 1 to left The final carry forms the MSD.

The answer is : $(5471)_8 + (3754)_8 = (11445)_8$

Subtraction

Example: Subtract the octal numbers 7451 and 5643

Sol : The subtraction process with procedure is shown below :

6 10 4 10 Borrows □ the barrows taken during subtraction is indicated here.

7 4 5 1 Minuend

- 5 6 4 3 Subtrahend

1 6 0 6 Difference

Procedure :

- Subtraction of first column $1-3= 6$, by borrowing carry from previous stage $1+8= 9$, hence $9-3=6$
- Subtraction of second column $4-4= 0$, now after the borrow 5 becomes 4 in II column.
- Subtraction of third column $4-6= 6$, by borrowing from previous stage, $8+4=12$, Hence $12-6 = 6$
- Subtraction of fourth column $6-5= 1$, 7 will become 6 after a borrow to the right. The answer is :
 $(7451)_8 - (5643)_8 = (1606)_8$

5.4.7 Binary to Octal and Octal to binary conversion

Binary to octal

Group 3 Bits and write its corresponding octal equivalent

Example: $100\ 111\ 010_2 = (100)\ (111)\ (010)_2 = 4\ 7\ 2_8$

Octal to Binary

Octal	0	1	2	3	4	5	6	7
Binary Equivalent	000	001	010	011	100	101	110	111

Each Octal digit is represented by three binary digits.

5.5 COMPLEMENT OF BINARY NUMBERS

The 1's complement of a given binary no. is the new no. obtained by changing all the 0's to 1, and all 1's to 0

Ex : 11010's 1's complement is 00101

The 2's complement of a given binary no. is the new no. obtained by changing all the 0's to 1, and all 1's to 0 and then adding 1 to the least significant bit

Ex : 11010's 2's complement is 1's complement $00101+1=00110$ Subtraction of smaller number from larger number

Method:

- Determine the 1's complement of the smaller no.
- Add the first complement to the larger no.
- Remove the carry and add it to the result. This is called end-around carry.

Ex : Subtract 101011_2 from 111001_2 using the 1's complement method Solution :

$$\begin{array}{r}
 111001 \\
 -101011 \quad \square \text{ Take 1's complement of } 101011 = 010100 \\
 \hline
 111001 + 010100 \\
 \hline
 \text{Carry } 1) 001101 \\
 \hline
 \text{---} + 1 \quad \square \text{ end around carry} \text{ ---} \\
 \hline
 1110 \quad \text{Final answer}
 \end{array}$$

Subtraction of larger number from smaller number

Method :

1. Determine the first complement of the larger no.
2. Add the first complement to the smaller no.
3. Answer is in the 1's complement form. To get the answer in true form take the 1's complement and assign –ve sign to the answer.

Advantages of 1's complement method

1. *The first complement subtraction can be accomplished with a binary adder. There fore, this method is useful in arithmetic logic circuits.*
2. *The first complement of a no. is easily obtained by inverting each bit in the no.*

2's complement method of subtraction

Subtraction of smaller number from larger number

Method:

1. Determine the 2's complement of a smaller no.
2. Add the 2's complement to the larger no.
3. Discard the carry.

Subtract 101011_2 from 111001_2 using the 1's complement method

Solution :

$$\begin{array}{r}
 111001 \\
 -101011 \quad \square \\
 \hline
 \text{Take 2's complement of } 101011 = 1's \text{ complement} + 1 = 010100 + 1 \text{ ---} = 010101 \\
 \hline
 111001 + 010101 \\
 \hline
 \end{array}$$

Carry 1) 001110-----□ discard the carry -----

1110 Final answer

Subtraction of larger number from smaller number

Method:

1. Determine the 2's complement of a larger no.
- 2 Add the 2's complement to the smaller no.
- 3 When there is no carry, answer is in the 2's complement form.

To get the answer in the true form take the 2's complement and assign –ve sign to the answer.

Ex :Subtract 111001_2 from 101011_2 using the 1's complement method Solution :

101011

-111001 -□ Take 2's complement of $111001 = 1$'s complement+1=000110+1 -----
=000111

101011 + 000111

110010-----□ no carry generated,hence take 2's complement of the result -----

and attach –ve sign to it.i.e $001101+1=001110$

001110

Therefore the answer is -0011

5.6 BOOLEAN ALGEBRA THEOREMS

Symbolic Logic

Boolean algebra derives its name from the mathematician George Boole. Symbolic Logic uses values, variables and operations

True is represented by the value **1**. **False** is represented by the value **0**.

Variables are represented by letters and can have one of two values, either 0 or 1. Operations are functions of one or more variables

AND is represented by $X \cdot Y$ **OR** is represented by $X + Y$

NOT is represented by X' . Throughout this tutorial the X' form will be used and sometime \bar{X} will be used.

These basic operations can be combined to give expressions

Example : $X \cdot X \cdot Y \cdot W \cdot X \cdot Y + Z$

Precedence

As with any other branch of mathematics, these operators have an order of precedence. NOT operations have the highest precedence, followed by AND operations, followed by OR operations. Brackets can be used as with other forms of algebra. e.g.

$X \cdot Y + Z$ and $X \cdot (Y + Z)$ are not the same function

Function Definitions

The logic operations given previously are defined as follows :

Define $f(X, Y)$ to be some function of the variables X and Y .

$$f(X, Y) = X \cdot Y$$

$$f(X, Y) = X + Y$$

1 if $X = 1$ and $Y = 1$

0 Otherwise

$$f(X, Y) = X + Y$$

1 if $X = 1$ or $Y = 1$

0 Otherwise

$$f(X) = X'$$

1 if $X = 0$

0 Otherwise

Boolean Switching Algebras

A Boolean Switching Algebra is one which deals only with two-valued variables. Boole's general theory covers algebras which deal with variables which can hold n values.

$$\text{Identity : } X + 0 = X, \quad X \cdot 1 = X$$

$$\text{Commutative Laws : } X + Y = Y + X,$$

$$\text{Distributive Laws : } X \cdot (Y + Z) = X \cdot Y + X \cdot Z,$$

Complement : $X + X' = 1$, $X \cdot X' = 0$,

The complement X' is unique.

Idempotent Law : $X + X = X$, $X \cdot X = X$

$$X + Y \cdot Z = (X + Y) \cdot (X + Z)$$

Boundedness Law: $X + 1 = 1$: $X \cdot 0 = 0$

Absorption Law : $X + (X \cdot Y) = X$: $X \cdot (X + Y) = X$

Elimination Law : $X + (X' \cdot Y) = X + Y$, $X \cdot (X' + Y) = X \cdot Y$

Involution theorem : $X'' = X$

5.7 DIGITAL CIRCUITS

5.7.1 Logic Gates

A logic gate is an electronic circuit/device which makes the logical decisions. To arrive at this decisions, the most common logic gates used are OR, AND, NOT, NAND, and NOR gates. The NAND and NOR gates are called universal gates. The exclusive-OR gate is another logic gate which can be constructed using AND, OR and NOT gate.

Logic gates have one or more inputs and only one output. The output is active only for certain input combinations. Logic gates are the building blocks of any digital circuit. Logic gates are also called switches. With the advent of integrated circuits, switches have been replaced by TTL (Transistor Transistor Logic) circuits and CMOS circuits. Here I give example circuits on how to construct simples gates.

Symbolic Logic

Boolean algebra derives its name from the mathematician George Boole. Symbolic Logic uses values, variables and operations.

Inversion

A small circle on an input or an output indicates inversion. See the NOT, NAND and NOR gates given below for examples.

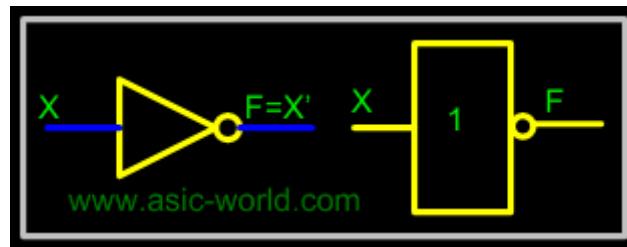


Figure 3.2 Inverter

Multiple Input Gates

Given commutative and associative laws, many logic gates can be implemented with more than two inputs, and for reasons of space in circuits, usually multiple input, complex gates are made. You will encounter such gates in real world (maybe you could analyze an ASIC lib to find this)

AND Gate

The AND gate performs logical multiplication, commonly known as AND function. The AND gate has two or more inputs and single output. The output of AND gate is HIGH only when all its inputs are HIGH (i.e. even if one input is LOW, Output will be LOW).

If X and Y are two inputs, then output F can be represented mathematically as $F = X \cdot Y$. Here dot (.) denotes the AND operation. Truth table and symbol of the AND gate is shown in the Figure below.

Symbol

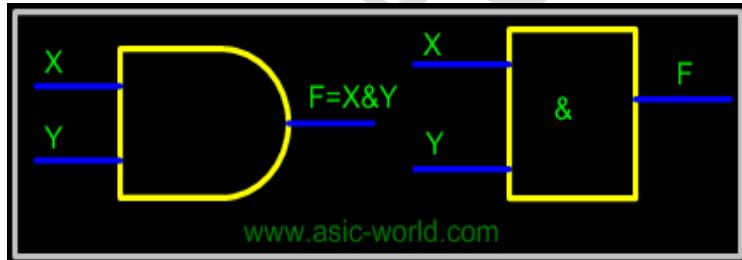


Figure. 3.3 AND Gate

Truth Table

X	Y	F
0	0	0
0	1	0
1	0	0
1	1	1

Two input AND gate using "diode-resistor" logic is shown in Figure below, where X, Y are inputs and F is the output

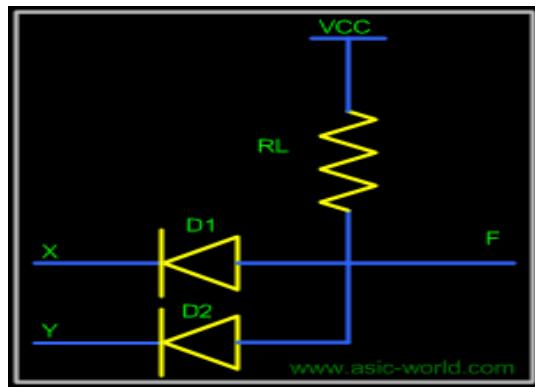


Figure 3.4 Diode resistor logic

If $X = 0$ and $Y = 0$, then both diodes D1 and D2 are forward biased and thus both diodes conduct and pull F low.

If $X = 0$ and $Y = 1$, D2 is reverse biased, thus does not conduct. But D1 is forward biased, thus conducts and thus pulls F low

If $X = 1$ and $Y = 0$, D1 is reverse biased, thus does not conduct. But D2 is forward biased, thus conducts and thus pulls F low.

If $X = 1$ and $Y = 1$, then both diodes D1 and D2 are reverse biased and thus both the diodes are in cut-off and thus there is no drop in voltage at F. Thus F is HIGH.

Switch Representation of AND Gate

In the Figure below, X and Y are two switches which have been connected in series (or just cascaded) with the load LED and source battery. When both switches are closed, current flows to LED.



Figure 3.5 Switch representation

OR Gate

The OR gate performs logical addition, commonly known as OR function. The OR gate has two or more

inputs and single output. The output of OR gate is HIGH only when any one of its inputs are HIGH (i.e. even if one input is HIGH, Output will be HIGH)

If X and Y are two inputs, then output F can be represented mathematically as $F = X+Y$. Here plus sign (+) denotes the OR operation. Truth table and symbol of the OR gate is shown in the Figure below.

Symbol

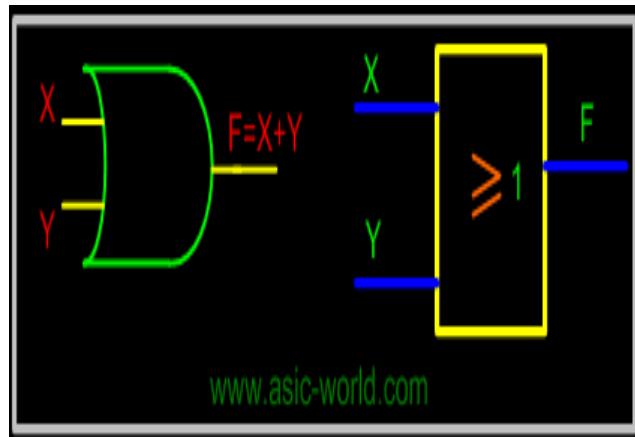


Figure 3.6 OR Gate

Truth Table

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	1

Circuit

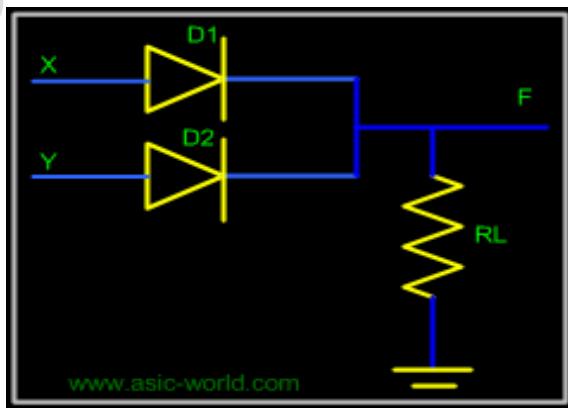


Figure. 3.7 Circuit Representation

If $X = 0$ and $Y = 0$, then both diodes D1 and D2 are reverse biased and thus both the diodes are in cut-off and thus F is low

If $X = 0$ and $Y = 1$, D1 is reverse biased, thus does not conduct. But D2 is forward biased, thus conducts and thus pulling F to HIGH.

If $X = 1$ and $Y = 0$, D2 is reverse biased, thus does not conduct. But D1 is forward biased, thus conducts and thus pulling F to HIGH.

If $X = 1$ and $Y = 1$, then both diodes D1 and D2 are forward biased and thus both the diodes conduct and thus F is HIGH.

Switch Representation of OR Gate

In the Figure, X and Y are two switches which have been connected in parallel, and this is connected in series with the load LED and source battery. When both switches are open, current does not flow to LED, but when any switch is closed then current flows.

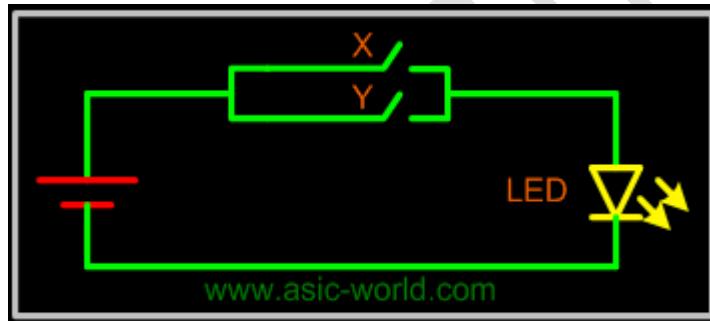


Figure 3.8 Switch representation

NOT Gate

The NOT gate performs the basic logical function called inversion or complementation. NOT gate is also called inverter. The purpose of this gate is to convert one logic level into the opposite logic level. It has one input and one output. When a HIGH level is applied to an inverter, a LOW level appears on its output and vice versa.

If X is the input, then output F can be represented mathematically as $F = X'$. Here apostrophe (') denotes the NOT (inversion) operation. There are a couple of other ways to represent inversion, $F = !X$, here ! represents inversion. Truth table and NOT gate symbol is shown in the Figure below

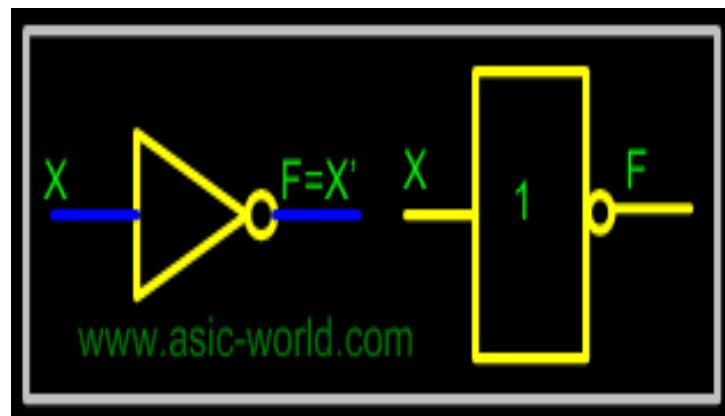


Figure 3.9 NOT Gate

Truth Table

X	F
0	1
1	0

NOT gate using "transistor-resistor" logic is shown in the Figure below, where X is the input and F is the output

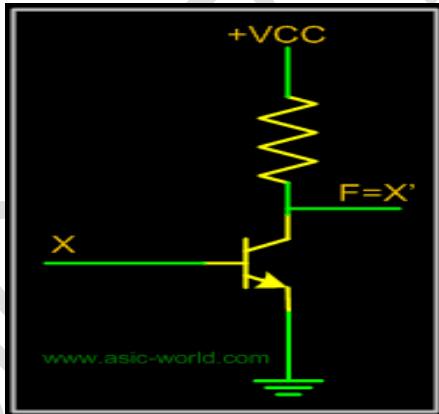


Figure. 3.10 Transistor resistor logic

When $X = 1$, The transistor input pin 1 is HIGH, this produces the forward bias across the emitter base junction and so the transistor conducts. As the collector current flows, the voltage drop across RL increases and hence F is LOW.

When $X = 0$, the transistor input pin 2 is LOW: this produces no bias voltage across the transistor base emitter junction. Thus Voltage at F is HIGH.

NAND Gate

NAND gate is a cascade of AND gate and NOT gate, as shown in the Figure below. It has two or more inputs and only one output. The output of NAND gate is HIGH when any one of its input is LOW (i.e. even if one input is LOW, Output will be HIGH).

NAND From AND and NOT

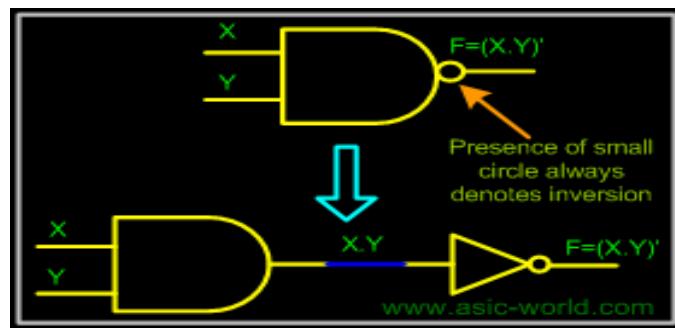


Figure 3.11 NAND gate realization from AND and NOT

If X and Y are two inputs, then output F can be represented mathematically as $F = (X \cdot Y)'$. Here dot (.) denotes the AND operation and (') denotes inversion. Truth table and symbol of the N AND gate is shown in the Figure below.

Symbol

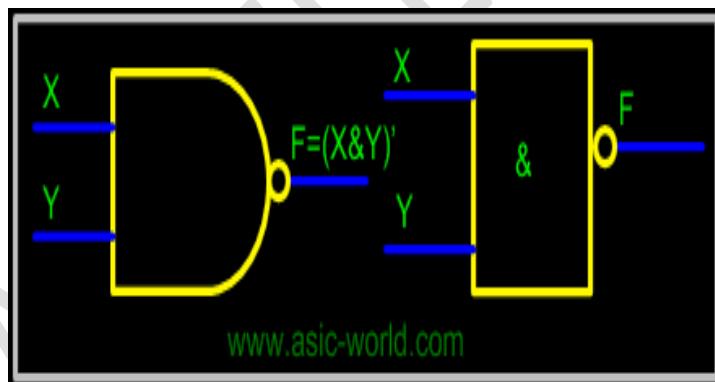


Figure 3.12 NAND Gate

Truth table

X	Y	F
0	0	1
0	1	1
1	0	1
1	1	1

NOR Gate

NOR gate is a cascade of OR gate and NOT gate, as shown in the Figure below. It has two or more inputs and only one output. The output of NOR gate is HIGH when all its inputs are LOW (i.e. even if one input is HIGH, output will be LOW)

Symbol

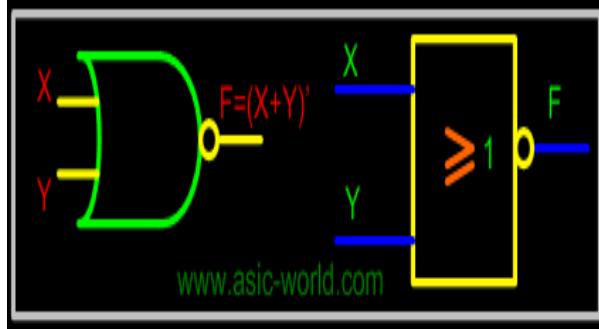


Figure. 3.13 NOR Gate

If X and Y are two inputs, then output F can be represented mathematically as $F = (X+Y)'$; here plus (+) denotes the OR operation and (') denotes inversion. Truth table and symbol of the NOR gate is shown in the Figure below.

Truth Table

X	Y	$F = (X+Y)'$
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

An Exclusive-OR (XOR) gate is gate with two or three or more inputs and one output. The output of a two-input XOR gate assumes a HIGH state if one and only one input assumes a HIGH state. This is equivalent to saying that the output is HIGH if either input X or input Y is HIGH exclusively, and LOW when both are 1 or 0 simultaneously

If X and Y are two inputs, then output F can be represented mathematically as $F = X \oplus Y$. Here \oplus denotes the XOR operation. $X \oplus Y$ and is equivalent to $X \cdot Y' + X' \cdot Y$. Truth table and symbol of the XOR gate is shown in the Figure below

XOR From Simple gates

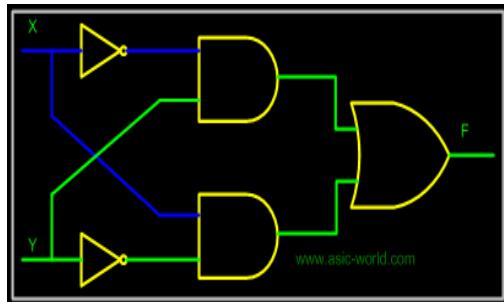


Figure 3.13 XOR from simple gate

Symbol

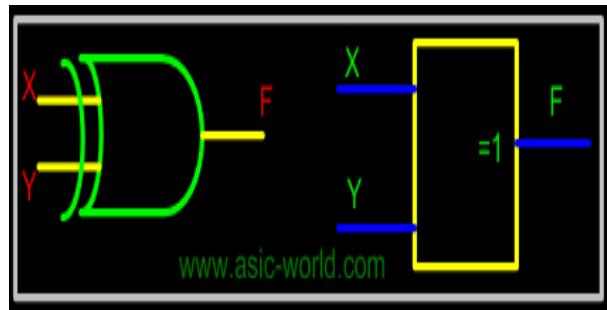


Figure 3.14 XOR symbol

Truth Table

X	Y	F
0	0	1
0	1	0
1	0	0
1	1	1

XNOR Gate

An Exclusive-NOR (XNOR) gate is a gate with two or three or more inputs and one output. The output of a two-input XNOR gate assumes a HIGH state if all the inputs assume the same state. This is equivalent to saying that the output is HIGH if both input X and input Y are HIGH exclusively or same as input X and input Y is LOW exclusively, and LOW when both are not same.

If X and Y are two inputs, then output F can be represented mathematically as $F = X \oplus Y$. Here \oplus denotes the XNOR operation. $X \oplus Y$ is equivalent to $X \cdot Y + X' \cdot Y'$. Truth table and symbol of the XNOR gate is shown in the Figure below.

Symbol

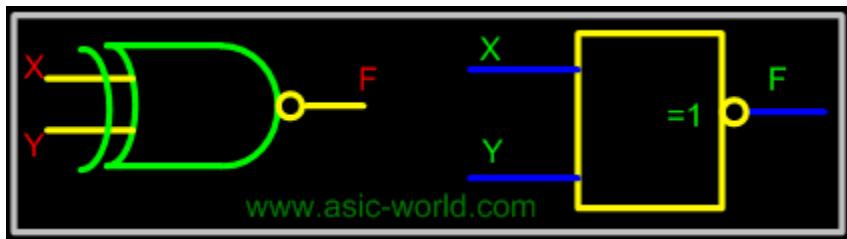


Figure. 3.15 XNOR symbol

Truth Table

X	Y	$F = (X \oplus Y)'$
0	0	1
0	1	0
1	0	0
1	1	1

Universal Gates

Universal gates are the ones which can be used for implementing any gate like AND, OR and NOT, or any combination of these basic gates; NAND and NOR gates are universal gates. But there are some rules that need to be followed when implementing NAND or NOR based gate

To facilitate the conversion to NAND and NOR logic, we have two new graphic symbols for these gates

NAND Gate

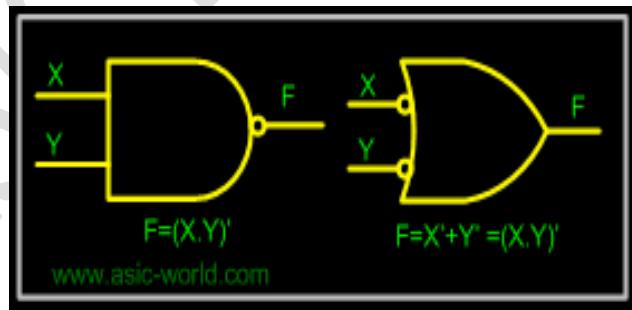


Figure. 3.16 NAND symbol

NOR Gate

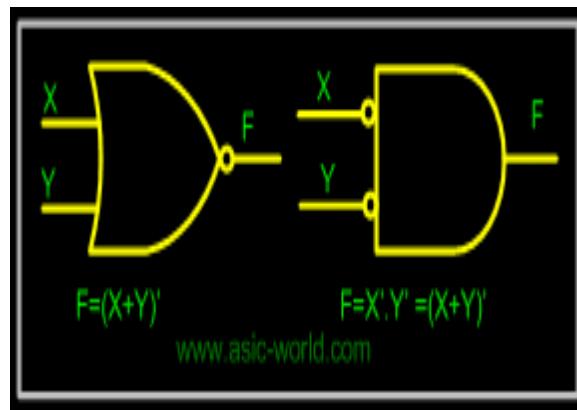


Figure. 3.15 XNOR symbol

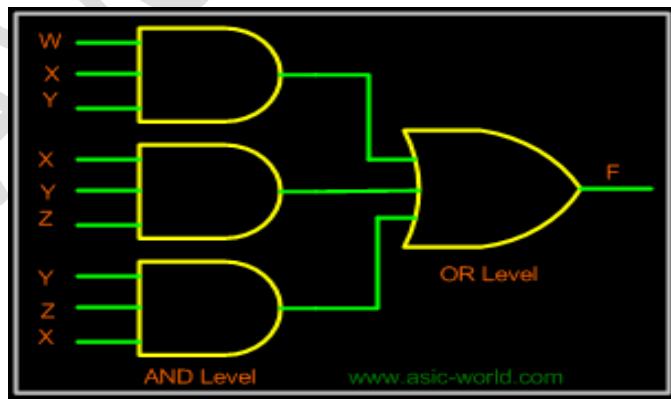
3.7.2 REALIZATION OF LOGICAL EXPRESSIONS USING NAND GATES

Any logic function can be implemented using NAND gates. To achieve this, first the logic function has to be written in Sum of Product (SOP) form. Once logic function is converted to SOP, then it is very easy to implement using NAND gate. In other words any logic circuit with AND gates in first level and OR gates in second level can be converted into a NAND-NAND gate circuit.

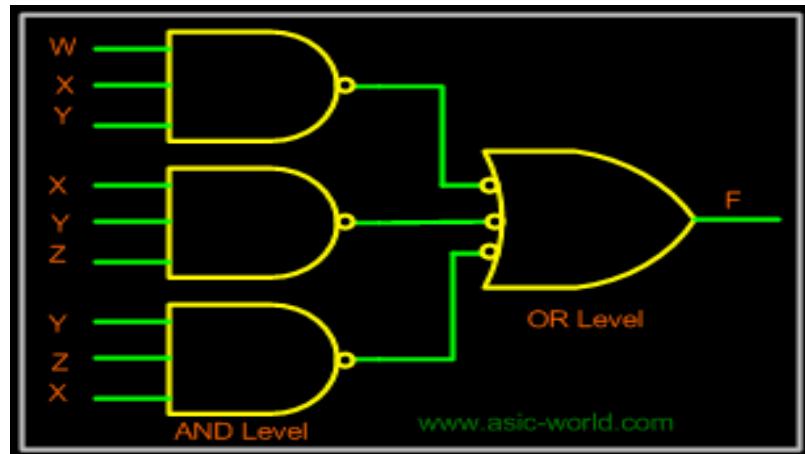
Consider the following SOP expression

$$F = W.X.Y + X.Y.Z + Y.Z.$$

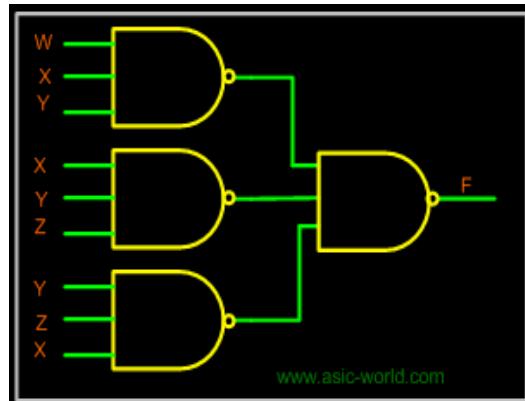
The above expression can be implemented with three AND gates in first stage and one OR gate in second stage as shown in Figure



If bubbles are introduced at AND gates output and OR gates inputs (the same for NOR gates), the above circuit becomes as shown in Figure



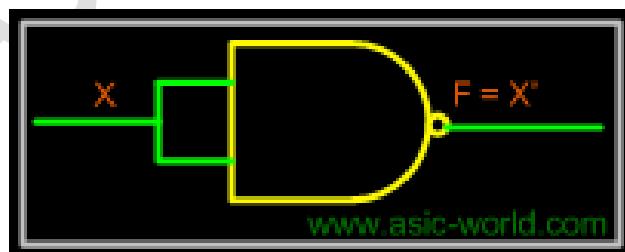
Now replace OR gate with input bubble with the NAND gate. Now we have circuit which is fully implemented with just NAND gates.



Realization of logic gates using NAND gates

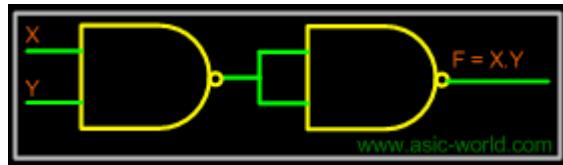
Implementing an inverter using NAND gate

Input	Output	Rule
$(X \cdot X)'$	$= X'$	Idempotent



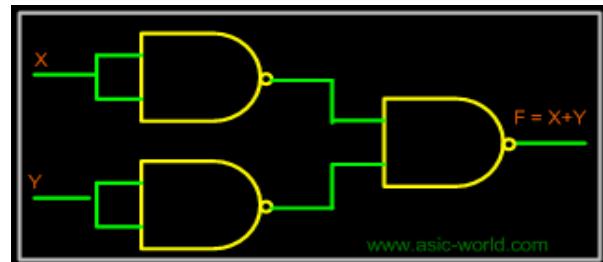
Implementing AND using NAND gates

Input	Output	Rule
$((XY)'(XY))'$	$= ((XY)')'$	Idempotent
	$= (XY)$	Involution



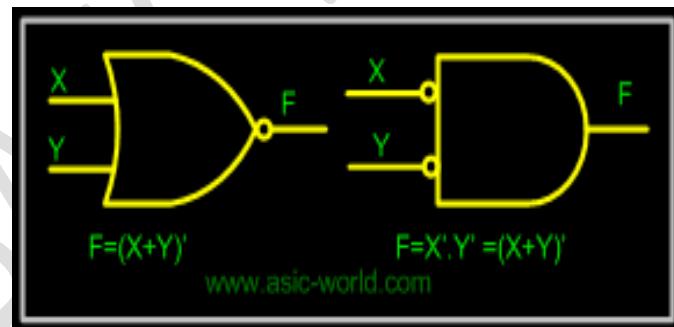
★ Implementing OR using NAND gates

Input	Output	Rule
$((XX)'(YY))'$	$= (X'Y)'$	Idempotent
	$= X''+Y''$	DeMorgan
	$= X+Y$	Involution



★ Implementing NOR using NAND gates

Input	Output	Rule
$((XX)'(YY))'$	$= (X'Y)'$	Idempotent
	$= X''+Y''$	DeMorgan
	$= X+Y$	Involution
	$= (X+Y)'$	Idempotent



5.7.3 REALIZATION OF LOGICAL EXPRESSIONS USING NOR GATES

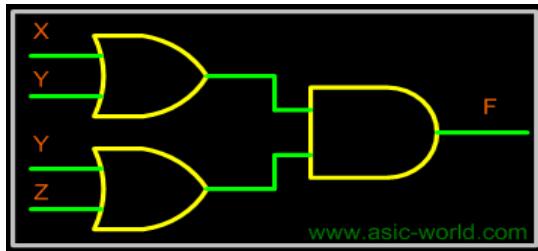
Any logic function can be implemented using NOR gates. To achieve this, first the logic function has to be written in Product of Sum (POS) form. Once it is converted to POS, then it's very easy to implement using NOR gate. In other words any logic circuit with OR gates in first level and AND gates in second level can be converted into a NOR-NOR gate circuit.

Consider the following POS expression

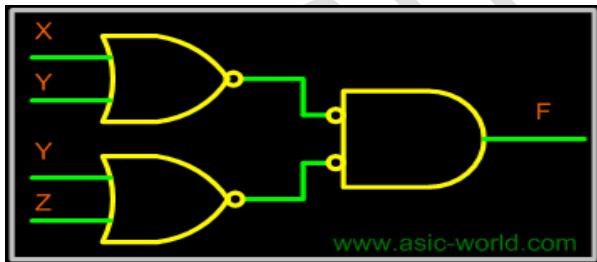
$$F = (X+Y)(Y+Z)$$

Input	Output	Rule	The above
-------	--------	------	--------------

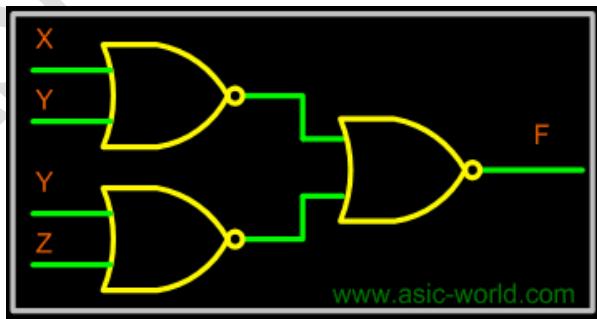
The expression can be implemented with three OR gates in first stage and one AND gate in second stage as shown in Figure.



If bubbles are introduced at the output of the OR gates and the inputs of AND gate, the above circuit becomes as shown in Figure.



Now replace AND gate with input bubble with the NOR gate. Now we have circuit which is fully implemented with just NOR gates.



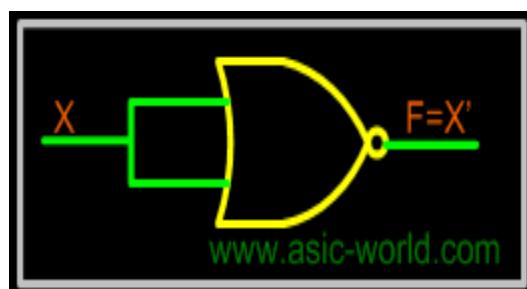
Realization of logic gates using NOR gates

Implementing an inverter using NOR gate

$$(X+X)'$$

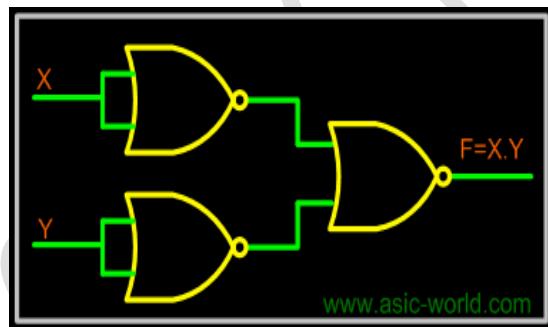
$$= X'$$

Idempotent



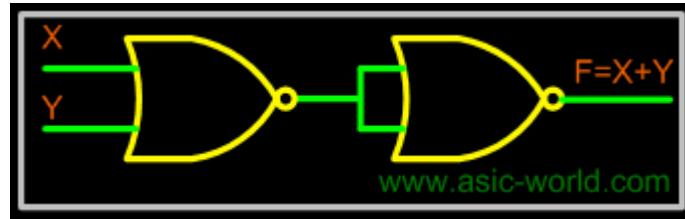
Implementing AND using NOR gates

	Output	Rule
$((X+X)' + (Y+Y))'$	$= (X'+Y)'$	Idempotent
	$= X'' \cdot Y''$	DeMorgan
	$= (X \cdot Y)$	Involution



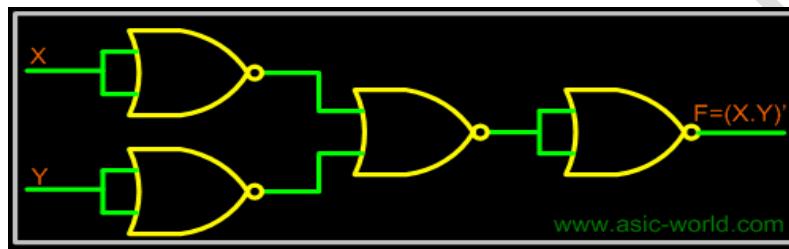
Implementing OR using NOR gates

Input	Output	Rule
$((X+Y)' + (X+Y))'$	$= ((X+Y)')'$	Idempotent
	$= X+Y$	Involution



Implementing NAND using NOR gates

Input	Output	Rule
$((X+Y)' + (X+Y))'$	$= ((X+Y)')'$	Idempotent
	$= X+Y$	Involution
	$= (X+Y)'$	Idempotent



Arithmetic circuits are the ones which perform arithmetic operations like addition, subtraction, multiplication, division, parity calculation. Most of the time, designing these circuits is the same as designing muxers, encoders and decoders.

In the next few pages we will see few of these circuits in detail.

5.7.4 HALF ADDERS AND FULL ADDER

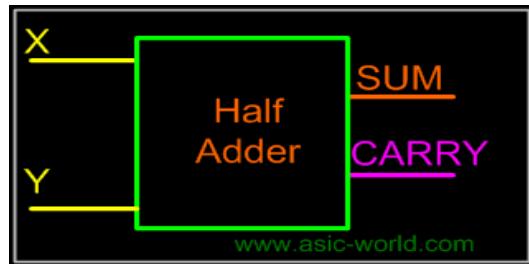
Adders are the basic building blocks of all arithmetic circuits; adders add two binary numbers and give out sum and carry as output. Basically we have two types of adders

Half Adder

Adding two single-bit binary values X, Y produces a sum S bit and a carry out C-out bit. This operation is called half addition and the circuit to realize it is called a half adder.

Truth Table

X	Y	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Symbol

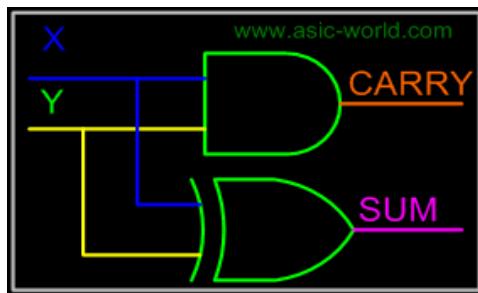
$$S(X,Y) = \Sigma(1,2)$$

$$S = X'Y + XY'$$

$$S = X \oplus Y$$

$$\text{CARRY}(X,Y) = \Sigma(3)$$

$$\text{CARRY} = XY$$

Circuit**Full Adder**

Full adder takes a three-bits input. Adding two single-bit binary values X, Y with a carry input bit C-in produces a sum bit S and a carry out C-out bit.

Truth Table

X	Y	Z	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{SUM}(X,Y,Z) = \Sigma(1,2,4,7)$$

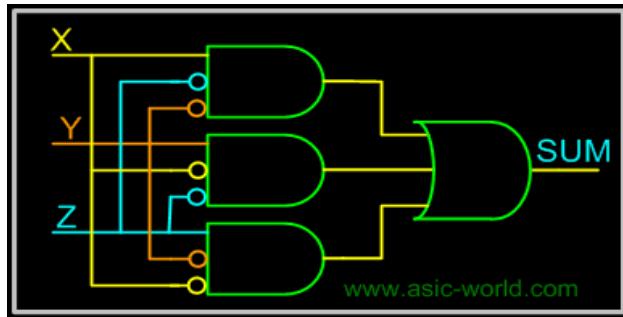
$$\text{CARRY}(X,Y,Z) = \Sigma(3,5,6,7)$$

Full Adder using AND-OR

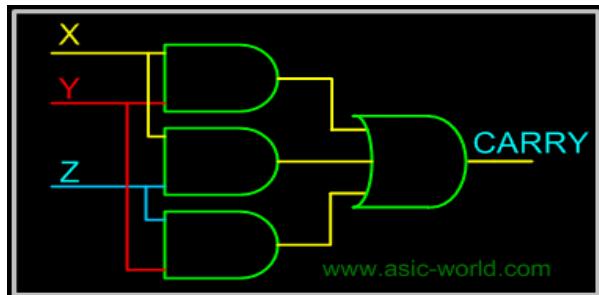
The below implementation shows implementing the full adder with AND-OR gates, instead of

using XOR gates. The basis of the circuit below is from the above Kmap.

Circuit-SUM

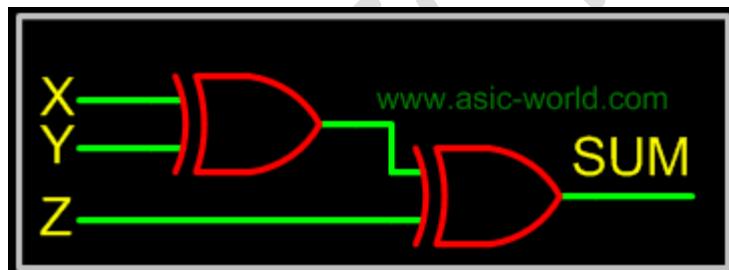


Circuit-CARRY

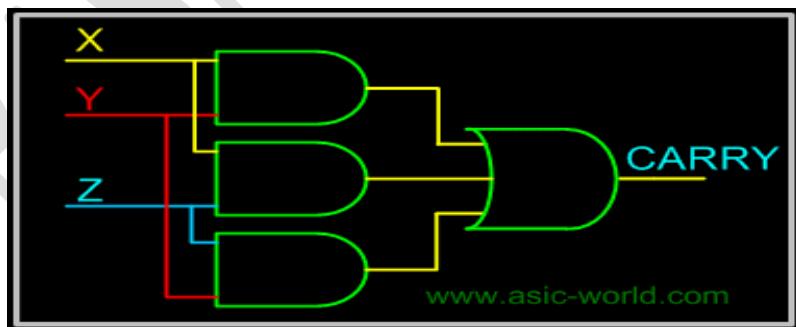


★ Full Adder using AND-OR

Circuit-SUM



Circuit-CARRY



5.8 FLIPFLOPS

Latches and *flip-flops* are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs

are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops: SR, D, JK, and T. The major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations.

The simplest sequential circuit or storage element is a *bistable element*, which is constructed with two inverters connected sequentially in a loop as shown in Figure . It has no inputs and two outputs labeled Q and \bar{Q} . Since the circuit has no inputs, we cannot change the values of Q and \bar{Q} . However, Q will take on whatever value it happens to be when the circuit is first powered up. Assume that $Q = 0$ when we switch on the power. Since Q is also the input to the bottom inverter, \bar{Q} , therefore, is a 1. A 1 going to the input of the top inverter will produce a 0 at the output Q , which is what we started off with. Similarly, if we start the circuit with $Q = 1$, we will get $\bar{Q} = 0$, and again we get a stable situation. A bistable element has memory in the sense that it can remember the content (or state) of the circuit indefinitely. Using the signal Q as the state variable to describe the state of the circuit, we can say that the circuit has two stable states: $Q = 0$, and $Q = 1$; hence the name “bistable.”

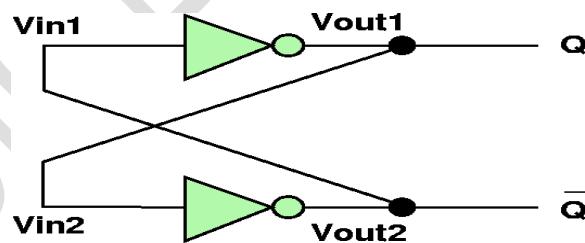


Fig Bistable Element

5.8.1 S R FLIPFLOP

The R-S (Reset Set) flip flop is the simplest flip flop of all and easiest to understand. It is basically a device which has two outputs one output being the inverse or complement of the other, and two inputs. A pulse on one of the inputs to take on a particular logical state. The outputs will then remain in this

state until a similar pulse is applied to the other input. The two inputs are called the Set and Reset input (sometimes called the preset and clear inputs).

Such flip flop can be made simply by cross coupling two inverting gates either NAND or NOR gate could be used Figure (a) shows on RS flip flop using NAND gate and Figure (b) shows the same circuit using NOR gate

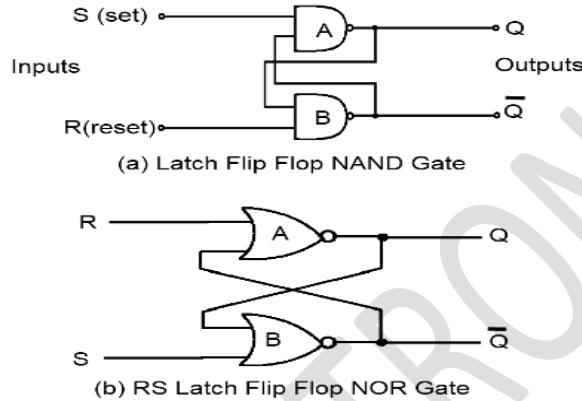


Figure : Latch R-S Flip Flop Using NAND and NOR Gates

To describe the circuit of Figure 4.6(a), assume that initially both R and S are at the logic 1 state and that output is at the logic 0 state.

Now, if $Q = 0$ and $R = 1$, then these are the states of inputs of gate B, therefore the outputs of gate B is at 1 (making it the inverse of Q i.e. 0). The output of gate B is connected to an input of gate A so if $S = 1$, both inputs of gate A are at the logic 1 state. This means that the output of gate A must be 0 (as was originally specified). In other words, the 0 state at Q is continuously disabling gate B so that any change in R has no effect. Also the 1 state at \bar{Q} is continuously enabling gate A so that any change S will be transmitted through to Q . The above conditions constitute one of the stable states of the device referred to as the Reset state since $Q = 0$.

Now suppose that the R-S flip flop in the Reset state, the S input goes to 0. The output of gate A i.e. Q will go to 1 and with $Q = 1$ and $R = 1$, the output of gates B (\bar{Q}) will go to 0 with \bar{Q} now 0 gate A is disabled keeping Q at 1. Consequently, when S returns to the 1 state it has no effect on the flip flop

whereas a change in R will cause a change in the output of gate B. The above conditions constitute the other stable state of the device, called the Set state since $Q = 1$. Note that the change of the state of S from 1 to 0 has caused the flip flop to change from the Reset state to the Set state.

There is another input condition which has not yet been considered. That is when both the R and S inputs are taken to the logic state 0. When this happens both Q and \bar{Q} will be forced to 1 and will remain so far as long as R and S are kept at 0. However when both inputs return to 1 there is no way of knowing whether the flip flop will latch in the Reset state or the Set state. The condition is said to be indeterminate because of this indeterminate state great care must be taken when using R-S flip flop to ensure that both inputs are not instructed simultaneously.

Table 1: The truth table for the NAND R-S flip flop

Initial Conditions		Inputs (Pulsed)		Final Output	
Q	S	R	Q	\bar{Q}	
1	0	0	indeterminate		
1	0	1	1	0	
1	1	0	0	1	
1	1	1	1	0	
0	0	0	indeterminate		
0	0	1	1	0	
0	1	0	0	1	
0	1	1	0	1	

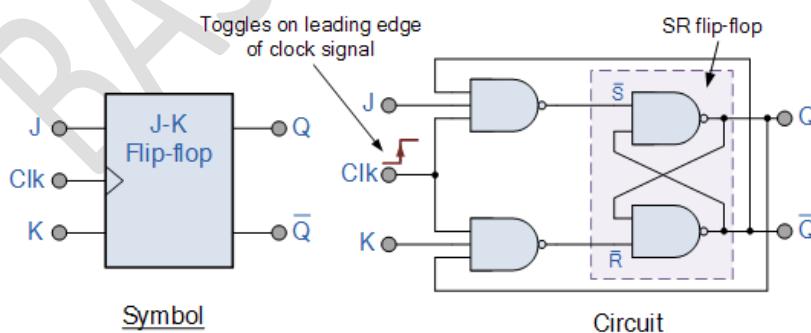
or more simply shown in Table 2

Table 2: Simple NAND R-S Flip Flop Truth Table		
S	R	Q
0	0	indeterminate
0	1	Set (1)
1	0	Reset(0)
1	1	No Change

When NOR gate are used the R and S inputs are transposed compared with the NAND version. Also the stable state when R and S are both 0. A change of state is effected by pulsing the appropriate input to the 1 state. The indeterminate state is now when both R and S are simultaneously at logic 1. Table 3 shows this operation.

Table 3: NOR Gate R-S Flip Flop Truth Table		
S	R	Q
0	0	No Change
0	1	Reset (0)
1	0	Set (1)
1	1	Indeterminate

5.8.2 JK FLIPFLOP



The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to

logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”. The symbol for a JK flip flop is similar to that of an SR Bistable Latch as seen in the previous tutorial except for the addition of a clock input.

Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: $J = S$ and $K = R$.

The two 2-input AND gates of the gated SR bistable have now been replaced by two 3-input NAND gates with the third input of each gate connected to the outputs at Q and \bar{Q} . This cross coupling of the SR flip-flop allows the previously invalid condition of $S = “1”$ and $R = “1”$ state to be used to produce a “toggle action” as the two inputs are now interlocked.

If the circuit is now “SET” the J input is inhibited by the “0” status of Q through the lower NAND gate. If the circuit is “RESET” the K input is inhibited by the “0” status of \bar{Q} through the upper NAND gate. As Q and \bar{Q} are always different we can use them to control the input. When both inputs J and K are equal to logic “1”, the JK flip flop toggles as shown in the following truth table.

The Truth Table for the JK Function

same as for the SR Latch	Input		Output		Description
	J	K	Q	\bar{Q}	
	0	0	0	0	Memory no change
	0	0	0	1	
	0	1	1	0	Reset $Q \gg 0$
	0	1	0	1	
	1	0	0	1	Set $Q \gg 1$

	1	0	1	0	
toggle action	1	1	0	1	Toggle
	1	1	1	0	

Then the JK flip-flop is basically an SR flip flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time thereby eliminating the invalid condition seen previously in the SR flip flop circuit.

Also when both the J and the K inputs are at logic level “1” at the same time, and the clock input is pulsed “HIGH”, the circuit will “toggle” from its SET state to a RESET state, or visa-versa. This results in the JK flip flop acting more like a T-type toggle flip-flop when both terminals are “HIGH”.

Although this circuit is an improvement on the clocked SR flip-flop it still suffers from timing problems called “race” if the output Q changes state before the timing pulse of the clock input has time to go “OFF”. To avoid this the timing pulse period (T) must be kept as short as possible (high frequency). As this is sometimes not possible with modern TTL IC’s the much improved Master-Slave JK Flip-flop was developed.

5.8.3 Shift register

We know that one flip-flop can store one-bit of information. In order to store multiple bits of information, we require multiple flip-flops. The group of flip-flops, which are used to hold (store) the binary data is known as register.

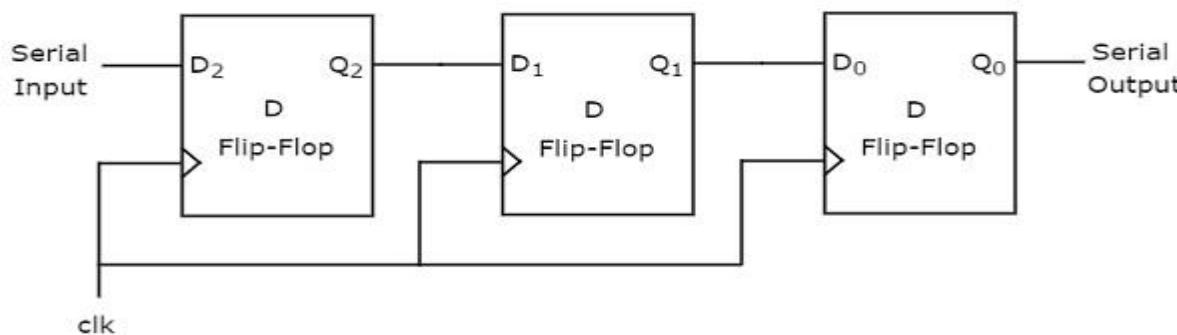
If the register is capable of shifting bits either towards right hand side or towards left hand side is known as shift register. An ‘N’ bit shift register contains ‘N’ flip-flops. Following are the four types of shift registers based on applying inputs and accessing of outputs.

- Serial In - Serial Out shift register
- Serial In - Parallel Out shift register

- Parallel In - Serial Out shift register
- Parallel In - Parallel Out shift register

Serial In - Serial Out (SISO) Shift Register

The shift register, which allows serial input and produces serial output is known as Serial In – Serial Out (SISO) shift register. The block diagram of 3-bit SISO shift register is shown in the following figure.



This block diagram consists of three D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as serial input. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we can receive the bits serially from the output of right most D flip-flop. Hence, this output is also called as serial output.

Example

Let us see the working of 3-bit SISO shift register by sending the binary information “011” from LSB to MSB serially at the input.

Assume, initial status of the D flip-flops from leftmost to rightmost is $Q_2Q_1Q_0=000$. We can understand the working of 3-bit SISO shift register from the following table.

No of positive edge of Clock	Serial Input	Q2	Q1	Q0
0	-	0	0	0
1	1(LSB)	1	0	0
2	1	1	1	0
3	0(MSB)	0	1	1(LSB)
4	-	-	0	1
5	-	-	-	0(MSB)

The initial status of the D flip-flops in the absence of clock signal is $Q_2Q_1Q_0=000$ $Q_2Q_1Q_0=000$.

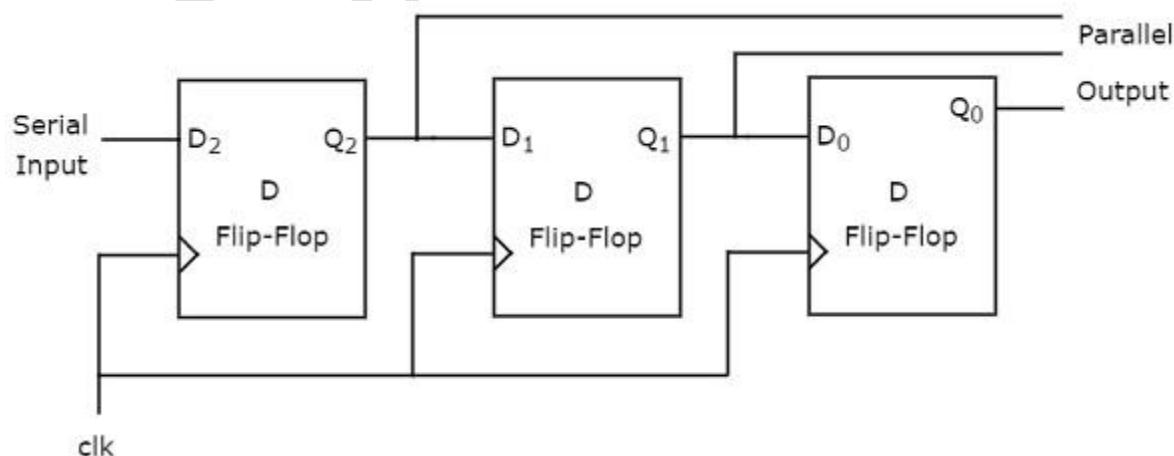
Here, the serial output is coming from Q_0Q_0 . So, the LSB (1) is received at 3rd positive edge of clock and the MSB (0) is received at 5th positive edge of clock.

Therefore, the 3-bit SISO shift register requires five clock pulses in order to produce the valid output.

Similarly, the N-bit SISO shift register requires $2N-1$ clock pulses in order to shift 'N' bit information.

Serial In - Parallel Out (SIPO) Shift Register

The shift register, which allows serial input and produces parallel output is known as Serial In – Parallel Out (SIPO) shift register. The block diagram of 3-bit SIPO shift register is shown in the following figure.



This circuit consists of three D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as serial input. For every positive edge triggering of clock signal, the data shifts from one stage to the next. In this case, we can access the outputs of each D flip-flop in parallel. So, we will get parallel outputs from this shift register.

Example

Let us see the working of 3-bit SIPO shift register by sending the binary information “011” from LSB to MSB serially at the input.

Assume, initial status of the D flip-flops from leftmost to rightmost is $Q_2Q_1Q_0=000$. Here, Q_2Q_2 & Q_0Q_0 are MSB & LSB respectively. We can understand the working of 3-bit SIPO shift register from the following table.

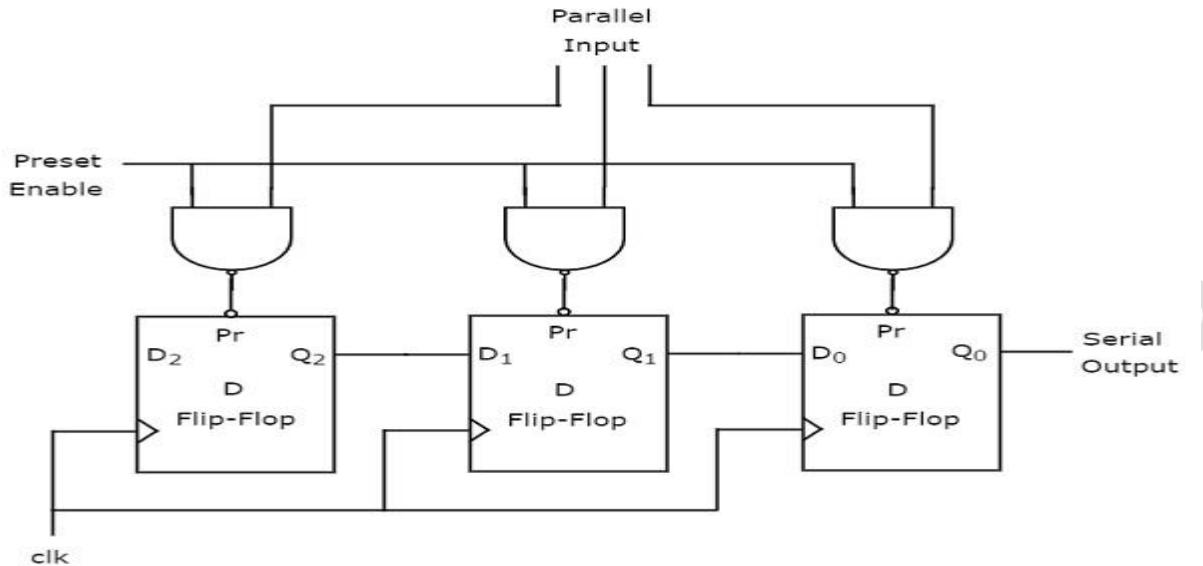
No of positive edge of Clock	Serial Input	Q_2 (MSB)	Q_1	Q_0 (LSB)
0	-	0	0	0
1	1(LSB)	1	0	0
2	1	1	1	0
3	0(MSB)	0	1	1

The initial status of the D flip-flops in the absence of clock signal is $Q_2Q_1Q_0=000$. The binary information “011” is obtained in parallel at the outputs of D flip-flops for third positive edge of clock.

So, the 3-bit SIPO shift register requires three clock pulses in order to produce the valid output. Similarly, the N-bit SIPO shift register requires N clock pulses in order to shift ‘N’ bit information.

Parallel In - Serial Out (PISO) Shift Register

The shift register, which allows parallel input and produces serial output is known as Parallel In – Serial Out (PISO) shift register. The block diagram of 3-bit PISO shift register is shown in the following figure.



This circuit consists of three D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

In this shift register, we can apply the parallel inputs to each D flip-flop by making Preset Enable to 1. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we will get the serial output from the right most D flip-flop.

Example

Let us see the working of 3-bit PISO shift register by applying the binary information “011” in parallel through preset inputs.

Since the preset inputs are applied before positive edge of Clock, the initial status of the D flip-flops from leftmost to rightmost will be $Q_2Q_1Q_0=011Q_2Q_1Q_0=011$. We can understand the working of 3-bit PISO shift register from the following table.

No of positive edge of Clock	Q2	Q1	Q0
0	0	1	1(LSB)
1	-	0	1
2	-	-	0(LSB)

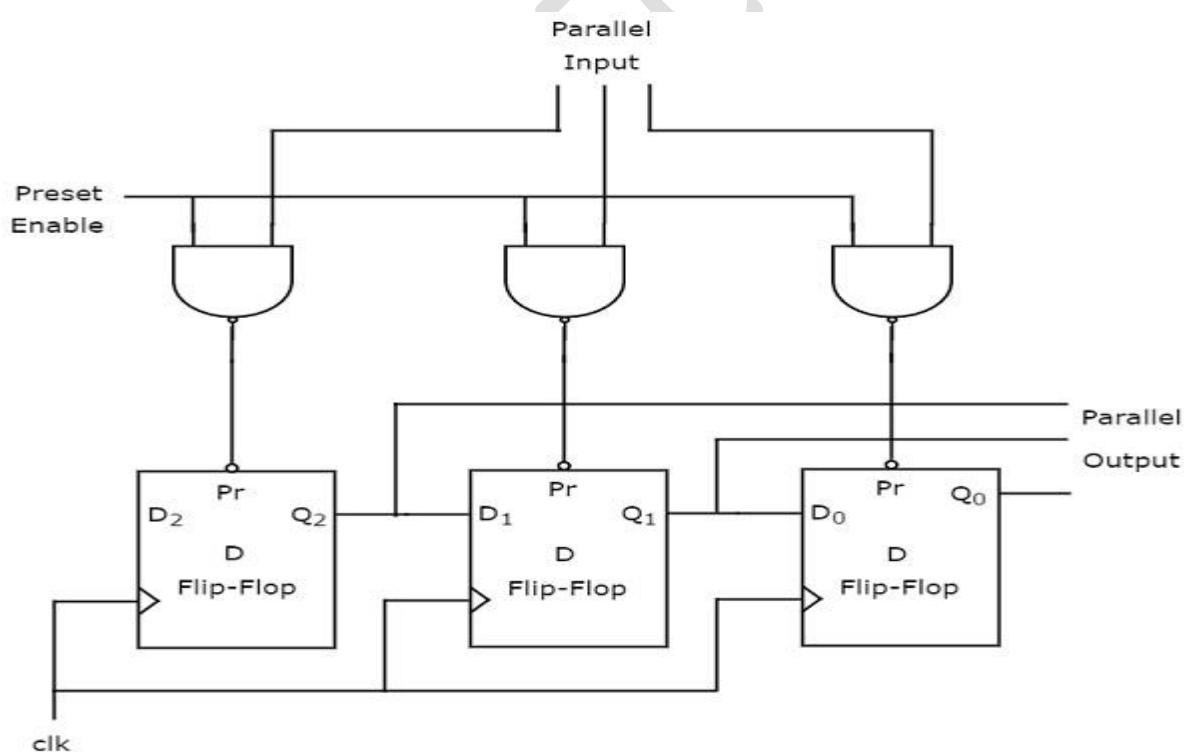
Here, the serial output is coming from Q0Q0. So, the LSB (1) is received before applying positive edge of clock and the MSB (0) is received at 2nd positive edge of clock.

Therefore, the 3-bit PISO shift register requires two clock pulses in order to produce the valid output.

Similarly, the N-bit PISO shift register requires N-1 clock pulses in order to shift 'N' bit information.

Parallel In - Parallel Out (PIPO) Shift Register

The shift register, which allows parallel input and produces parallel output is known as Parallel In – Parallel Out (PIPO) shift register. The block diagram of 3-bit PIPO shift register is shown in the following figure.



This circuit consists of three D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

In this shift register, we can apply the parallel inputs to each D flip-flop by making Preset Enable to 1. We can apply the parallel inputs through preset or clear. These two are asynchronous inputs. That means, the flip-flops produce the corresponding outputs, based on the values of asynchronous inputs. In this case, the effect of outputs is independent of clock transition. So, we will get the parallel outputs from each D flip-flop.

Example

Let us see the working of 3-bit PIPO shift register by applying the binary information “011” in parallel through preset inputs.

Since the preset inputs are applied before positive edge of Clock, the initial status of the D flip-flops from leftmost to rightmost will be $Q_2Q_1Q_0=011$ $Q_2Q_1Q_0=011$. So, the binary information “011” is obtained in parallel at the outputs of D flip-flops before applying positive edge of clock.

Therefore, the 3-bit PIPO shift register requires zero clock pulses in order to produce the valid output. Similarly, the N-bit PIPO shift register doesn't require any clock pulse in order to shift ‘N’ bit information.