

Unit - 1

$$n_i = p_i$$

$n \cdot p = n_i^2$ → for extrinsic semiconductors at a given temperature

$n \cdot p$ = constant for piece of Silicon
with variable doping

$$G = M_{ne} + M_{ph}$$

↑ ↓

mobility of e⁻ mobility of holes

↓ ↓

electron holes

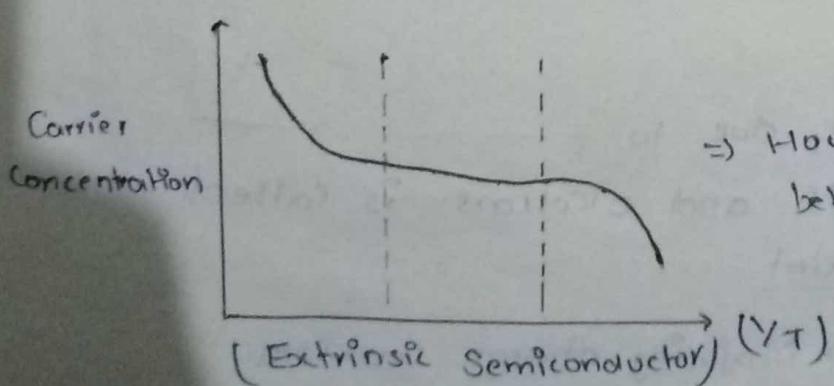
$$M_n > M_p$$

$$\left. \begin{array}{l} \text{for N-type} \Rightarrow n \gg p \\ \text{and } n \approx n_{\text{doping}} \end{array} \right\}$$

$$P = \frac{n_i^2}{n_{\text{doping}}}$$

$$\left. \begin{array}{l} \text{for P-type} \Rightarrow \\ p = n_{\text{doping}} \end{array} \right\}$$

$$n = \frac{n_i^2}{n_{\text{doping}}}$$

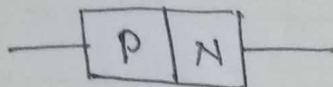


⇒ How extrinsic semiconductor behaves with temp

Two Processes

- ① Thermal generation \rightarrow Creating e⁻ hole pair
- ② e⁻ hole recombination \rightarrow depletion of e⁻ hole at equilibrium both rates are equal.

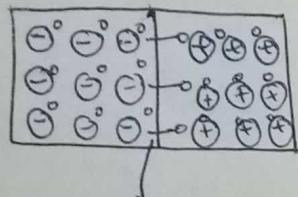
P-N Junction



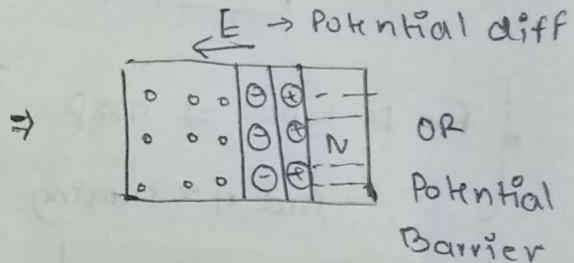
.because of concentration diff Carrier flow.

N to P \rightarrow electron

P to N \rightarrow holes



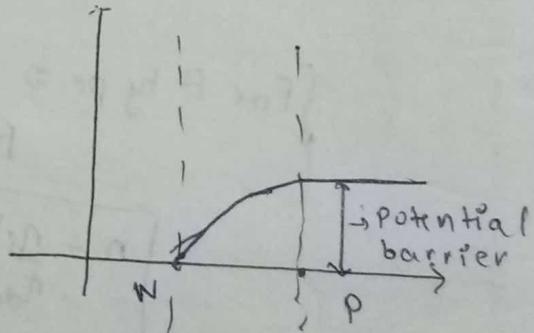
Combination of holes and electron



* Current produced due to Potential difference developed

is called (drift current),

\downarrow
Minority charge carrier

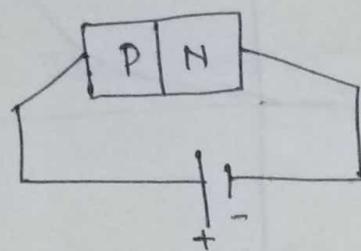


* Current produced due to diffusion of holes and electrons is called diffusion current

\downarrow
Majority charge carrier

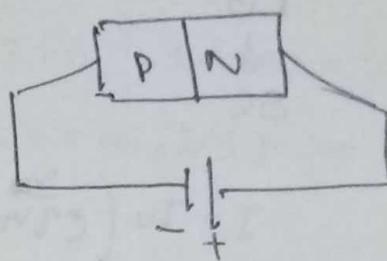
Biassing

① forward biassing

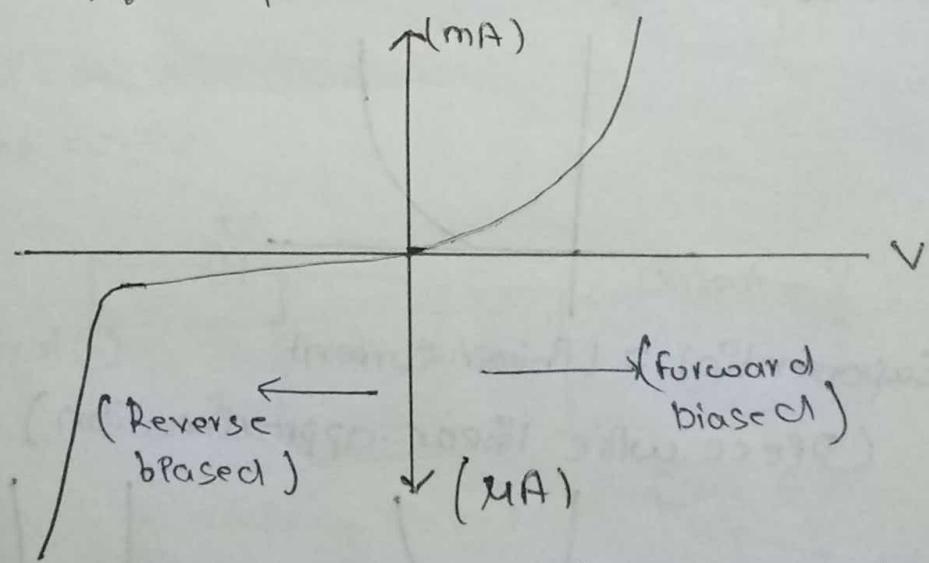
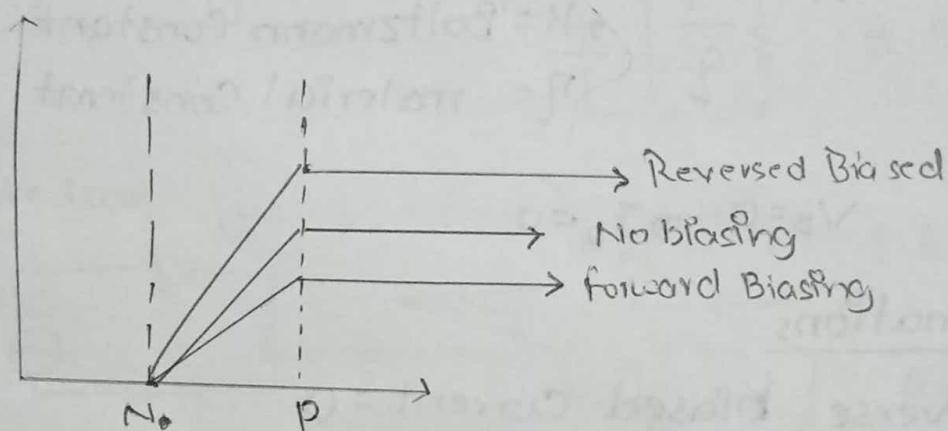


(Current flows)

② Reverse Biased.



(very small amount of current flows)



* Open circuit - Current = 0, Voltage needs to be calculated

* Short circuit - Voltage = 0, Current needs to be calculated

30/5/2022

PN-Junction

FB

SC

RB

OC

$$I = I_0 \left(e^{\frac{V_D}{V_T}} - 1 \right)$$

V_T = Thermal Voltage

V_D = Diode Voltage

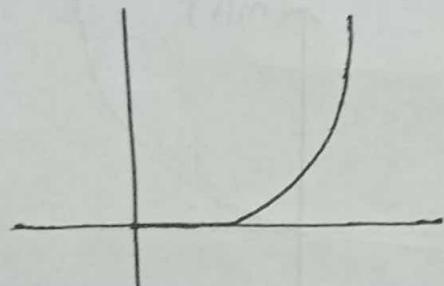
$$V_T = \frac{kT}{q}, k = \text{Boltzmann Constant}$$

$\eta = \text{material Constant}$

$$V_D = 0 \Rightarrow I_D = 0$$

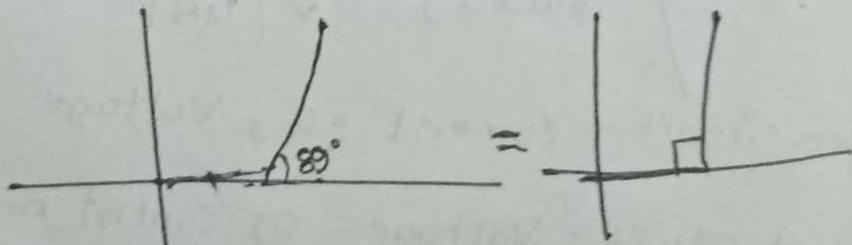
Approximations

1) Reverse Biased Current = 0



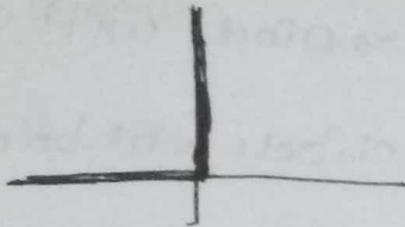
2) Exponential \approx Linear Current

(Piece wise linear approximation)



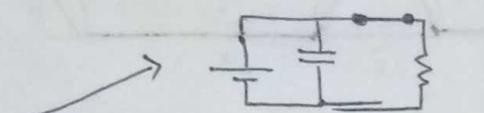
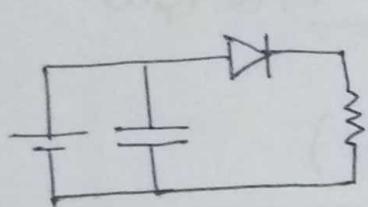
3) Ideal diode

⇒ No potential drop in this scenario
and current is flowing

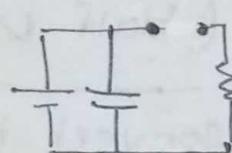


Ideal Diode $\begin{cases} F.B \rightarrow S.C \rightarrow V_D = 0, R = 0, I \rightarrow \text{to be calculated} \\ R.B \rightarrow O.C \rightarrow I_D = 0, R = \infty, V \rightarrow \text{to be calculated} \end{cases}$

Equivalent Circuit Diagram -

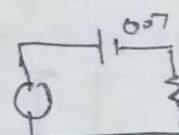
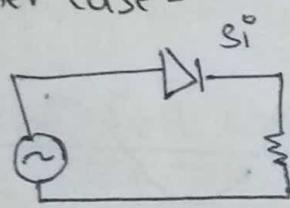


F.B.

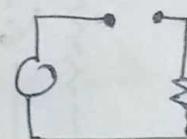


R.B.

In other case -



F.B.

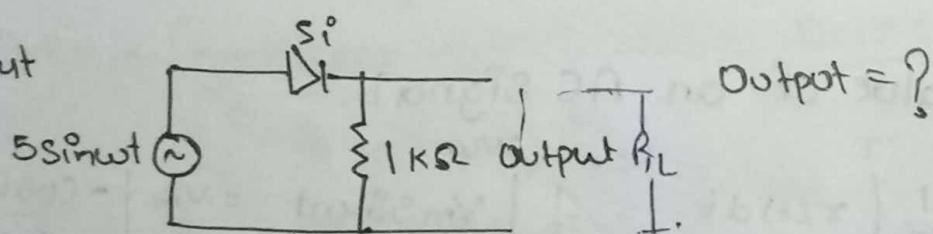


R.B.

$$\text{for } S_i^o = 0.7V$$

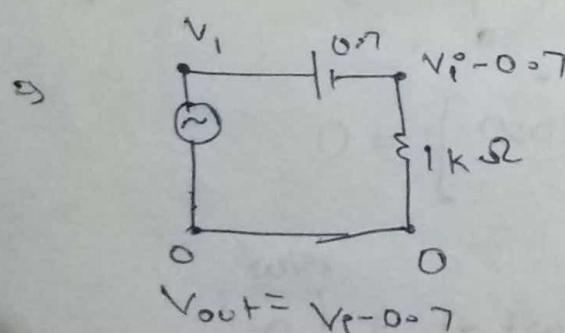
$$G_{re} = 0.3V$$

\Rightarrow Output



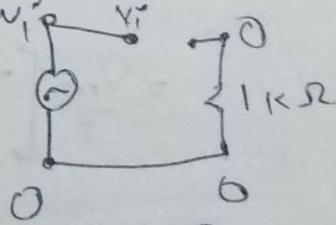
Output = ?

for F.B.



$$V_{out} = V_i - 0.7$$

for R.B.

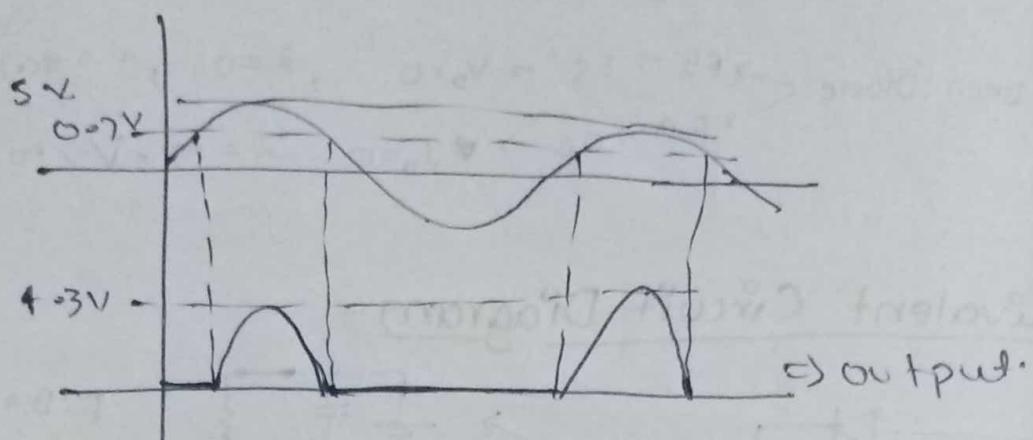


$$V_{out} = 0$$

(But P.D across
Diode = V_i)

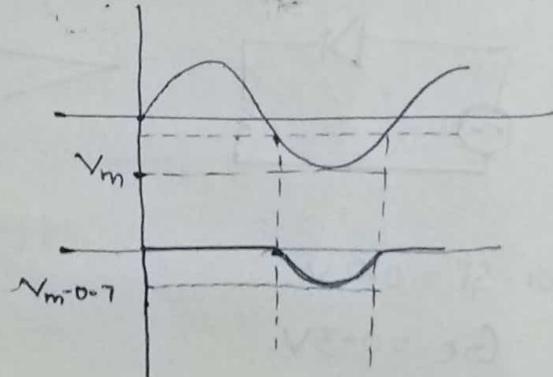
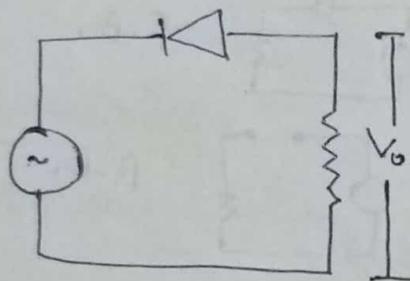
when $V_i \geq 0.7V$ \rightarrow Diode will work

and $V_i < 0.7V$ diode will be off



(Half Wave rectifier)

* Rectifier \rightarrow convert bidirectional to unidirectional



Average Value of an AC Signal

$$x_{avg} = \frac{1}{T} \int_0^T x(t) dt = \frac{1}{T} \int_0^{2\pi/\omega} V_m \sin \omega t dt = \frac{V_m}{T} \left[-\frac{\cos \omega t}{\omega} \right]_0^{2\pi/\omega}$$
$$= \frac{V_m}{T} \left[-\frac{\cos 2\pi + \cos 0}{\omega} \right] = 0$$

$$\text{For Output} - \frac{1}{T} \int_0^{\pi/\omega} V_m \sin \omega t dt + \int_{\pi/\omega}^{2\pi/\omega} 0$$

$$-\frac{V_m}{\omega T} (\cos \pi - \cos 0) = \frac{2V_m \pi \omega}{\omega \times 2\pi} = \boxed{\frac{V_m}{\pi}}$$

for full wave rectifier -

$$\frac{1}{T} \int_0^{T/2} V_m \sin \omega t dt$$

$$= 2\pi \cdot \frac{1}{T} \int_0^{T/2} V_m \sin \omega t dt$$

$$= \frac{V_m}{T} \left| -\frac{\cos \omega t}{\omega} \right|_0^{T/2}$$

$$= \frac{V_m}{T} \times \frac{2}{\omega} = \frac{V_m \times \omega \times 2}{\pi}$$

$$= \frac{2V_m}{\omega}$$

Output Half wave rectifier = V_m/ω

Output full wave rectifier = $2V_m/\omega$

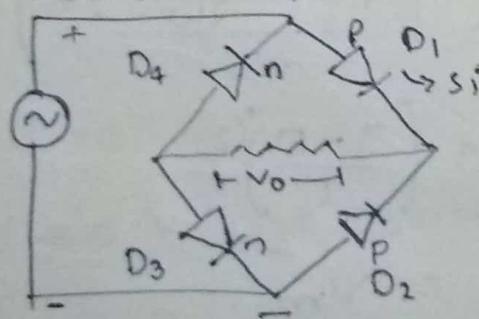
Types of full wave rectifier -

Two types of full wave rectifier

↳ Bridge Rectifier

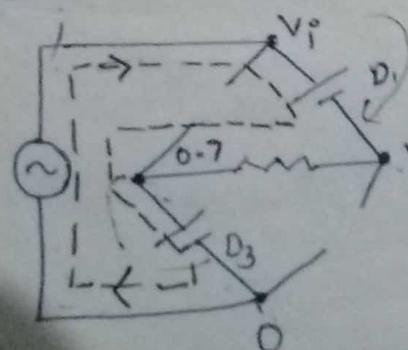
↳

① Bridge Rectifier -



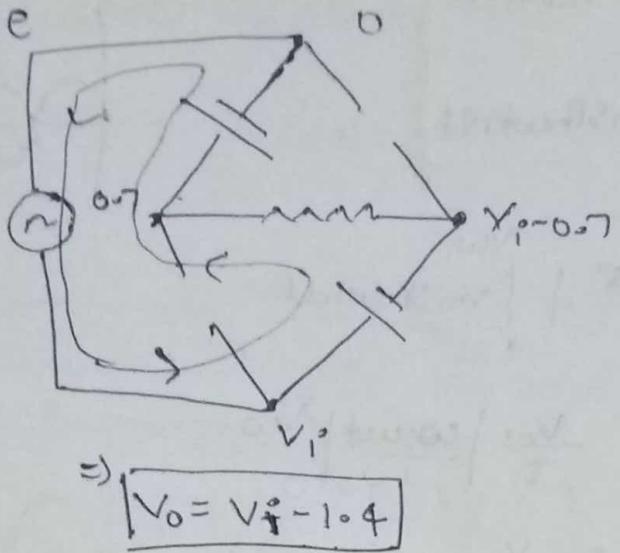
Across - Resistance

In +ive Cycle



$$\begin{aligned} V_o &= V_i - 0.7 - 0.7 \\ V_o &= V_i - 1.4 \end{aligned}$$

In -Pve Cycle



RMS value

$$\sqrt{\frac{\int_0^T (\sin \omega t)^2 dt}{T}} = \left(\frac{\int_0^T V_m^2 \sin^2 \omega t dt}{T} \right)^{1/2}$$

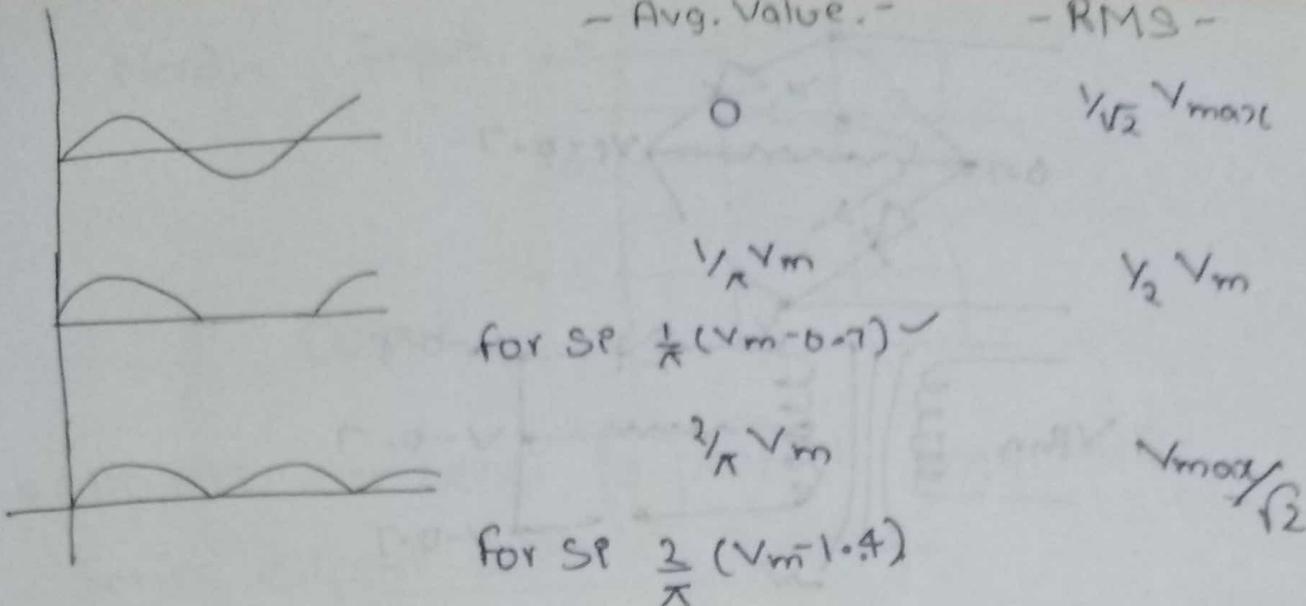
$$V_m \left(\frac{\int_0^T 1 - \cos 2\omega t dt}{T} \right)^{1/2}$$

$$V_m \left(\frac{1}{2} \int_0^T 1 - \cos 2\omega t dt \right)^{1/2}$$

$$\frac{V_m}{\sqrt{2}} \left(\frac{1 - \sin 2\omega T}{2\omega} \right)^{1/2}$$

$$\frac{V_m}{\sqrt{2}} \left(\frac{T - 0}{T} \right)^{1/2}$$

$$= \frac{V_m}{\sqrt{2}}$$



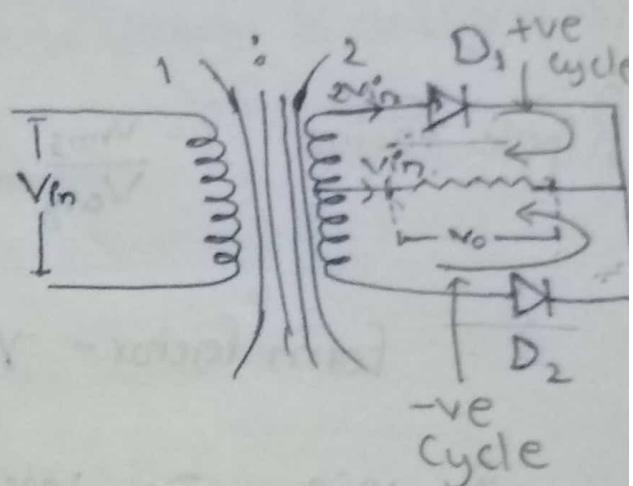
② Centre tap Rectifier -

for both +ve and -ve cycle

$$V_o = V_m - 0.7.$$

$$(V_o)_{avg} = \frac{2}{\pi} (V_m - 0.7)$$

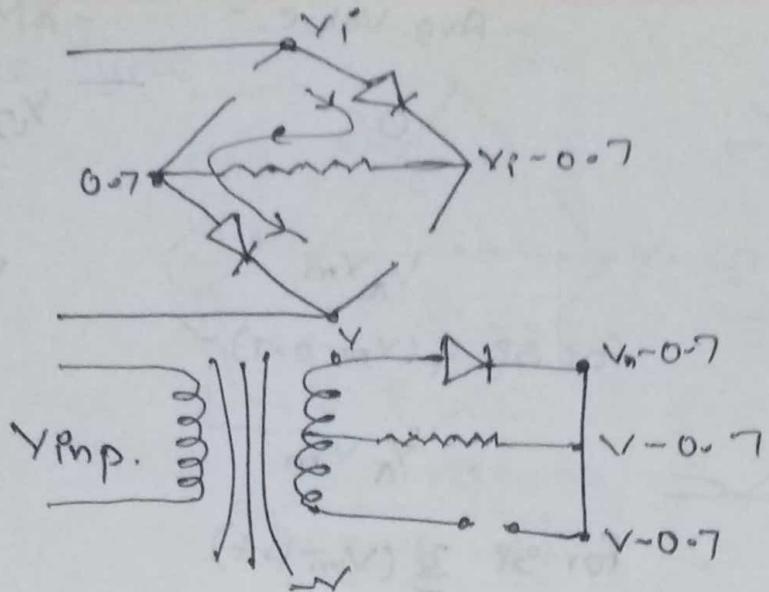
In secondary coil no. of turns increase 2 times of primary one So that V in resistor is same as V_{input}



Peak Inverse Voltage (PIV). (rating of Diode)

In reverse cycle Voltage across the terminal is V_i but if it exceeds to reverse breakdown Voltage then diode will breakdown.

"Diode के across में Reverse case में Maximum Induced Voltage ही स्थित है। इसी के Peak Voltage अपर्याप्त है।"



Ripple factor

$$r = \frac{V_{rms}}{V_{avg}}$$

Half-wave-rectifier

$$\frac{V_2}{V_A} = \frac{\pi}{2}$$

Full wave Rectifier

$$\frac{V_2}{2V_A} = \frac{\pi}{2\sqrt{2}}$$

Form factor - $\sqrt{(r)^2 - 1}$

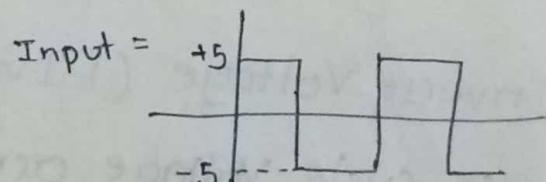
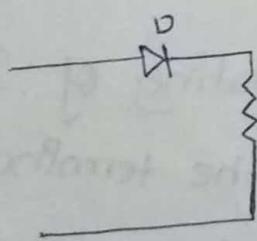
(also Ripple factor)

Rectifier with less form factor is good
or better than the high one.

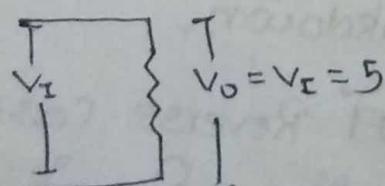
Clippers

It clips the circuit ~~at~~ input.

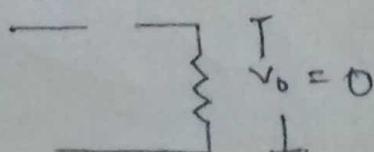
by e.g.



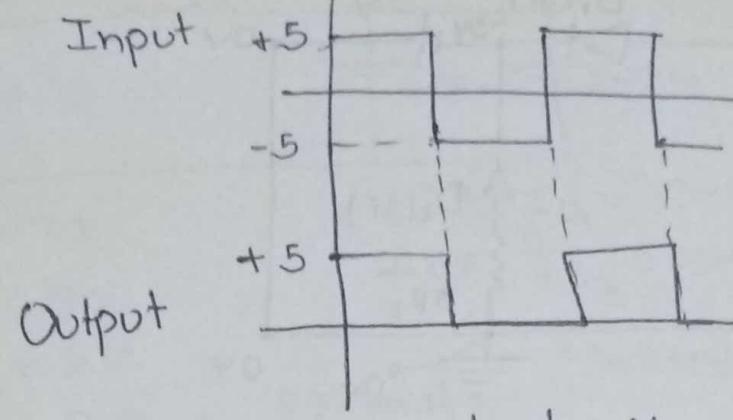
when diode - ON



When diode - OFF

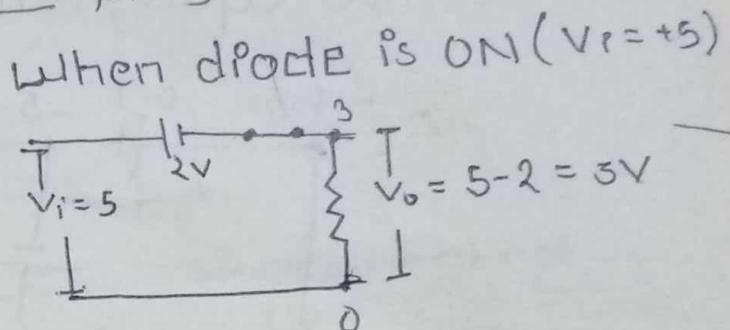
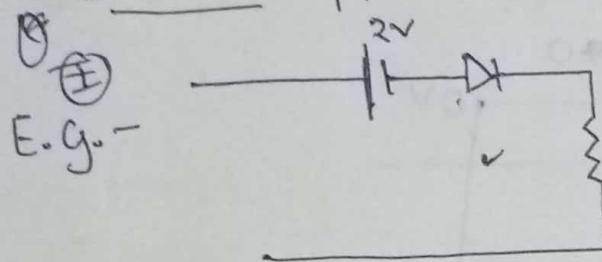


Now,

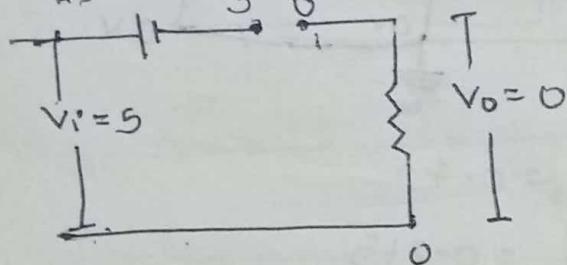


*clippers are used to protect the device.

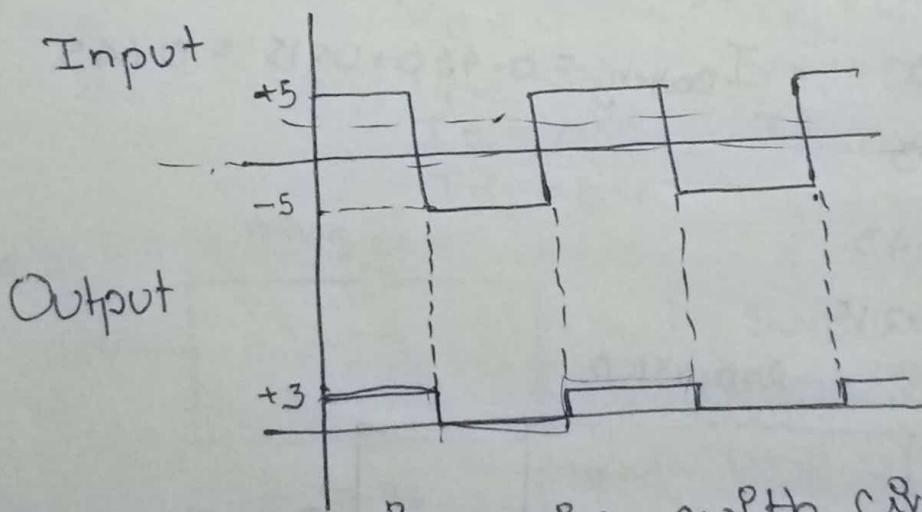
Series clipper with DC supply-



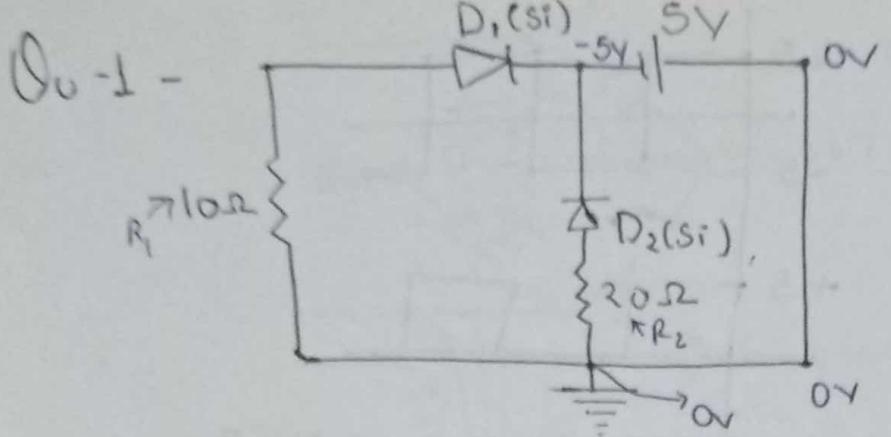
When diode is OFF



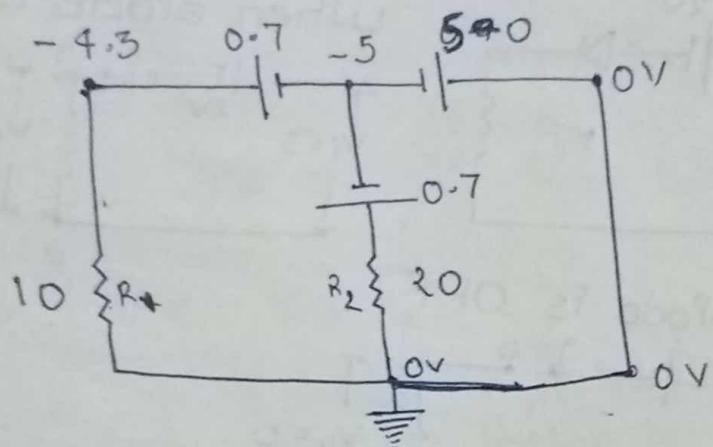
Input



→ when diode is in series with circuit it is said to be series clipper.



Both D_1 and D_2 are forward biased
so equivalent circuit is -



$$V_{D_1} = 0.7 \quad I_{D_1} = 0.43$$

$$V_{D_2} = 0.7 \quad I_{D_2} = 0.215$$

$$V_{R_1} = 4.3 \quad I_{\text{Battery}} = 0.430 + 0.215 = 0.645$$

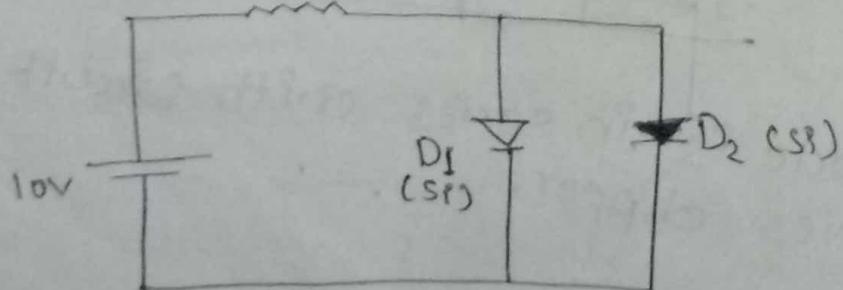
$$V_{R_2} = 4.3$$

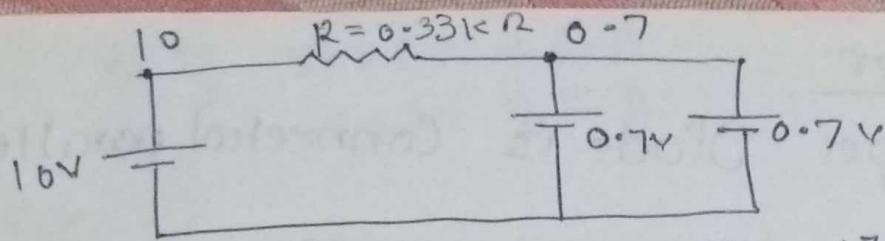
$$I_{R_1} = 0.43$$

$$I_{R_2} = 0.215$$

$$R = 0.33 \text{ k}\Omega$$

(Q_u-2 -)





$$V_{D_1} = 0.7 \text{ V}$$

$$V_{D_2} = 0.7 \text{ V}$$

$$V_R = 8.3 \text{ V}$$

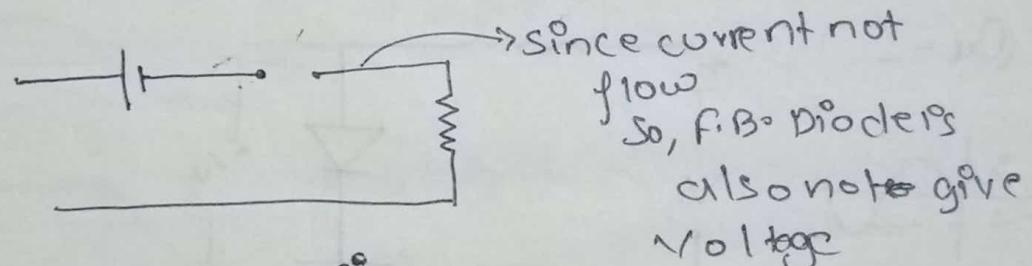
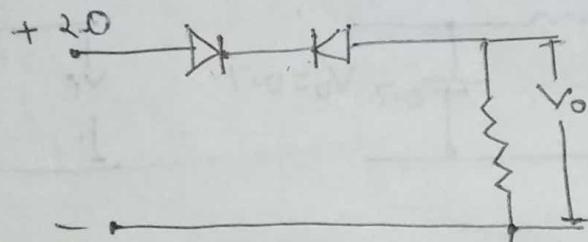
$$I_R = \frac{9.3}{1.3} = 27.9 \text{ mA}$$

$$I_{D_1} = 13.95 \text{ mA}$$

$$I_{D_2} = 13.95 \text{ mA}$$

$$I_{\text{Battery}} = 27.9 \text{ mA}$$

Ques-3 -



$$V_{D_1} = 0$$

$$V_{D_2} = 20 \text{ V}$$

$$I_{D_1} = 0 \text{ V}$$

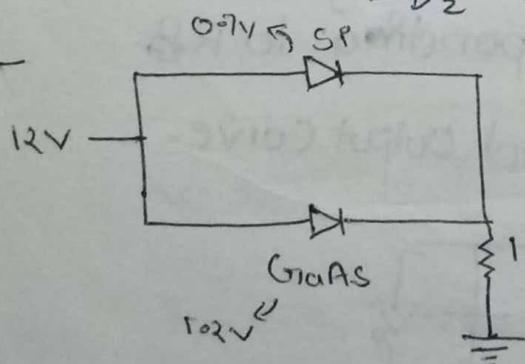
$$I_{D_2} = 0 \text{ V}$$

$$I_{R_1} = 0$$

$$V_{R_1} = 0$$

$$I_{\text{Battery}} = 0$$

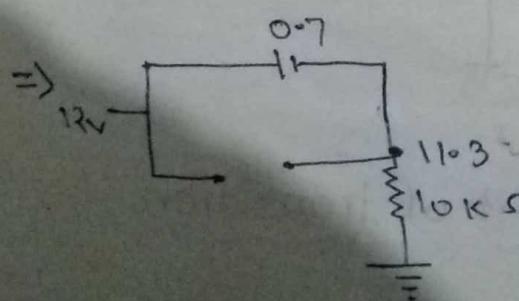
Ques 4 -



In such case, lower voltage diode is considered

and other one is reverse biased

Since it's never get sufficient Potential Difference.

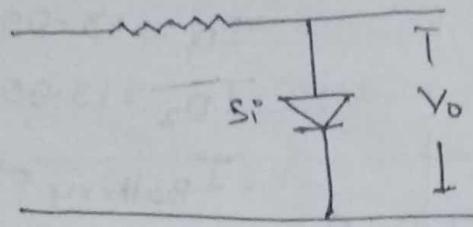
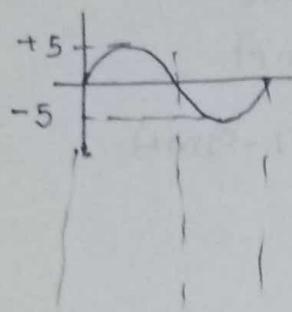


$$V_{D_1} = 0.7, V_{D_2} = 0.7, V_R = 11.3$$

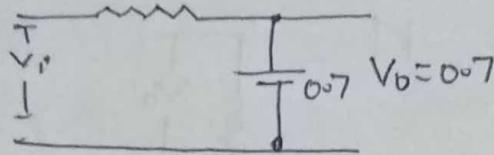
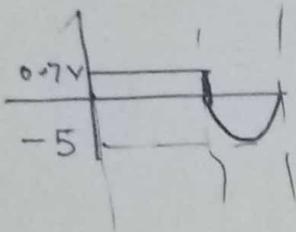
$$I_{D_2} = 0, I_{R_1} = 1.13 \text{ mA}, I_{D_1} = 1.13 \text{ mA}$$

Parallel clipper

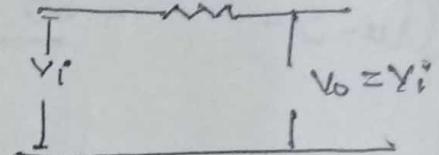
in such clipper Diode is connected parallel.



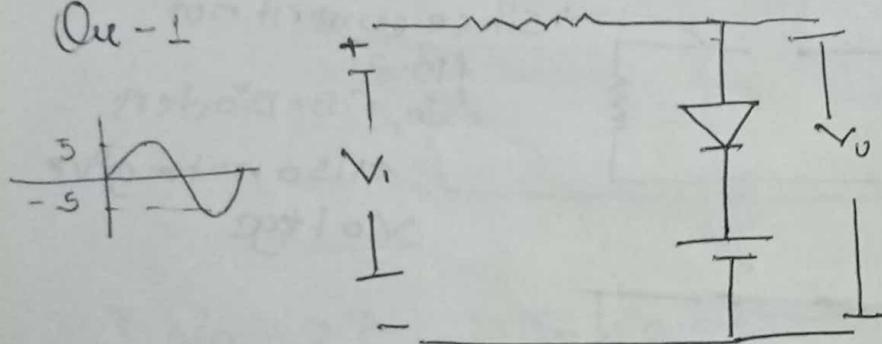
FB (in +ve cycle)



RB (in -ve cycle)



Ques - 1

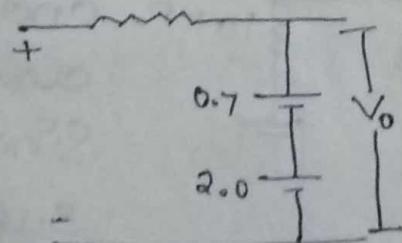


Steps ① - Find out point of transition

FB region, RB region

② - Output corresponding to FB
Output corresponding to RB

③ To plot find Output Curve.

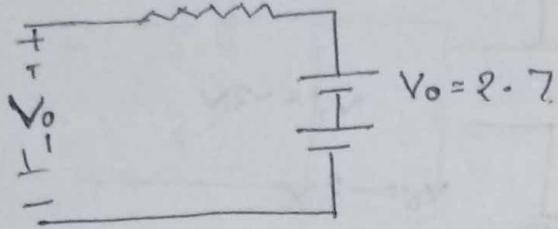


$$V_i = 2.0 - 0.7 = 1.3$$

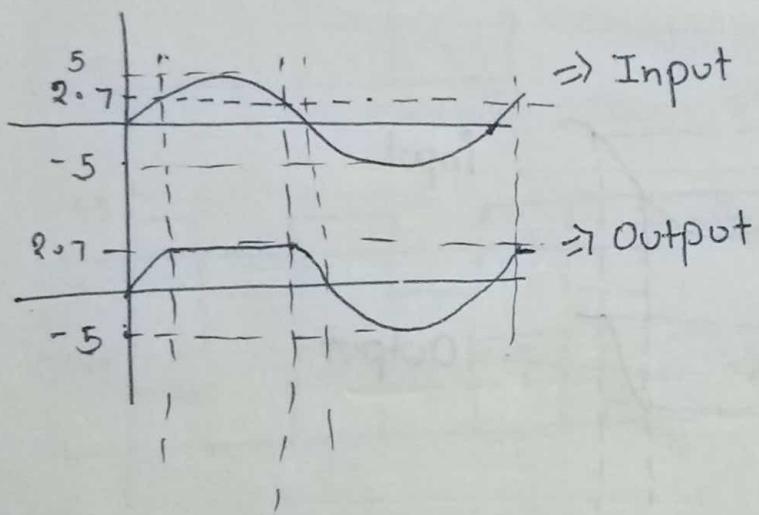
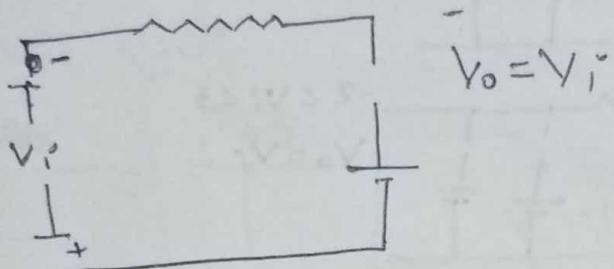
$V_i = 2.0V \Rightarrow$ point of transition

$$\Rightarrow \text{if } V_i > 2.7 \Rightarrow F \cdot B \\ V_i < 2.7 \Rightarrow R \cdot B$$

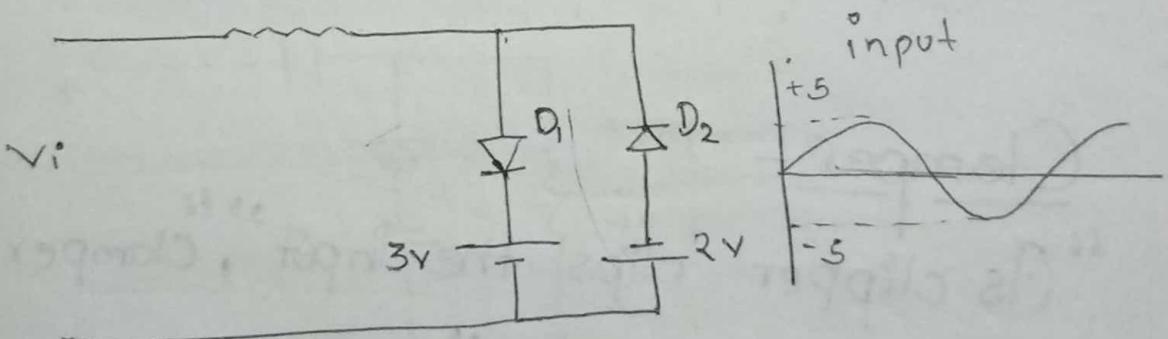
F · B



R · B



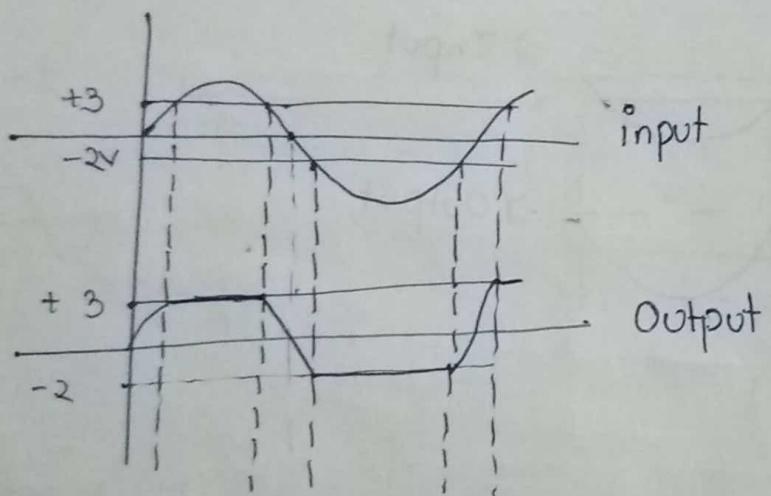
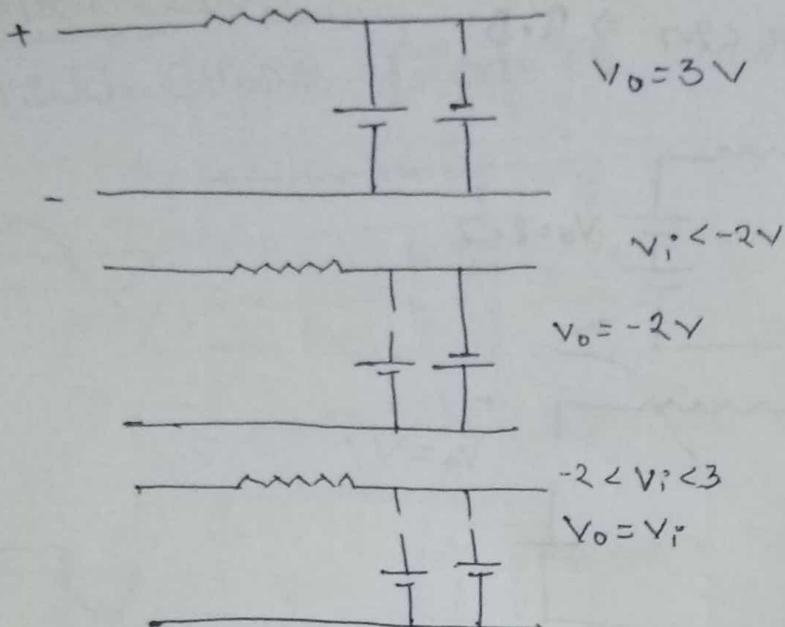
Ques 2-



$V_i > 3V \rightarrow D_1 \rightarrow \text{ON}$
 $D_2 \rightarrow \text{OFF}$

$V_i < -2V \rightarrow D_1 \rightarrow \text{OFF}$
 $D_2 \rightarrow \text{ON}$

$-2 < V_i < 3 \rightarrow D_1 \text{ & } D_2 \rightarrow \text{OFF}$

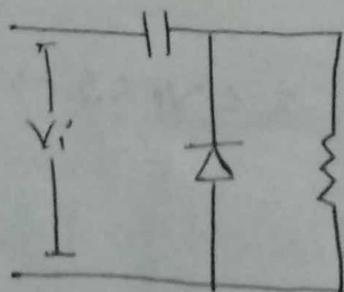
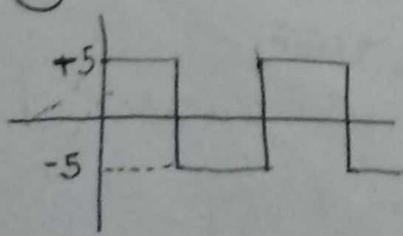


Clammer -

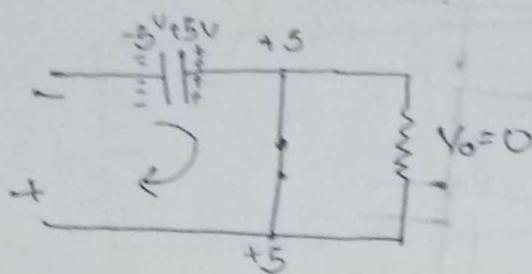
"As clipper clips the input", "Clammer Shift the input (DC level)"

Start analysis when diode is F.B.

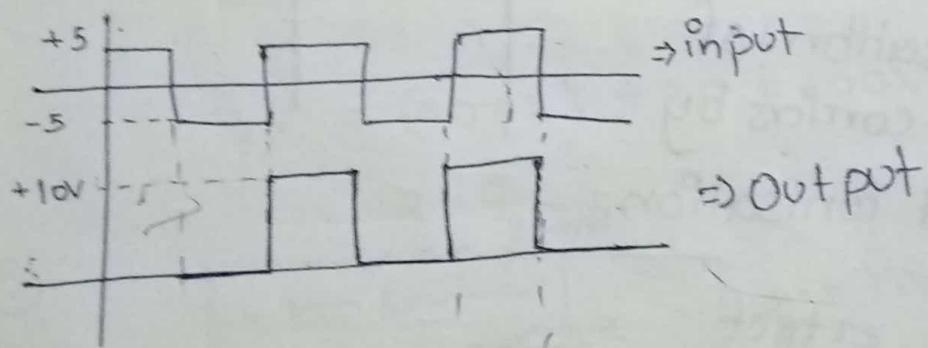
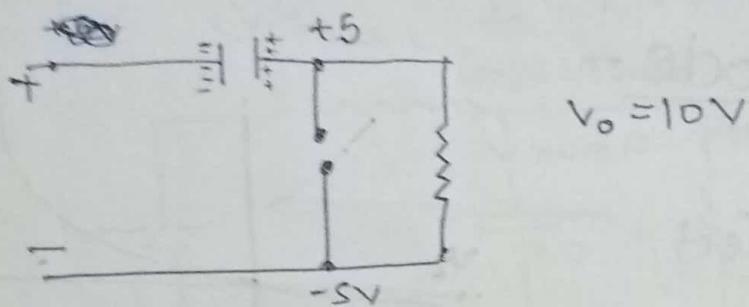
e.g. ①



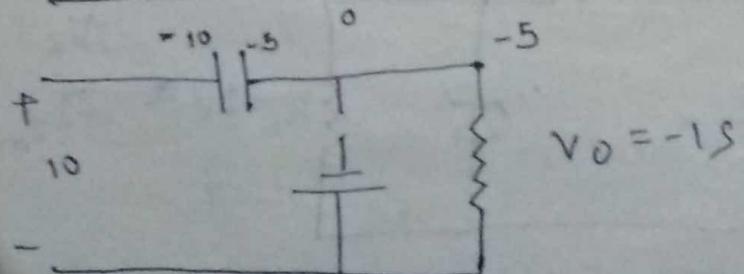
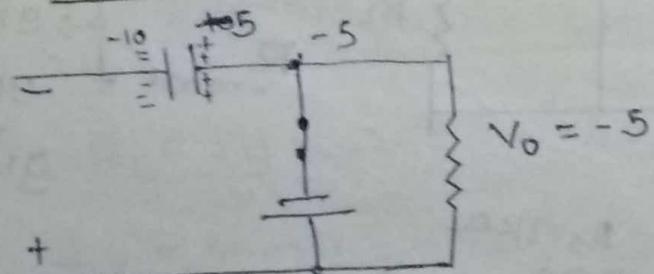
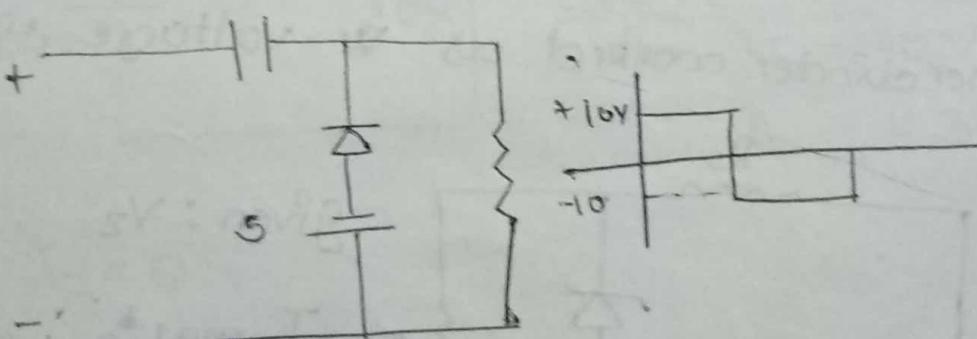
we consider +ive cycle as Diode is F.B.
(ideal)

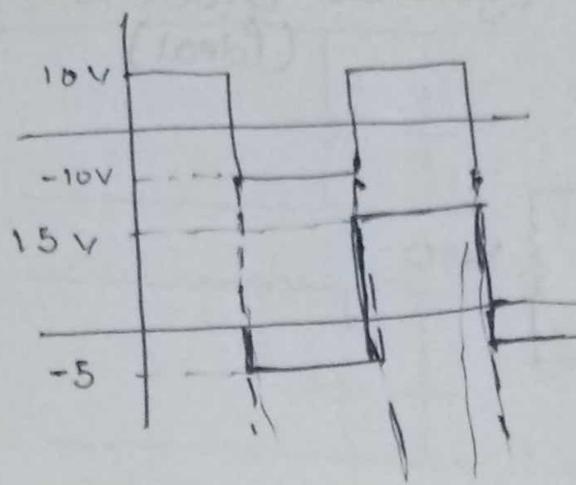


in +ive cycle



②

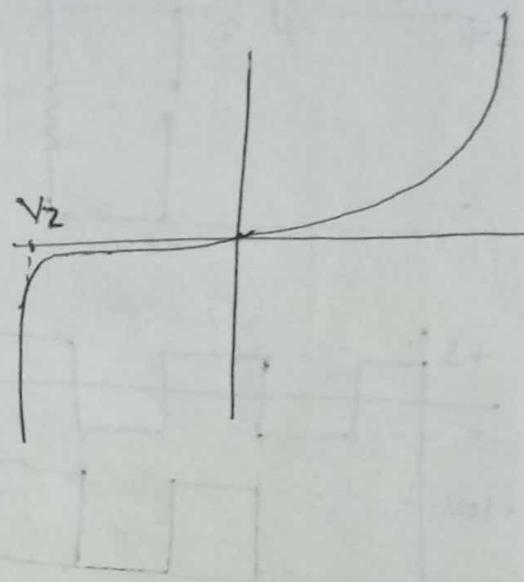




Zener diode -

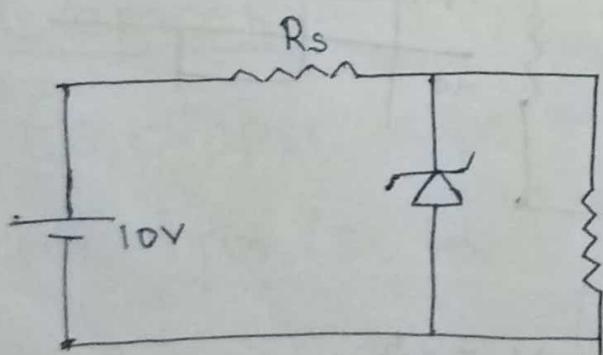
* Avelancho effect

↓
Multiplication of
charge carriers by
impact ionisation.



* Zener effect

→ Zener diode worked as a voltage regulator.

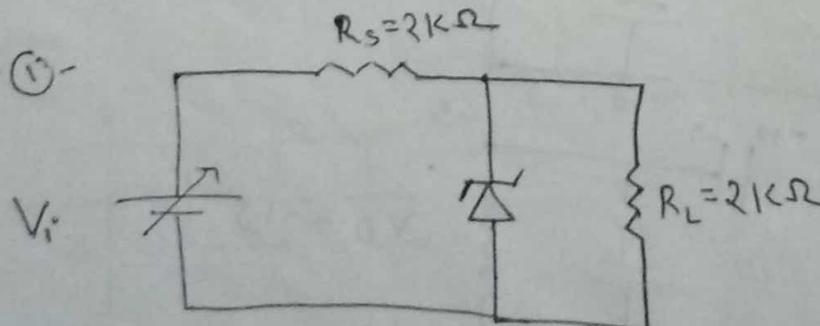


Given : V_Z

$I_{Z\max}$,
 $P_{Z\max}$

either of them
one is always
given

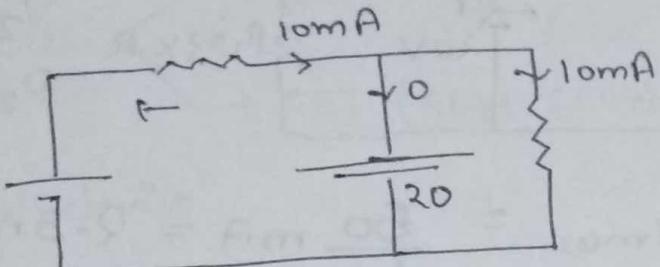
Ques-①-



$$V_Z = 20V$$

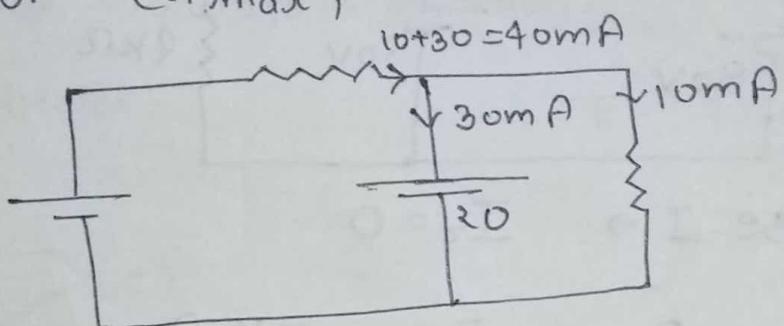
$$I_{Z\max} = 30 \text{ mA}$$

For $(V_i)_{\min}$, $I_z = 0$

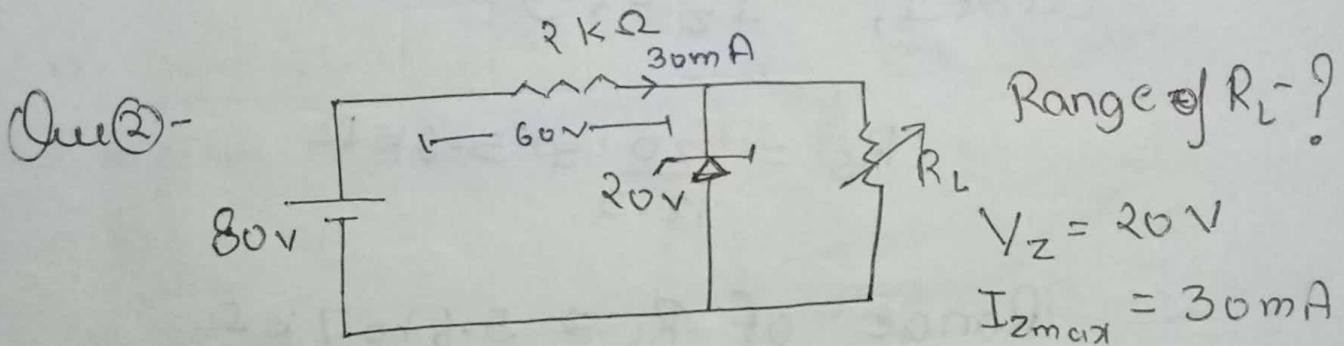


$$V_i = (10 \times 2) + 20 = 40V$$

For $(V_i)_{\max}$, $I_z = 30mA$



$$V_i = (40 \times 2) + 20 = 100V$$



Case① $I_z = 0$

$$I_{R_L} = 30mA$$

$$V = 20$$

$$R_L = \frac{20}{30} K\Omega = 0.66 K\Omega$$

Case② $I_z = 30mA$

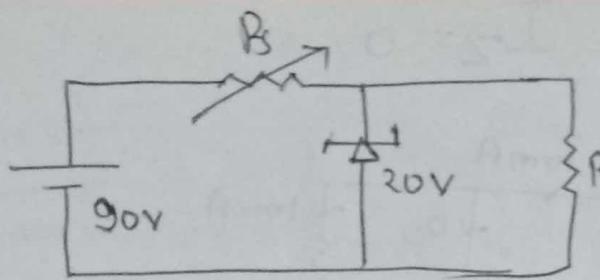
$$I_{R_L} = 0$$

$$V = 20$$

$$R_L = \frac{20}{0} \approx \infty K\Omega$$

Range in $0.66 K\Omega$ to ∞

Ques 3 →

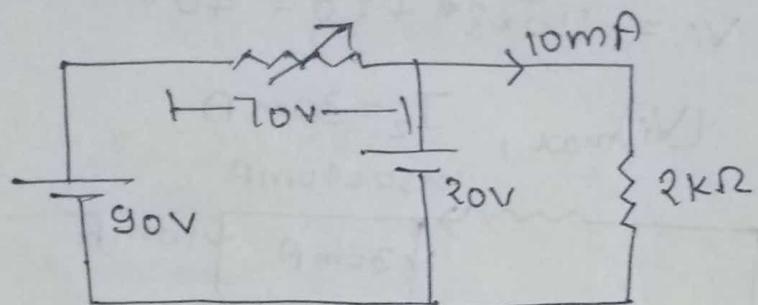


Range of R_S

$$V_Z = 20\text{V}$$

$$P_{Z_{max}} = 50\text{mW}$$

$$I_{Z_{max}} = \frac{50}{20} \text{ mA} = 2.5 \text{ mA}$$



Case I $\rightarrow I_z = 0$

$$R_S = \frac{70}{10} = 7\text{ k}\Omega$$

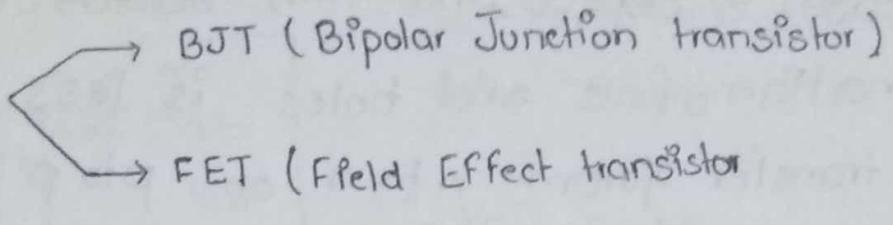
Case II, $I_z = 2.5$

$$R_S = \frac{70}{12.5} = 5.6\text{ k}\Omega$$

Range of $R_S \Rightarrow 5.6 + 0.7\text{ k}\Omega$

UNIT-2 -

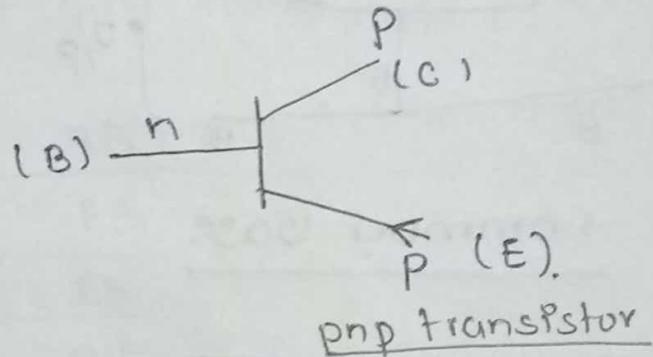
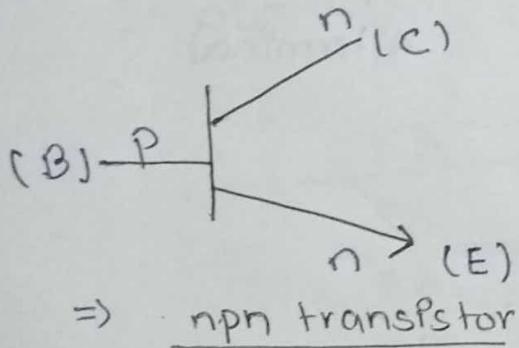
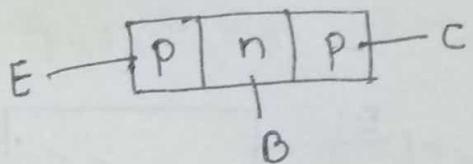
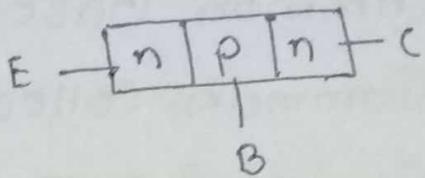
Transistors



3-Terminal device

Both
are
either
nor p

Emitter
Base → always in middle
Collector



arrow \rightarrow ~~arrow~~ \rightarrow E (emitter) ~~arrow~~ \rightarrow 1

outward = n
arrow

inward = p
arrow

Doping order Emitter \gg Collector $>$ Base

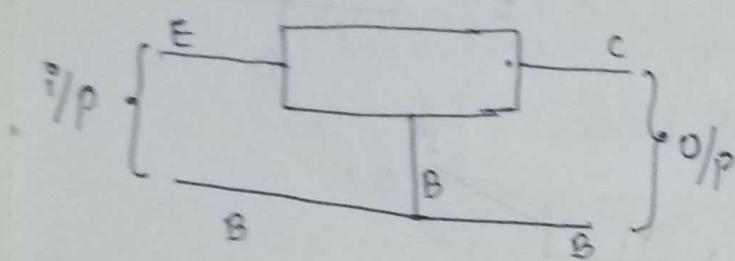
Thickness Collector $>$ Emitter $>$ Base
(thinnest)

* To minimize corner recombination in Base
thickness and doping of Base is less

* Size of collector is thick - to dissipate energy

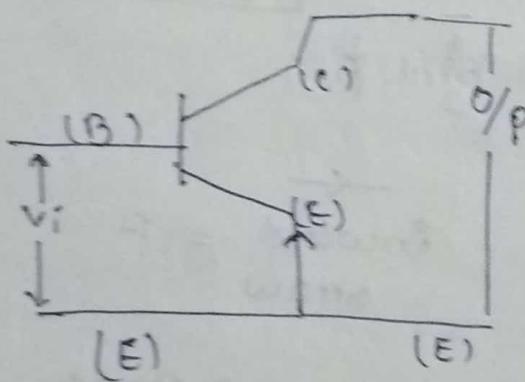
base is doped and thin because so that recombination of e^- and holes is less so that e^- transfer from n to n' or p to p' is maximum

- Common Base
- Common Collector
- Common Emitter

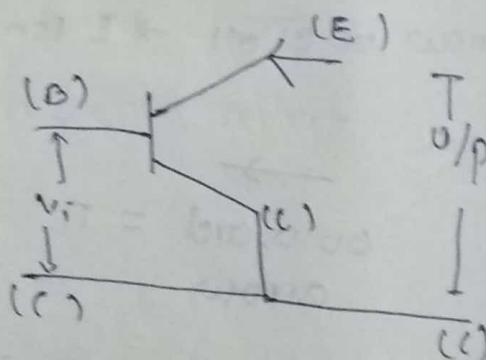


$i/p \{ \quad \} o/p$
input or
4 terminal

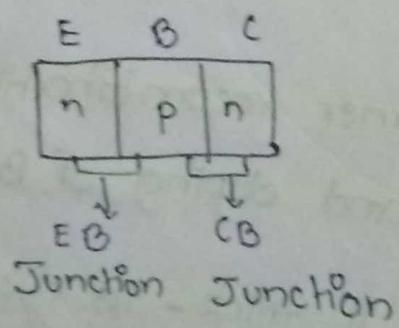
Common Base

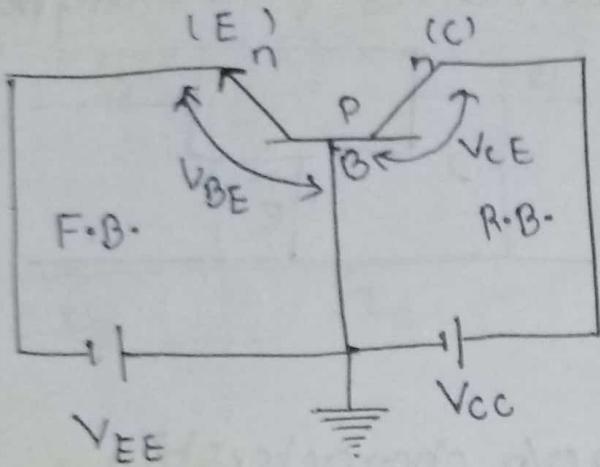


Common Emitter



Common Collector





V_{BE} = Potential difference b/w Base-Emitter

in this case

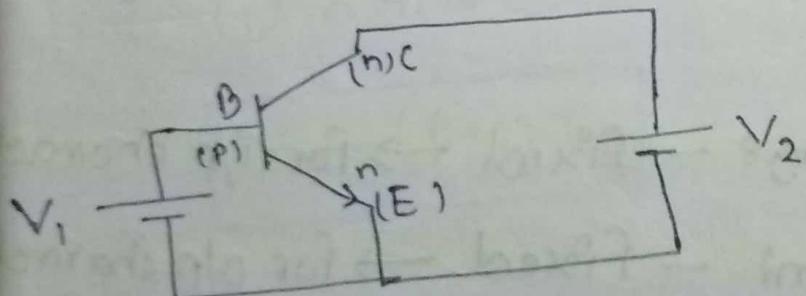
$$V_{BE} = V_{EE}$$

But when resistance is introduced in this circuit then it is not the same.

In above, ^{type of} circuit we have four possibility

	R_B	Active mode.
F_B	R_B	
F_B	F_B	
R_B	F_B	
R_B	R_B	

for F_B and R_B in Common emitter.

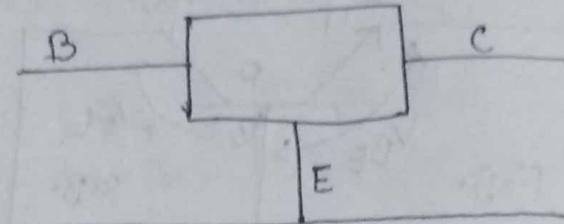


In this case for F_B and R_B

$$V_2 > V_1$$

$$\therefore V_{CC} > V_{BB}$$

* I/P and O/P characteristics (also study from Book)



i/p current = I_B
 O/p current = I_C
 I/p Voltage = V_{BE}
 O/p Voltage = V_{CE}
 i/p characteristics
 o/p characteristics

characteristics of

imp

Common Base

Common Emitter

Common Collector

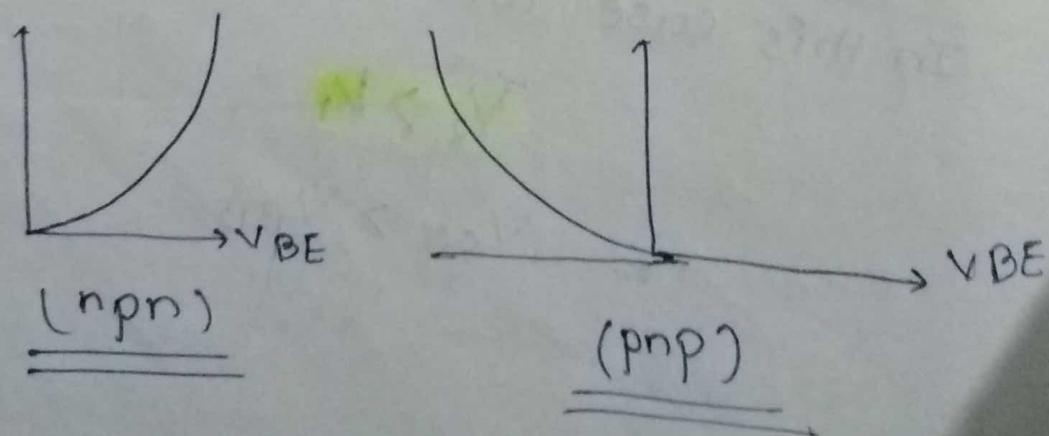
→ Study
from Book
also

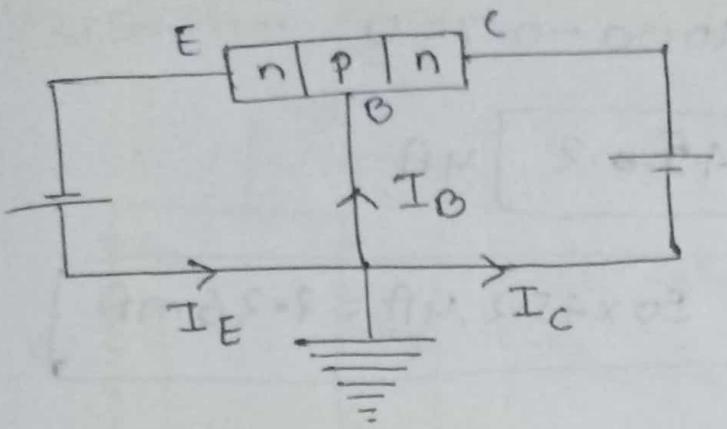
V-I characteristic graph.

* For i/p characteristics one of the o/p parameter is fixed, and vice-versa, generally -

~~for~~ O/p voltage - fixed \rightarrow for i/p characteristics

i/p Current - fixed \rightarrow for o/p characteristics





$$I_E = I_B + I_C \quad \text{--- (1)}$$

α and β

$\Rightarrow \beta = \frac{I_C}{I_B}$ current given in Common Emitter Configuration

$$\Rightarrow \beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{--- (2)}$$

$\alpha \rightarrow$ for DC analysis (in our case)

$$\Rightarrow \alpha = \frac{I_C}{I_E}, \alpha = \text{current gain of common base}$$

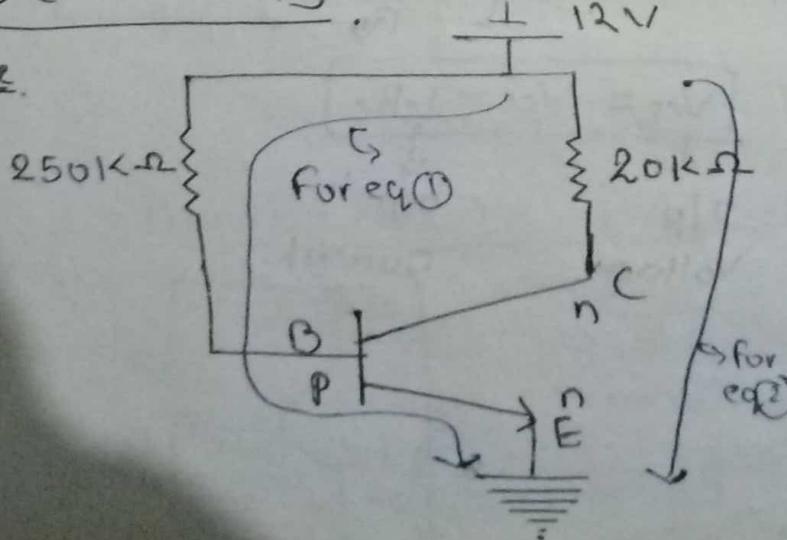
$\alpha < 1$ or $\alpha \approx 1$.

from (1) and (2)

$$I_E = (\beta + 1) I_B$$

DC Biasing

Ques.



$$\beta = 50$$

By KVL

$$12 - I_B R_B - V_{BE} = 0 \quad \text{--- (1)}$$

$$12 - I_C R_C - V_{CE} = 0 \quad \text{--- (2)}$$

$$V_{BE} = 0.7 \text{ (Silicon diode)}$$

$$I_C = \beta I_B$$

$$\Rightarrow 12 - I_p \times 280 \times 1000 - 0.7 = 0$$

$$\Rightarrow [I_p = 45.2] \text{ mA}$$

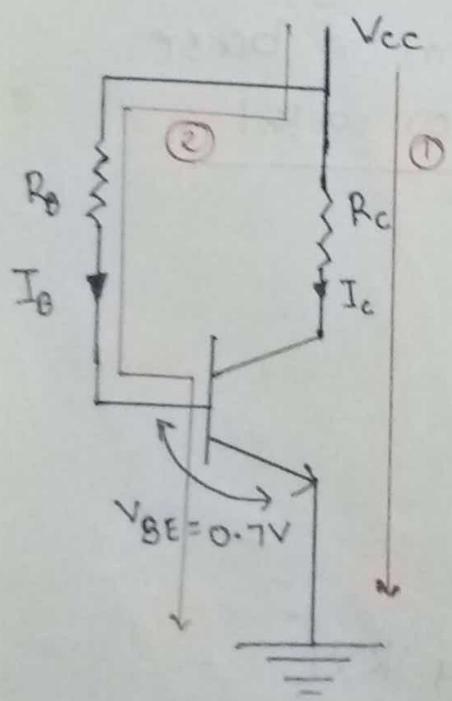
$$I_c = \beta I_p = 50 \times 45.2 \text{ mA} = 2.26 \text{ mA}$$

$$12 - 2.26 \times 10^3 \times 20 \times 10^3 - V_{CE} = 0$$

$$V_{CE} = -33.2 \text{ V}$$

DC-Biasing

1) Particular fixed biasing -



V_{cc} given

β

from ②

$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$V_{cc} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$I_C = \beta \left(\frac{V_{cc} - V_{BE}}{R_B} \right)$$

$$[V_{CE} = V_{cc} - I_C R_C]$$

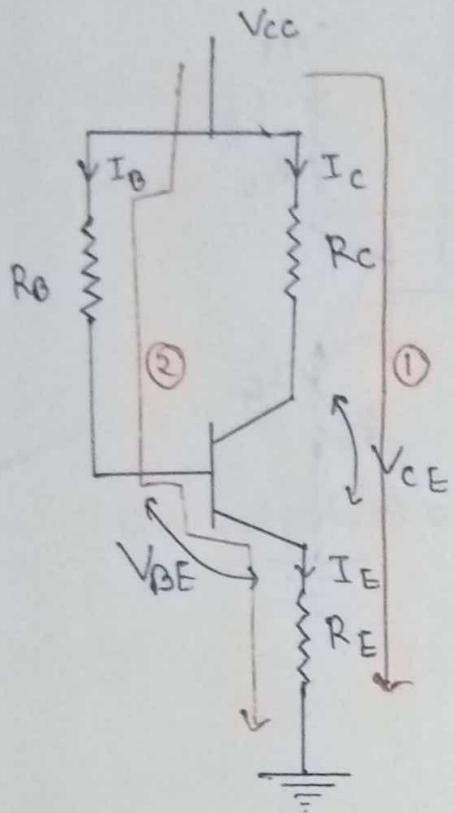
o/p

Voltage

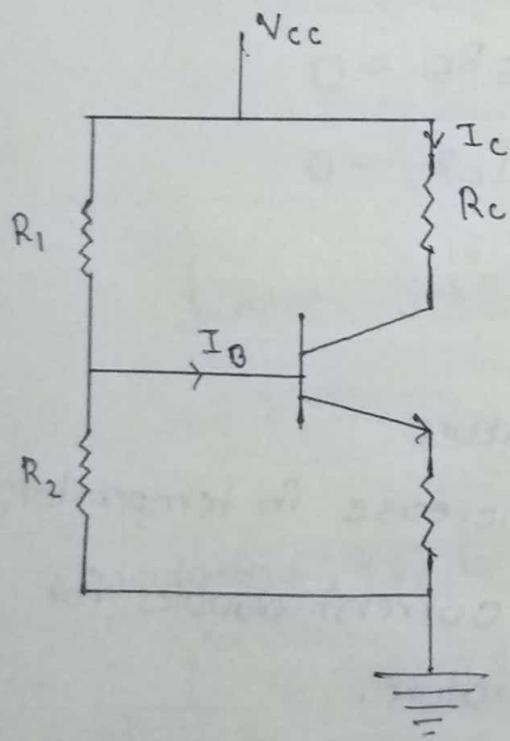
o/p

Current

2) Emitter Bias -



3) Voltage Divider Biasing

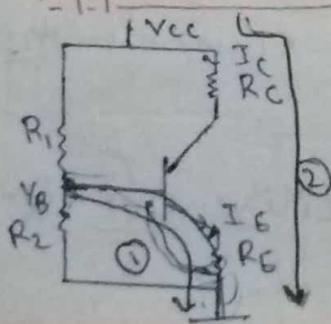


There are two methods to solve such question:-

1) Exact analysis

2) Approximate analysis

Approximate Analysis - In this we assume $I_B \rightarrow$ very-very-very small.



$$\Rightarrow V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

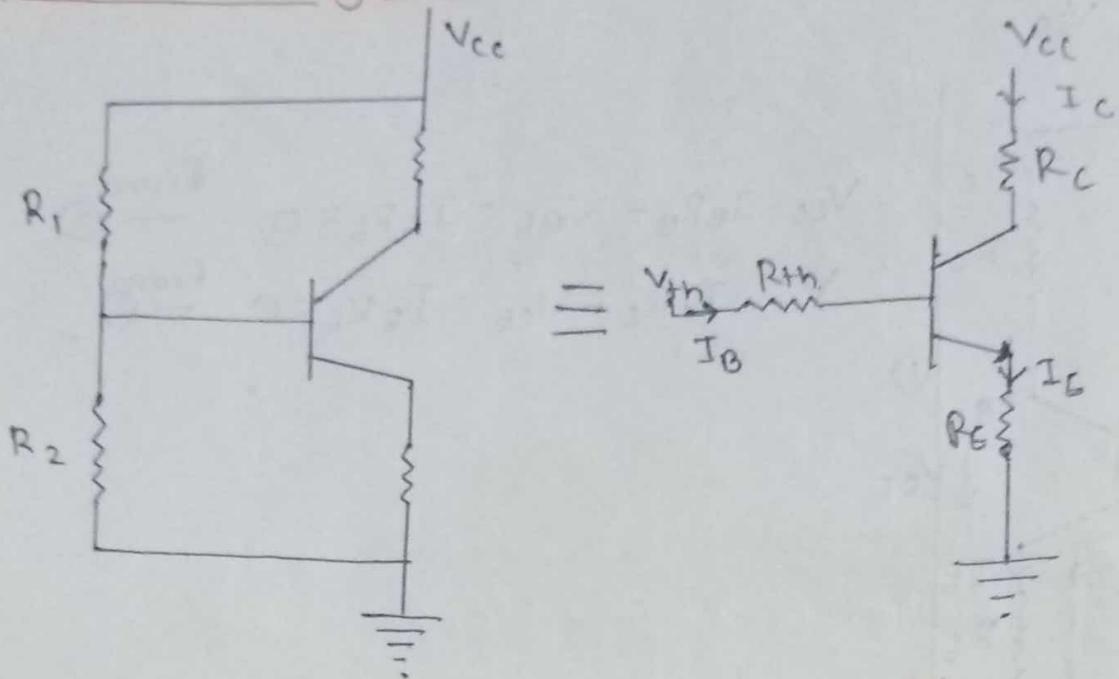
from ①

$$V_B - V_{BE} - I_E R_E = 0$$

from ②

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

Exact analysis



$$R_{th} = R_1 \parallel R_2$$

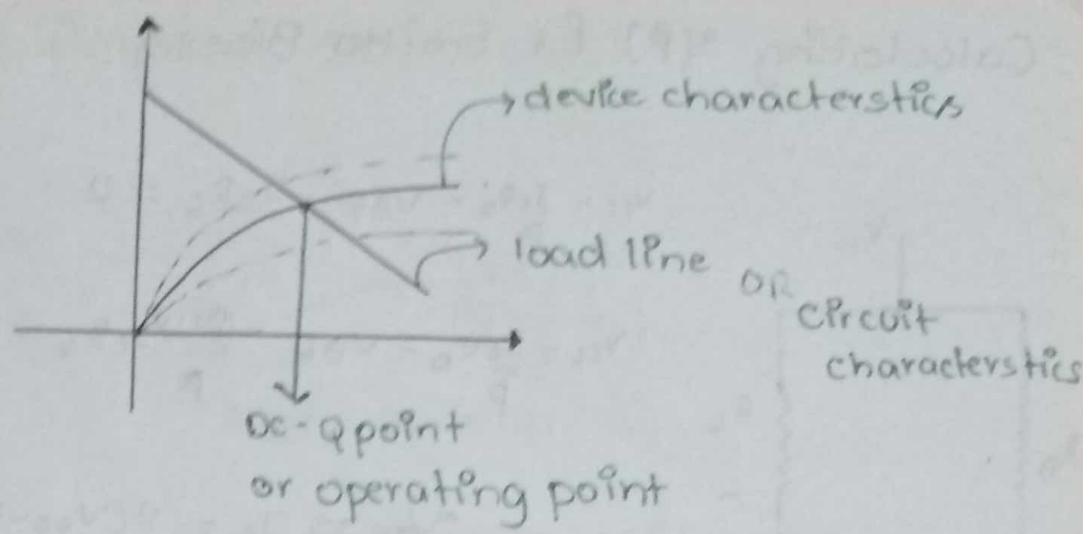
$$V_{th} = \frac{V_{cc} \times R_2}{R_1 + R_2}$$

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

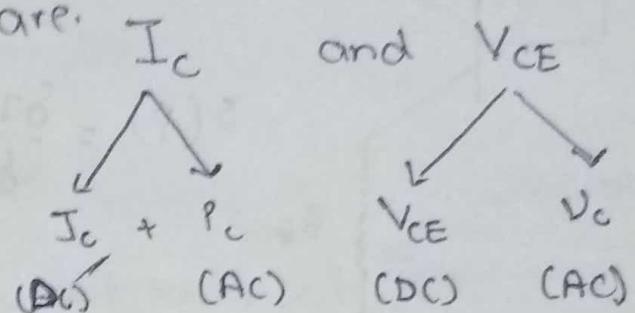
$$V_{cc} - I_C R_C - V_{ce} - I_E R_E = 0$$

Stability Analysis

- $\beta \rightarrow$ increase with temperature
 - $V_{BE} \rightarrow$ decrease $2.5 \text{ mV}/^\circ\text{C}$ increase in temperature
 - $I_{Co} \rightarrow$ Reverse saturation current doubles for 10°C rise in temperature.
- $\left\{ I_{Co0} = I_{Co} = \text{Collector Base current with open emitter} \right.$
- These situations destabilize our Q-point



Our output characteristics are:

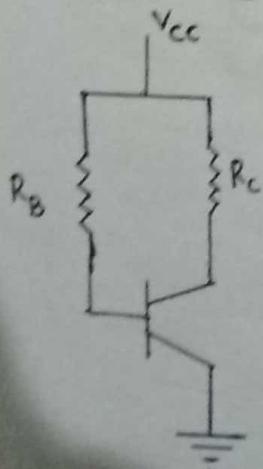


For overcoming the instability
we calculate -

$$S(I_{C_0}) = \frac{\Delta I_c}{\Delta I_{C_0}}, \quad S(V_{BE}) = \frac{\Delta I_c}{\Delta V_{BE}}, \quad S(\beta) = \frac{\Delta I_c}{\Delta \beta}$$

Where $S \rightarrow$ Stability factor for each of
the parameters affecting bias
stability

Calculating $S(\beta)$ for fixed biasing -



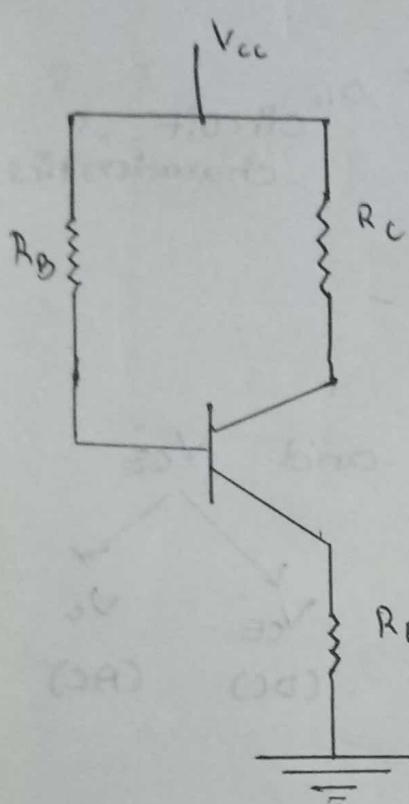
$$V_{CC} - I_B R_B - V_{BE} = 0 \Rightarrow V_{CC} - \frac{I_c}{\beta} R_B - V_{BE} = 0$$

$$V_{CC} - I_c R_C - V_{CE} = 0 \Rightarrow V_{CC} - I_c R_C - V_{CB} = 0$$

$$I_c = \frac{\beta(V_{CC} - V_{BE})}{R_B}$$

$$S(\beta) = \frac{\partial I_c}{\partial \beta} = \frac{V_{CC} - V_{BE}}{R_B}$$

Calculating $s(\beta)$ for Emitter Biasing



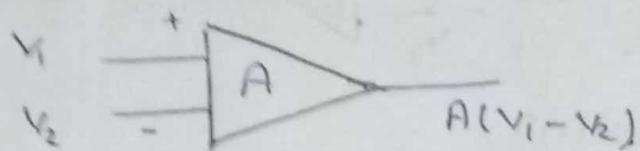
$$V_{cc} - \frac{I_c R_B}{\beta} - V_{BE} - I_R R_E = 0$$

$$V_{cc} - \frac{I_c R_B}{\beta} - V_{BE} - \frac{(\beta+1) I_c R_E}{\beta} = 0$$

$$\cancel{V_{cc}} \Rightarrow I_C = \frac{\beta(V_{cc} - V_{BE})}{\beta R_E + (R_B + R_E)}$$

$$s(\beta) = \frac{\delta I_C}{\delta \beta} = \frac{(V_{cc} - V_{BE})(R_B + R_E)}{[R_B + (1+\beta)R_E]^2}$$

Operational Amplifier (OP-AMP)



Basic - Op-Amp

It simply amplifies potential difference.

A → gain of operating Amplifier

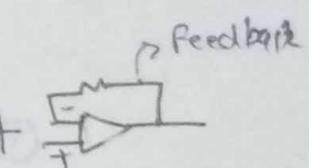
for Ideal Op-Amp, $A = \infty$

Feedback → A line from output to input

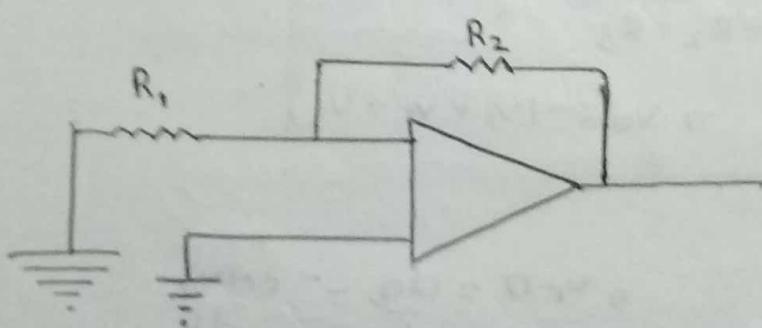
↳ feedback controls the amplification or gain.

$A = \infty \rightarrow$ for ideal

↳ But feedback \Rightarrow finite gain.



↳ line of inverter terminal
↳ connect inductor &
↳ feedback will
↳ like in this
case it is
negative feedback.

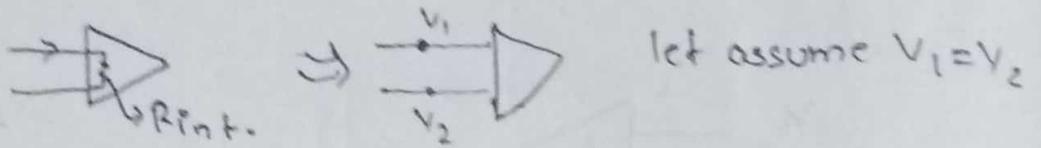


$$\Rightarrow A = \frac{R_2}{R_1}$$

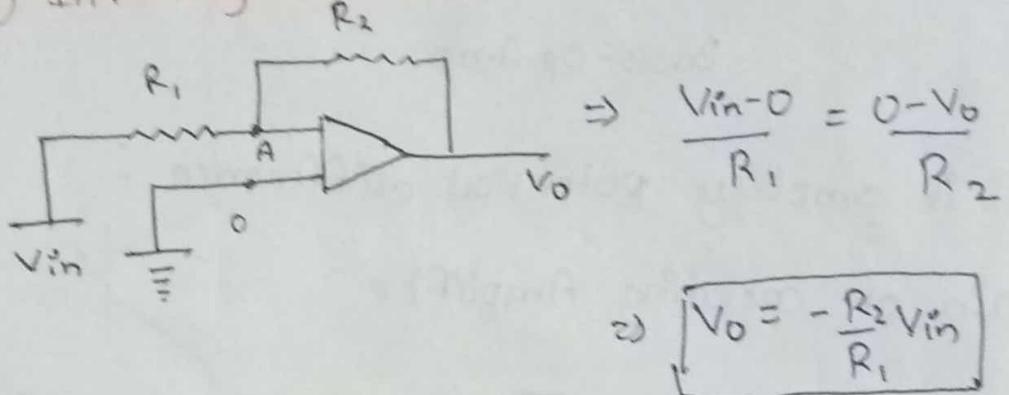
↳ this is result

\Rightarrow Gain depends on value of external resistance.

Concept of Virtual Ground -



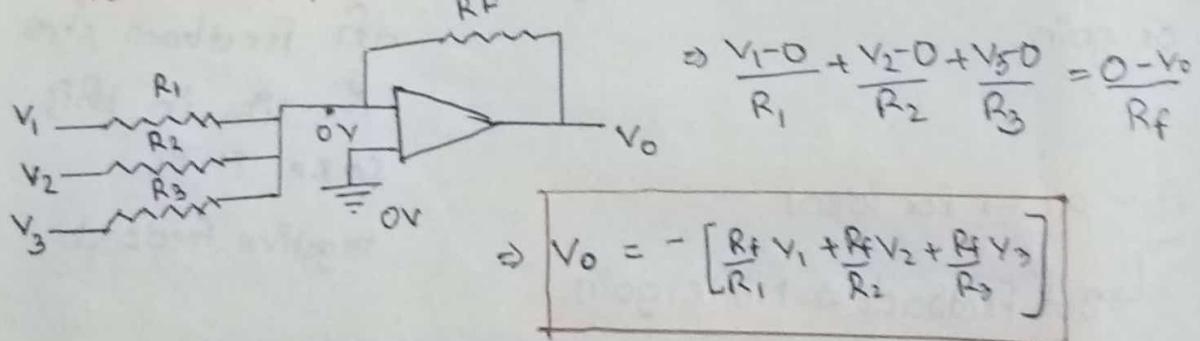
① Inverting Amplifier



$$① V_A = V_B$$

$$② I_{inside} = 0$$

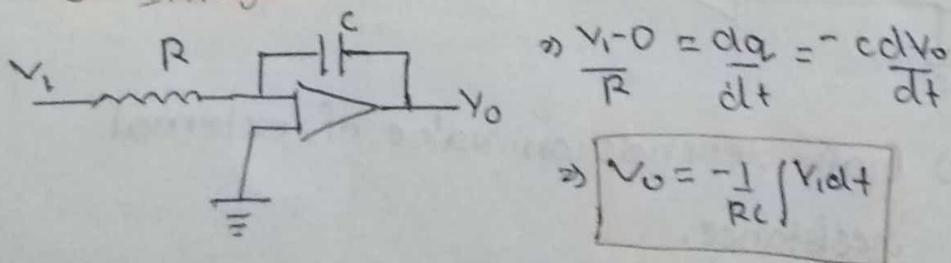
② ADDER By op-Amp -



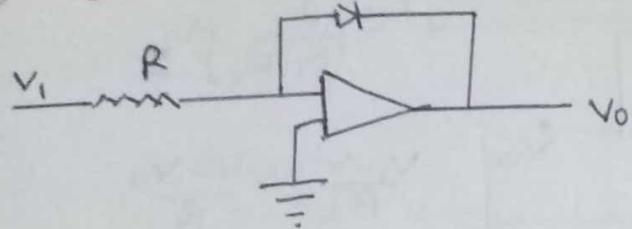
$$\text{when } R_f = R_1 = R_2 = R_3$$

$$\Rightarrow V_o = -(V_1 + V_2 + V_3)$$

③ Integrator



④ logarithmic



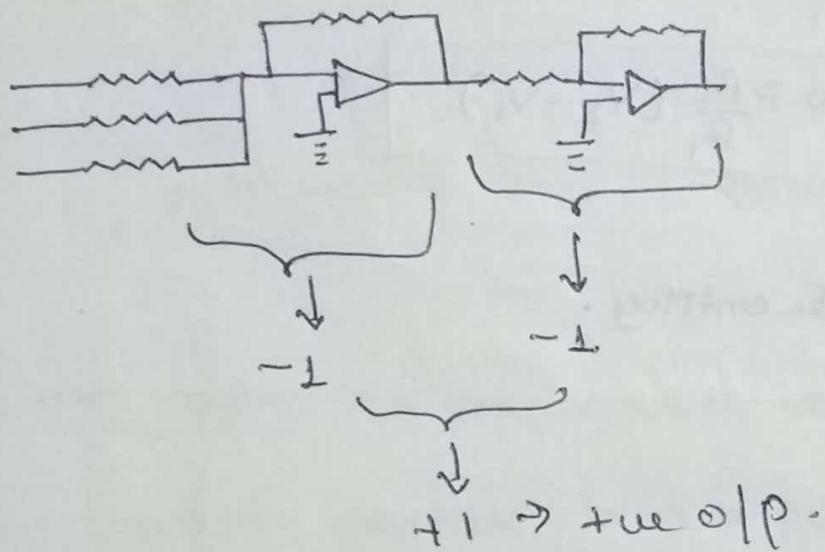
$$\frac{V_1 - 0}{R} = I_0 e^{\frac{V_0}{nV_T}}$$

$$\frac{V_1}{R} = I_0 e^{-\frac{V_0}{nV_T}}$$

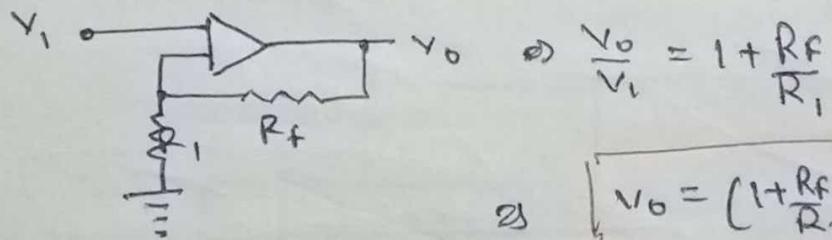
$$-\frac{V_0}{2V_T} = \ln \frac{V_1}{R I_0}$$

$$V_0 = nV_T \ln \frac{R I_0}{V_1}$$

⑤ for +ve o/p

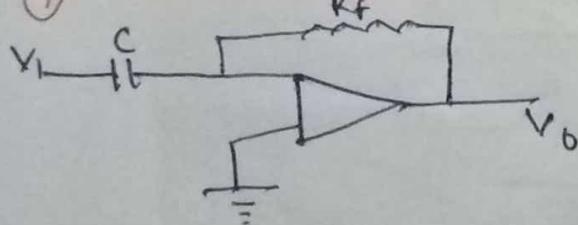


⑥ Non-Inverting



$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_1$$

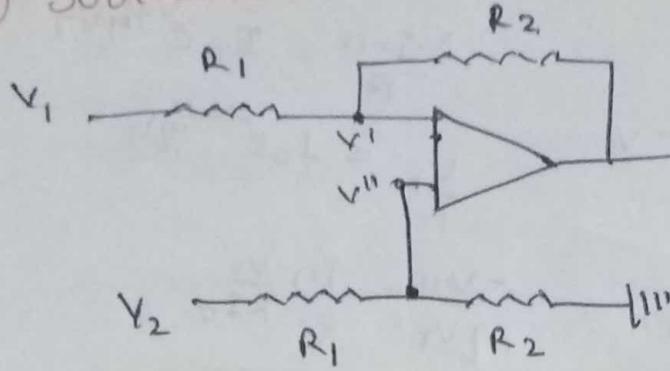
⑦ Differentiator



$$C_1 \frac{dV_1}{dt} = -\frac{V_0}{R_1}$$

$$V_0 = -R_f C_1 \frac{dV_1}{dt}$$

⑧ Subtractor



$$V' = \left(\frac{R_2}{R_1 + R_2} \right) V_2$$

$$\frac{V_1 - V'}{R_1} = \frac{V_1 - V_0}{R_2}$$

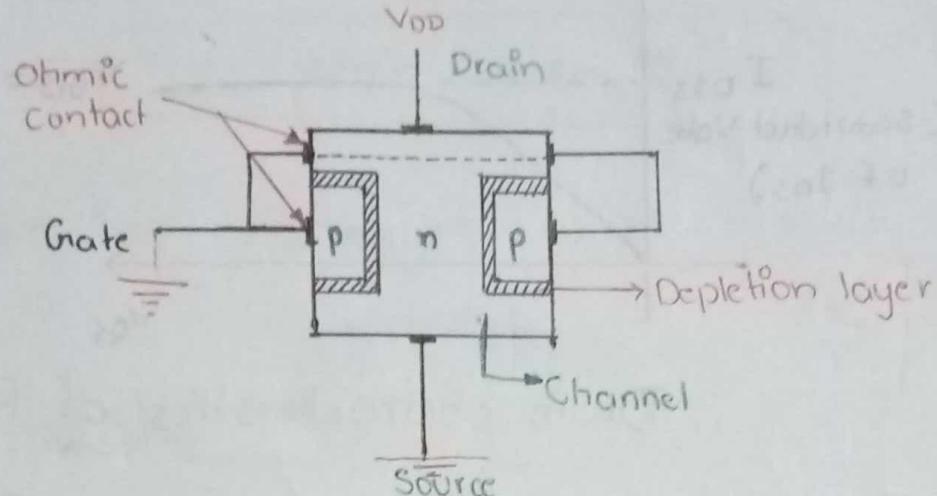
$$\therefore \frac{V_0}{R_2} = V' \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_1}{R_1}$$

$$\therefore \frac{V_0}{R_2} = \left[\frac{R_1 + R_2}{R_1 R_2} \cdot \frac{R_2}{R_1 + R_2} \right] V_2 - \frac{V_1}{R_1} = \frac{V_2 - V_1}{R_1}$$

$$\boxed{\frac{V_0}{R_2} = \frac{R_2}{R_1} (V_2 - V_1)}$$

• we can also make antilog.

Field Effect Transistor (FET)

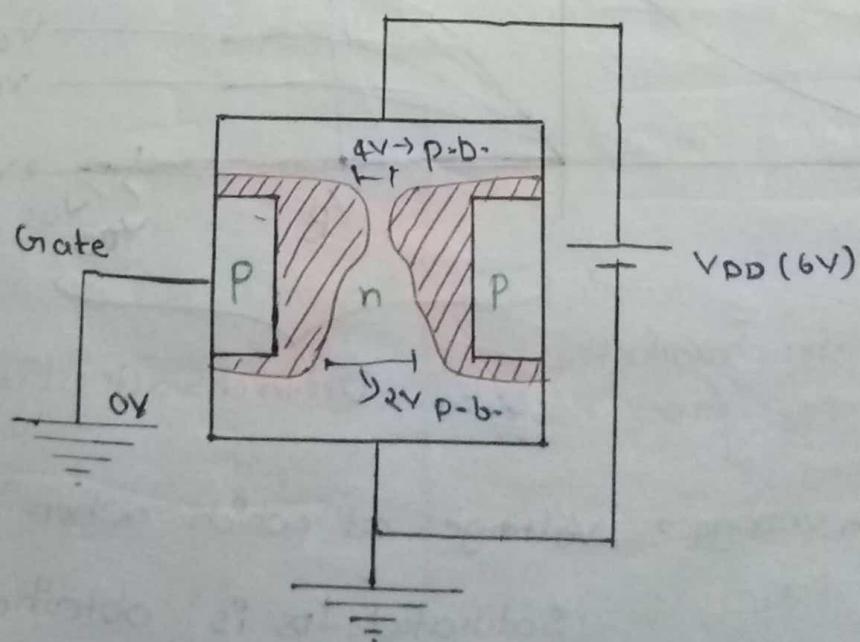


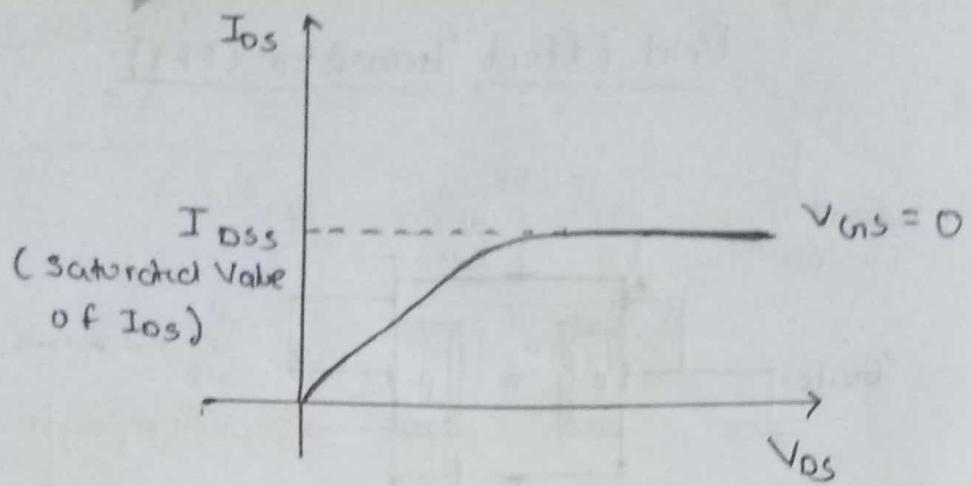
$$\cancel{V_{DS} > 0}$$

a) Let assume V_{GS} (voltage across Gate) = 0V.

As we applied V_{DD} it increases width of channel
width decrease because potential barrier in drain

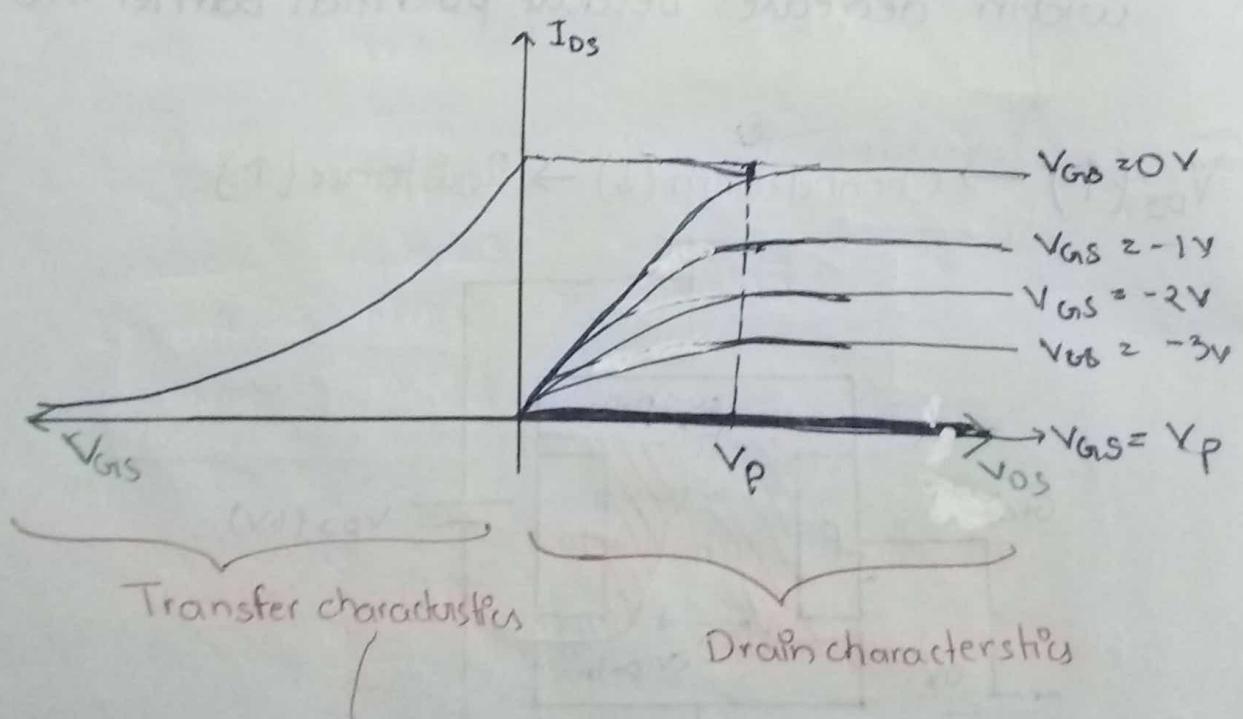
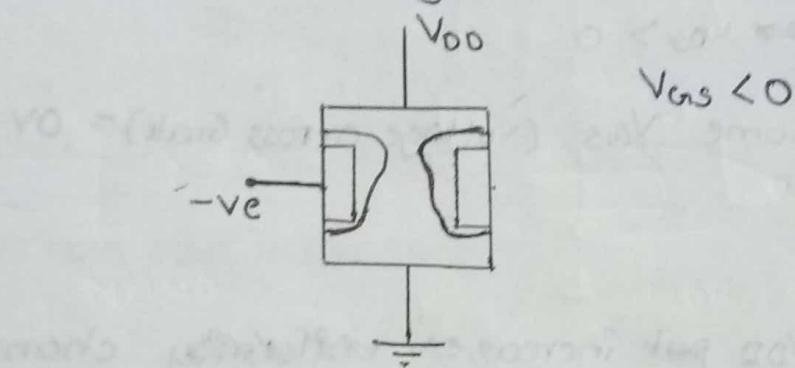
$V_{DS} (\uparrow) \rightarrow$ Channel width (\downarrow) \rightarrow Resistance (\uparrow)





Drain characteristics of FET

Now let us apply Voltage across Gate.



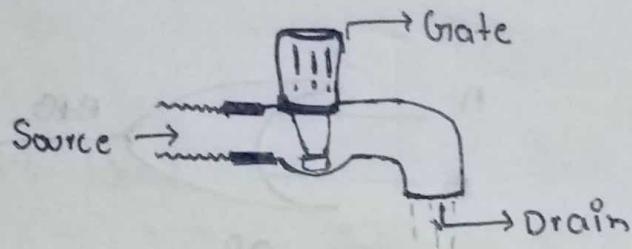
$V_p \Rightarrow$ pinch voltage \Rightarrow Voltage at which when $V_{GS} = 0$
Saturated I_{DS} is obtained

$$V_p = V_{DS\min} \text{ when } I_D = I_{DSS}$$

OR

$$V_p = V_{GS\min} \text{ when } I_D = 0$$

water tap analogy



Shockley Equation -

$$I_D = I_{DSS} \left[1 - \frac{|V_{GS}|}{|V_p|} \right]^2$$

Difference
b/w FET and BJT

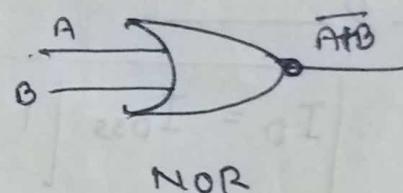
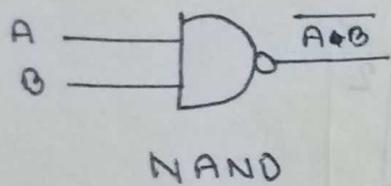
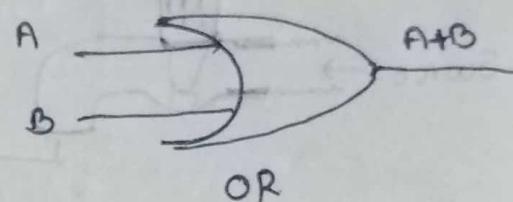
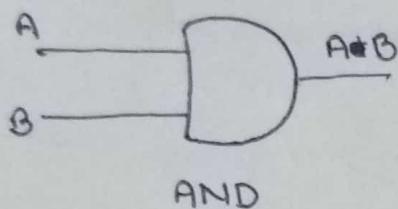
	BJT	FET
①	Bigger in size as compared to FET	Smaller in size than BJT
②	Current controlled device	Voltage controlled devices
③	Bipolar device (i.e. current carries by both holes & e-)	Unipolar device (i.e. Only one type of carrier is responsible for current carrying)
④	Thermally less stable	Thermally more stable
⑤	less input impedance compared to FET	Very high input impedance

3. Digital Electronics

① No. System

② Boolean algebra

Gates \rightarrow OR, AND, NOT



$$\text{AND} \rightarrow A \cdot B$$

$$\text{OR} \rightarrow A + B$$

$$\text{NAND} \rightarrow \overline{A \cdot B}$$

$$\text{NOR} \rightarrow \overline{A + B}$$

~~$A \oplus B \rightarrow \text{EX-OR}$~~

$$\text{EX-OR} \rightarrow A \oplus B = \overline{A}B + A\overline{B}$$

$$\text{EX-NOR} \rightarrow A \odot B$$

Truth Table

A	B	$A + B$	$A \cdot B$	$A \oplus B$	$A \odot B$
0	0	0	0	0	1
0	1	1	0	1	0
1	0	1	0	1	0
1	1	1	1	0	1

Boolean laws -

$$x + 1 = 1$$

$$x + 0 = x$$

$$0 \cdot x = 0$$

$$x \cdot 1 = x$$

$$x + \bar{x} = 1$$

$$x \cdot \bar{x} = 0$$

$$a+b = b+a$$

$$a+(b+c) = (a+b)+c$$

$$a(b+c) = ab+bc$$

$$a + (b \cdot c) = (a+b)(a+c)$$

\hookrightarrow distribution of addn over multiplication.

$$\text{Demorgan's law} \rightarrow \overline{A+B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

e.g. - ① $A + \bar{A}B$

$$A + \bar{A}B = (A + \bar{A})(A + B) = A + B$$

② $AB + \bar{A}C + \bar{B}C$

$$AB + (\bar{A} + \bar{B})C \Rightarrow (\underline{AB} + \underline{\bar{A} + \bar{B}}) \cdot (\underline{AB + C})$$

$$(\bar{B} + A + \bar{A}) \cdot (AB + C)$$

$$(\bar{B} + 1) \cdot (AB + C)$$

$$= (AB + C)$$

Redundancy theorem -

$$AB + BC + \bar{C}A$$

$$AB(C + \bar{C}) + BC + \bar{C}A$$

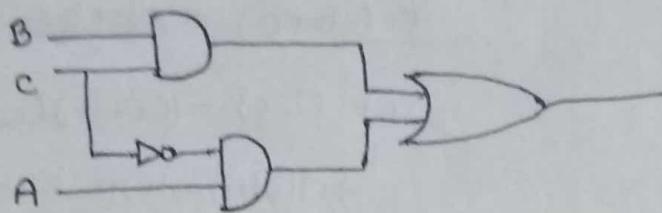
$$\underline{ABC} + \underline{AB\bar{C}} + \underline{BC} + \underline{\bar{C}A}$$

$$\boxed{\underline{BC} + \underline{\bar{C}A}}$$

$$\boxed{AB + BC + \bar{C}A = BC + \bar{C}A}$$

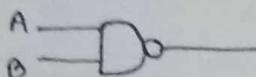
Implementation of Boolean by boolean gates -

$$① BC + \bar{C}A$$



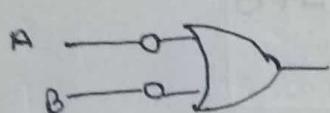
Now using universal gate - (i.e. 1NAND and NOR gate)

NAND



$$= \bar{AB}$$

$$= \bar{A} + \bar{B}$$

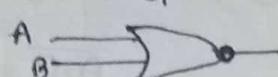


↳ this is equivalent
to NAND gate

and known as.

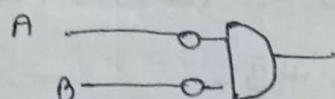
Bubbled OR gate

NOR



$$= \overline{A+B}$$

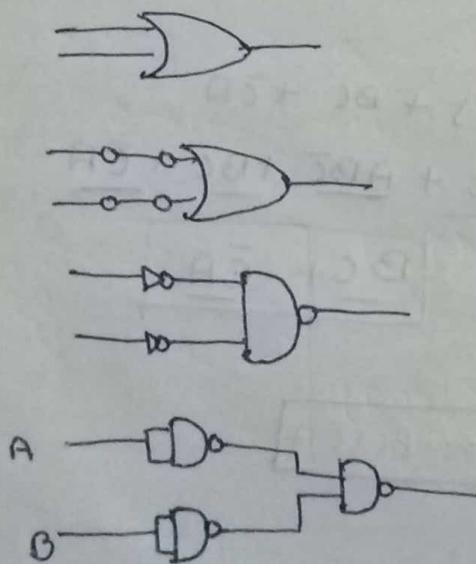
$$= \bar{A} \cdot \bar{B}$$



↳ this is equivalent
to NOR gate and
known as -

Bubbled AND gate

e.g. Solving $A+B$ by universal gate - NAND



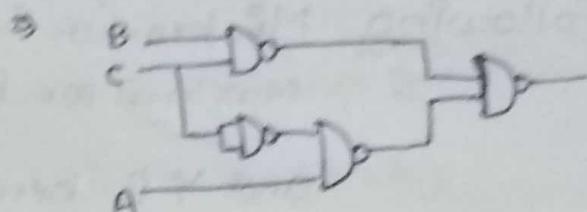
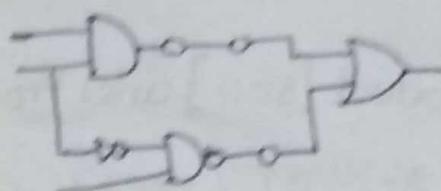
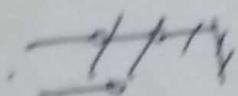
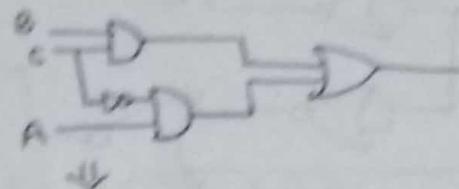
$$\# A \longrightarrow \overline{\overline{A}} = A$$

Similarly

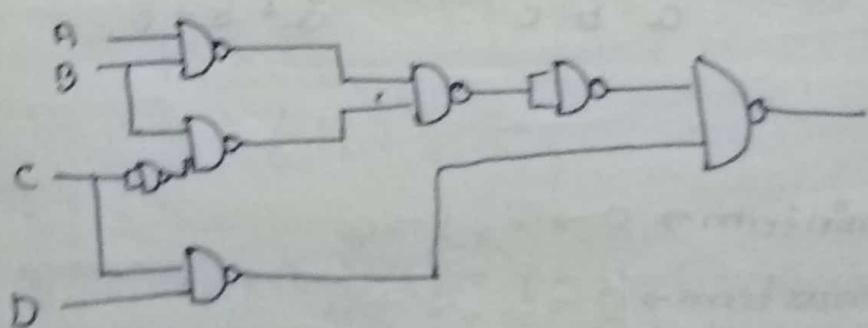
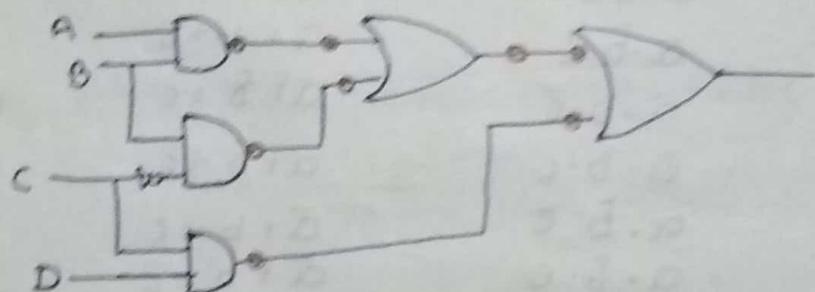
$$A \longrightarrow \overline{\overline{A+A}} = \overline{A} = A$$

② Solving $B+C+\bar{C}A$ by NAND gate.

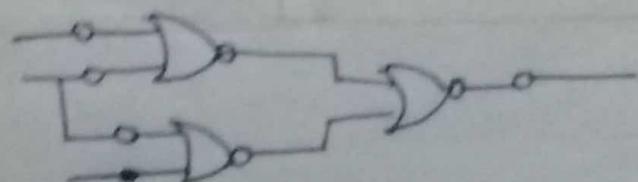
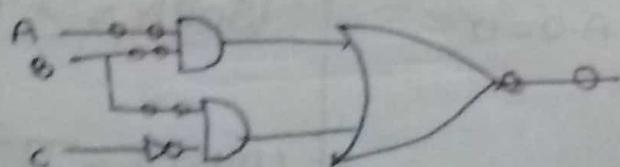
$$B+C+\bar{C}A \Rightarrow$$

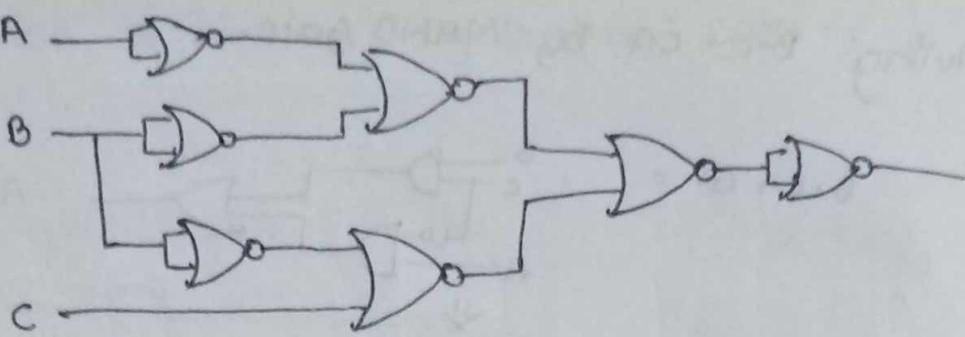


③ $AB + B\bar{C} + CD$ by NAND



④ $B\bar{C}+AB$ by NOR





Sum of Product [SOP] and Product of Sum [POS]

Consider following Minterm for SOP.

Maxterm for POS

and Y is here for e.g..

A B C	Minterm	Maxterm	Y
0. 0 0 0	$\bar{a} \cdot \bar{b} \cdot \bar{c}$	$a + b + c$	0
1. 0 0 1	$\bar{a} \cdot \bar{b} \cdot c$	$a + b + \bar{c}$	0
2. 0 1 0	$\bar{a} \cdot b \cdot \bar{c}$	$a + \bar{b} + c$	1
3. 0 1 1	$\bar{a} \cdot b \cdot c$	$a + \bar{b} + \bar{c}$	1
4. 1 0 0	$a \cdot \bar{b} \cdot \bar{c}$	$\bar{a} + b + c$	0
5. 1 0 1	$a \cdot \bar{b} \cdot c$	$\bar{a} + b + \bar{c}$	1
6. 1 1 0	$a \cdot b \cdot \bar{c}$	$\bar{a} + \bar{b} + c$	0
7. 1 1 1	$a \cdot b \cdot c$	$\bar{a} + \bar{b} + \bar{c}$	1

* In minterm $\rightarrow 0 \rightarrow \bar{a}, 1 \rightarrow a$

In maxterm $\rightarrow 0 \rightarrow a, 1 \rightarrow \bar{a}$

Duality - $A+1=1, A \cdot 0=0$

$$\begin{aligned} 1 &\rightarrow 0 \\ 0 &\rightarrow 1 \\ + &\rightarrow : \\ : &\rightarrow + \end{aligned}$$

$$(SOP)Y = \sum (\text{of minterm having } Y \text{ value } 1)$$

$$(POS)Y = \prod (\text{of maxterm having } Y \text{ value } 0)$$

for above, table,

$$(SOP) \Rightarrow Y = \sum (2, 3, 5, 7)$$

$$Y = \bar{a}b\bar{c} + \bar{a}bc + a\bar{b}c + abc$$

and
(POS) $Y = \sum (0, 1, 4, 6)$

$$Y = (a+b+c) \cdot (a+b+\bar{c}) \cdot (\bar{a}+b+c) \cdot (\bar{a}+\bar{b}+c)$$

Ques - $A+BC$, write SOP and POS.

$$A(B+\bar{B})(C+\bar{C}) + BC(A+\bar{A})$$

$$(AB+A\bar{B})(C+\bar{C}) + BC(EA + \bar{A}BC)$$

$$\underline{ABC} + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \underline{ABC} + \bar{ABC}$$

$$\Rightarrow \underbrace{ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}}_{SOP} + \bar{ABC}$$

$$= \sum (7, 6, 5, 4, 3).$$

If POS is

$$= \overline{TT}(6, 1, 2).$$

SOP to POS

$$\hookrightarrow (a+b+c) \cdot (a+b+\bar{c}) \cdot (a+\bar{b}+c)$$

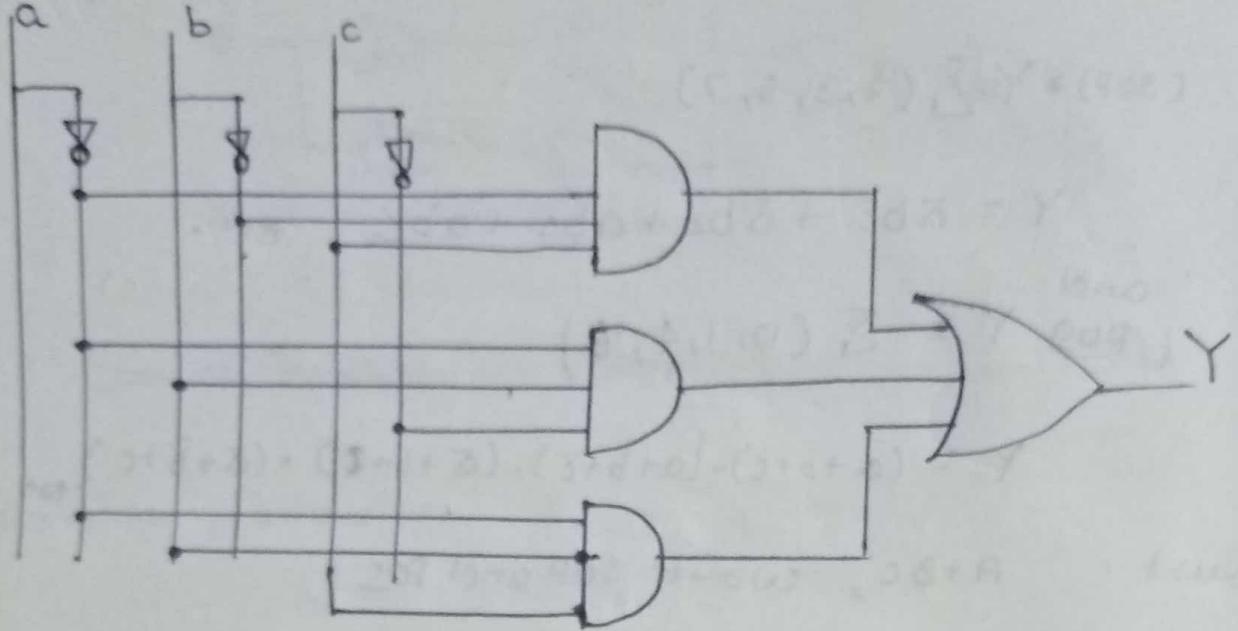
Question - Boolean expression \rightarrow SOP $\rightarrow \sum (1, 2, 3)$

$$\Rightarrow \bar{a}\bar{b}c + \bar{a} \cdot b \cdot \bar{c} + \bar{a} \cdot b \cdot c$$

$$\Rightarrow POS - \overline{TT}(0, 4, 5, 6, 7)$$

$$\Rightarrow (a+b+1) \cdot (\bar{a}+\bar{b}+\bar{c}) \cdot (\bar{a}+b+\bar{c}) \cdot (\bar{a}+\bar{b}+c) \cdot (\bar{a}+b+c)$$

Implementation using gate of given Question



K-Map

K-map minimization of boolean expression

Step 1 -

→ Box are made according to no. of variable - 'n'
i.e - 2^n boxes

	\bar{b}	b
\bar{a}	0	1
a	2	3

	$\bar{a}\bar{b}$	$\bar{a}b$	$a\bar{b}$	ab
\bar{a}	0	1	3	2
a	4	5	7	6

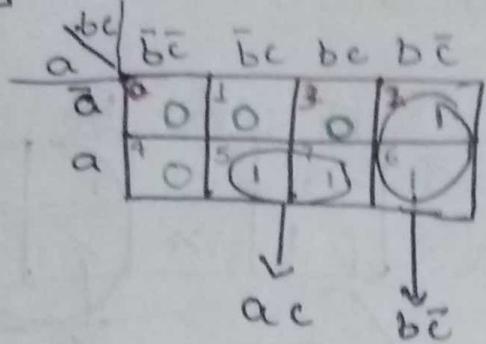
	$\bar{c}\bar{d}$	$\bar{c}d$	$c\bar{d}$	cd
$\bar{a}\bar{b}$	0	1	3	2
$\bar{a}b$	4	5	7	6
ab	12	13	15	14
$a\bar{b}$	8	9	11	10

Let takes e.g -

$$y = ac + b\bar{c}$$

a	b	c	ac	$b\bar{c}$	$ac+b\bar{c}$
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	1	0	1
1	1	1	1	0	1

$$\Rightarrow y = \sum (2, 5, 6, 7)$$



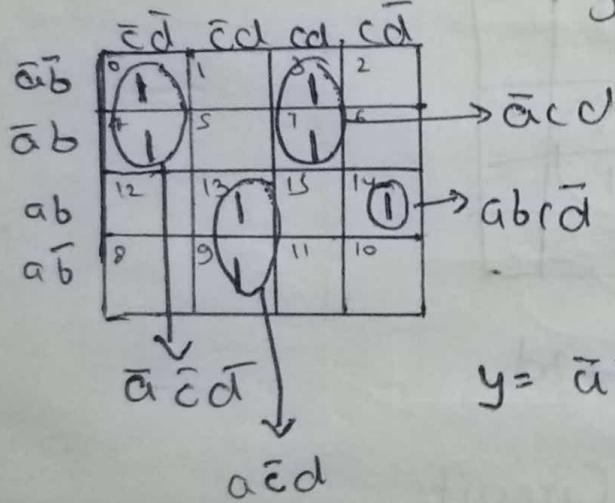
$$y = ac + b\bar{c}$$

\rightarrow Always form group of 2^n

\Rightarrow group of 2^n -sudius n-variable

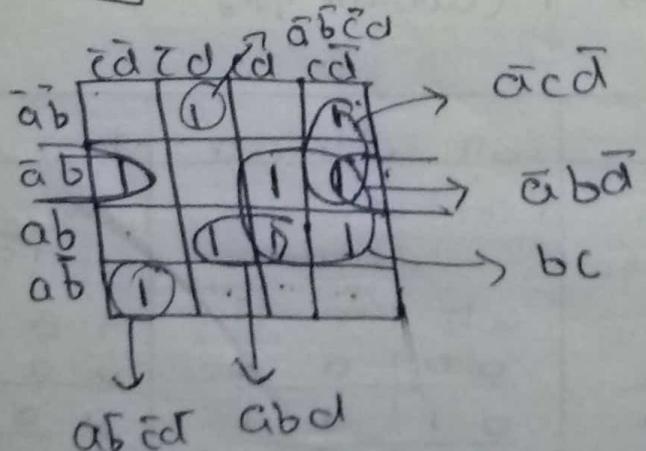
Question make group in following k-map and write output -

$$i) \sum (0, 3, 4, 7, 9, 13, 14)$$



$$y = \bar{a}\bar{c}\bar{d} + a\bar{c}d + \bar{a}cd + ab\bar{c}\bar{d}$$

$$ii) e \sum (1, 2, 4, 6, 7, 8, 13, 14, 15)$$



Don't Care Condition -

Q. $a \ b \ c \quad Y$

$a \ b \ c$	Y	$\bar{b} \bar{c}$	$\bar{b}c$	$b\bar{c}$	$b\bar{c}$
0 0 0	0	0	0	1	1
0 0 1	0	0	1	X	X
0 1 0	1	1	0	0	0
0 1 1	1	1	0	X	X
1 0 0	1	0	1	0	0

don't care condn

$\Rightarrow \sum(3, 3, 4) + \bar{d}(5, 6, 7)$

* when X helps in minimization we will encircle them otherwise we will leave them.

$$Q \rightarrow Y = \sum(0, 1, 5, 7, 13, 15) + \bar{d}(8, 9, 12)$$

$a \bar{b}$	$\bar{c} \bar{d}$	$\bar{c} d$	$c \bar{d}$	$c d$
1	1			
ab		1	X	
ab	X	1	1	
$a \bar{b}$	X	X		

$$\Rightarrow \bar{b}\bar{c} + bd$$

Combinational Circuits

O/p $\rightarrow f$ (current o/p)

	Half adder	Half subtractor	Full adder																																																																																					
Bits -	add $\rightarrow 2$ bits sum carry	add $\rightarrow 2$ bits difference borrow	add $\rightarrow 3$ bits sum cout																																																																																					
Truth table -	<table border="1"> <tr> <td>a</td><td>b</td> <td>sum</td> <td>carry</td> </tr> <tr> <td>0</td><td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td><td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td><td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td><td>1</td> <td>0</td> <td>1</td> </tr> </table>	a	b	sum	carry	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	1	<table border="1"> <tr> <td>a</td><td>b</td> <td>d</td> <td>b</td> </tr> <tr> <td>0</td><td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td><td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td><td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td><td>1</td> <td>0</td> <td>0</td> </tr> </table>	a	b	d	b	0	0	0	0	0	1	1	1	1	0	1	0	1	1	0	0	<table border="1"> <tr> <td>A</td><td>B</td><td>Cin</td><td>S</td><td>Cout</td> </tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>0</td> </tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>0</td> </tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>1</td> </tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>1</td> </tr> <tr> <td>1</td><td>1</td><td>0</td><td>0</td><td>1</td> </tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td> </tr> </table>	A	B	Cin	S	Cout	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	1	1	0	1	1	0	0	1	0	1	0	1	0	1	1	1	0	0	1	1	1	1	1	1
a	b	sum	carry																																																																																					
0	0	0	0																																																																																					
0	1	1	0																																																																																					
1	0	1	0																																																																																					
1	1	0	1																																																																																					
a	b	d	b																																																																																					
0	0	0	0																																																																																					
0	1	1	1																																																																																					
1	0	1	0																																																																																					
1	1	0	0																																																																																					
A	B	Cin	S	Cout																																																																																				
0	0	0	0	0																																																																																				
0	0	1	1	0																																																																																				
0	1	0	1	0																																																																																				
0	1	1	0	1																																																																																				
1	0	0	1	0																																																																																				
1	0	1	0	1																																																																																				
1	1	0	0	1																																																																																				
1	1	1	1	1																																																																																				

Minimizⁿ
by K-map
for S_{1d}

	\bar{b}	b
\bar{a}	0	1
a	1	0

$$S = a\bar{b} + \bar{a}b$$

$$S = a \oplus b$$

	\bar{b}	b
\bar{a}	0	1
a	1	0

$$d = a\bar{b} + b\bar{a}$$

$$d = a \oplus b$$

	$\bar{b}\bar{c}$	$\bar{b}c$	bc	$b\bar{c}$
\bar{a}	0	1	0	1
a	1	0	1	0

$$S = \underline{\bar{a}\bar{b}\bar{c}_{in}} + \underline{\bar{a}\bar{b}c_{in}}$$

$$+ \underline{abc_{in}} + \underline{ab\bar{c}_{in}}$$

$$S = (\bar{a}\bar{b} + \bar{a}b)c_{in} + (ab + a\bar{b})\bar{c}_{in}$$

$$S = (a \oplus b)\bar{c}_{in} + (a \oplus b)c_{in}$$

$$S = \underline{(a \oplus b)\bar{c}_{in}} + \underline{(a \oplus b)c_{in}}$$

Minimizⁿ
by K-map
for -Cout_{1d},
b

	\bar{b}	b
\bar{a}	0	0
a	0	1

$$C = ab$$

	\bar{b}	b
\bar{a}	0	1
a	0	0

$$\bar{b} = \bar{a}b$$

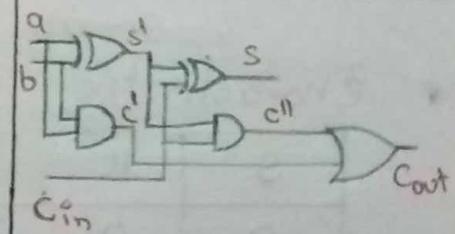
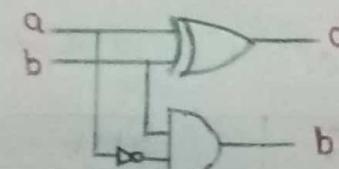
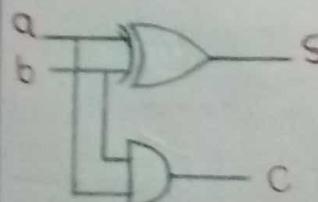
	$\bar{b}\bar{c}$	$\bar{b}c$	bc	$b\bar{c}$
\bar{a}	0	0	1	0
a	0	1	0	1

$$C_{out} = ac + bc + ab$$

$$= ab + (a+b)\bar{c}$$

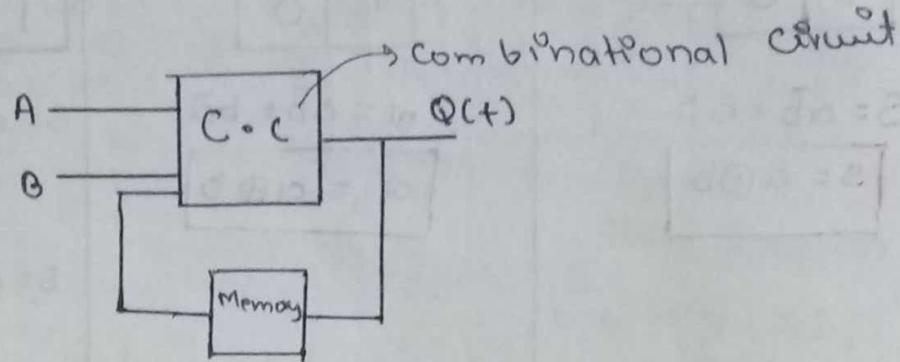
$$C_{out} = ab + (a \oplus b)c_{in}$$

Implementⁿ
using
GATES



Sequential Circuit

O/P \rightarrow f (current I/P, previous O/P)



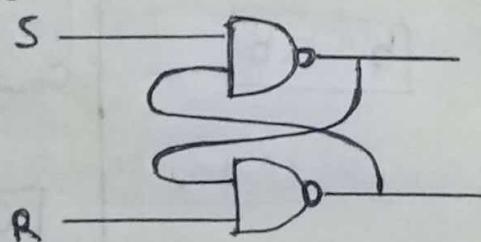
$$\Rightarrow Q_{t+1} = f(A, B, Q_t)$$

\Rightarrow Sequential circuit involve a combinational circuit and some memory elements.

→ LATCH ←

* How we Study SR-Latch

By NAND GATE

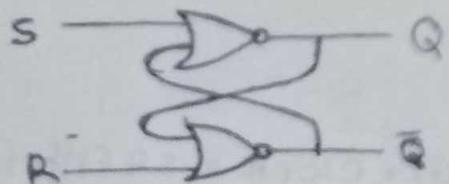


S	R	Q _t	Q _{t+1}
0	0	0	→ Undesire
0	0	1	1 → Set
1	0	0	0 → Reset
1	1	Q	Q → M

Characteristic table.

S	R	Q	Q _{t+1}
0	0	0	
0	0	1	{ Undesirable }
0	1	0	1 } Set
0	1	1	1 }
1	0	0	0 } Reset
1	0	1	0 }
1	1	0	0 } Memory
1	1	1	1 }

SR-Latch by NOR gate.



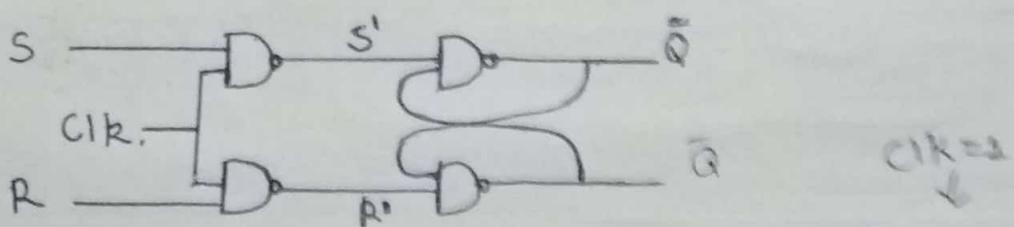
Characteristic table:

S	R	Q	Q_{t+1}
0	0	0	0 } → Memory
0	0	1	1
0	1	0	0 } → Reset
0	1	1	0
1	0	0	1 } → Set
1	0	1	1
1	1	0	} → Undesirable
1	1	1	

Flip-Flop

① SR-flip-flop

SR-latch + clock \rightarrow flip-flop



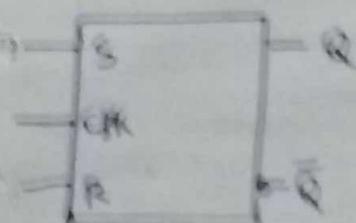
CLK \rightarrow work as controller
at CLK=0, \rightarrow No change

Characteristic Table

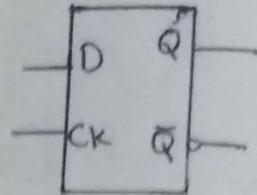
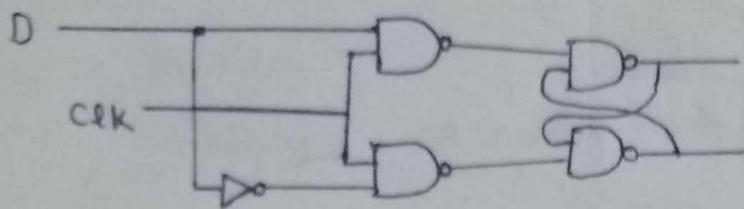
SR	Q_{t+1}
00	undesirable
01	&
10	0
11	memory

CLK	S	R	S'	R'	Q
0	x	x	x	x	No change
1	0	0	1	1	Memory
1	0	1	1	0	Reset
1	1	0	0	1	Set
1	1	1	0	0	Undesirable

\Rightarrow



② D-flip-flop



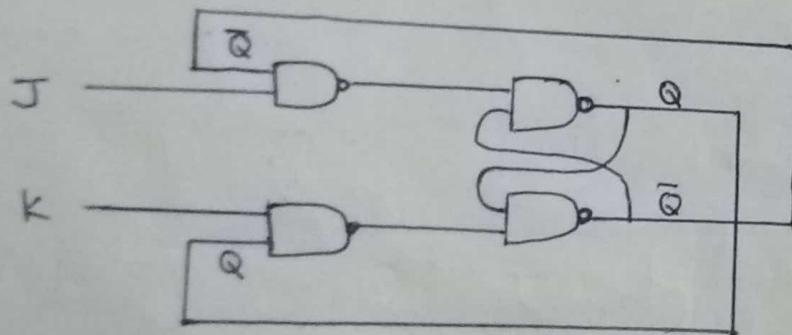
D	S	R	Q_{n+1}
0	0	1	0
1	1	0	1

CLK	D	Q_{n+1}
0	X	Q_n (no change)
1	0	0
1	1	1

Characteristic table

- This is delay flip-flop, also known as Transparent flip-flop

③ P J-K flip-flop



J	K	Q	S	R	Q_{n+1}
0	0	1	1	1	Memory
0	1	0	1	1	0
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	1	0	0	0

} Reset

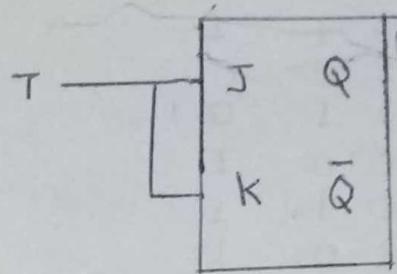
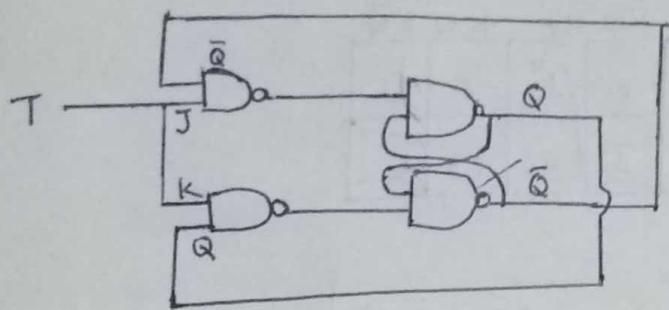
} Set

} P Toggle

J	K	Q_{n+1}
0	0	Memory
0	1	
1	0	Reset
1	1	Set
1	1	Toggle

Characteristic table

④ Toggle flip-flop OR T-flip flop



when, $T=0$, NO change

when, $T=1$, Toggle

T	J	K	Q_{n+1}
0	0	0	Q_n
1	1	1	Q_n

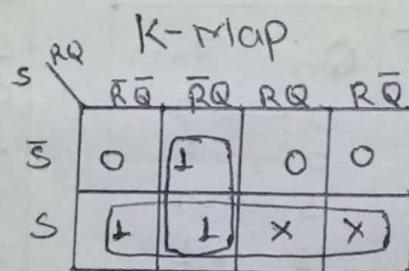
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristics table.

Characteristic Equations -

① SR-flip-flop

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

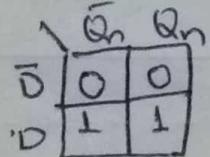


$$Q_{n+1} = S + \bar{R}Q$$

② D-flip flop

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$\Rightarrow Q_{n+1} = D$$



③ J-K flip flop.

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J/K

\bar{J}	\bar{K}	\bar{Q}_n	Q_{n+1}
0	1	0	1
1	0	1	0

$$Q_{n+1} = \bar{J}\bar{Q} + \bar{K}Q$$

④ Toggle flip flop

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

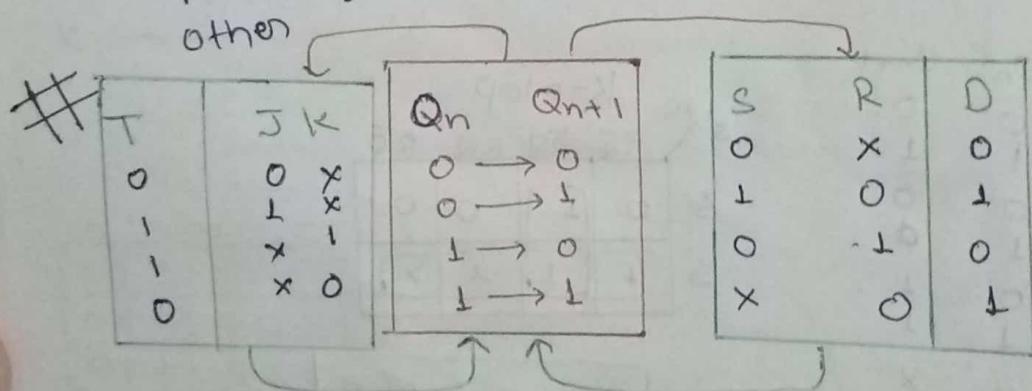
T

\bar{T}	Q_n	\bar{Q}_n
0	0	1
1	1	0

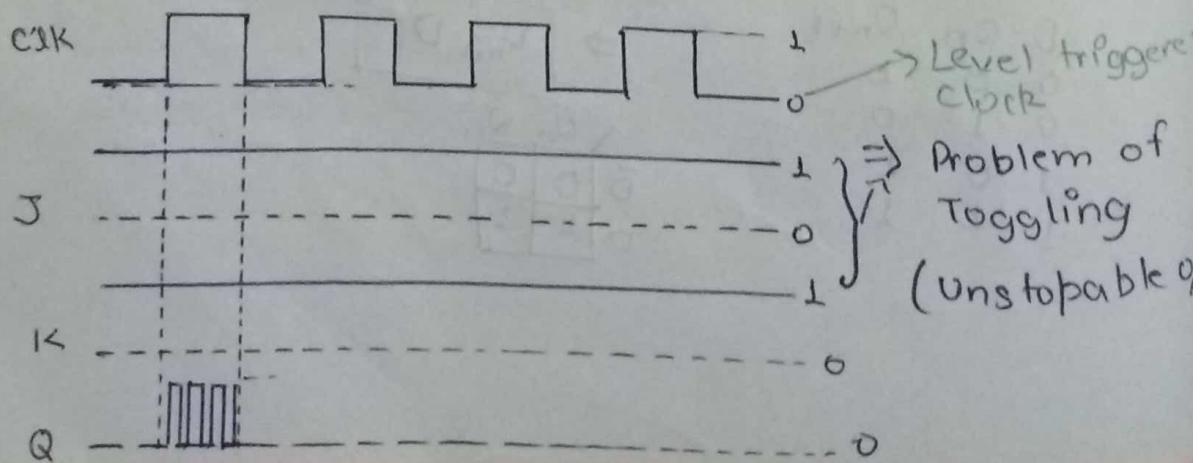
$$Q_{n+1} = \bar{T}\bar{Q}_n + TQ_n$$

- Excitation table -

Input required for transition from one state to other



Master-Slave flip flop.



Solution —

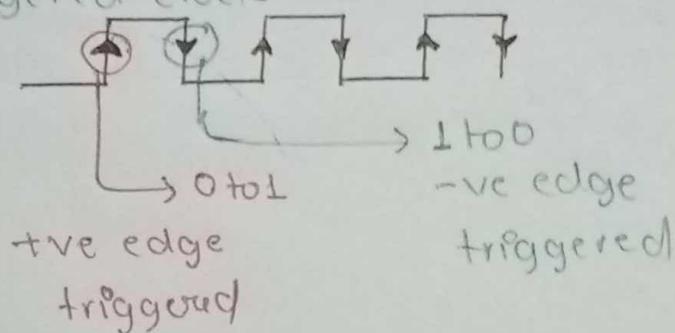
- ① $T_{cik} < P \cdot D \rightarrow$ (execution time of device).
(Prop. Delaly)

But this make device very - very costly so,
we donot accept this method

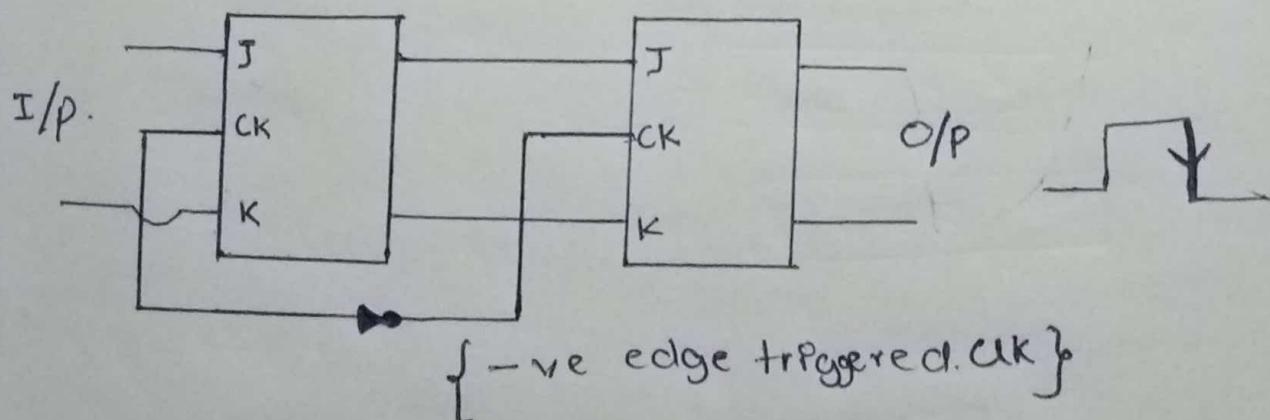
- ② By converting .

Level triggered clock to Edge triggered.

Edge triggered clock.



for this we use Master Slave concept



How, triggered resolve by conversion of -

Level triggering \rightarrow Edge triggering .