

DIGITAL

LOGIC

(6)

PUSHP

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DATE : 27/09/10

DIGITAL ELECTRONICS

1) Minimization And Logical Expression

- A) Boolean Algebra
B) K-Map

2) Logic Gate

- Half Adder
Half Subtractor
Full Adder
Full Subtractor
PA
LAC

3) Combinational Gate

- MUX
DeMUX
Decoder
Encoder
Comparator
Code Converter

4) Sequential circuit

- Flip-flop
Register
Counter

5) Number System, Codes, Data Representation.

- A) ADC / DAC
B) Logic family
C) Semiconductor Memories.

References:-

Digital Logic Design — M. Mano

Logic Design → Roth

Digital Integrated Electronic — Taneja & Schilling

Minimization And Logic Expression.

- Boolean Algebra is used when number of variables are less & off may be 0 & 1.
- K-map is used for 5 variable and output 0, 1, X
- Tabulation method is used when no. of variables are more

2) Boolean Algebra: →

Switch \rightarrow ON \rightarrow 1
 \rightarrow OFF \rightarrow 0

1. NOT : →

$$A \rightarrow \bar{A} \text{ or } A'$$

$$\bar{A} \rightarrow A$$

2. AND : →

$$0 \cdot 0 = 0$$

$$A \cdot A = A$$

$$0 \cdot 1 = 0$$

$$\bar{A} \cdot 0 = 0$$

$$1 \cdot 0 = 0$$

$$A \cdot 1 = A$$

$$1 \cdot 1 = 1$$

$$A \cdot \bar{A} = 0$$

3. OR : →

$$A + A = A$$

$$A \quad B \quad Y$$

$$0 \quad 0 \quad 0$$

$$A + 0 = A$$

$$0 \quad 1 \quad 1$$

$$A + 1 = 1$$

$$1 \quad 0 \quad 1$$

$$A + \bar{A} = 1$$

$$1 \quad 1 \quad 1$$

$$AB + A\bar{B}$$

$$\text{Sol: } = A(B + \bar{B})$$

$$= A$$

Q. $AB + A\bar{B}C + A\bar{B}\bar{C}$ Then minimum no. of NAND gates.

Q. D b) 1 c) 2 d) 3

Sol: $AB + A\bar{B}C + A\bar{B}\bar{C}$

$$= AB + A\bar{B}(C + \bar{C})$$

$$= AB + A\bar{B}$$

$$= A(B + \bar{B})$$

$$= A$$

\therefore Minimum no. of gate = 0

\therefore (a) True.

→ Advantages of Minimization :-

- i) Number of logic gates decreased.
- ii) Speed of operation will increase.
- iii) Power dissipation will reduced.
- iv) Complexity of circuit is less.
- v) Fan in may be reduces.

Q. $A\bar{B} + AB\bar{C} + A\bar{B}\bar{C}D$

Sol: $A\bar{B} + AB\bar{C} + A\bar{B}\bar{C}D$

$$= A\bar{B}(1 + \bar{C}D) + AB\bar{C}$$

$$= A\bar{B} + AB\bar{C}$$

$$= A(\bar{B} + B\bar{C})$$

$$= A(\bar{B} + \bar{C}) \quad [\because \bar{B} + B\bar{C} = \bar{B} + \bar{C}]$$

→ $(A+B)(A+C) = A+BC \rightarrow \text{Transposition}$

$$= A + AC + AB + BC$$

$$= A[1 + C + B] + BC$$

$$= A + BC$$

Q. $(\bar{x}+y)(\bar{x}+z) = ?$ Ans. $\bar{x}+yz$

$$\textcircled{1}: (A+B+C)(A+\bar{B}+C) : (A+B+\bar{C})$$

$$\text{Sol: } (A+B+C)(\underbrace{A+\bar{B}+C}) (\underbrace{A+B+\bar{C}})$$

$$= (A+B+C\bar{C})(A+\bar{B}+C)$$

$$= (A+B)(A+\bar{B}+C)$$

$$= A \cdot A + B(\bar{B}+C)$$

$$= A + BC \quad \text{Ans.}$$

$$\textcircled{2}: (A+B)(A+\bar{B})(\bar{A}+B)(\cancel{\bar{A}}+\bar{B})$$

$$= (A+B\bar{B})(\bar{A}+B\bar{B})$$

$$= A \cdot \bar{A} = 0 \quad \text{Ans.}$$

$$\rightarrow A + BC = (A+B)(A+C)$$

$\downarrow \textcircled{1} + \downarrow \textcircled{2} \textcircled{3}$ $\downarrow \textcircled{1} + \downarrow \textcircled{2}$ $\downarrow \textcircled{1} + \textcircled{3}$

$$\rightarrow A + \bar{A}B = (A+\bar{A})(A+B) = A+B$$

$$\rightarrow A + A\bar{B} = (A+\bar{A})(A+\bar{B}) = A+\bar{B}$$

$$\rightarrow \bar{A} + AB = (\bar{A}+A)(\bar{A}+B) = \bar{A}+B$$

$$\rightarrow \bar{A} + \bar{A}\bar{B} = \bar{A} + \bar{B}$$

$$\textcircled{3}: AB + \bar{A}\bar{B} + A\bar{B}$$

$$\text{Sol: } AB + \bar{A}\bar{B} + A\bar{B}$$

$$= A(\dot{B}+\bar{B}) + \bar{A}\bar{B}$$

$$= A + \bar{A}\bar{B}$$

$$= A + \bar{B} \quad \text{Ans.}$$

$$\textcircled{4}: AB + \bar{A}B + A\bar{B}$$

$$\text{Sol: } AB + A(\dot{B}+\bar{B}) + \bar{A}B$$

$$= A + \bar{A}B = A + B \quad \text{Ans.}$$

Q. $AB\bar{C} + ABC + \bar{A}\bar{B}C$

Sol:
$$\begin{aligned} & AB\bar{C} + ABC + \bar{A}\bar{B}C && \text{2nd Method} \\ & = AB(C + \bar{C}) + \bar{A}BC && \underbrace{AB\bar{C} + ABC}_{AB + BC} + \underbrace{\bar{A}\bar{B}C}_{\bar{A}BC} \\ & = AB + \bar{A}BC \\ & = B(A + \bar{A}C) \\ & = B(A + C) \\ & = AB + BC \quad \text{Ans} \end{aligned}$$

$$AB(C + \bar{C}) + BC(A + \bar{A})$$

$$AB + BC \quad \text{Ans}$$

* Complement or Redundancy Theorem: \rightarrow

$$AB + \bar{A}C + \underline{\bar{B}C} = AB + \bar{A}C$$

Proof:

$$\begin{aligned} & AB + \bar{A}C + BC \\ & = AB + \bar{A}C + BC(A + \bar{A}) \\ & = AB + \bar{A}C + \underline{ABC + \bar{A}BC} \\ & = AB(1 + C) + \bar{A}C(1 + B) \\ & = AB + \bar{A}C \quad \text{Proved.} \end{aligned}$$

\rightarrow Three variables

\rightarrow Each variable used two times.

\rightarrow One variable is complemented / uncomplemented.

\rightarrow It is also called sum of product

Q. $AB + B\bar{C} + AC$

Sol: $AB + B\bar{C} + AC = B\bar{C} + AC \quad \text{Ans.}$

Q. $A\bar{B} + B\bar{C} + AC$

Sol: $A\bar{B} + B\bar{C} + AC = A\bar{B} + B\bar{C} \quad \text{Ans.}$

* Product of sum (POS) :-

$$(A+B)(\bar{A}+C)(B+C)$$

$$=(\bar{A}+C)(A+B)$$

Q. $(A+B)(\bar{B}+C)(A+C)$

$$=(\bar{B}+C)(A+B)$$

Q. $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C}$
SOL: $\bar{A}\bar{B} + A\bar{C}$

Q. $\bar{A}\bar{B} + \bar{B}C + \bar{A}\bar{C}$
 $\bar{B}C + \bar{A}\bar{C}$

Q. $(\bar{A}+\bar{B})(\bar{B}+\bar{C})(\bar{A}+C)$
 $(\bar{A}+C)(\bar{B}+\bar{C})$ Ans.

* DeMorgan's Theorem :-

$$\overline{ABC} = \bar{A} + \bar{B} + \bar{C}$$

$$\overline{A+B+C} = \bar{A}\bar{B}\bar{C}$$

→ Boolean Algebra:-

- | | |
|---------------------------|----------------------|
| 1) Minimization. | 5) Truth table |
| 2) SOP → Minimal | 6) Venn diagram |
| 3) POS → Minimal | 7) Switching circuit |
| 4) Dual | 8) Statement |
| 5) Complement expression. | |

1) Minimisation: →

Q) $X\bar{Y} + \bar{X}\bar{Y}WZ$
 $A + \bar{A}B$.

Sol: $= XY + WZ$ Ans.

Q. Let $f(A, B) = \bar{A} + B$. Then the value of $f(f(x+y, \bar{z}), z)$ is

a) $X\bar{Y} + Z$ b) $\bar{X}\bar{Y} + Z$ c) $\bar{X}\bar{Y} + Z$ d) X

Sol: $f(x+y, \bar{z}) = \bar{x}+y + \bar{z}y$ $[\because f(A, B) = \bar{A}+B]$
 $= \bar{x} \cdot \bar{y} + y$
 $= \bar{x}+y$

$$\begin{aligned} f(\bar{x}+y, z) &= \bar{\bar{x}}+y + z \\ &= x\bar{y} + z = f(f(x+y, \bar{z}), z) \end{aligned}$$

Q. Let $X+Y = \bar{X}+Y$ & $Z = X \cdot Y$ then the value of $Z \cdot X$ is

a) X b) 1 c) 0 d) \bar{X}

Sol: $X+Y = \bar{X}+Y$ } given.
 $Z = X \cdot Y$ }

$\therefore Z = X \cdot Y = \bar{X}+Y$ ~~Ans.~~

$$\begin{aligned} Z \cdot X &= \bar{Z} + X \\ &= \bar{\bar{X}}+Y + X \\ &= X\bar{Y} + X \\ &= X(1+\bar{Y}) \\ &= X \end{aligned}$$

2) Sum of Product (SOP): →

$ABC + \bar{A}BC + (\bar{A}\bar{B}\bar{C}) \rightarrow$ Product term.

In SOP form each product term is known as min term or minterm. It is used when O/P of logical expr. is 1.

Ex 5 $\rightarrow 101$

$$ABC$$

$$9 \rightarrow 1001$$

$$ABC\bar{D}$$

Q. For the given truth table minimize SOP expression.

Sol:

A	B	Y	Min term
0	0	0	01
1	0	1	10
2	1	0	11
3	1	1	0

$$Y = \bar{A}\bar{B} + A\bar{B}$$

$$= \bar{B}(A + \bar{A})$$

$$= \bar{B} \text{ Min.}$$

$$Y(A, B) = \sum m(0, 2)$$

Q. Simplified the expression for $Y(A, B) = \sum m(0, 2, 3)$

Sol:

$$\begin{aligned} Y(A, B) &= \sum m(0, 2, 3) \\ &= \bar{A}\bar{B} + A\bar{B} + AB \\ &= A(B + \bar{B}) + \bar{A}\bar{B} \\ &= A + \bar{A}\bar{B} \\ &= A + \bar{B} \quad (\text{one}) \end{aligned}$$

→ SOP → Minimal $A + \bar{B}$.
→ Canonical

$$A \cdot 1 + \bar{A}B$$

$$A(B + \bar{B}) + \bar{A}B$$

$$AB + A\bar{B} + \bar{A}B$$

In canonical SOP or standard SOP form each minimum contain all variable.

Date - 2010

Q. In canonical SOP form the number of min term in logical expression $A + \bar{B}C$ is

- a) 4 b) 5 c) 6 d) 7

Sol: $A + \bar{B}C = A(B + \bar{B})(C + \bar{C}) + \bar{B}\bar{C}(A + \bar{A})$

$$= A[B(C + \bar{C}) + \bar{B}C + \bar{B}\bar{C}] + A\bar{C}C + \bar{A}\bar{B}C$$

$$= ABC + ABC + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$$

$$= 5 \text{ min term}$$

* Product of Sum (POS) :-

$$(A+B+\bar{C})(\bar{A}+B+\bar{C})(A+B+C)$$

\hookrightarrow Max term.

POS form are used when O/P is logic 0

Ex $\rightarrow 5 \rightarrow 101$

$$\bar{A} B \bar{C}$$

Q. For the given truth table minimise POS expression:-

A	B	Y	MAX term
0	0	1	$\bar{A} \bar{B}$
0	1	0	$(A+\bar{B})$
1	0	1	$\bar{A} B$
1	1	0	$(\bar{A}+\bar{B})$

$$Y(A,B) = (A+\bar{B})(\bar{A}+B) = A\bar{A} + A.B + \bar{A}\bar{B} + B\bar{B}$$

$$= \bar{B}$$

$$Y(A,B) = \pi M(1,3) = \bar{B}$$

$$\therefore Y(A,B) = \sum m(0,2) = \bar{B}$$

$$\sum m(0,2) = \pi M(1,3)$$

Note:-

→ With n variables max^m possible min term are max term 2^n

$$AB \rightarrow 16$$

AB	$\bar{A}\bar{B}$	A	1
$A+\bar{B}$	$\bar{A}B$	\bar{A}	0
$\bar{A}\bar{B}$	$A+\bar{B}$	B	$\bar{A}B+A\bar{B}$
$\bar{A}+B$	$\bar{A}+B$	\bar{B}	$AB+\bar{A}\bar{B}$

→ With n variables max^m possible logical expression are 2^{2^n}

$$\text{for } n = 2 \quad 2^2 = 4$$

$$\therefore 3 \quad 2^2 = 8$$

$$\therefore 4 \quad 2^4 = 2^6 = 2^2 \times 2^4 = 16$$

$$= 65536$$

* Dual :-

+Ve logic

Logic 0 \rightarrow 0V

Logic 1 \rightarrow +5V

Ex :-

-Ve logic

Logic 0 = +5V

Logic 1 = 0V

\rightarrow Logic 0 \rightarrow -5V \rightarrow +ve logic.

Logic 1 \rightarrow 0V

\rightarrow FCL :-

Logic 0 \rightarrow -1.7V \rightarrow +ve logic.

Logic 1 \rightarrow -0.8V

\rightarrow +ve logic AND			\rightarrow -ve logic OR			\rightarrow +ve logic OR		
A	B	Y	A	B	Y	A	B	Y
0	0	0	1	1	1	0	0	0
0	1	0	1	0	0	0	1	1
1	0	0	0	1	0	1	0	1
1	1	1	0	0	0	1	1	1

+ve logic AND = -ve logic OR

-ve logic AND = +ve logic OR

\rightarrow Dual expression is used +ve logic to -ve logic and
 -ve logic to +ve logic.

\rightarrow STEPS:-

1) AND \leftrightarrow OR

• \leftrightarrow +

2) 1 \leftrightarrow 0

3) Keep Variable as it is

\rightarrow for any logical expression if two times dual is used result is same expression.

Q. Write dual expression of the following expression.

$$ABC + \bar{A}BC + ABC$$

Sol:

$$AB\bar{C} + \bar{A}\bar{B}C + A\bar{B}C$$

$$(A+B+\bar{C}) \cdot (\bar{A}+B+C) \quad \text{Ans.}$$

$$AB\bar{C} + \bar{A}\bar{B}C + A\bar{B}C$$

★ Self Dual: →

$$AB + BC + AC$$

$$= (A+B) (B+C) (A+C)$$

$$= (B+AC) (A+C)$$

$$= AB + BC + AC$$

→ In self dual expression if one time dual is used resulting in same expression.

→ In n -variables, max^m possible dual expression is,

$$\text{Max}^m \text{ possible dual Expression} = 2^{2^{n-1}}$$

$$\text{for } n = 1 \quad 2$$

$$= 2 \quad 4$$

$$= 3 \quad 16$$

★ Complement: →

→ Steps:-

1) AND \leftrightarrow OR

2) 1 \leftrightarrow 0

3) Complement each variables.

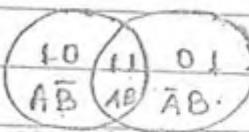
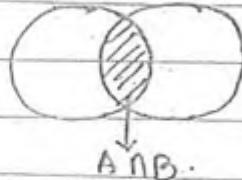
Q. $Y = ABC + \bar{A}BC + A\bar{B}C$

$$\bar{Y} = (\bar{A}+\bar{B}+\bar{C}) (A+\bar{B}+\bar{C}) (\bar{A}+B+\bar{C}) \quad \text{Ans.}$$



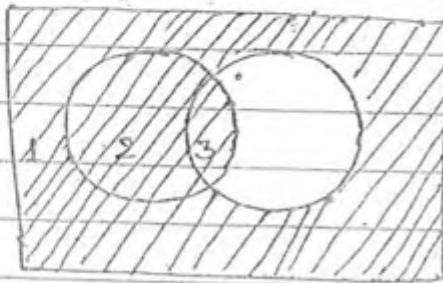
Venn Diagram:

$$A \quad B$$



$$A \cap B$$

- Q. For the given Venn diagram, minimise SOP expression for shaded areas.



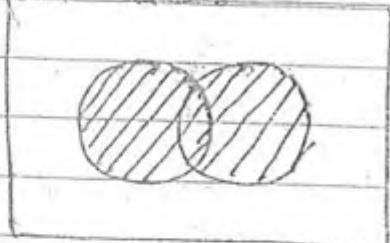
$$\bar{A}\bar{B} + A\bar{B} + AB$$

$$= A(B + \bar{B}) + \bar{A}\bar{B}$$

$$= A + \bar{A}\bar{B}$$

$$= A + \bar{B}$$
 Ans

- Q. For the given Venn diagram, minimise the expression for shaded areas.

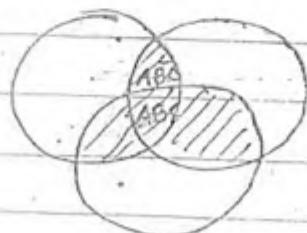


Sol:

$$A\bar{B} + A\bar{B} + \bar{A}\bar{B}$$

$$A(B + \bar{B}) + \bar{A}\bar{B} = A + \bar{A}\bar{B} = A + B$$

Q.



$$ABC + ABC\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$$

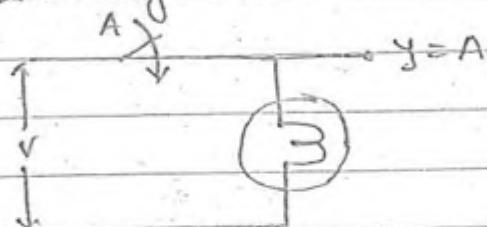
$$AB[C + \bar{C}] + AC[B + \bar{B}] + BC[A + \bar{A}]$$

$$AB + AC + BC$$

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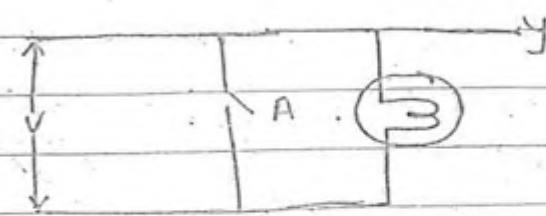
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* Switching Circuit :→



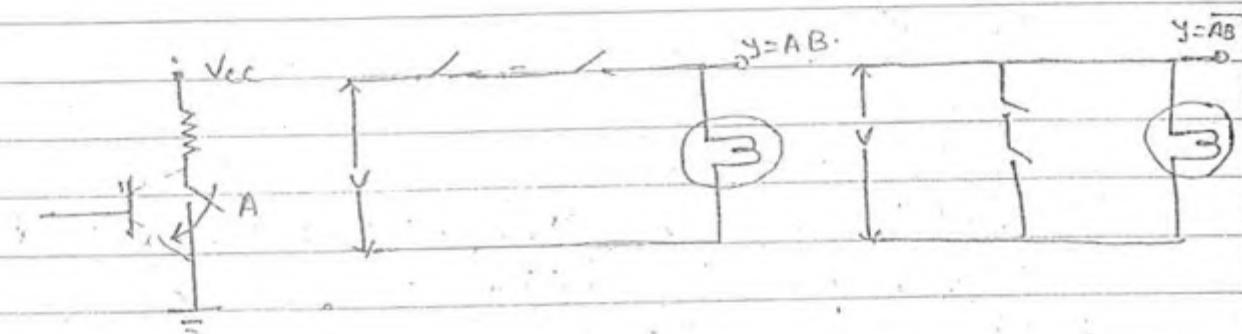
Series.

A	y
0	0
1	1

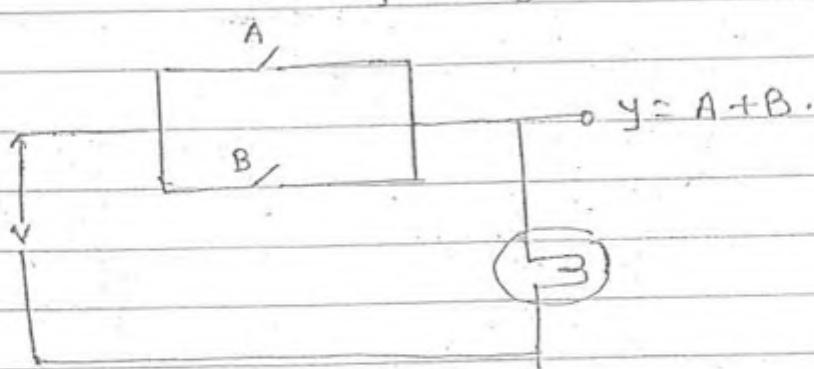


Parallel.

A	y
0	1
1	0

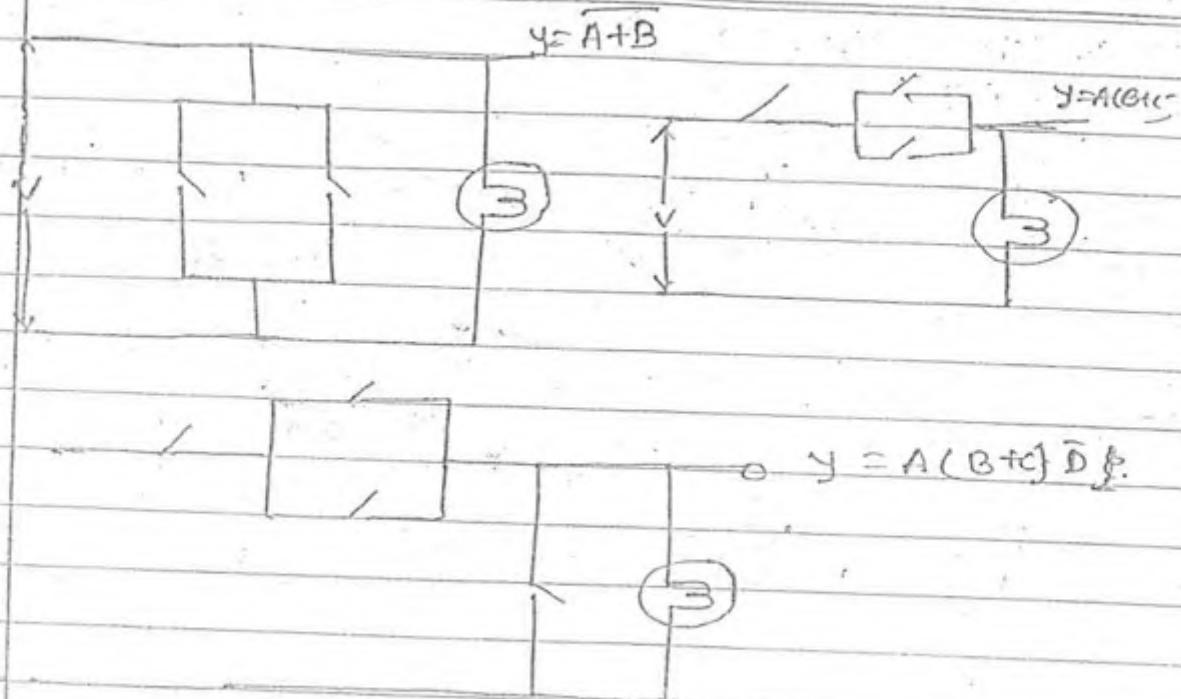


A	y
0	1
1	0



A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

$$0 \rightarrow \text{max term } \bar{A} + \bar{B} = \bar{A}\bar{B}$$



Statements :-

- Q. In logic circuit have three I/P, A, B, C and O/P is Y.
Y is 1 for the following combinations.
- B and C are true $\rightarrow BC$
 - A and C are false $\rightarrow \bar{A}\bar{C}$
 - A, B and C are true $\rightarrow ABC$
 - A, B and C are false $\rightarrow \bar{A}\bar{B}\bar{C}$

Then minimise the expression for Y.

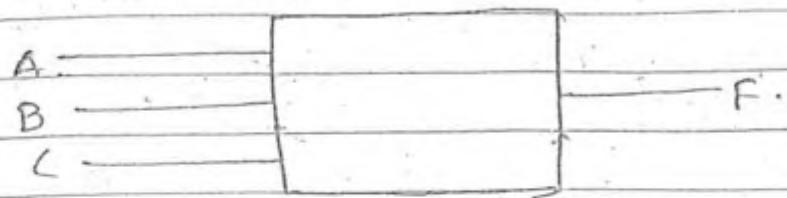
Sol:-
$$Y = BC + \bar{A}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$$

$$= BC(1+A) + \bar{A}\bar{C}(1+\bar{B})$$

$$= BC + \bar{A}\bar{C}$$

- Q. A logic circuits have three I/P, A, B, C & O/P is F.
F is 1 When majority no. of I/P are at logic 1.
- Minimise the expression for F
 - Implement logic circuit.

Sol:-



A	B	C	F	Min term
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\bar{A}BC$
1	0	0	0	
1	0	1	1	$A\bar{B}C$
1	1	0	1	$AB\bar{C}$
1	1	1	1	ABC

$$\begin{aligned}
 F &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\
 &= AB + BC + AC
 \end{aligned}$$

* Logic gates : \rightarrow

Basic building blocks.

NOT

OR

AND

\rightarrow Basic gate.

NAND

NOR

\rightarrow Universal gate.

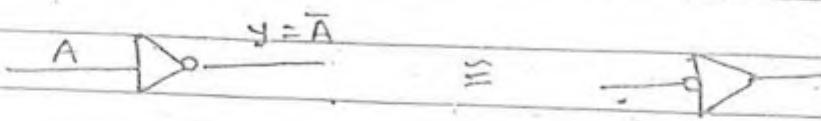
EXOR

EXNOR

\rightarrow Arithmetic CKT

comparator

Parity generator | Checkers
Code converter.

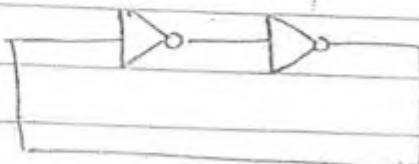
1. NOT ! \rightarrow 

A Y

0 1

1 0

Q) The circuit shown in figure:



a) Buffer

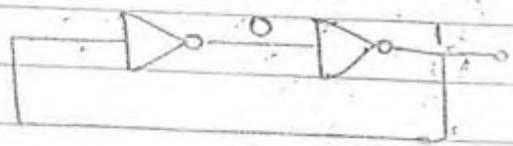
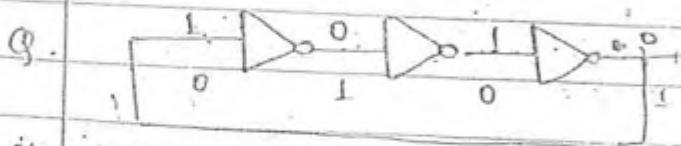
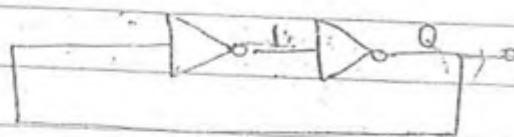
(When we apply the input we obtain)

b) Adjustable Multivibrator

c) Bistable Multivibrator

d) Square wave generator.

Sol:

Basic Memory
Bistable multivibrator

<---3tpd---> 3tpd

$$T = 6tpd$$

$$= 2 \times 3tpd = 2Ntpd$$

N = No. of inverter

a) Adjustable Multivibrator

b) Square wave generator

c) Clock generator

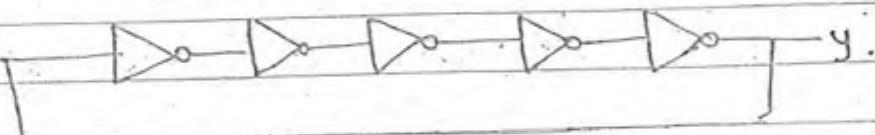
d) Ring oscillator.

→ Ring oscillator, $T = 2Ntpd$.

Where N = NO. of inter feedback

- Q. The circuit shown in figure, propagation delay of each NOT gate is 100 ps then frequency of square wave is
 a) 10 GHz b) 16 Hz c) 50 GHz d) 5 GHz.

Sol:



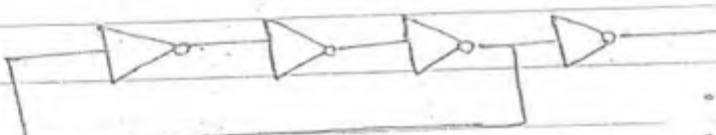
$$T = 2Ntpd$$

$$= 2 \times 5 \times 100 \times 10^{-12} = 10^9$$

$$f = \frac{1}{T} = \frac{1}{10^9} = 1 \text{ Hz}$$

- Q. The circuit shown in figure, propagation delay of each NOT gate is 2 ns, then time period of generated squarewave

- a) 6 b) 12 c) 14 d) 16

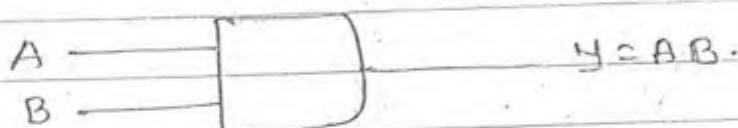


Sol:

$$T = 2Ntpd$$

$$= 2 \times 4 \times 2 = 16$$

2 AND gate :-



→ Truth Table :-

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

→ Commutative Law:-

$$AB = BA$$

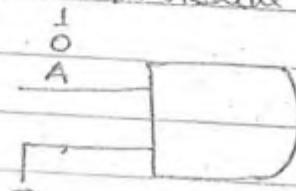
→ Associative Law:-

$$ABC = (AB)C = A(BC)$$

Note:-

- * AND gate follows commutative as well as associative law.
- * AND gate is series switcher.

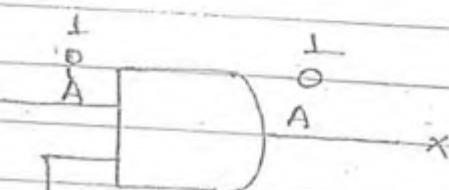
→ Enable / Disable :-



$0 \rightarrow$ control

O/P not change

∴ disable

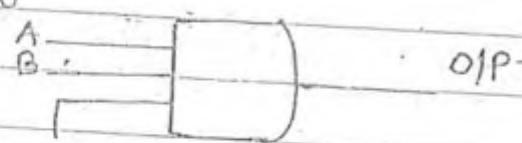


$1 \rightarrow$ control

$1 \oplus 0$ changes

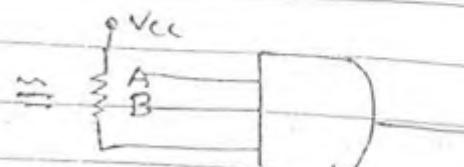
∴ to enable.

→ In TTL logic family open or floating I/P will act as logic 1. Whereas in ECL, I/P will act as logic 0.

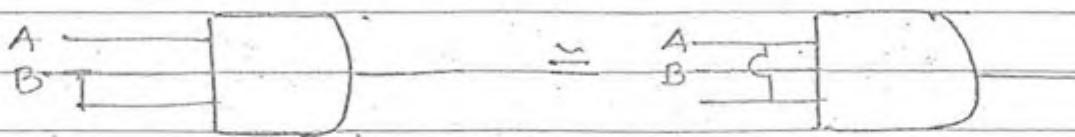


Open or floating I/P.

→ In multi I/P AND gate unused I/P can be connected to Logic 1 or pull up:-



B) Connected to one of one S/P :-

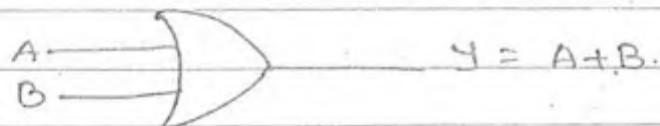


C) If it is TTL logic family then unused S/P can be open or float.



D) Best way of connecting unused S/P of AND gate is connected to logic 1.

3 OR Gate:-



→ Truth table:-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

4 OR gate in parallel switch.



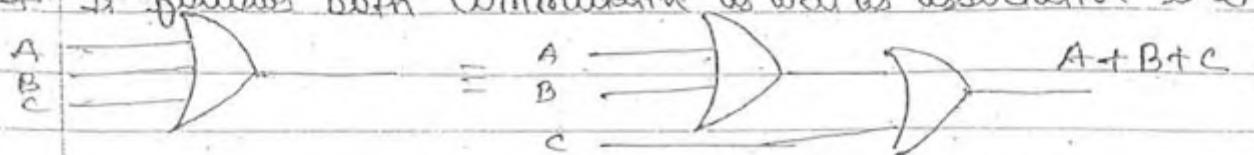
→ Commutative law:-

$$A + B = B + A$$

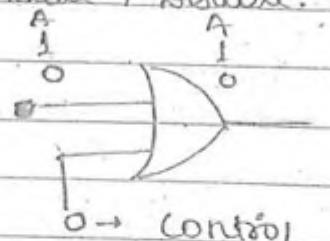
→ Associative Law:-

$$A + B + C = (A + B) + C$$

It follows both commutative as well as associative law.



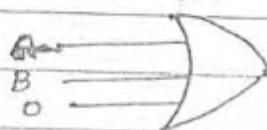
→ Enable / Disable :-



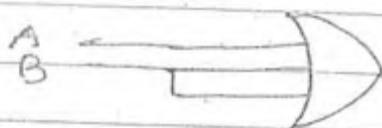
1 Control
Disable

→ In multi I/P OR gate, unused I/P can be connected

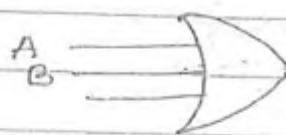
A) Logic 0 or pull down:-



B) One of used I/P



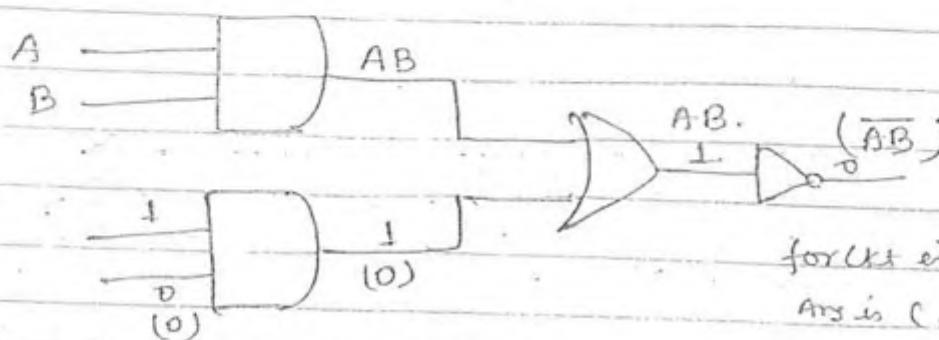
C) If it is ECL, then unused I/P can be open/floating



Note - 204

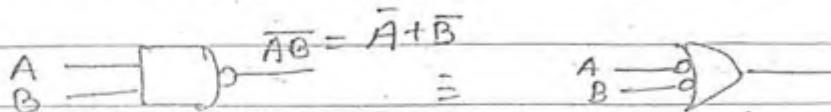
Q. The circuit shown in figure is TTL AND-OR inverter. Then for the given I/P, O/P is

- a) 0 b) 1 c) AB d) \overline{AB}



for Ukt in ECL
Ans is C ...)

4. NAND Gate :-



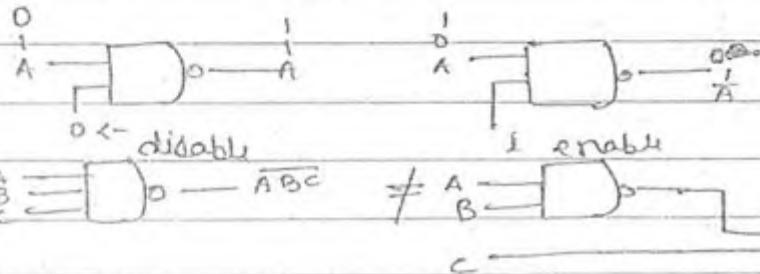
A B Y

0 0 1 ..

0 1 1

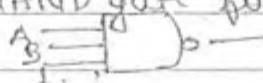
1 0 1

1 1 0



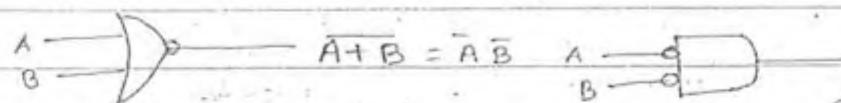
$$\bar{ABC} = AB + C$$

NAND gate follows associative law but not follow commutative.



Unused I/P of a NAND gate can be connected similar to unused I/P of a AND gate.

5 NOR Gate :-



Bubbled AND

A B Y

0 0 1

0 1 0

1 0 0

1 1 0

1 0

0 1

1 0

0 1

A 0

0 0

1 0

0 0

0 <-- enabled

1 <-- disabled

It follows commutative law but not associative law.

→ Commutative Law:-

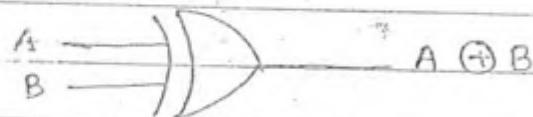
$$A+B = B+A$$

→ Associative Law: →

$$A+B+C \neq \bar{A}+\bar{B}+C$$

→ Unused DIP of NOR gate can be connected similar to OR gate

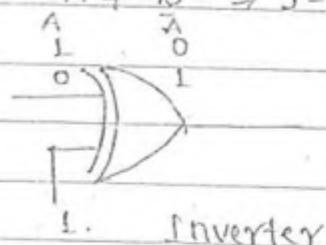
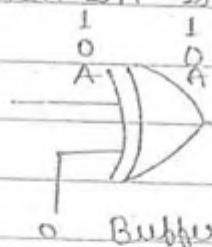
6 EXOR or XOR gate (Exclusive OR gate) : →



A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

In XOR gate output is 0 when $A=B \Rightarrow y=0$

When DIP is 1 then $A \neq B \Rightarrow y=1$



Enable

It is also called controlled inverter.

$$A \oplus A = 0$$

$$A \oplus \bar{A} = 1$$

$$A \oplus 0 = A$$

$$A \oplus 1 = \bar{A}$$

Q. If $A \oplus B = C$ then $A \oplus C = ?$

Sol: $A \oplus C = B$

$$B \oplus C = A$$

$$(A \oplus B) \oplus C = 0$$

$\rightarrow A \oplus A = 0$

$$A \oplus A \oplus A = A$$

$$A \oplus A \oplus A \oplus A = 0$$

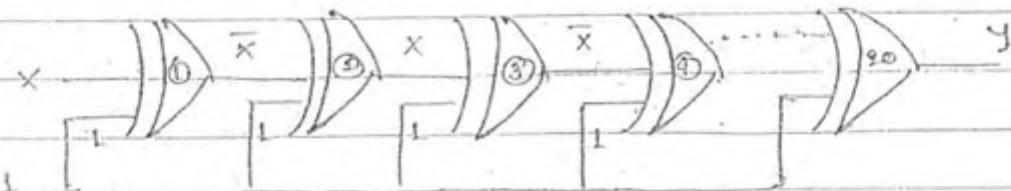
etc

$\rightarrow B \oplus B \oplus B \oplus \dots$ n terms.

$$= B \text{ when } n \text{ is odd}$$

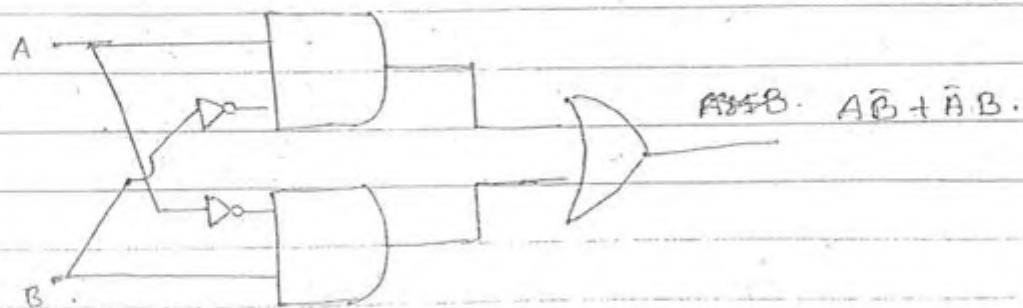
$$= 0 \text{ when } n \text{ is even.}$$

- Q. The circuit shown in figure contains cascading of XOR gate for given I/P, O/P Y is as follows



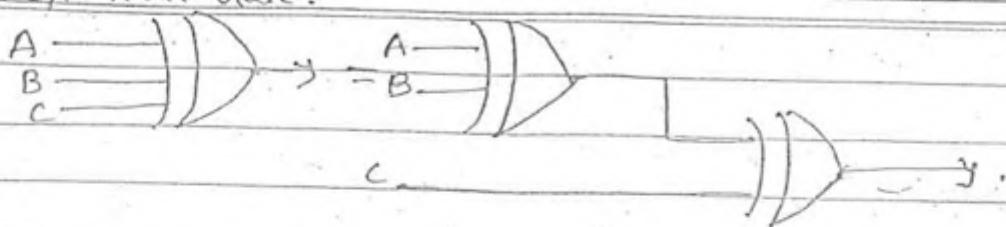
D

Q



\rightarrow XOR gate follows both commutative or associative law.

→ 3 I/P XOR Gate: →



A B Y

0 0 0

0 1 1 ✓

1 0 1 ✓

1 1 0

→ In X-OR gate O/P is 1 when no of 1's at I/P = odd number

→ A B C $Y = A \oplus B \oplus C$

0 0 0 0

0 0 1 1 ✓

0 1 0 1 ✓

0 1 1 0

1 0 0 1 ✓

1 0 1 0

1 1 0 0

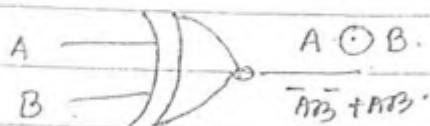
1 1 1 1 ✓

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

0 0 1 0 1 0 1 0 0 1 1 1 → odd no. of 1's.

$$= \Sigma m(1, 2, 4, 7)$$

7 EXNOR or XNOR [Exclusive NOR Gate]: →



$A \oplus B$

$\bar{A}\bar{B} + A\bar{B}'$

A B Y

0 0 1

0 1 0

1 0 0

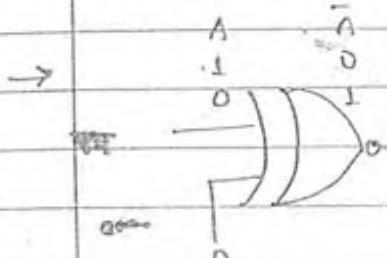
1 1 1

$$SOP \rightarrow \bar{A}\bar{B} + AB$$

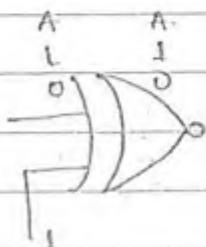
$$POS \rightarrow (A+B)(\bar{A}+B)$$

D/P is 1 when $A=B \Rightarrow 1$. coincidence logic ckt
Equivalence detector

D/P is 0 when $A \neq B$



Inverter



Buffer

$$A \oplus A = 1$$

$$A \oplus \bar{A} = 0$$

$$A \oplus 0 = A$$

$$A \oplus 1 = \bar{A}$$

* Comparison Between XOR & XNOR:-

$$A \oplus A = 0$$

$$A \odot A = 1$$

$$A \oplus A \oplus A = A$$

$$A \odot A \odot A = A$$

$$A \oplus A \oplus A \oplus A = 0$$

$$A \odot A \odot A \odot A = 1$$

$$\rightarrow A \oplus B = \bar{A} \oplus \bar{B}$$

$$A \oplus B \oplus C = A \odot B \odot C$$

$$A \oplus B \oplus C \oplus D = A \odot B \odot C \odot D$$

XOR & XNOR are not complement to each other, when number of 1's are odd.

$$(A \odot B) \odot C = (\bar{A}\bar{B} + AB) \odot C$$

$$(\bar{A}\bar{B} + AB) \bar{C} + (\bar{A}\bar{B} + AB) C$$

$$(AB + A\bar{B}) \bar{C} + A\bar{B}C + ABC$$

Q For the given truth table the logical expression is

$$A \cdot B \cdot C \quad Y = A \oplus B \oplus C = A \odot B \odot C$$

$$0 \quad 0 \quad 0 \quad 1$$

$$0 \quad 0 \quad 1 \quad 0$$

$$0 \quad 1 \quad 0 \quad 0$$

$$0 \quad 1 \quad 1 \quad 1$$

$$1 \quad 0 \quad 0 \quad 0$$

$$1 \quad 0 \quad 1 \quad 1$$

$$1 \quad 1 \quad 0 \quad 1$$

$$1 \quad 1 \quad 1 \quad 0$$

a) $A \oplus B \oplus C$

b) $A \odot B \odot C$

c) $A \odot B \odot C$

d) $AB + BC + AC$

Ans:

→ XNOR gate is even no of 1's detector when no of I/P are even

→ XNOR gate is odd no of 1's detector when no of I/P are odd.

$$\rightarrow \bar{A} \oplus B = A \odot B$$

$$\downarrow \\ x \oplus y$$

$$\bar{x}y + x\bar{y}$$

$$AB + \bar{A}\bar{B}$$

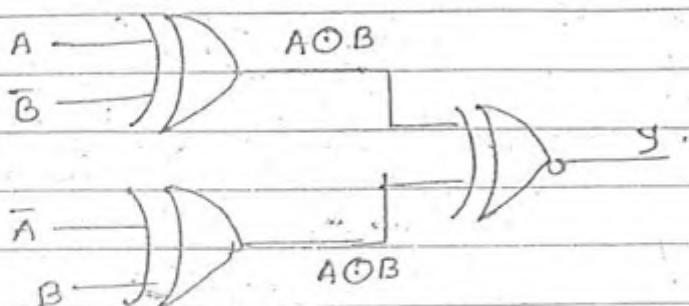
$$\rightarrow A \odot \bar{B} = A \odot B$$

$$\bar{A} \odot B = A \oplus B$$

$$A \odot \bar{B} = A \oplus B$$

$$\rightarrow A \oplus B \oplus AB = A + B$$

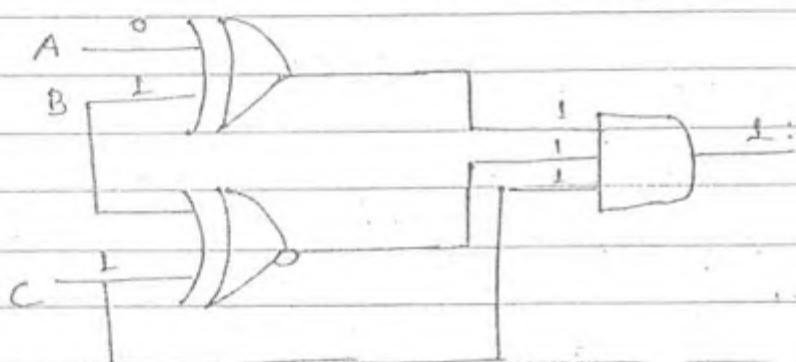
Q) For the given circuit OIP Y is



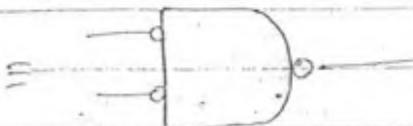
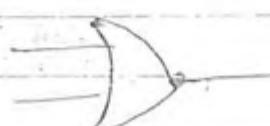
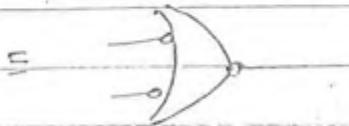
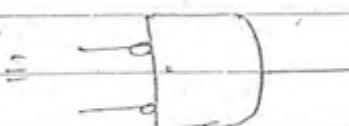
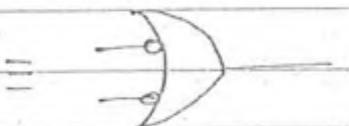
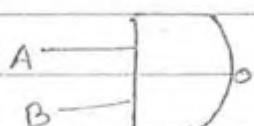
- a) 0 b) 1 c) $A \oplus B$ d) $A \odot B$.

ANS:

Q)

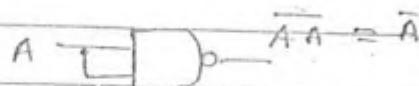


* NAND



i) NAND Gate As Universal Gate: \Rightarrow

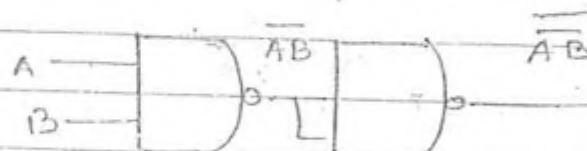
ii) NOT: -



No. of Gate.

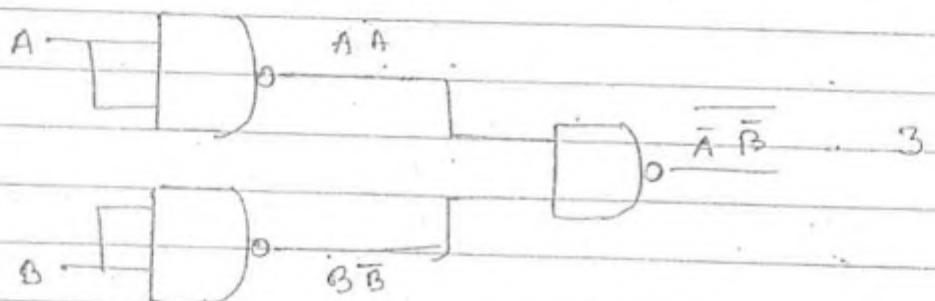
1

iii) AND: -



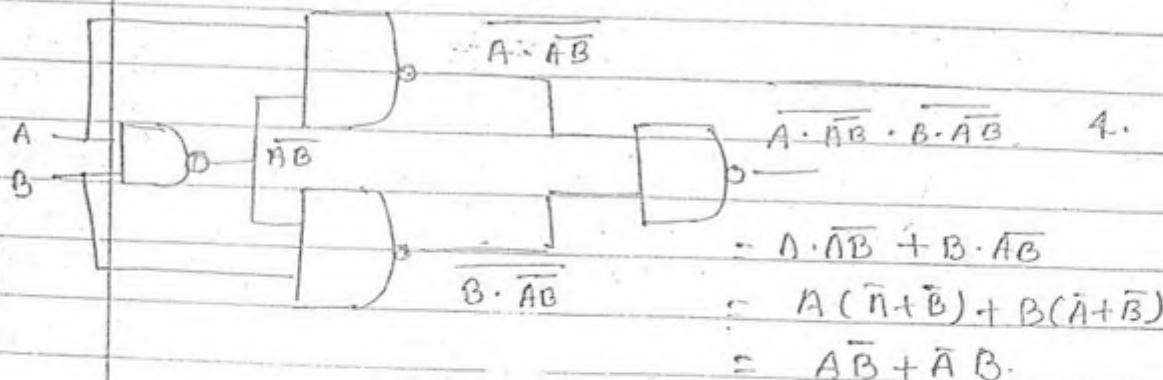
2.

iv) OR: \Rightarrow



3.

v) EXOR: -



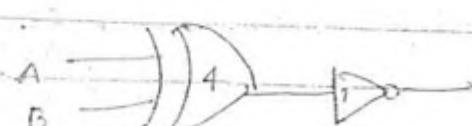
4.

$$= A \cdot \bar{A}B + B \cdot \bar{A}B$$

$$= A(\bar{A} + B) + B(\bar{A} + B)$$

$$= \bar{A}B + A\bar{B}$$

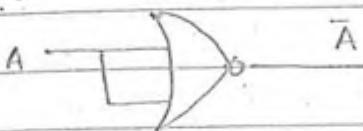
vi) ExNOR: -



5

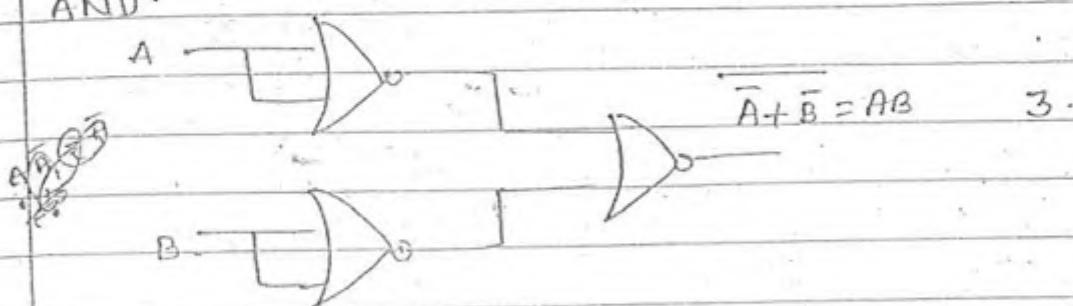
2. NOR gate As Universal Gate! \rightarrow

i) NOT:-



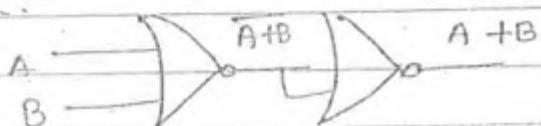
No. of gate 1

ii) AND:-



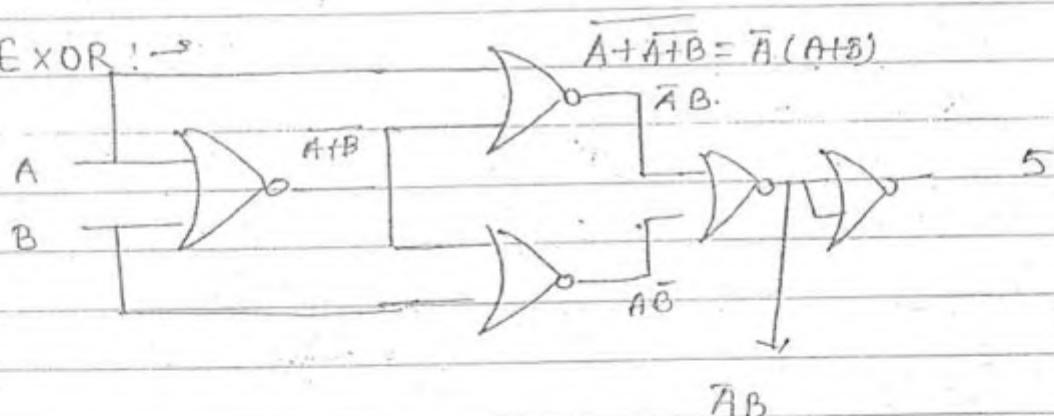
3.

iii) OR:-



2

iv) EXOR:-



5

v) EXNOR:-

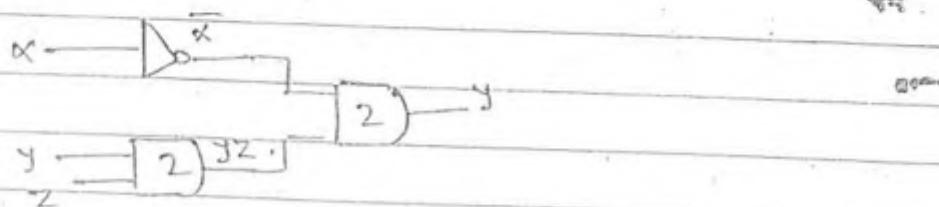
vi) NAND:-

Logic Gate	No. of NAND	No. of NOR
NOT	1	1
AND	2	3
OR	3	2
EXOR	4	5
EXNOR	5	4

Q. To implement $\bar{x}yz$ minimum no. of two I/P NAND gate

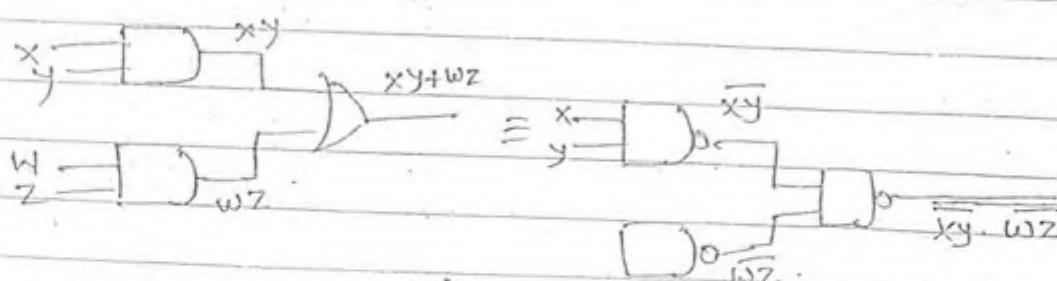
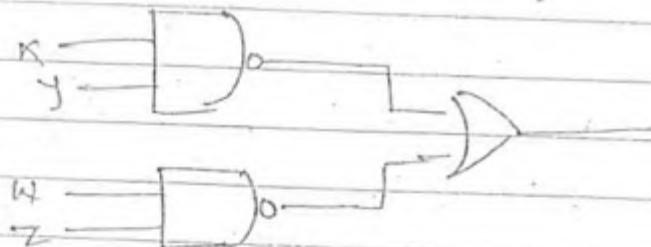
- a) 3 b) 4 c) 5 d) 7

Sol:



Q. To implement $xy + wz$ minimum no. of two I/P NAND gate

a)



Two level AND-OR = Two level NAND-NAND.

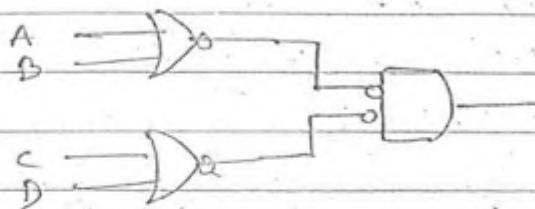
Q. To implement $(A+B)(C+D)$ minimum number of NOR gate required

Sol:

(3)

PAGE NO.

DATE :



3

OR-AND \Leftrightarrow NOR-NOR

POS \Rightarrow only NOR gates.

1AB

32 (a)

31 (b)

30 (c)

$$AB + AC \quad [(\bar{A}\bar{B})(\bar{A}C)]$$

\downarrow \downarrow

$\neg AB$.

29 D

28 b

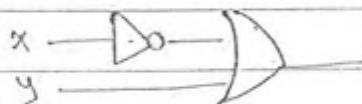
27 d x y f

0 0 1

0 1 1

1 0 0 $\leftarrow \bar{x} + y$

1 1 1



24 (a)

23 Inverse function \rightarrow complement

$$c \rightarrow a + bc \Rightarrow \bar{a}(\bar{b} + \bar{c})$$

c = 1

a = 2

D = 4

$$b \rightarrow (ab + \bar{a}\bar{b}) + c$$

$$(a \oplus b) \cdot c$$

3

21 (d) $AD + ABCD + ACD + \bar{A}B + \bar{A}\bar{B}$
 $AD[1 + C + BC] + \bar{A}(B + \bar{B})$
 $\bar{A} + AD = \bar{A} + D$

20 (a)

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

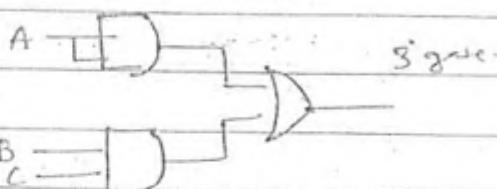
$$\bar{A}BC + AB\bar{C}$$

$$B[\bar{A}C + A\bar{C}]$$

$$B[A + C][\bar{A} + \bar{C}]$$

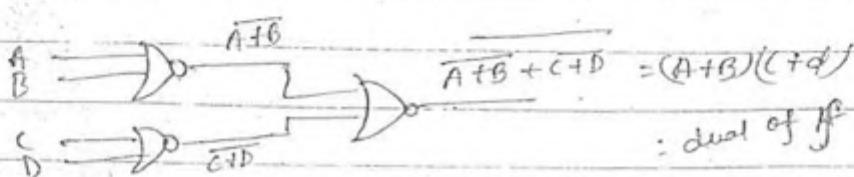
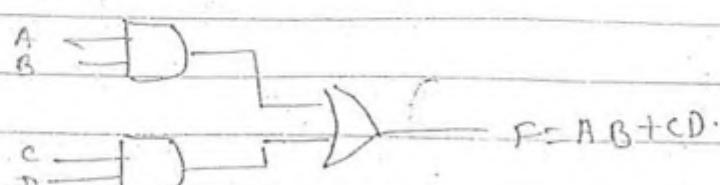
19 $A + BC$

$A \cdot A + BC$



18 a

17 (c)



PAGE NO.

STAC

PAGE NO.

DATE :

$$\begin{array}{l} \xrightarrow{\text{DUAL}} \text{AND} \leftrightarrow \text{OR} \\ \text{NAND} \xleftarrow{\text{DUAL}} \text{NOR} \\ \text{EXOR} \xleftarrow{\text{DUAL}} \text{EXNOR} \\ \text{NOT} \leftrightarrow \text{NOT} \end{array}$$

16

15

$$X \oplus Y \rightarrow \textcircled{4}$$

14 (C)

13 (A)

$$(A + B)(A + \bar{C})(\bar{B} + \bar{C})$$

$$= (\bar{C} + A\bar{B})(\bar{A} + B)$$

$$= \bar{A}\bar{C} + B\bar{C}$$

$$= \bar{C}(\bar{A} + B)$$

11 C,D

10

9 D

8 A,C

7 (b)

6 (a)

Digital circuit



Combinational circuit

→ Present O/P depends on only present I/P

→ NO feedback

→ NO Memory

Ex: H.A

F.A जैसा

MUX

DeMUX

Sequential circuit

Present O/P

→ Present I/P.
Previous
Present O/P.

Feedback

Memory

Ex: flip-flop

Registers

Counters

- * Combinational circuit :→
- Procedure To Design Combinational circuit :→
- 1) Identify inputs and outputs.
- 2) Construct truth table.
- 3) Write logical expression in SOP or POS.
- 4) Minimize logical expression.
- 5) Implement Logic circuit.

⇒ Arithmetic circuit

1) Half Adder :→

A	B	H.A.	Sum (Σ)	Carry (C)
0	0		0	0

Truth table:-

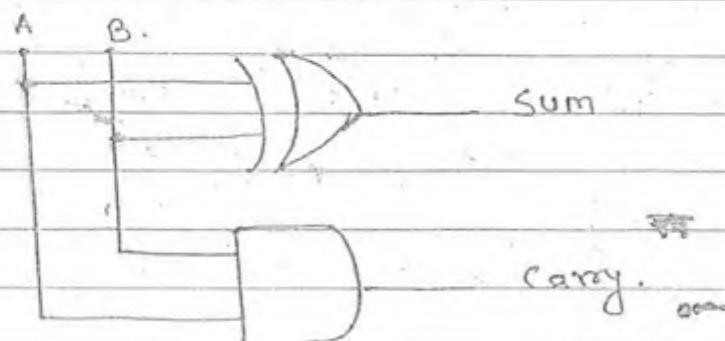
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

→ Logical Expression:-

$$\text{Sum} = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Carry} = AB$$

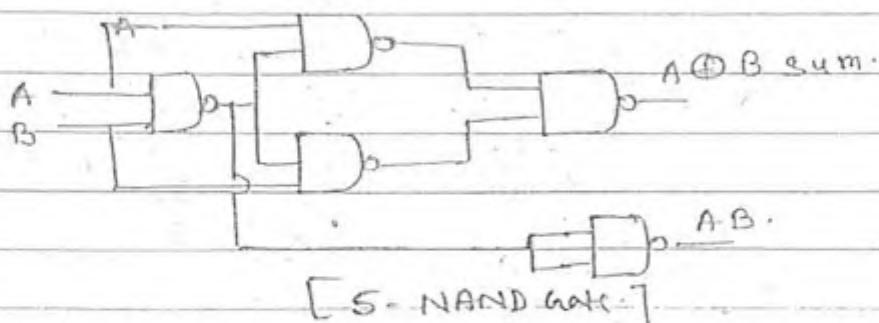
→ Implement :-



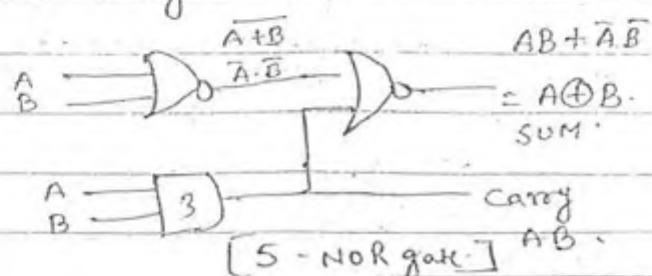
- 1) Logical Expression of SUM
- 2) Logical expression of Carry
- 3) Minimum no. of NAND. (5)
- 4) Minimum no of NOR (5)
- 5) No. of MUX
- 6) No. of Deodors.

Q. Implement HA into NAND gate

SOL Half Adder using NAND :-



Half Adder using NOR:-



2. Half Subtractor :-

A	H.S.	Difference
B		Borrow
0	0	0
0	1	1
1	0	1
1	1	0

→ Truth table

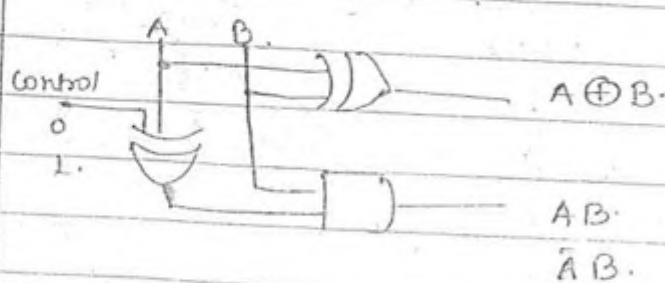
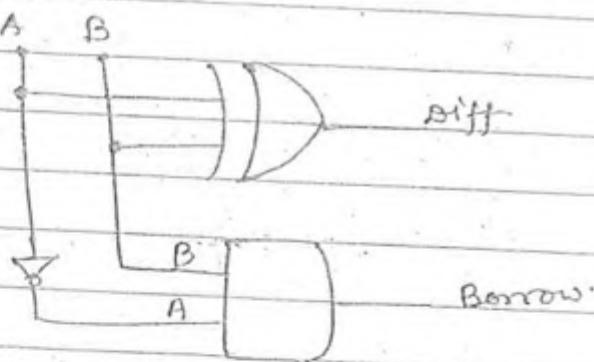
A	B	Diff(A-B)	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

→ Logical Expression:-

$$\text{Difference} = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$

→ Implement:-



Control=0 → Half Adder.

Control=1 → Half Subtractor.

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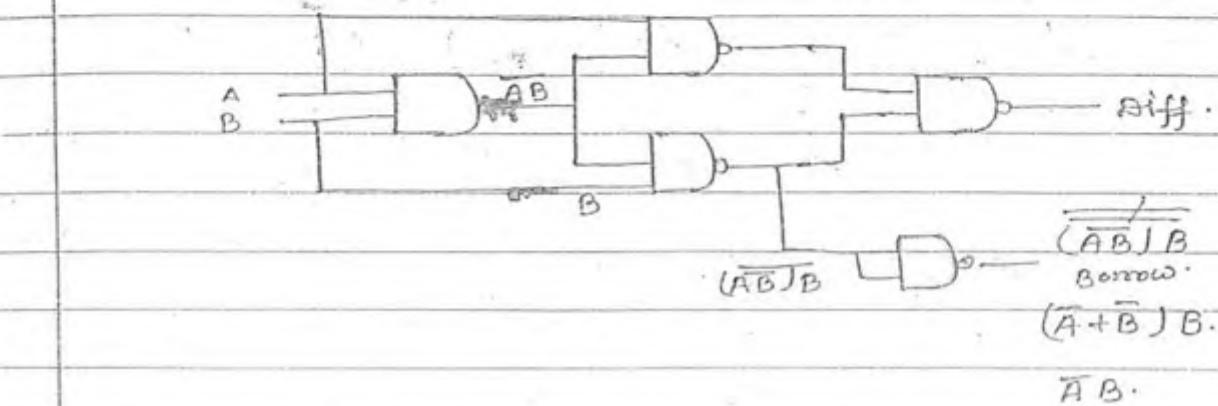
→ No. of NAND gate. ⑤

→ No. of NOR gate ⑥

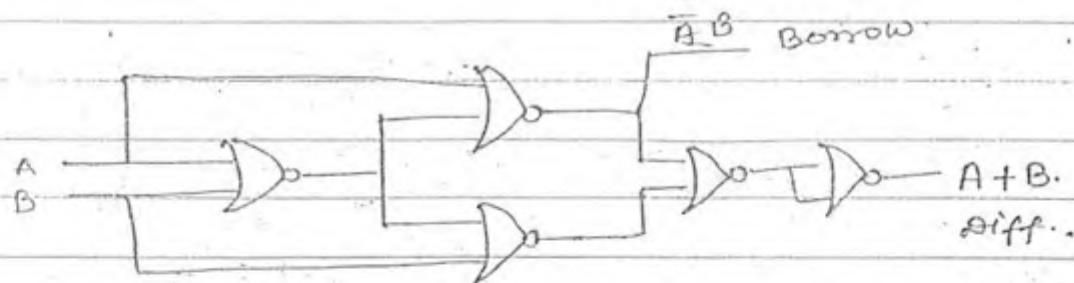
→ No. of MUX

→ No. of Decoder.

→ Implementation of Half Subtractor using NAND gate:-

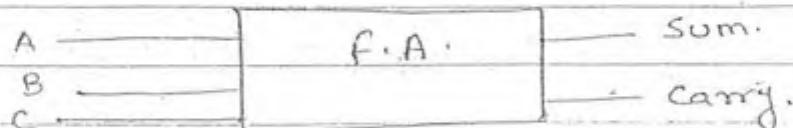


→ Implementation of Half Subtractor using NOR gate:-



NOR - 5

3) Full Adder :-



→ Truth table .

A	B	C	sum.	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

→ Logical Expression :-

$$\text{SUM} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= A \oplus B \oplus C$$

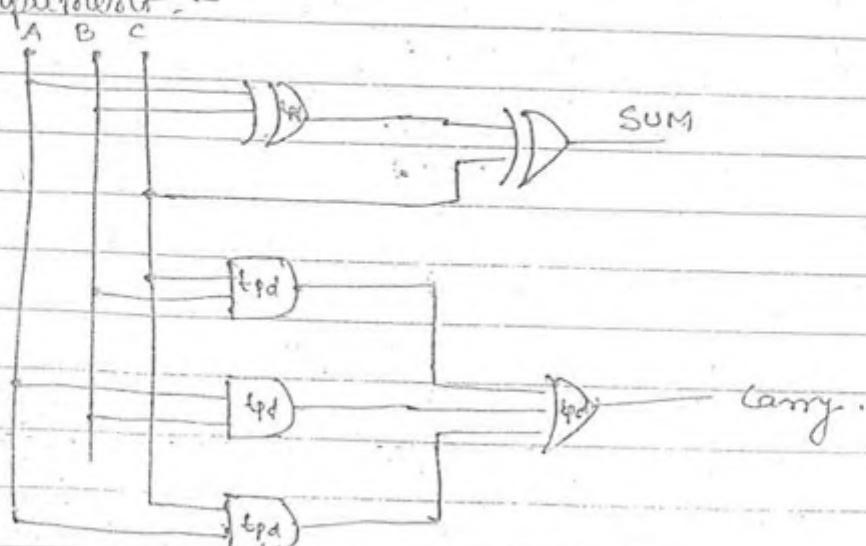
$$= \Sigma m(1, 2, 4, 7)$$

$$\text{Carry} = \underbrace{A\bar{B}C + A\bar{B}\bar{C}}_{1} + \underbrace{AB\bar{C} + ABC}_{1}$$

$$= AB + BC + AC$$

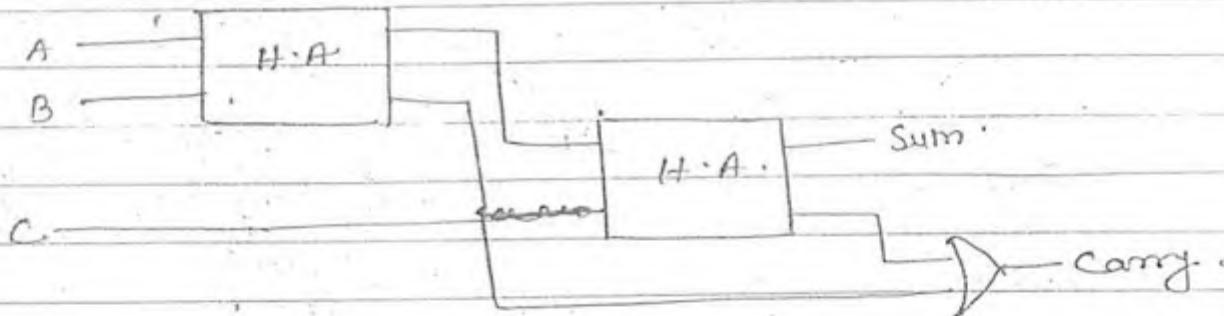
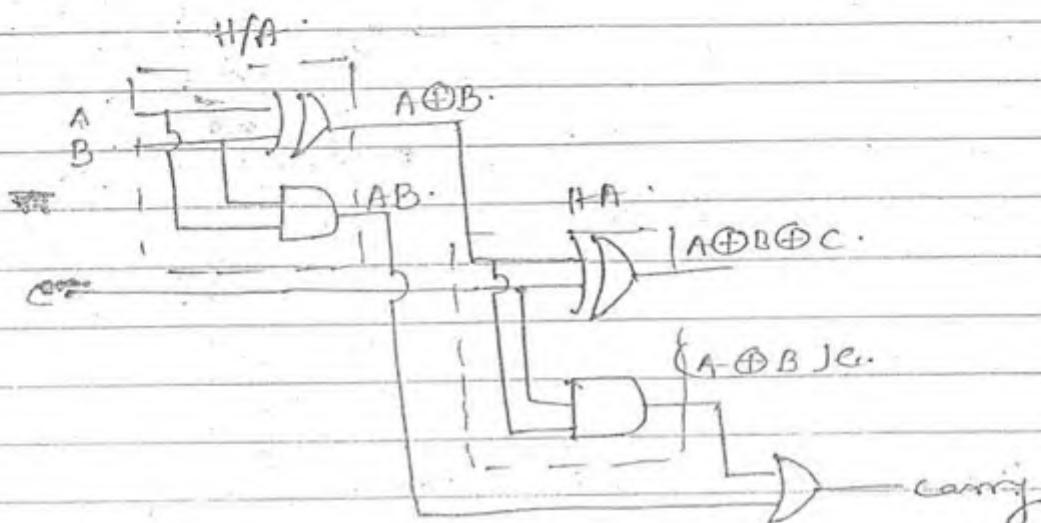
$$= \Sigma m(3, 5, 6)$$

→ Implement :-



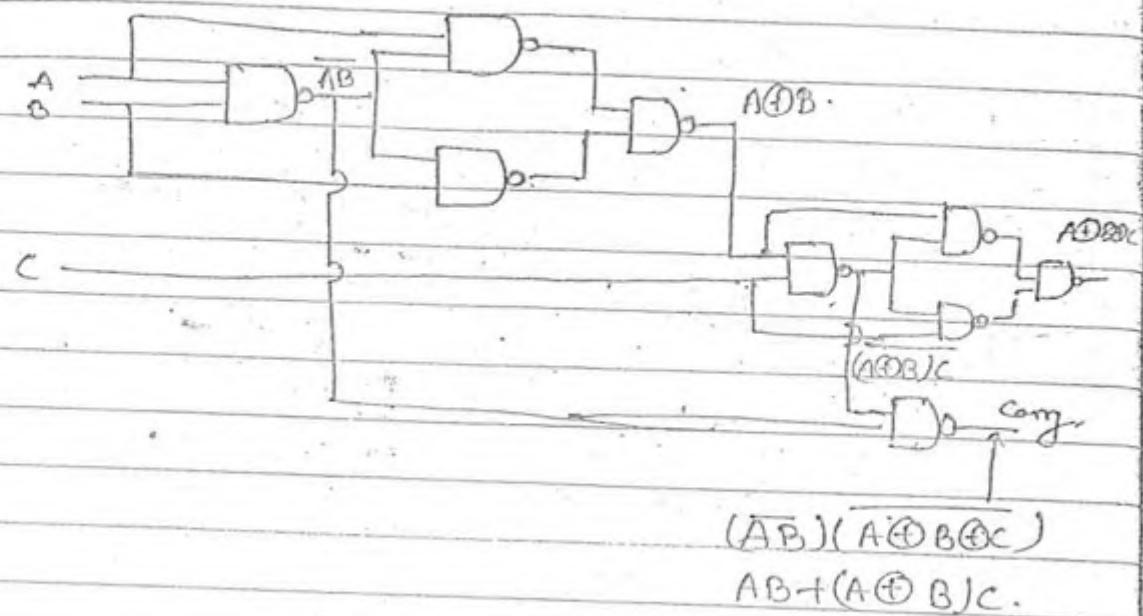
In full Adder each logic gate have propagation delay of t_{pd}
to provide sum or carry O/P it require $2t_{pd}$.

$$\text{Carry} = \bar{A}Bc + A\bar{B}C + A\bar{B}\bar{C} + ABC \\ = \bar{A}B + C(\bar{A}B + A\bar{B})$$

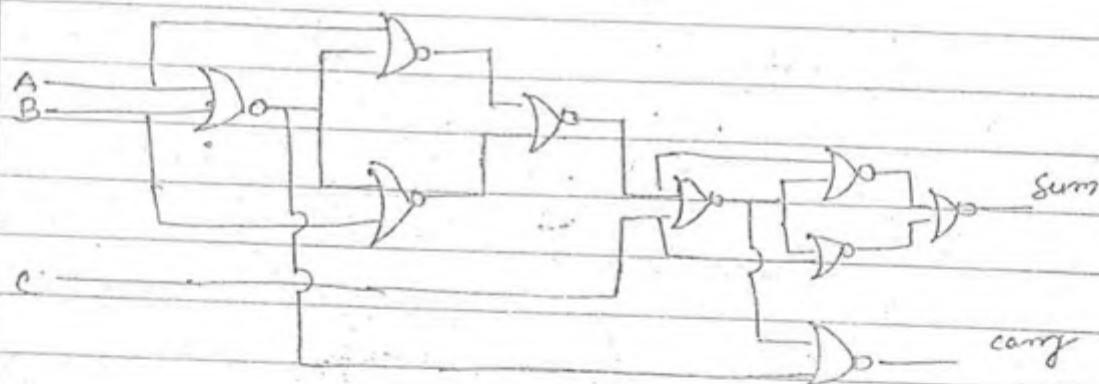


- 1) Logical exp. Sum
- 2) Logical exp. Carry
- 3) No. of HA & OR.
- 4) Minimum no. of NAND. (7)
- 5) Minimum no. of NOR. (7)
- 6) No. of MUX
- 7) No. of DEMUX

Implementation of Full Adder using NAND gates:



Implementation of Full Adder using NOR gates:



⇒ Parallel Adder:

→ In Serial Adder only one full adder is used to add group of bit. It is slowest adder.

1 1 0 1

1 0 1 1

1 1 0 0 0

→ 4 bit → 3FA × 1H.A

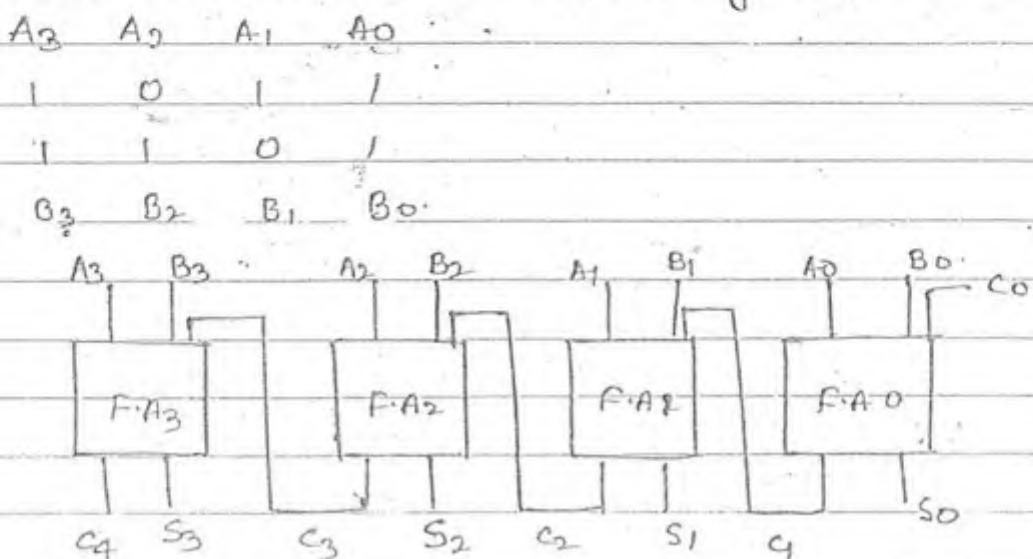
4 F · A

7 H · A

Parallel Adder is used to add group of bits:

To add two n-bit numbers it requires $(n-1)$ Full Adder and one Half Adder or n Full Adder or $(2n-1)$ HA & $(n-1)$ OR gates.

→ 4 bit Parallel Adder :→ [Ripple carry Adder]



$C_4 \Rightarrow$ Carry:

$S_3, S_2, S_1, S_0 \rightarrow$ Sum.

- In parallel Adder propagation delay travel from LIP to OIP carry hence it is also known as Ripple Carry Adder
- In parallel Adder each full adder provide two logic gate delay.
- In n-bit Parallel Adder to provide final result it required $2n$ tpd.

W/B
250¹¹

1 add → 100 ns.

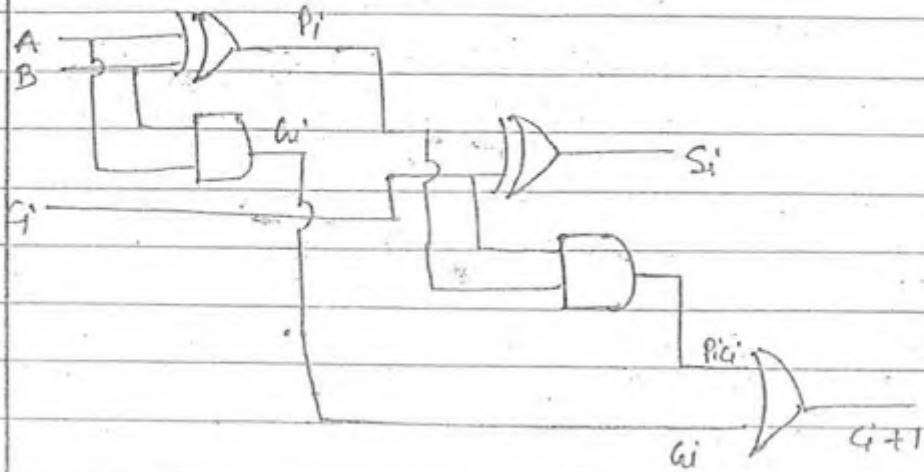
$$18 \rightarrow \frac{1}{100 \times 10^9} = 10^7 \text{ add.}$$

→ Disadvantages :→

→ Carry propagation delay will present as no if bit is increased speed of operation is reduced to avoid this

Look ahead carry adder is used.

→ Look Ahead Carry Adder : →



where P_i = Propagation.

G_i = Generation term.

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

$$S_i = P_i \oplus G_i$$

$$A_3 \quad A_2 \quad A_1 \quad A_0$$

$$B_3 \quad B_2 \quad B_1 \quad B_0$$

$$C_{i+1} = P_i G_i + G_i \rightarrow \text{Look ahead carry generation equation.}$$

→ 4-bit Look Ahead Carry Adder : →

$$P_0 = A_0 \oplus B_0 \quad G_0 = A_0 B_0 \quad S_0 = P_0 \oplus G_0$$

$$P_1 = A_1 \oplus B_1 \quad G_1 = A_1 B_1 \quad S_1 = P_1 \oplus G_1$$

$$P_2 = A_2 \oplus B_2 \quad G_2 = A_2 B_2 \quad S_2 = P_2 \oplus G_2$$

$$P_3 = A_3 \oplus B_3 \quad G_3 = A_3 B_3 \quad S_3 = P_3 \oplus G_3$$

C₀ → Input Carry.

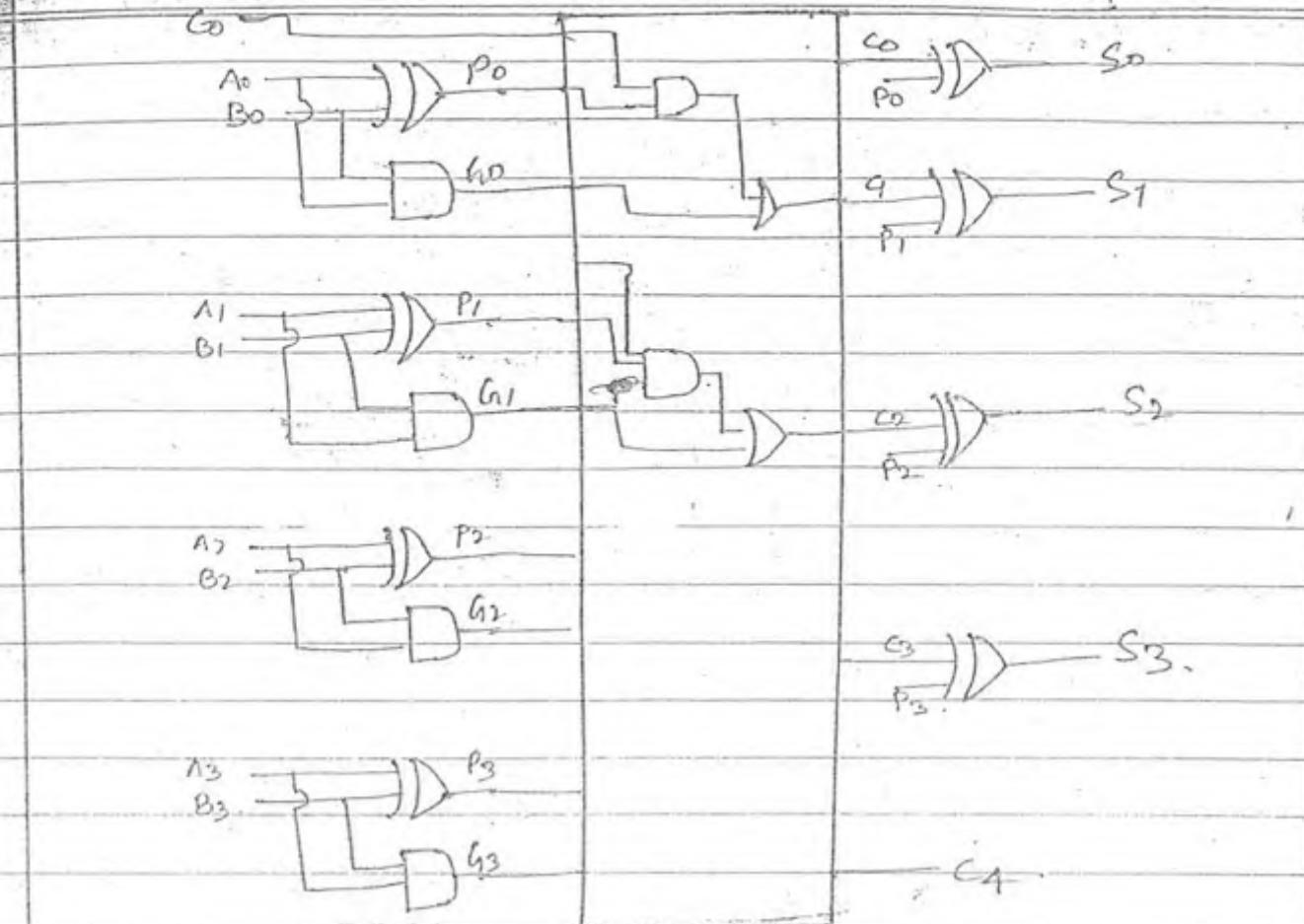
$$C_1 = P_0 G_0 + G_0$$

$$C_2 = P_1 C_1 + G_1 = P_0 C_0 + P_1 G_0 + G_1$$

$$C_3 = P_2 C_2 + G_2 = P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$$

$$C_4 = P_3 C_3 + G_3$$

$$= P_3 P_2 P_1 P_0 C_0 + P_3 P_2 P_1 P_0 G_0 + P_3 P_2 G_1 + P_3 G_2 + G_3$$



In look ahead carry adder to provide carry o/p it requires three logic gates.

To provide sum o/p it require 4 logic gates.

Carry ckt is implemented with two level AND-OR gate.

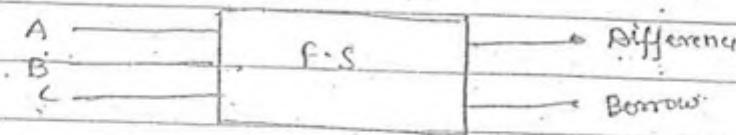
No. of AND gate required in carry ckt = $n \left(\frac{n+1}{2} \right)$

No of OR gate required in carry ckt = n.

$$5) c \text{ duty cycle} = \frac{t_{on}}{t} \times 100$$

$$= \frac{1.7 - 0.4}{2.2 - 0.4} \times 100 = 32\%$$

\rightarrow Full Subtractor :-



\rightarrow Truth table :-

A	B	C	Sig	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

\rightarrow Logic Expression .

$$\text{Difference} : - A \oplus B \oplus C$$

$$\text{Borrow} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \underbrace{\bar{A}BC}_{1} + A\bar{B}C$$

$$= \bar{A}B(C + \bar{C}) + \bar{A}C(B + \bar{B} + BC(A + \bar{A}))$$

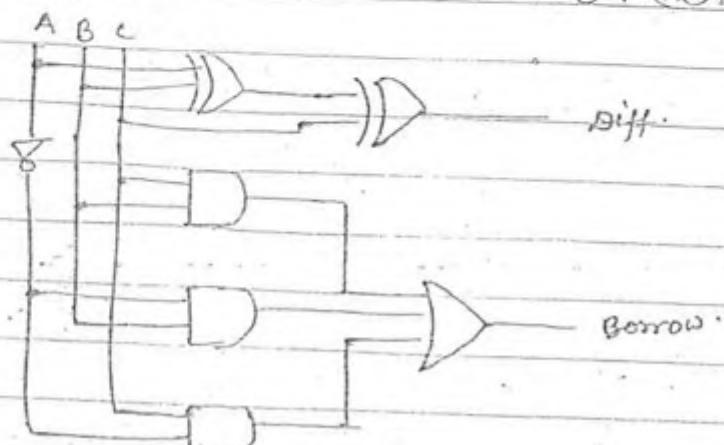
$$= \bar{A}B + \bar{A}C + BC$$

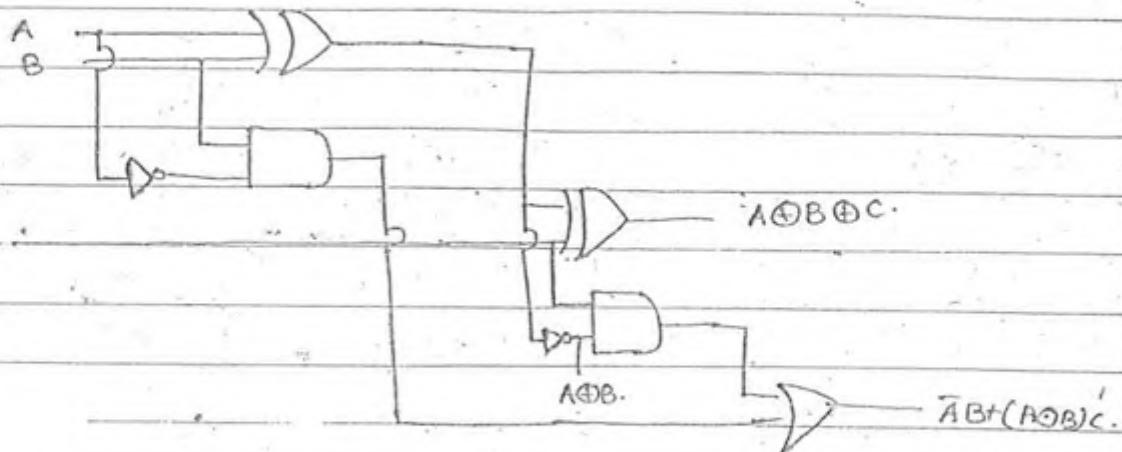
$$= \sum m(1, 2, 3, 7)$$

$$\Rightarrow \bar{A}B[C + \bar{C}] + [\bar{A}\bar{B} + AB]C$$

$$\bar{A}B + (A \oplus B)C$$

\rightarrow Implement :-



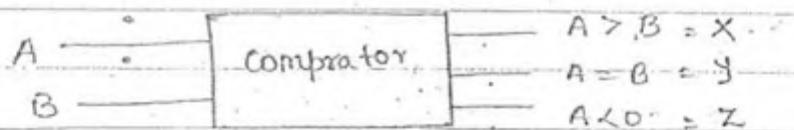


F.S \rightarrow 2 H.S and 1 O.R.

NAND - 9

NOR \rightarrow 9.

★ Comparator \rightarrow



\rightarrow Truth table:-

A	B	X (A > B)	Y (A = B)	Z (A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

\rightarrow Logic Expression :-

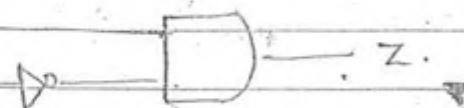
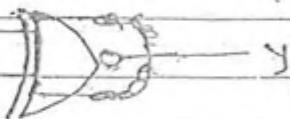
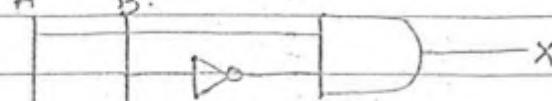
$$X = A\bar{B}$$

$$Y = \bar{A}\bar{B} + AB$$

$$Z = \bar{A}B$$

Implement \rightarrow

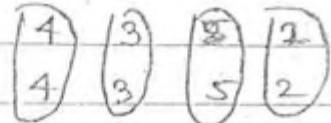
A B.



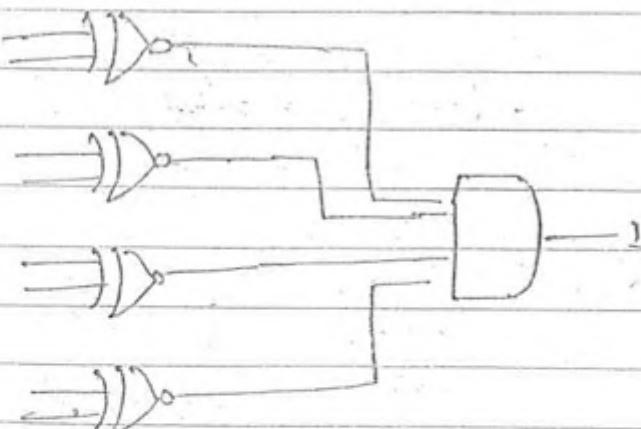
* 4 bit Comparator \rightarrow

$A_3 \ A_2 \ A_1 \ A_0 \rightarrow A$

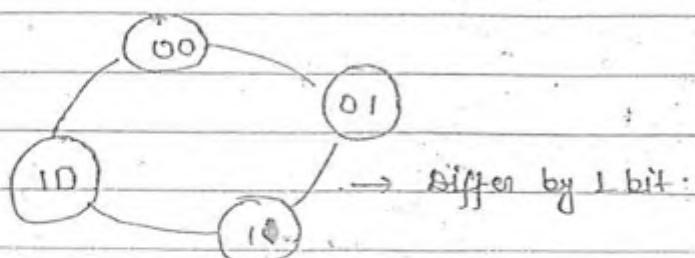
$B_3 \ A_2 \ B_1 \ B_0 \rightarrow B$



$$(A_3 \odot B_3) \cdot (A_2 \odot B_2) \cdot (A_1 \odot B_1) \cdot (A_0 \odot B_0).$$



A) K-Map : →



In K-map gray code representation is used.

→ 2 Variable K-map :-

		B	0	1
		A	0	1
		0	00	01
		1	10	11

→ 3-Variable K-map :-

		BC				
		00	01	101	10	
		0	0	1	3	2
		1	4	5	7	6
		c	c	c	c	c
		c	c	c	c	c

→ four-variable K-map :-

		CD				
		00	01	11	10	
		00	0	1	3	2
		01	4	5	7	6
		11	12	13	15	14
		10	8	9	11	10

→ SOP :-

$$f(A, B) = \sum m(0, 2, 3)$$

A	B	0	1
0	0	0	1
1	1	1	1

$$A + B$$

$$\text{Q. } f(A, B) = \sum m(1, 2, 3)$$

A	B	0	1
0	0	0	1
1	1	0	1

$$A + B$$

$$\text{Q. } f(A, B) = \sum m(0, 1, 2, 3)$$

A	B	0	1
0	0	1	1
1	1	1	1

$$A + B$$

$$\text{Q. } f(A, B) = \sum m(1, 3) + \sum d(2)$$

A	B	0	1
0	0	0	1
1	1	2X	3

$$\text{Q. } f(A, B) = \sum m(0, 3) + \sum d(2)$$

A	B	0	1
0	1	0	1
1	X	1	1

$$A + \bar{B}$$

Q

$$f(A, B) =$$

1	X
X	1

$$\Rightarrow 1$$

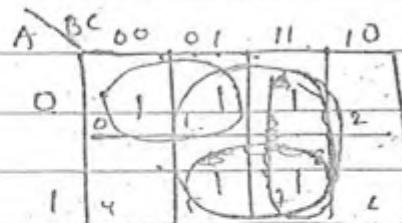
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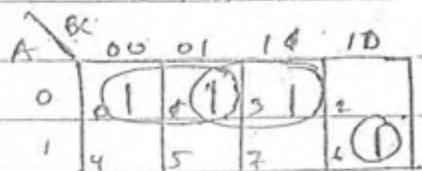
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$$\textcircled{Q} \quad f(A, B, C) = \Sigma m(0, 1, 3, 5, 7)$$



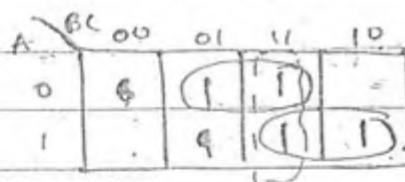
$$C + \bar{A}\bar{B}$$

$$\textcircled{Q} \quad f(A, B, C) = \Sigma m(0, 1, 3, 6)$$



$$\bar{A}\bar{B} + \bar{A}C + AB\bar{C}$$

$$\textcircled{Q} \quad f(A, B, C) = \Sigma m(1, 3, 6, 7)$$

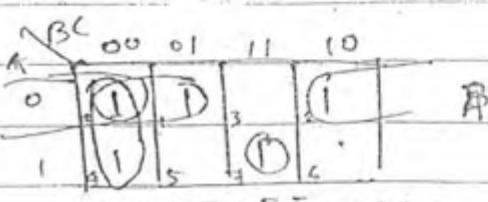


$$\bar{A}B + AB + \bar{B}C \xrightarrow{x} \text{Redundant.}$$

* Procedure to draw K-map:-

- 1) Octets
- 2) Squads
- 3) Pairs Pairs
- 4) Single term.
- 5) Remove redundant

$$\textcircled{Q} \quad f(A, B, C) = \Sigma m(1, 2, 4, 7)$$



$$\bar{A}\bar{B} + \bar{B}C + \bar{A}C + ABC$$

DATE :

Q. $f(A, B, C) = \sum m(0, 1, 5, 6, 7)$

		BC		A		m	
		00	01	11	10		
A	0	1	1	X	X		
	1	X	1	X	1		

$$AB + \bar{A}\bar{B} + AC$$

Note: $AB + \bar{A}\bar{B} + \bar{B}C$

→ K-map provides minimize expression but not necessarily unique

Q. $f(A, B, C) = \sum m(0, 1, 2, 5, 7) + \sum d(3, 6)$

		BC		A		m	
		00	01	11	10		
A	0	1	1	X	D		
	1	X	1	1	X		

$$\bar{A} + C$$

Q. $f(A, B, C) = \sum m(0, 1, 6, 7) + \sum d(3, 5)$

		BC		A		m	
		00	01	11	10		
A	0	1	1	X	1		
	1	X	1	1	1		

$$\bar{A}\bar{B} + A\bar{B}$$

Q. $f(A, B, C) = \sum m(0, 1, 6, 7) + \sum d(3, 4, 5)$

$$A + \bar{B}$$

		BC		A		m	
		00	01	11	10		
A	0	1	1	X	1		
	1	X	1	1	1		

Q. $f(A, B, C, D) = \sum m(0, 1, 3, 5, 7, 8, 9, 11, 13, 15)$

COMBINE

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AB	CD	00	01	11	10
00	01	11	31	2	
01	4	51	71	6	
11	12	13	151	14	
10	8	191	111	10	

$$D + \bar{B}C$$

Q. $f(A, B, C, D) = \sum m(0, 1, 4, 5, 8, 9, 13, 15)$

AB	CD	00	01	11	10
00	01	1	1		
01	1	1			
11	1	1	1		
10	1	1	1		

$$\bar{A}\bar{C} + \bar{B}\bar{C} + ABD$$

Q.

AB	CD	00	01	11	10
00	01	1			
01	1	1	1		
11		1	1	1	
10		1			

4-pair \rightarrow ⑤ one

Q.

~~WY~~ ~~XZ~~

①			①
.	K	.	
.	K	①	①

→ POS :-

Q) $f(A, B) = \pi M(0, 2, 3)$

A	B	0	1
A	0	0	0
A	1	0	0

Q) $f(A, B) = \pi M(0, 3) + \pi d(1)$

A	B	0	X
A	1	0	0

$$A \cdot \bar{B}$$

Q) $f(A, B, C) = \pi M(0, 1, 3, 5, 7)$

A	BC	$\bar{B}C$	$B\bar{C}$	$B\bar{C}$	$\bar{B}\bar{C}$
0	00	00	01	11	10
1	.	.	00	01	.

$$\bar{C} \cdot (A+B)$$

Q) for the given K-map minimised POS expression.

A	B	00	01	11	10
0	0	0	X	0	X
1	0	0	0	X	X

$$(B+C)(\bar{B}+\bar{C})$$

Q.

1	1		1
1		1	

1	1		1
1		1	

$$x = y$$

1	1	1	
1		1	

$$z = x$$

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$\bar{P}Q$	$\bar{R}\bar{S}$	$\bar{R}S$	RS	$R\bar{S}$			
$\bar{P}\bar{Q}$		1	1	1		1	
$\bar{P}Q$	1	1	1	1		q	
$P\bar{Q}$		1	1	1		1	
PQ			1	1		1	

111

X

	1	1	1
1	1	1	1
	1	1	1
000	1	1	

Z

$$W = Z$$

$$W = \bar{X}$$

$$Z = \bar{X}$$

A B Y

0 0 0

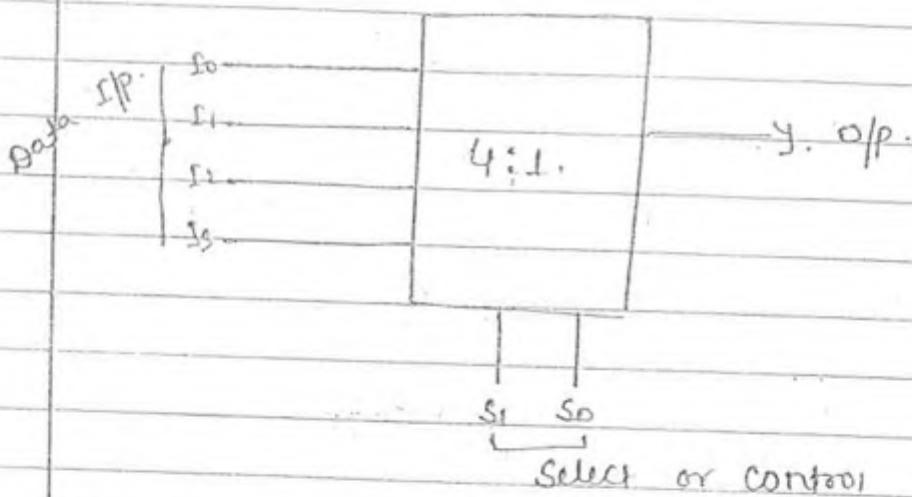
0 1 1

1 0 0

1 1 0

$$\begin{aligned}
 Y &= \bar{A}\bar{B}\cdot 0 + \bar{A}B\cdot 1 + A\bar{B}\cdot 0 + AB\cdot 1 \\
 &= \bar{A}B + ABC \\
 &= B(\bar{A} + AC) \\
 &= B(\bar{A} + C)
 \end{aligned}$$

* Multiplexer :-



It is a combinational CKT which have many data I/P and single O/P depending on control or select I/P one of the I/P transfer to the O/P.

→ Control or Select :-

- 1) Data Selector
- 2) Many to one CKT
- 3) Universal logic CKT
- 4) Parallel to serial

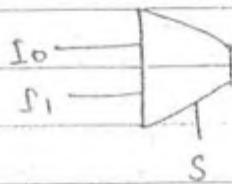
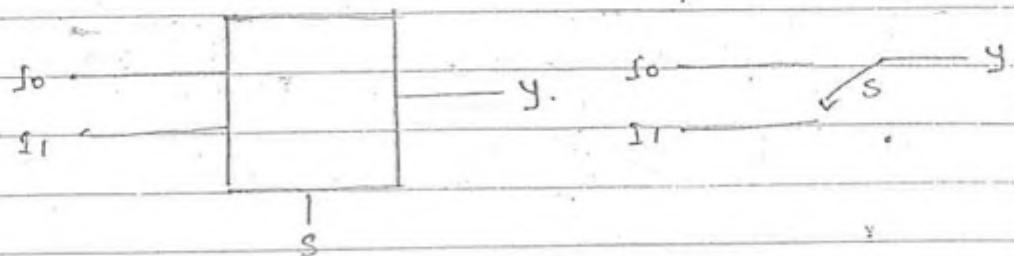
$$m = 2^n$$

$$n = \log_2 m$$

where,

 $M = \text{no. of data SLP}$ $n = \text{Select SLP}$

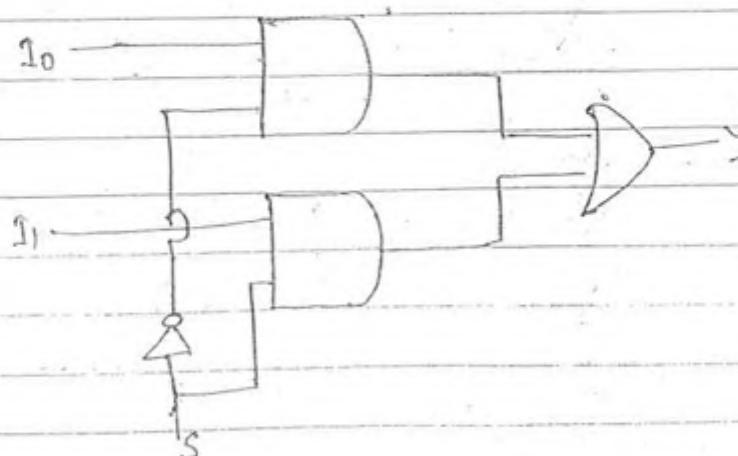
$\Rightarrow 2:1$ Multiplexer : \rightarrow



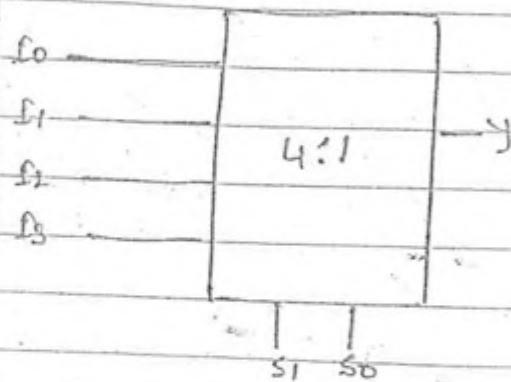
\rightarrow Truth table.

S	Y
0	I0
1	I1

$$Y = \bar{S}I_0 + S I_1$$



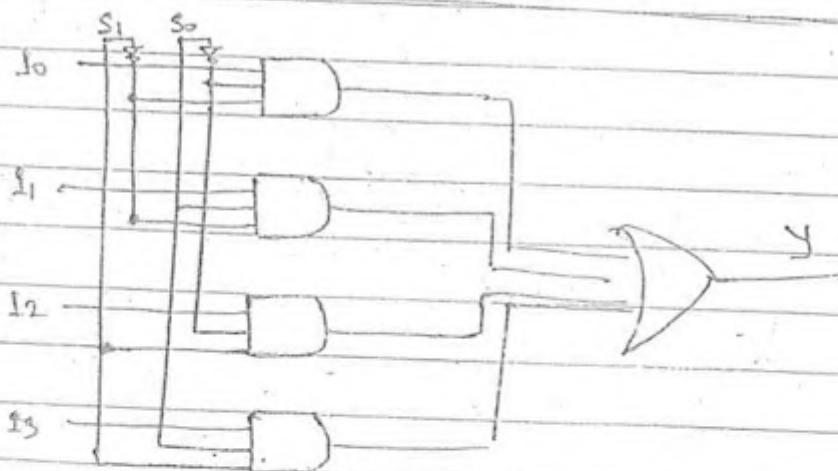
→ 4:1 Multiplexer :-



→ Truth table:-

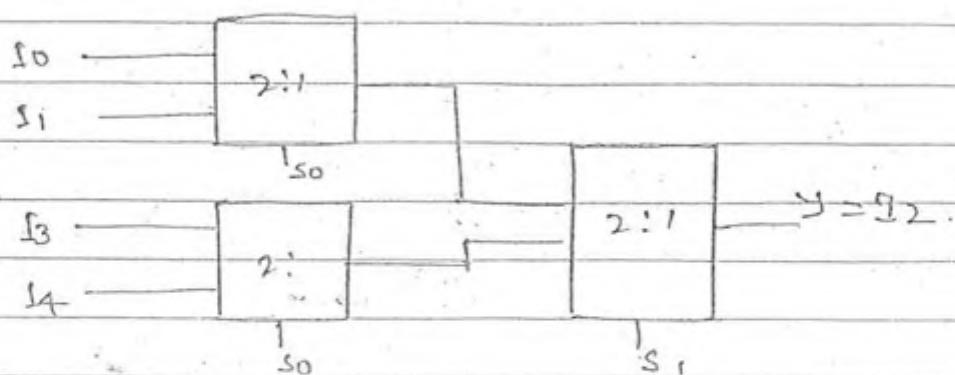
S ₁	S ₀	Y
0	0	I ₀
0	1	I ₁
1	0	I ₂
1	1	I ₃

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$



→ Implementation of Higher Order MUX With Lower Order:-

$$1) 4 \times 1 \xrightarrow{3} 2 \times 1$$



2) ~~Dependence~~ $8 \times 1 \longrightarrow 2 \times 1$
 $4 + 2 + 1 = 7$

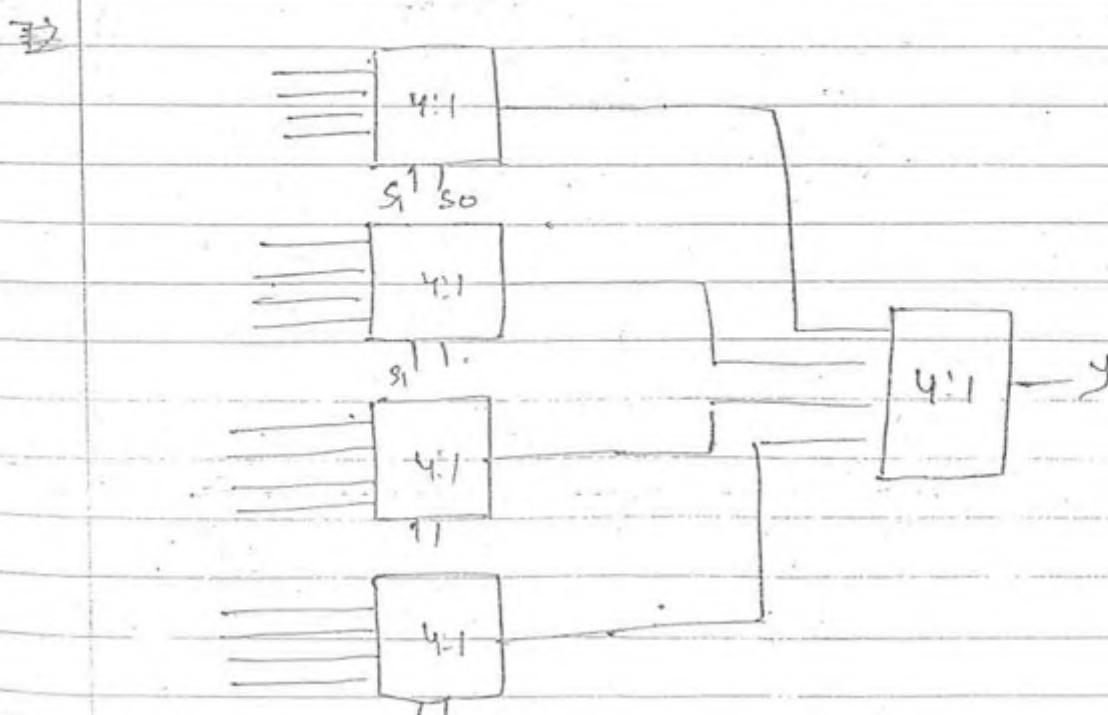
3) $16 \times 1 \longrightarrow 2 \times 1$
 $8 + 4 + 2 + 1 = 15$

4) $64 \times 1 \longrightarrow 2 \times 1$
 63

5) $256 \times 1 \longrightarrow 2 \times 1$
 255

$2^n \times 1 \longrightarrow 2 \times 1$
 $2^n - 1$

6) $16 \times 1 \longrightarrow 4 \times 1$
 $4 + 1 = 5$



$$7 \quad 64 \times 1 \longrightarrow 4 \times 1$$

$$16+4+1 = 21$$

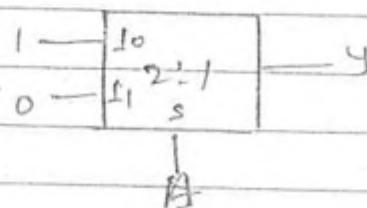
$$8 \quad 64 \times 1 \longrightarrow 8 \times 1$$

$$8+1 = 9$$

$$9 \quad 256 \times 1 \longrightarrow 16 \times 1$$

$$16+1 = 17$$

\Rightarrow Multiplexer As Universal :-



$$Y = \bar{S}I_0 + S\bar{I}_1$$

$$= \bar{A} \cdot 1 + A \cdot 0$$

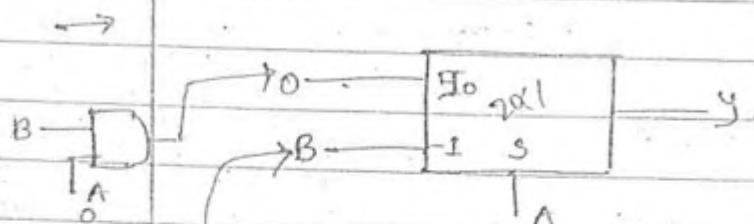
$$= \bar{A}$$

1 NOT gate required

$$A \quad Y$$

$$0 \rightarrow 1$$

$$1 \rightarrow 0$$

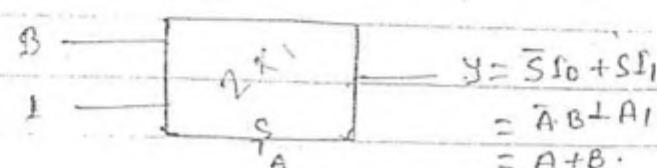


$$Y = \bar{S}I_0 + S\bar{I}_1$$

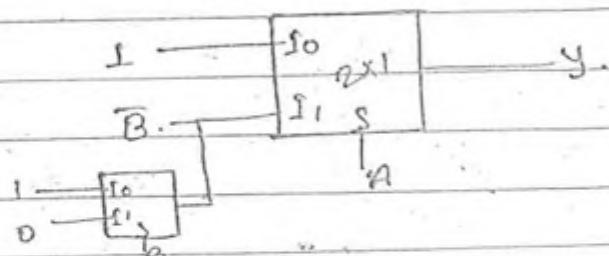
$$= \bar{A} \cdot 0 + A \cdot B$$

$$= AB.$$

Q) Implement OR using 2:1 Mux.

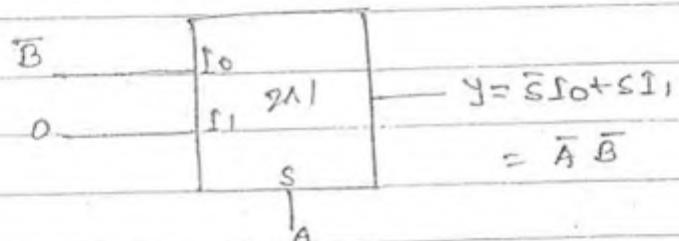


Q) Implement NAND gate using 2x1 MUX.

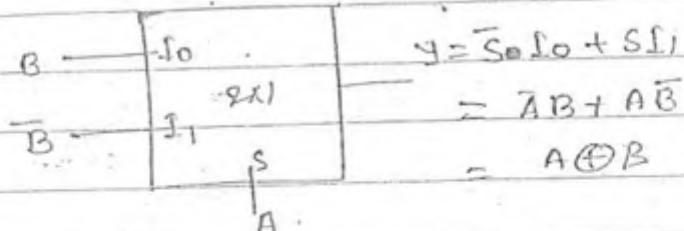


$$\begin{aligned} Y &= \bar{S}.I_0 + S\bar{I}_1 \\ &= \bar{A}.I + A\bar{B} \\ &= \bar{A} + \bar{B} \\ &= \bar{AB} \end{aligned}$$

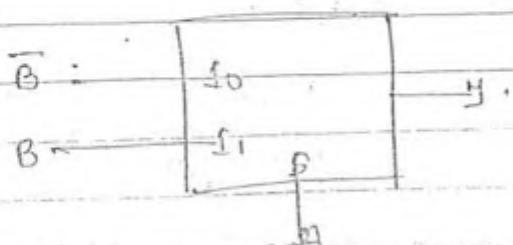
NOR :-



EXOR :-



EXNOR :-



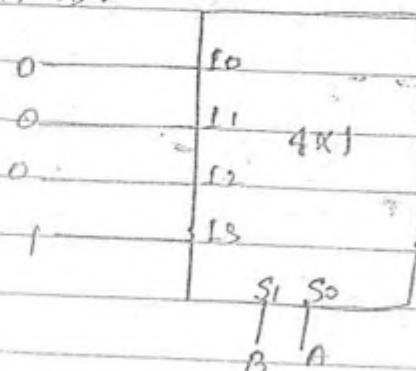
Note:-

NOT, AND, OR \rightarrow Require $\Rightarrow 1$ 2x1 MUX.

$$\begin{array}{l} H \cdot A \\ H \cdot S \end{array} \quad \begin{array}{c} 3 \\ \hline 3 \end{array} \quad 2 \times 1$$

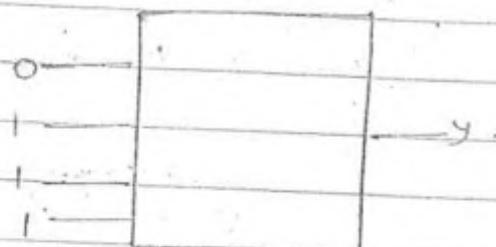
\Rightarrow 4:1 MUX :-

\rightarrow AND :-



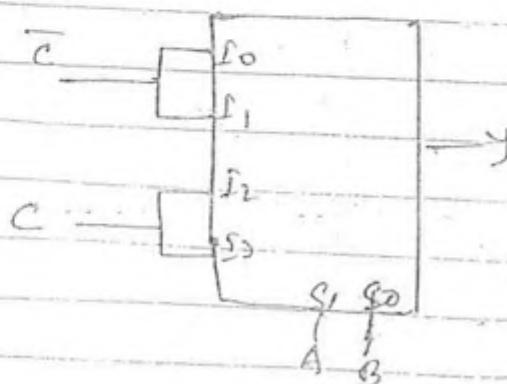
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

\rightarrow OR :-



\Rightarrow Determine minimised logical Expression :-

- Q. For the given 4×1 Mux minimised logical expression is



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$$\begin{aligned}
 Y &= \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3 \\
 &= \bar{A} \bar{B} \bar{C} + \bar{A} B \bar{C} + A \bar{B} C + ABC \\
 &= \bar{A} \bar{C} (B + \bar{B}) + AC (B + \bar{B}) \\
 &= \bar{A} \bar{C} + AC \\
 &= A \oplus C
 \end{aligned}$$

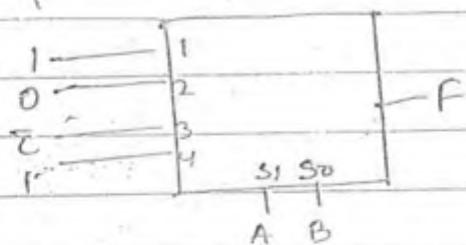
Q

			C
1			$A \oplus C$
0			
1			
	$S_1 \bar{S}_0$		
	1 1		
	A B		

$$\begin{aligned}
 Y &= \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3 \\
 &= \bar{A} \bar{B} \bar{C} + \bar{A} B \cdot 1 + A \bar{B} \cdot 1 + ABC \\
 &= \bar{A} \bar{B} C + \bar{A} \cdot B (C + \bar{C}) + A \bar{B} \bar{C} \\
 &= \underbrace{\bar{A} \bar{B} C}_{\bar{A} \bar{C}} + \underbrace{\bar{A} B C}_{ABC} + \underbrace{\bar{A} \bar{B} \bar{C}}_{AC} + \underbrace{A \bar{B} \bar{C}}_{B \bar{C}}
 \end{aligned}$$

⇒ Implementation of Given logical Expression:

Q Implement, $f(A, B) = \Sigma m(0, 1, 4, 6, 7)$ using 4×1 shown in fig.



Sol:

A B C

6 0 0 0 $\rightarrow \bar{C}$ 1 0 0 1 $\rightarrow C$ 2 0 1 0 $\rightarrow \bar{C}$ 3 0 1 1 $\rightarrow C$ 4 1 0 0 $\rightarrow \bar{C}$ 5 1 0 1 $\rightarrow C$ 6 1 1 0 $\rightarrow \bar{C}$ 7 1 1 1 $\rightarrow C$

I ₀	I ₁	I ₂	I ₃
1	0	1	1

\bar{C}	\oplus	2	4
1	1	3	7

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

1	0	\bar{C}	1
---	---	-----------	---

Q) Implement a logic expression.

$$f(A, B, C) = \Sigma m(1, 2, 3, 5, 6, 7)$$

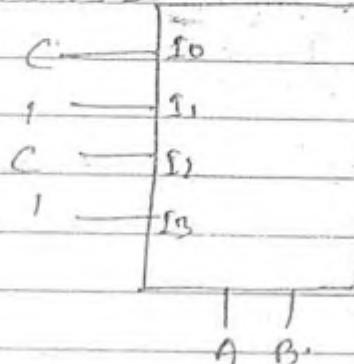
i) AB as select

ii) AC as select

iii) BC as select

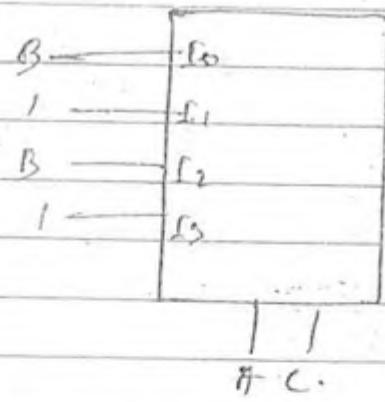
Sol:

i) AB as Select



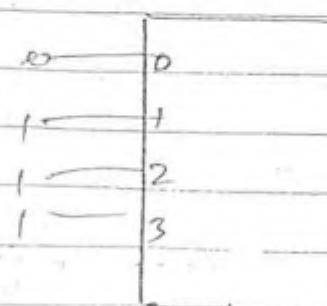
	s_0	s_1	s_2	s_3
\bar{C}	0	2	4	6
C	1	3	5	7
C	1	1	1	1

ii) AC as Select



	s_0	s_1	s_2	s_3
\bar{B}	0	1	4	5
B	2	3	6	7
B	1	1	1	1
A	0	0	0	\bar{B}
\bar{A}	0	1	\bar{B}	\bar{B}
\bar{A}	0	0	0	\bar{B}
\bar{A}	0	1	\bar{B}	\bar{B}

iii) BC as select :-



A	1	0	0	\bar{B}
\bar{A}	1	0	1	\bar{B}
A	1	1	0	B
\bar{A}	1	0	1	B

	s_0	s_1	s_2	s_3
0	0	1	2	3
4	5	6	7	8
0	1	1	1	1

using one 4×1 MUX any two variable function, some of three variable function can be implemented.

using one 4×1 MUX ^{& one NOT}, all two variable function, all three variable function can be implemented.

one 4×1 & one NOT

All two

one 8×1

All Three

Some Four

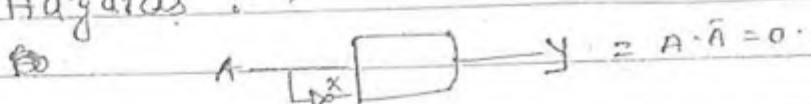
one 8×1 & one NOT

All Three

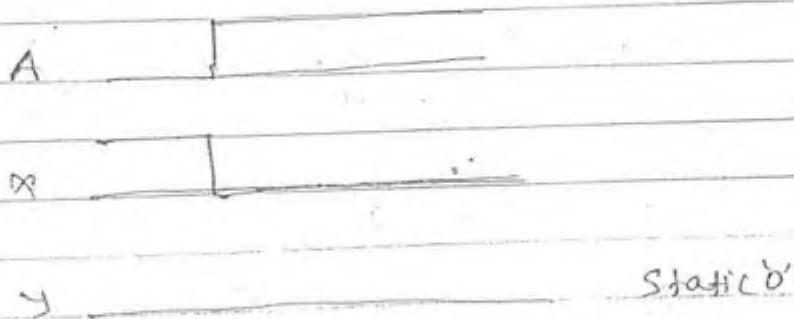
All Four

Q) Implement

* Hazards :-



Case I for the given CKT determine O/P Waveform when there is no propagation delay.



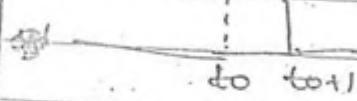
Case II

Determine O/P waveform for the given fig if there is a propagation delay of 1ns in NOT gate & no propagation delay in AND

Sol:



B



do to+1

y' AND(1ns)

Static '0' Hazard

1

Y AND(0ns) < -2ns →

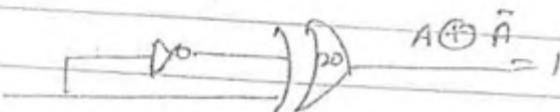
t0+2 t0+3

100

$$t_1 = t_0 + 10\text{ns}$$

$$t_2 = t_0 + 20\text{ns}$$

$$t_3 = t_0 + 30\text{ns}$$



$$A \oplus \bar{A} = 1$$

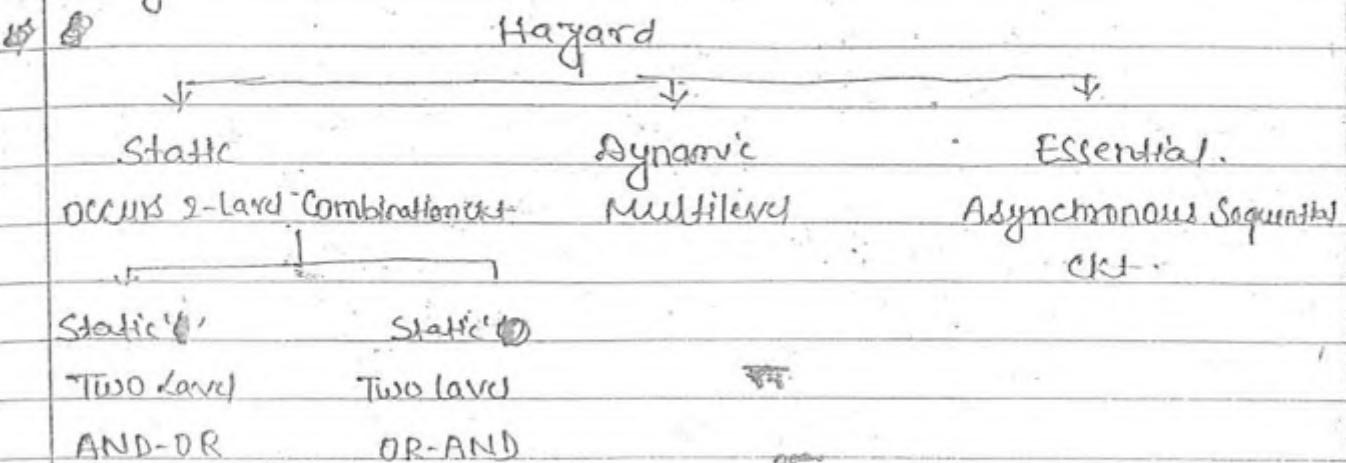
A

t+1

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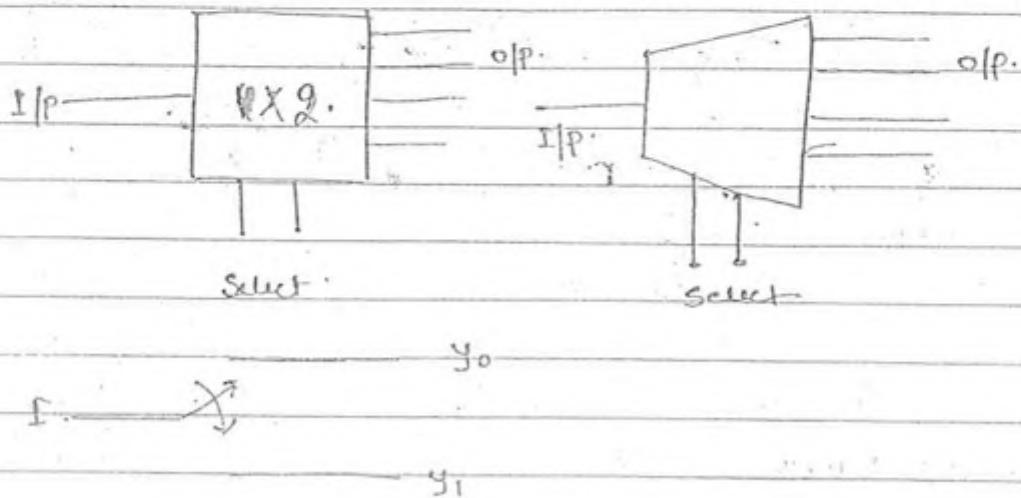
- ⇒ Hazards are unwanted change in the O/P due to propagation delay.



To avoid static and dynamic hazard, redundant terms are added in the combinational circuit.

\rightarrow DeMux :-

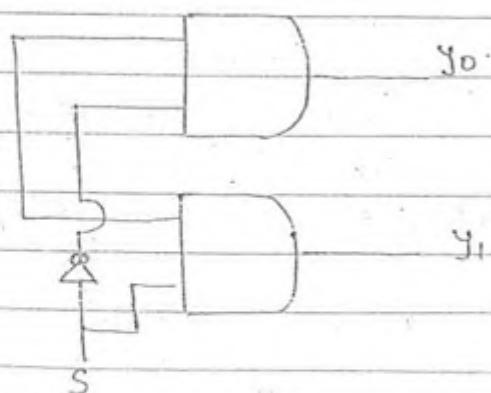
Demux is a combinational ckt which have one I/P and many O/Ps. O/P depends upon selector I/P & control I/P is transferred to one of the many O/P.



\rightarrow Truth table :-

S	Y ₁	Y ₀
0	0	1
1	1	0

\rightarrow Implement :-

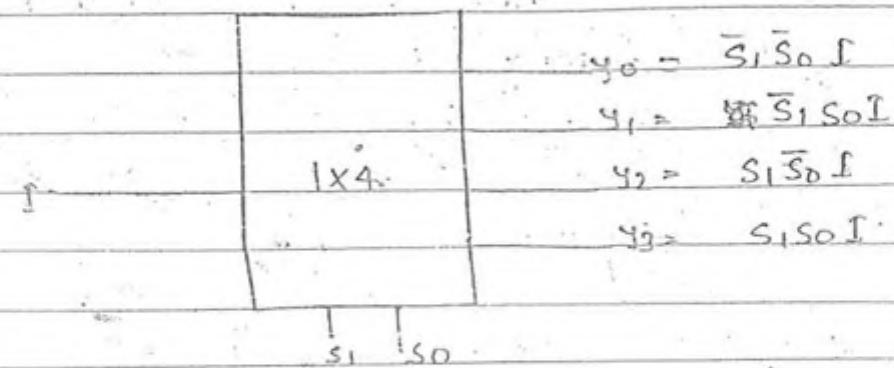


We can not use Demux as universal ckt.

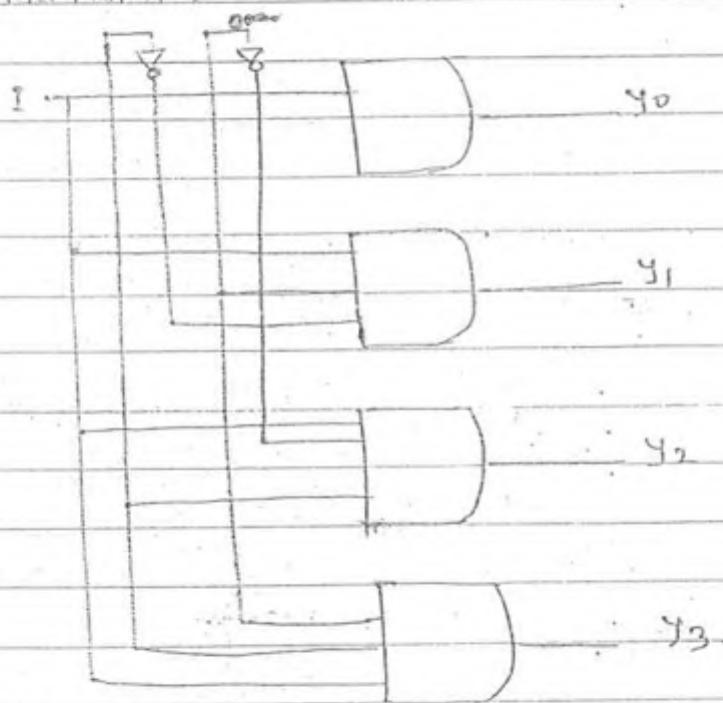
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→ 1 : 4 Demux :-



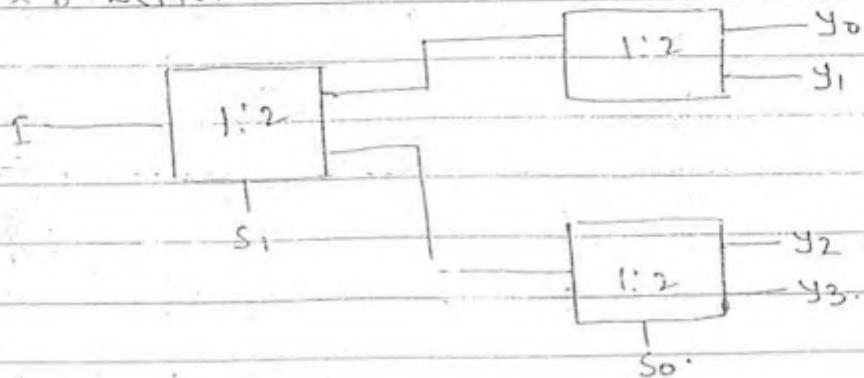
→ Implementation :-



→ 1 X 4 DEMUX $\frac{3}{3}$ 1 X 2

4 X 1 DEMUX $\frac{3}{3}$ 2 X 1

1 X 8 DEMUX $\frac{7}{7}$ 1 X 2



\star Decoder :-

- Decoder is a combinational circuit which have many I/P and many O/P.
- It is used to convert binary data into other code

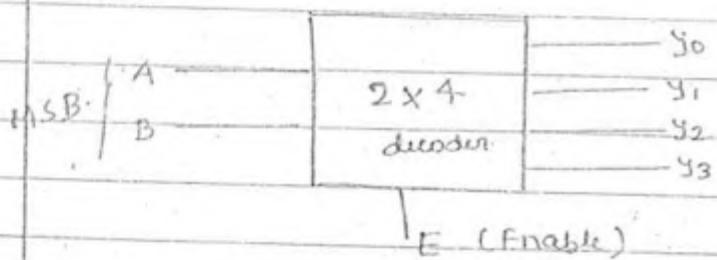
Binary to Octal

BCD to Decimal

Binary to Hexa

BCD to Seven Segment

Minimum Possible Decoder:-



→ Truth table:-

F	A	B	y_3	y_2	y_1	y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

$$y_0 = \bar{A}BE$$

$$y_1 = \bar{A}\bar{B}E$$

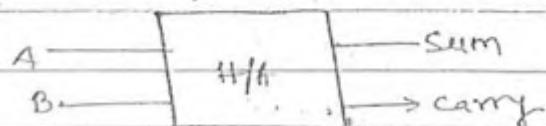
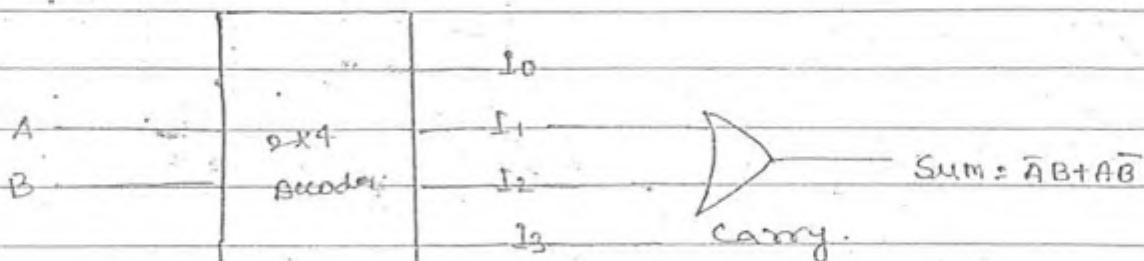
$$y_2 = A\bar{B}E$$

$$y_3 = ABE$$

→ Decoder and Demux internal ckt outline same

Q Implement HA using 2x4 decoder.

Sol:

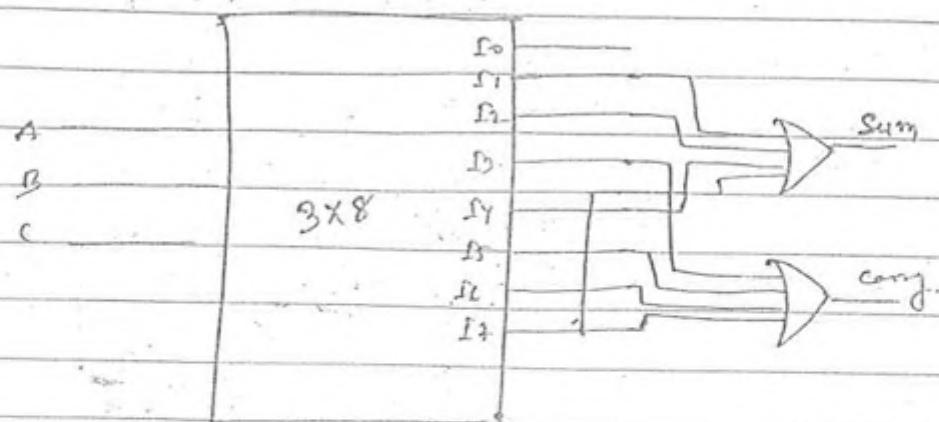


→ 3x8 Decoder (Binary to Octal Decoder): -

(MS.B)		Binary to Octal decoder	A	$\bar{A}\bar{B}C$
A		y ₀		$\bar{A}\bar{B}C$
B		y ₁		$\bar{A}BC$
C		y ₂		$\bar{A}B\bar{C}$
		y ₃		$\bar{A}BC$
		y ₄		$A\bar{B}C$
		y ₅		$A\bar{B}\bar{C}$
		y ₆		ABC
		y ₇		$A\bar{B}C$

→ Implement Full Adder: -

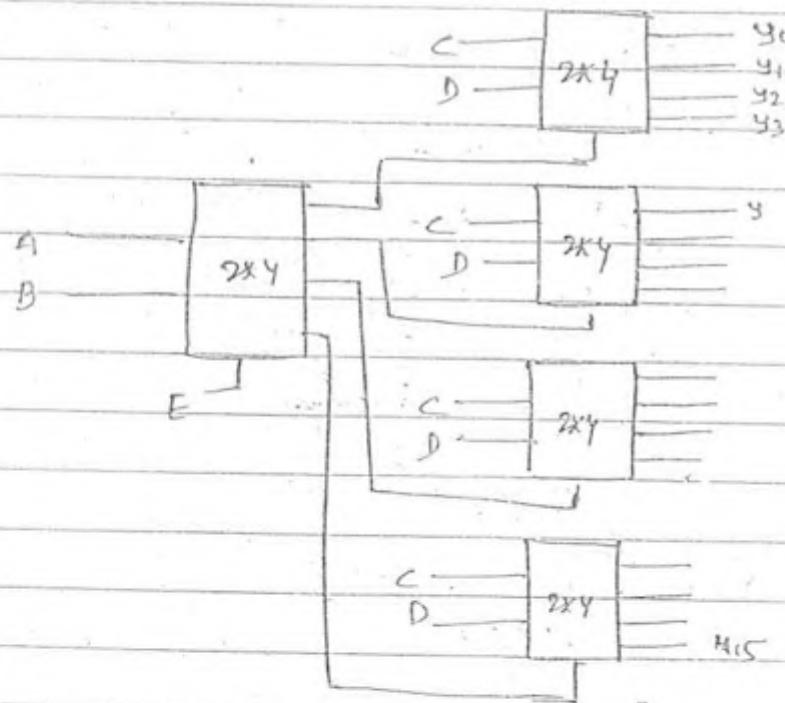
$$\begin{array}{|c|c|} \hline & \text{F.A.} \\ \hline \end{array} \quad \begin{aligned} \text{sum} &= \sum m(1, 2, 4, 7) \\ \text{carry} &= \sum m(3, 5, 6, 7) \end{aligned}$$



→ Implementation of higher order to lower order \Rightarrow

$$4 \times 16 \quad 5 \quad 2 \times 4$$

$$\begin{array}{c} 1 \times 16 \text{ Biner} \\ 16 \times 1 \end{array} \xrightarrow{5} \begin{array}{c} 1 \times 4 \text{ Biner} \\ 4 \times 1 \end{array}$$

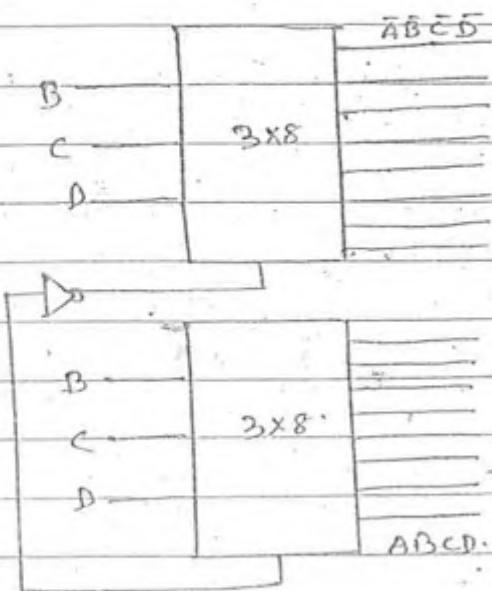


To implement

$$6 \times 64 \xrightarrow[1+4+16]{21} 2 \times 4$$

$$8 \times 256 \xrightarrow{\quad} 4 \times 16$$

→ Implement 4×16 Decoder using 3:8 decoder : →

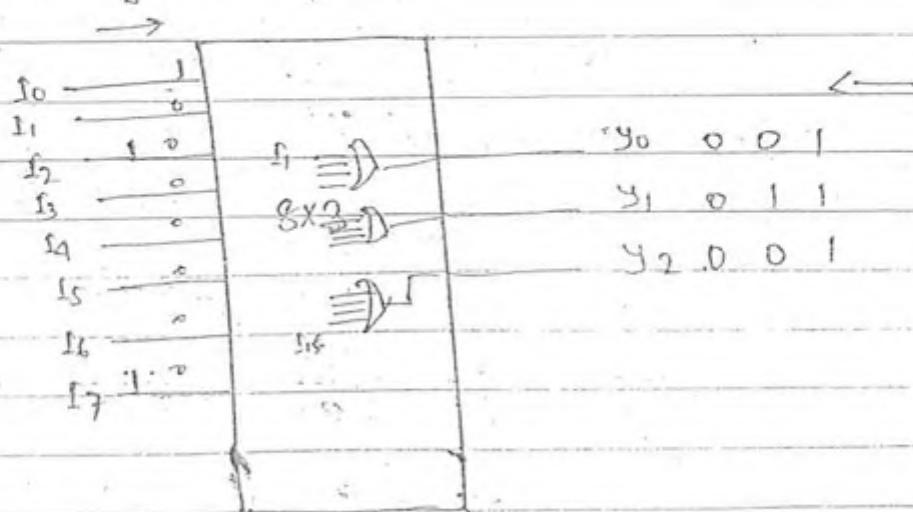


[2, 3x8 decoder, 1 NOT]

* Encoder : →

- It is combinational ckt which have many I/P & many O/P.
- It is used to convert other codes to binary.
- * Octal to binary conversion
- * Decimal to BCD
- * Hex to Binary.

1 Octal to Binary Encoder:



- In normal encoder one of I/P is high and corresponding O/P is available at O/P.
- In priority encoder, no. of I/P is high only highest priority corresponding binary is available at O/P.
- Truth table :-

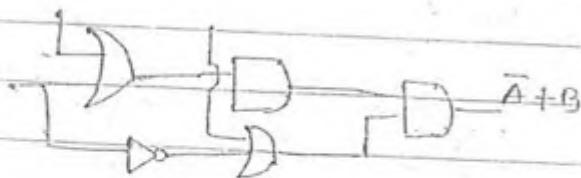
I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	y_2, y_1, y_0
0	0	0	0	0	0	0	1	0 0 0 0
0	0	0	0	0	0	1	0	0 0 ① 1
0	0	0	0	0	1	0	0	0 ① 0 2
0	0	0	0	1	0	0	0	0 ① 3
0	0	0	1	0	0	0	0	1 0 0 4
0	0	1	0	0	0	0	0	1 0 ① 5
0	1	0	0	0	0	0	0	1 ① 0 6
1	0	0	0	0	0	0	0	1 ① ① 7

$$y_0 = I_1 + I_3 + I_5 + I_7$$

$$y_1 = I_2 + I_3 + I_6 + I_7$$

$$y_2 = I_4 + I_5 + I_6 + I_7$$

प्र० 15

W.B. (d) 2) (a) 3) (b) 4) (b) 5) $\bar{x}+y+z$, 6) c 8) (a)9) (d) 10) 12) c 13) (b) 14) (b) 15) 16) (A) $I_1=1, I_2=0$.

17) (d) 18) c

Sequential Circuit

- * flip-flop: →
 - i) it is a basic memory element
 - ii) FF can store 1 bit
 - iii) FF have two o/p which are complementary to each other.
 - iv) FF have two stable state hence it is known as bistable multivibrator.

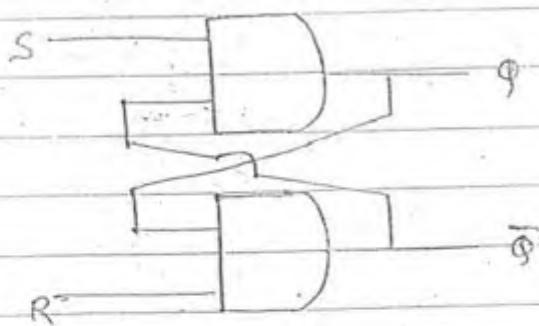
* S-R Latch \rightarrow NAND
 NOR

* SR FF	CKT
* JK FF	
* D FF	
* T FF	

Truth table
 Characteristic table
 Characteristic equation
 Excitation table.

- * conversion from one FF to other
- * Sample circuit

I SR Latch Using NAND Gate: →



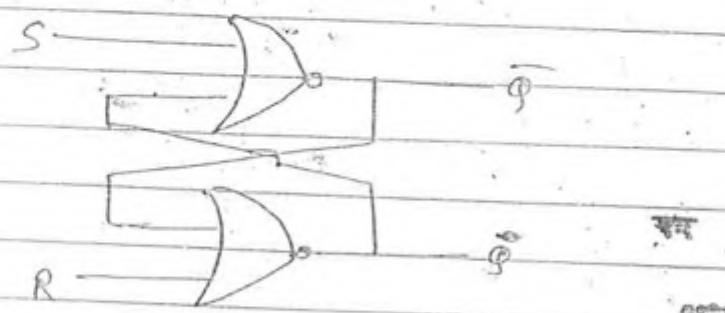
A	B	Y	S	R	Q
0	0	1	0	0	Invalid ($Q \cdot \bar{Q} = 1$)
0	1	1	0	1	1
1	0	1	1	0	← Previous state ($Q = 1, \bar{Q} = 0$)
1	1	0	1	1	→ $Q = 0 \quad \bar{Q} = 1$

Enable $\rightarrow 1$:

Disable $\rightarrow 0$

In S-R latch, if both gates are enable, O/P remains in previous state and if both are disable the O/P remains in invalid.

2. SR - Latch using NOR gate :-



A B Y S R Q

0 0 1 0 0 Previous State.

0 1 0 0 1 0

1 0 0 1 0 1

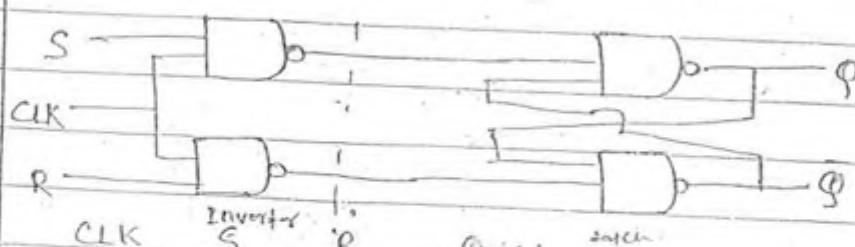
1 1 0 1 1 Invalid.

Enable $\rightarrow 0$

Disable $\rightarrow 1$.

\rightarrow S-R latch is used to eliminate switch bouncing.

3. S-R flip-flop: \rightarrow [using NAND]



0 X X Q_n \Rightarrow HOLD

1 0 0 Q_n \rightarrow Reset

1 0 1 0 \rightarrow Set

1 1 1 Invalid \rightarrow unused

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S R Q_{n+1}

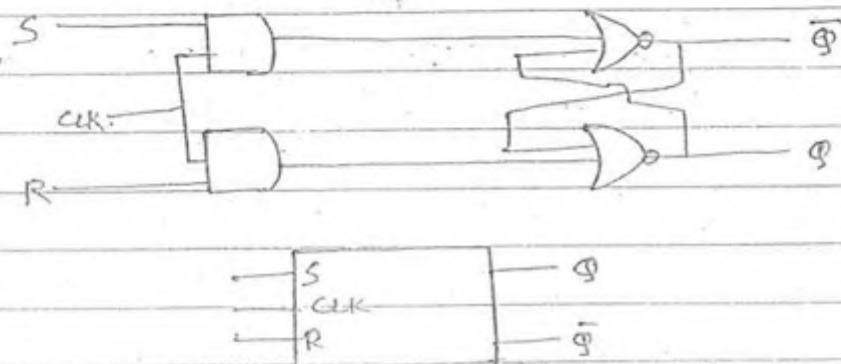
0 0 Q_n

0 1 0

1 0 1

1 1 Invalid

→ 4. S.R Flip-flop using NOR gate :-



→ Characteristic Table :-

	S	R	Q_n	Q_{n+1}
0	0	0	0	0
	0	1	0	1
1	0	1	0	0
	1	1	1	1
X	1	1	0	X
	1	1	1	X

→ Characteristic Equation :-

$$S \quad \overline{R} Q_n \quad \overline{R} \bar{Q}_n \quad \bar{R} Q_n \quad \bar{R} \bar{Q}_n$$

S		-1		
S	1	1	0X	X

$$Q_{n+1} = S + \bar{R} Q_n \quad \& \quad S \cdot R = 0$$

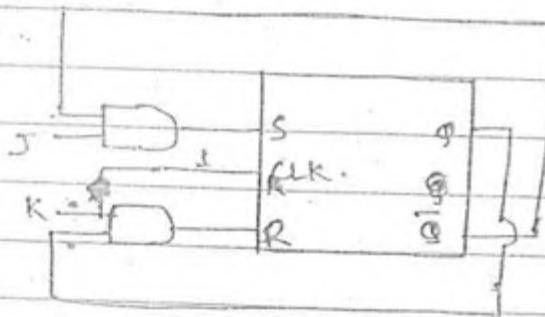
→ Excitation Table:→

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Disadvantage:-

→ Invalid State is present When S & R I/P are 1.
To avoid this J-K Flip-Flop is used.

5 J-K - FLIP-Flop :→



CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Q_n

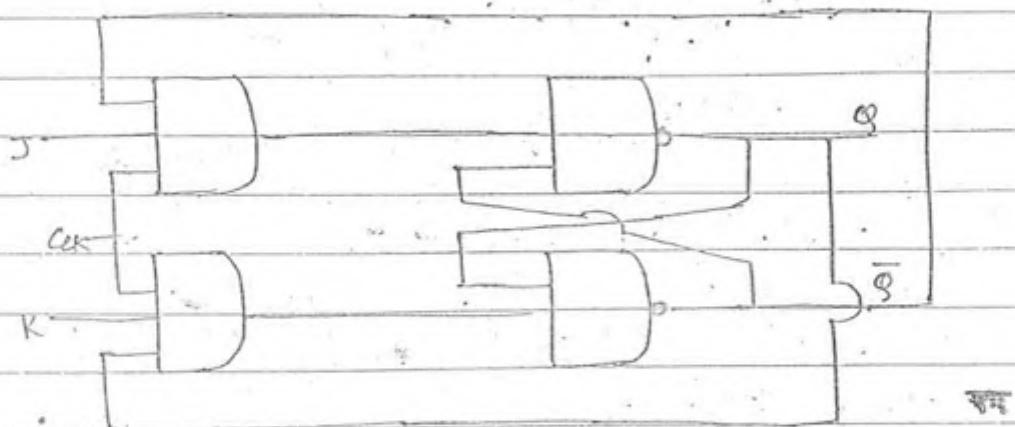
J	K	Q_{n+1}
0	0	$Q_n \rightarrow$ Hold.
0	1	0 \rightarrow Reset
1	0	1 \rightarrow Set
1	1	$\bar{Q}_n \rightarrow$ Toggle.

$S = J\bar{Q}$
$R = KQ$

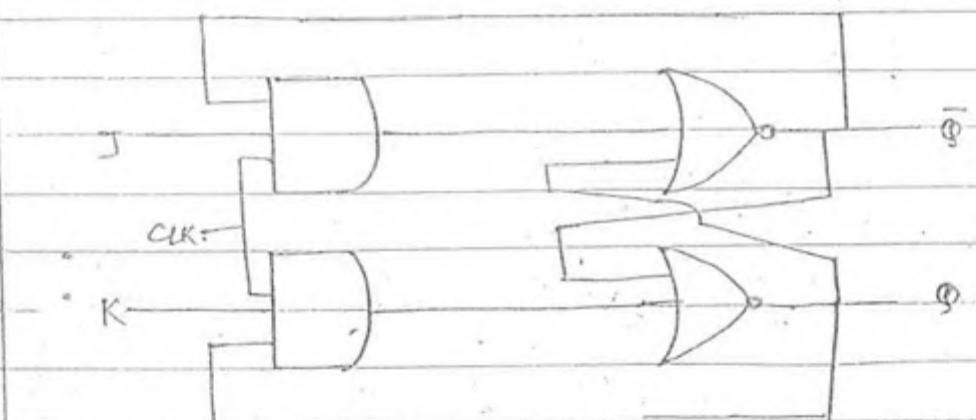
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→ J-K Flip-Flop Using NAND Gate :-



→ J-K Flip-Flop Using NOR Gate :-



→ Characteristic Table (J-K F-F) :-

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

→ Characteristic Equation :-

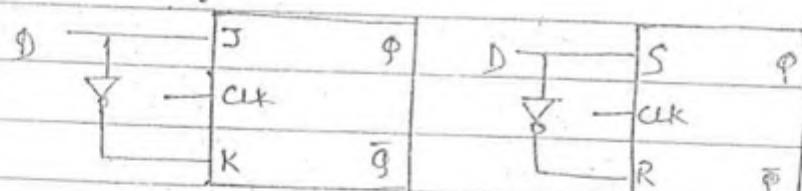
$J \cancel{K\bar{n}}$	$\bar{R}Q_n$	$\bar{K}Q_n$	KQ_n	$\bar{K}\bar{Q}_n$
J		1		
J	1	1		1

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

→ Excitation table :-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

6. D- Flip-Flop :- [Transparent Latch]



$$J = D ; K = \bar{D}$$

$$S = \bar{D} ; R = \bar{\bar{D}}$$

→ Truth table.

CK	D	Q_{n+1}	CK	D	Q_{n+1}
0	X	Q_n	0	0	0
1	0		1	1	
1	1	1			

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→ Characteristic table : →

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

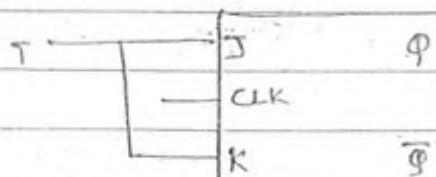
$$\boxed{Q_{n+1} = D}$$

D-flip-flop is also called transparent latch.

→ Excitation table : →

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

7 T-flip-flop : → [Toggle flip-flop]



$$\boxed{J=K=T}$$

CLK	T	Q_{n+1}	T	Q_{n+1}
0	X	Q_n	0	Q_n
1	0	Q_n	1	\bar{Q}_n
1	1	\bar{Q}_n		

→ Characteristic Table :→

	$T \oplus n$	\bar{Q}_{n+1}
Q_n	0 0 0	
	0 1 1	
\bar{Q}_n	1 0 1	
	1 1 0	

$$\bar{Q}_{n+1} = \bar{T}Q_n + T\bar{Q}_n = T \oplus Q_n$$

→ Excitation table :→

Q_n	Q_{n+1}	T
0 → 0	0	
0 → 1	1	
1 → 0	1	
1 → 1	0	

NOTE! —

	J	K	Q_{n+1}
S-R	0 0	0	Q_n
	0 1	0	$\rightarrow D\text{-F.F.}$
	1 0	1	
	1 1	\bar{Q}_n	

Therefore J-K F.F is a universal F.F.

Excitation Table:-

Q_n	Q_{n+1}	S	R	J	K	D	T
0	0	0	x	0	x	0	0
0	1	1	0	1	x	1	1
1	0	x	1	x	1	0	1
1	1	x	0	x	0	1	0

→ Characteristic Equation:

$$Q_{n+1} = S + \bar{R}Q_n$$

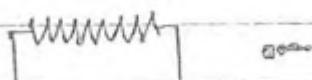
$$Q_{n+1} = \bar{S}\bar{Q}_n + \bar{R}Q_n$$

$$Q_{n+1} = D$$

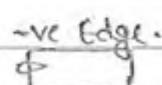
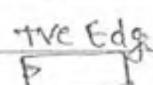
$$Q_{n+1} = T \oplus Q_n$$

Trigger
Up

Level trigger



Edge Trigger.

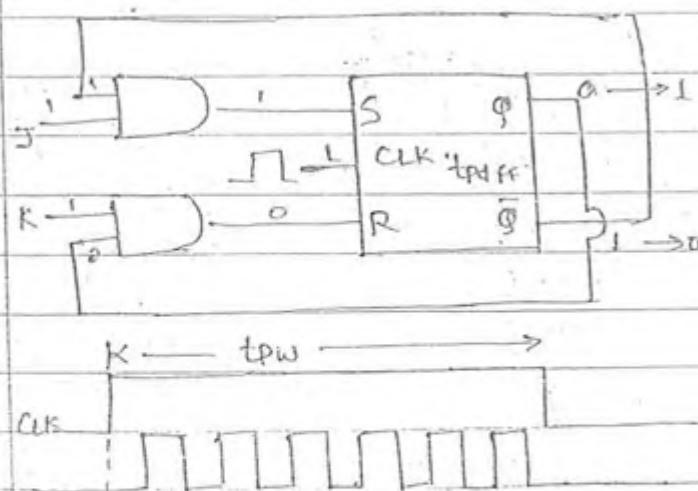


$0 \rightarrow 1$

$1 \rightarrow 0$

- In level triggered ckt of P may change many times in single CLK
- In edge triggered ckt of P will change only once in single CLK.

* Race-Around condition



$tpdff \ll tpw$

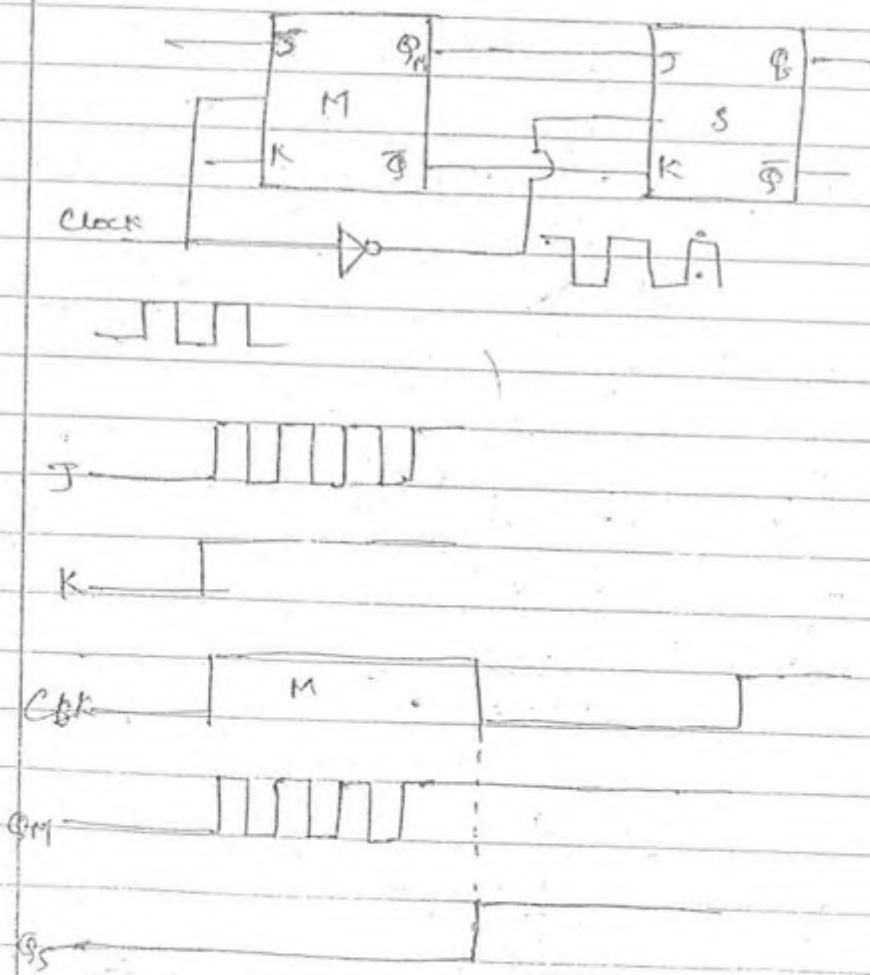
$J = K = 1$

- In J-K FF race around condition occurs when J & K S/I/P are 1 & $t_{pdff} \ll t_{pw}$. ~~During~~
- During race around O/P will change many times in a single CLK even if S/I/P is constant.
- Condition to avoid race around:

$$t_{pw} < t_{pdff} < t_{lk}$$

$$t_{pw} < t_{pdff} < t_{lk}$$

- To avoid race-around condition Master Slave JK flip-flop
- Master Slave J-K flip-flop :-



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- i) In Master Slave F-F, O/P will change only when slave O/P is changing.
- ii) In Master Slave F-F, Master is level triggered & Slave is edge triggered.

* Conversion of one F-F to other :-

1) JK to D FF :-

Procedure

- i) Required F-F characteristic table.
- ii) Available F-F excitation table.
- iii) Write logical expression for excitation.

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

Q_n	\bar{Q}_n	Q_{n+1}
0	0	X
1	X	0

Q_n	\bar{Q}_n	Q_{n+1}
D	(R)	(D)
D	X	

$$J = D.$$

$$K = \bar{D}$$

2) S-R to JK FF :-

$$S = J\bar{Q}$$

$$R = KQ.$$

3) SR to D :-

$$S = D$$

$$R = \bar{D}$$

4) SR to T-F-F :-

$$S = T\bar{Q}$$

$$R = TQ.$$

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5) JK - SR FF :-

$$J = S$$

$$K = R$$

6) JK - T FF :-

$$J = K = T$$

7) D to SR FF :-

$$D = S \bar{R} Q$$

8) D to JK :-

$$D = J \bar{Q} + \bar{R} Q$$

9) D to T :-

$$D = T \oplus Q$$

10) T to SR :-

$$T = S \bar{Q} + R Q$$

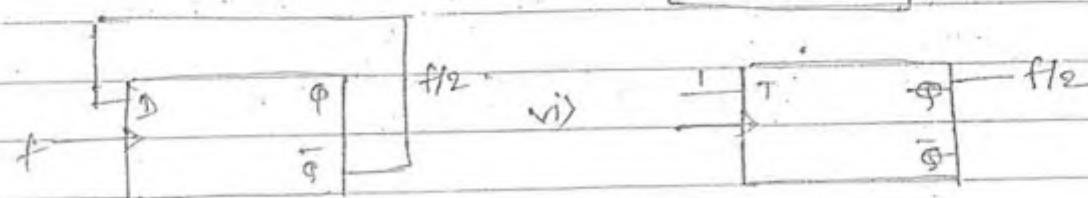
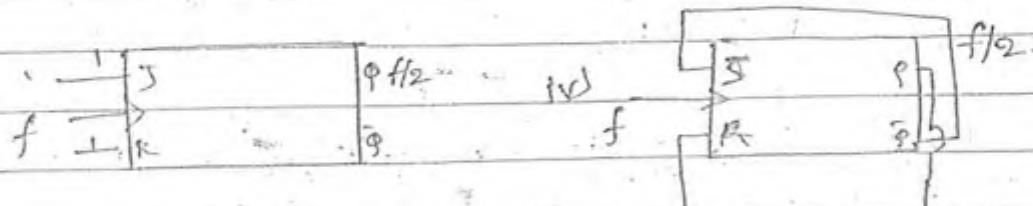
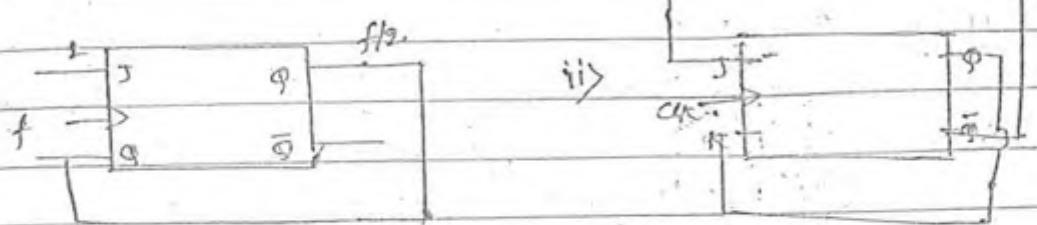
11) T to JK :-

$$T = J \bar{Q} + K Q$$

12) T to D :-

$$T = D \oplus Q$$

a) $\overline{D} \rightarrow d$



Register

→ Register are used to stored store group of bit.

→ To store n-bit n-bit F-F are cascaded in register.

→ Types of Register:-

1) SISO [Serial In Serial Out] :-

2) SIPO [Serial In Parallel Out] :-

3) PISO [Parallel In ^{Serial} Parallel Out].

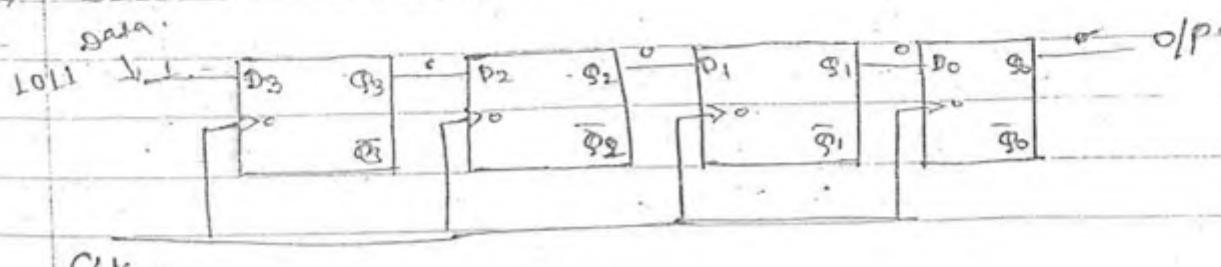
4) PIPO [Parallel In Parallel Out].

→ Depending upon Application Register can be classified into

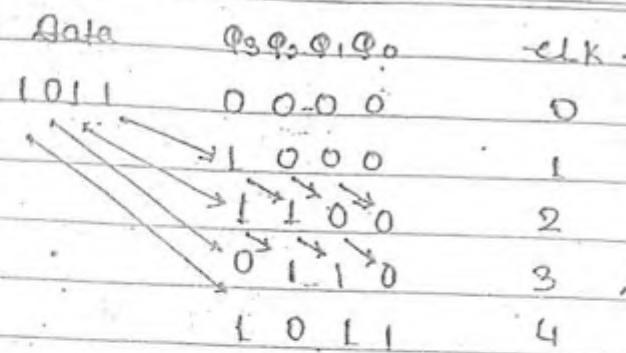
A. Shift Registers.

B. Storage Registers.

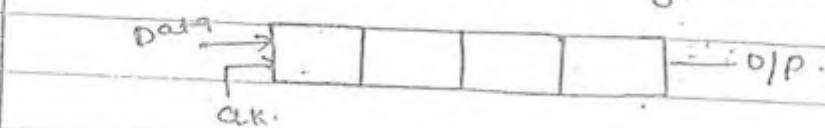
1) SISO :-



Clk.

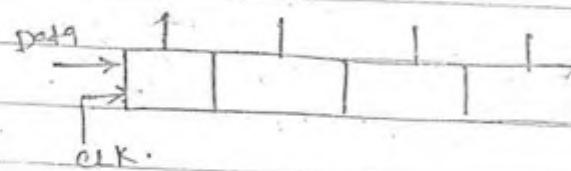
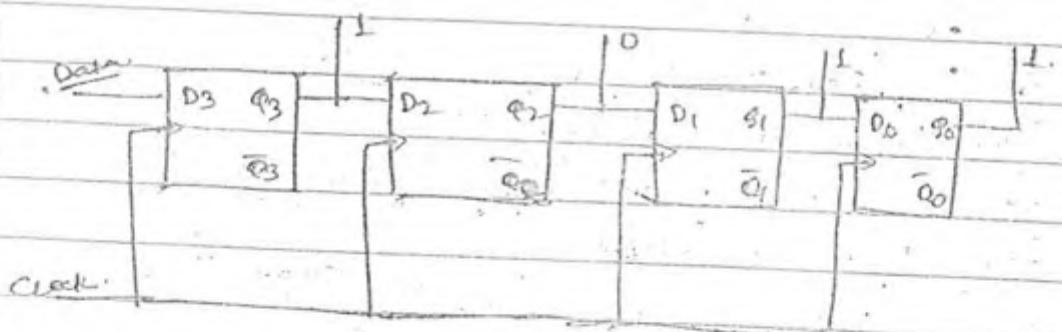


- In SISO register, to store n bit data it requires n clock pulse.
- To provide a n clock pulse delay to the S/P data.



- To provide n-bit data serially out it requires $(n-1)$ pulse.

2. SIPO :-

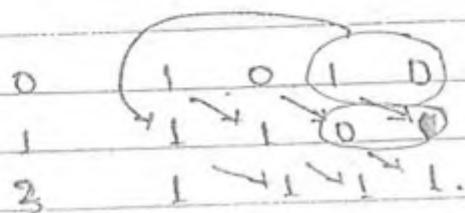
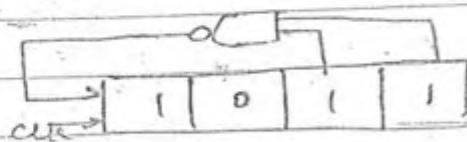


- In SIPO register, To provide n-bit data serially in it require n clock pulse and to provide parallel o/p 0 clock pulse are required.
- Serial Data \rightarrow Temporal code.
- Parallel data \rightarrow Spacial code.

→ SIPO is used to convert temporal code to serial code.

Q The circuit shown in fig. is 4 bit SIPO which is initially coded with 1010. If 3 CLK pulses are applied then the data at the output is

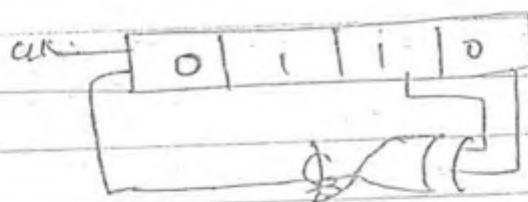
$$a) 1010 \quad b) 1101 \quad c) 1111 \quad d) 0000$$



W.B
8

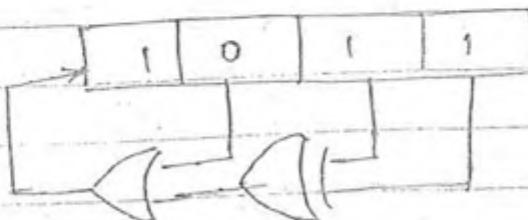
4

Q



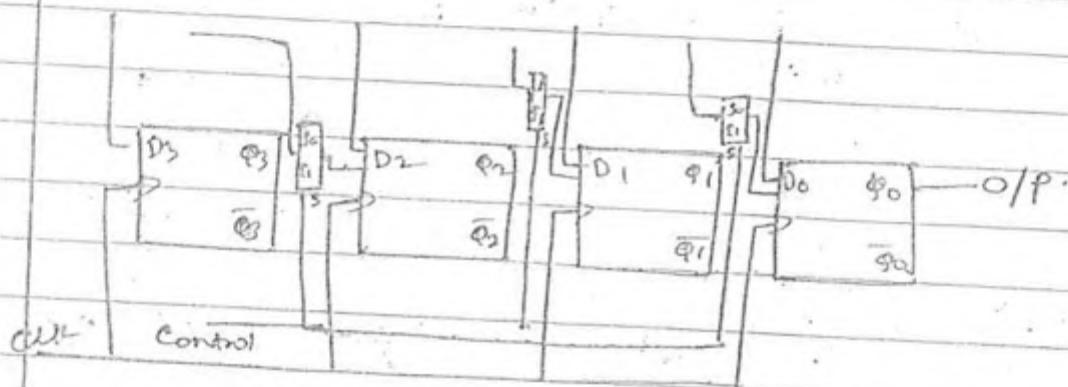
SFS 2010

Q The circuit shown in fig. is 4 bit SIPO which is initially coded with 1010. If CLK pulses are applied continuously after how many clock pulse the data given is 1011?



CLK	Q_3	Q_2	Q_1	Q_0
0	1	0	1	1
1	0	1	0	1
2	1	0	0	1
3	1	1	0	0
4	1	1	1	0
5	0	1	1	1
6	1	0	1	1
7				

3. PISO \rightarrow



Control = 0 \rightarrow P.I.

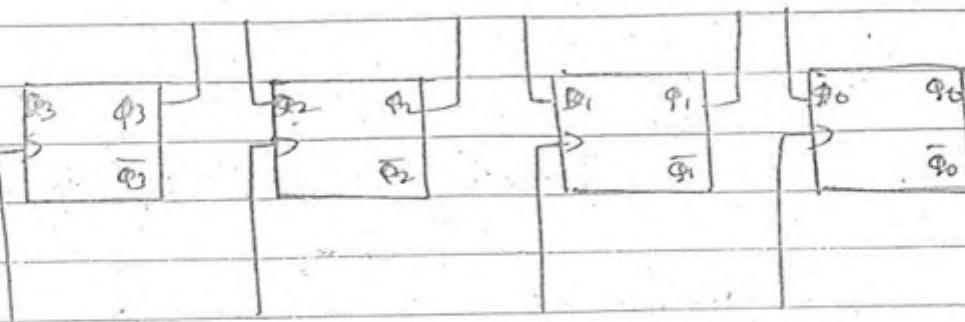
1 \rightarrow Serial O/P

- In PISO register, to provide parallel in we require one CLK pulse & to provide serial out it require $(n-1)$ clk pulse.
- PISO can be also used to convert special code to temporal code.
- In PISO

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4) PIPO : →



PIPO is used for storage register.

control = 1 → Parallel In. (1 clock pulse req.)
 0 → Parallel Out. (0, " " , ").

SISO n n-1
 CSPO n 0

PISO 1 n-1
 PIPO 1 0

Each shift register is to provide multiple the data
by (2)

36 n shift left operation will

Counters:

- It is basically used to count no. of clock pulse are applied.
- It can be also used in frequency divider.
- i) Frequency Divider.
- ii) Time measurement.
- iii) Frequency measurement.
- iv) Range measurement.
- v) Pulse width.
- vi) Wave form generation.

→ With n FF max^m possible state in a counter = 2^n .

Let N = No of state.

$n = \text{No. of flip-flop}$

$$N \leq 2^n$$

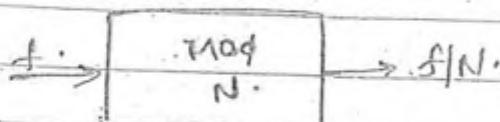
$$\Rightarrow n \geq \log_2 N$$

→ Depending upon clock pulse apply counters are classified as

- | | |
|---|---|
| i) Asynchronous counter | ii) Synchronous counter |
| iii) Different FF are applied in different clock pulse. | iv) All FF are applied with same clock pulse. |
| v) Slower | vi) Faster. |
| vii) operating with fixed count sequence | viii) Any count sequence is possible. |
| → up. | |
| → down. | |
| ix) Decoding errors | x) No decoding errors |
| x) Ripple counter | xi) Ex → Ring counter. |

★ Modulus Counter: →

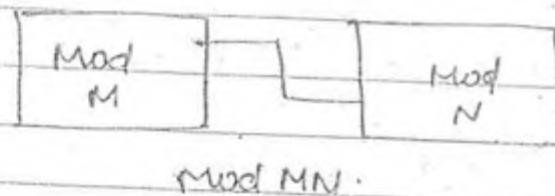
No. of states used in a counter is called modulus counter.
Ex Mod 5 → 5 state.



Q A decade counter is applied with a clock freq. of 10MHz then off frequency is

$$\text{Sol: } \frac{10}{10} = 1 \text{ MHz}$$

→ Let M and Mod N counters are cascaded then it acts as Mod MN counter.

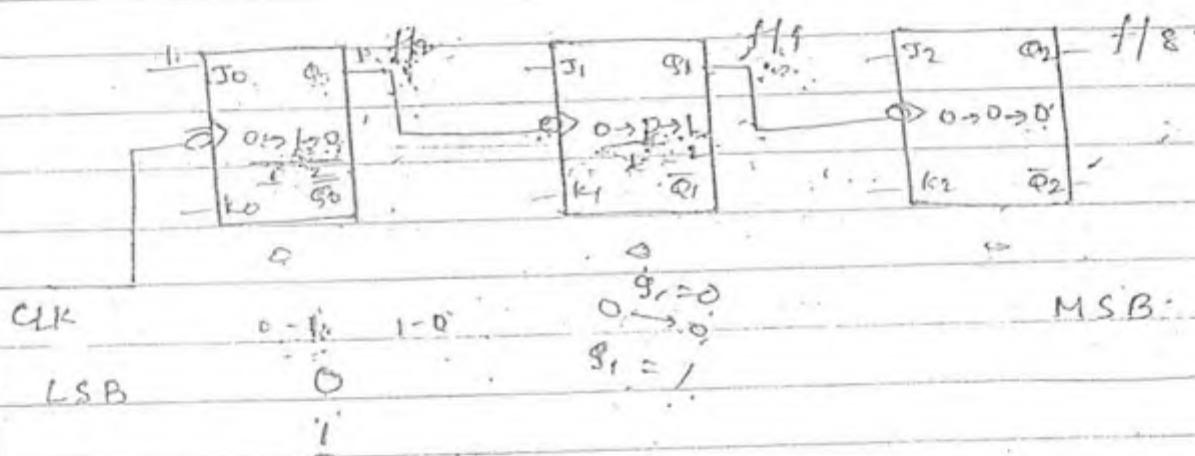


- 1) Ripple counter
- 2) Non binary ripple counter
- 3) Ring counter
- 4) Thornton counter
- 5) Synchronous serial carry
- 6) Synchronous parallel carry.
- 7) Synchronous counter Design & Analysis.

Yank for PSU
With

1) Ripple Counter: →

- It is a asynchronous counter
- Different clock pulse
- Toggle mode
- In ripple counter only one F.F is applied with external clock & other FF clocks is from previous F.F QP (Q or \bar{Q})
- In ripple counter the F.F applied with external CLK will act as LSB bit
- 3-bit Ripple counter: → [up counter]



In the Ckt shown in fig → toggle for every CLK pulse
 Q_1 change when Q_0 is changing from $1 \rightarrow 0$ and Q_2 changes when Q_1 is changing from $1 \rightarrow 0$

$Q_0 \rightarrow$ every clock

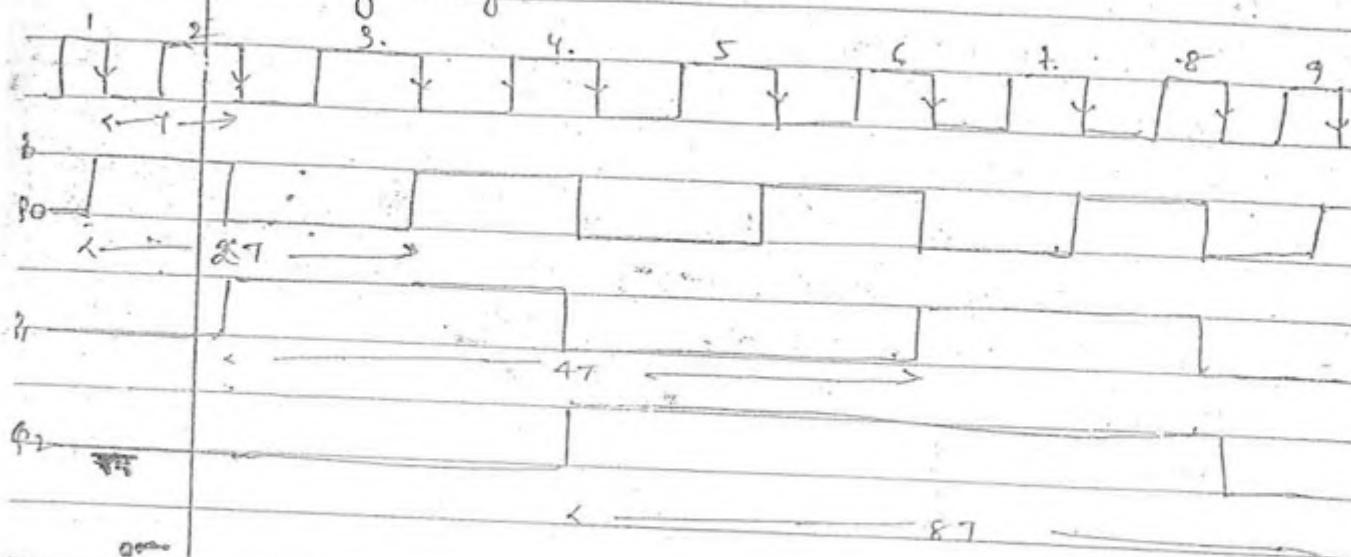
$Q_1 \rightarrow Q_0 \rightarrow 1 \rightarrow 0$

$Q_2 \rightarrow Q_1 \rightarrow 1 \rightarrow 0$

Truth table:

CLK	Q_2	Q_1	Q_0	CLK	Q_2	Q_1	Q_0
0	0	0	0	5	1	0	1
1	0	0	1	6	1	1	0
2	0	1	0	7	1	1	1
3	0	1	1	8	0	0	0
4	1	0	0				

→ Timing diagram :-



$$T_{clk} \geq n t_{pdff}$$

→ In a n bit ripple counter propagation delay of each ff is t_{pdff} then time period of clk

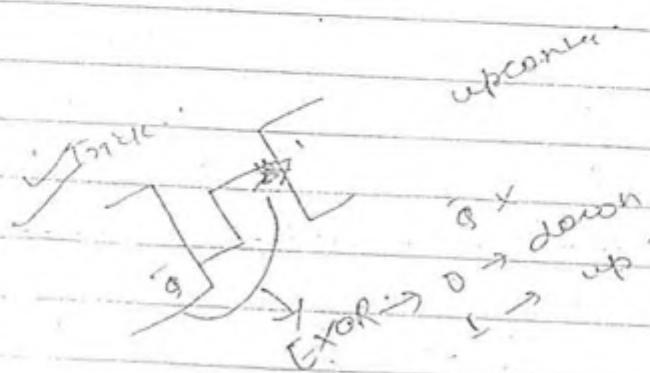
$$T_{clk} \geq n t_{pdff}$$

$$f_{max} = \frac{1}{n t_{pdff}}$$

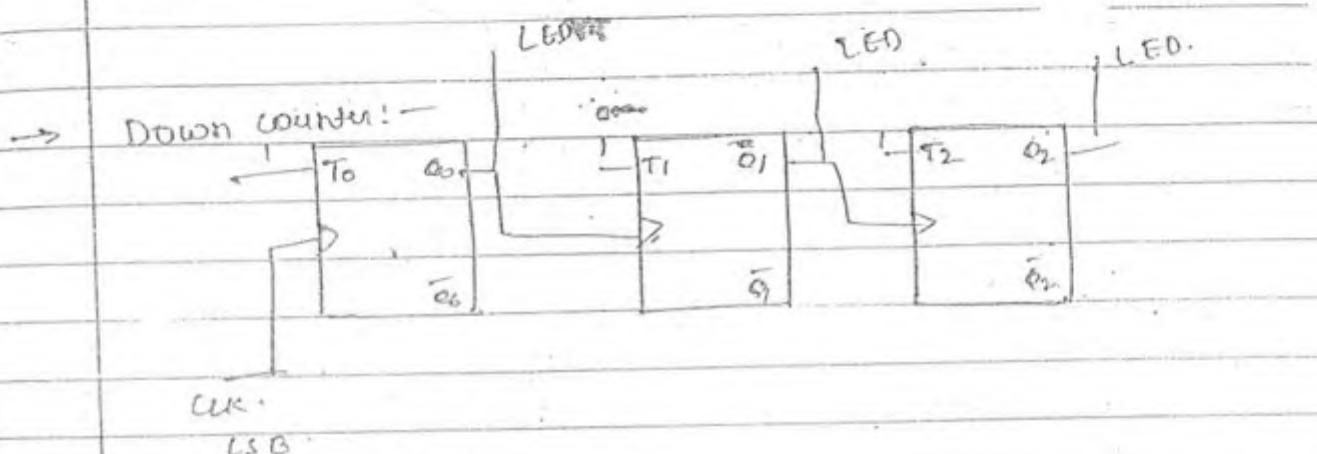
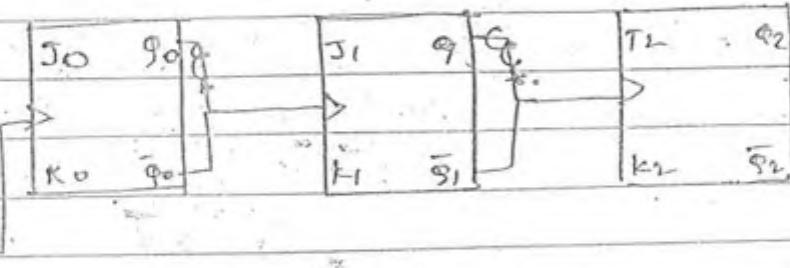
$$f_{max} = \frac{1}{n t_{pdff}}$$

30 (d)

32 (e)



→ -ve edge triggered, Q_1 as clock \rightarrow up counter
 → +ve edge trigger \bar{Q}_1 as clock \rightarrow up counter



The circuit shown in fig 90 toggle for every CLK pulse. Q_1 toggle when Q_0 change from $0 \rightarrow 1$. When Q_2 toggle when Q_1 change from $0 \rightarrow 1$.

$Q_0 \rightarrow$ Toggle for every CLK pulse.

$Q_1 \rightarrow$ " When $Q_0 \rightarrow 0 \rightarrow 1$

$Q_2 \rightarrow$ " " $Q_1 \rightarrow 0 \rightarrow 1$

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

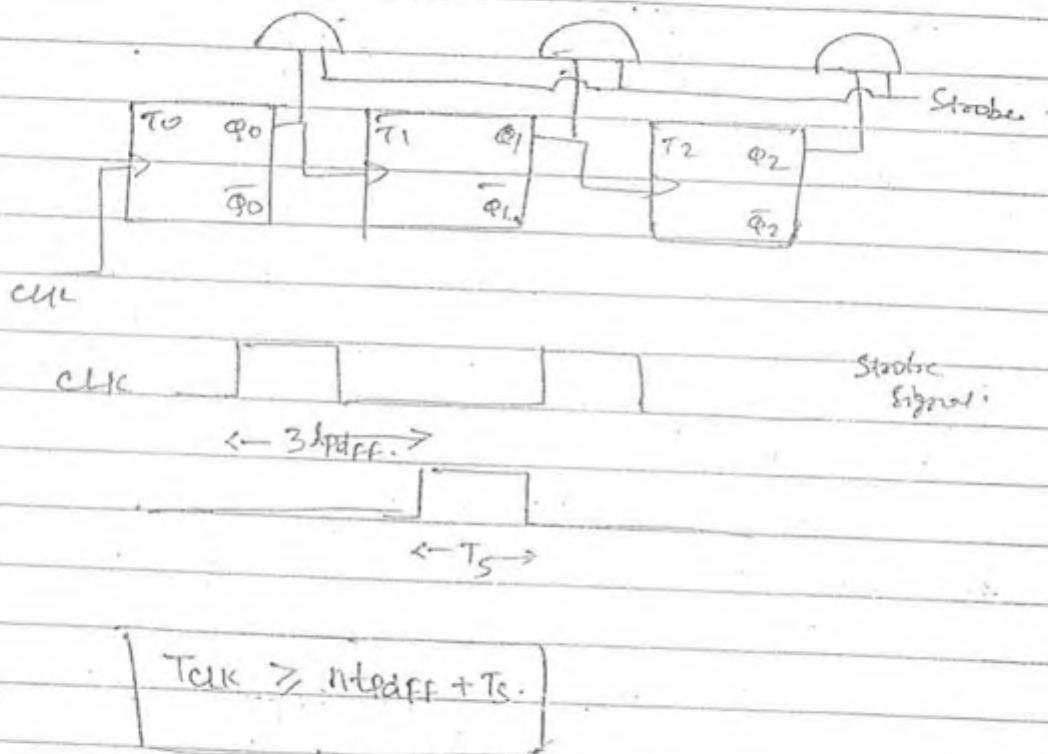
001
011
" "
Transient
or
error
accident

- +ve edge triggered @ as clock \rightarrow Down Counter
- -ve edge triggered @ as clock \rightarrow Down Counter.

WB 20 b) up counter:

* Decoding Error: \rightarrow

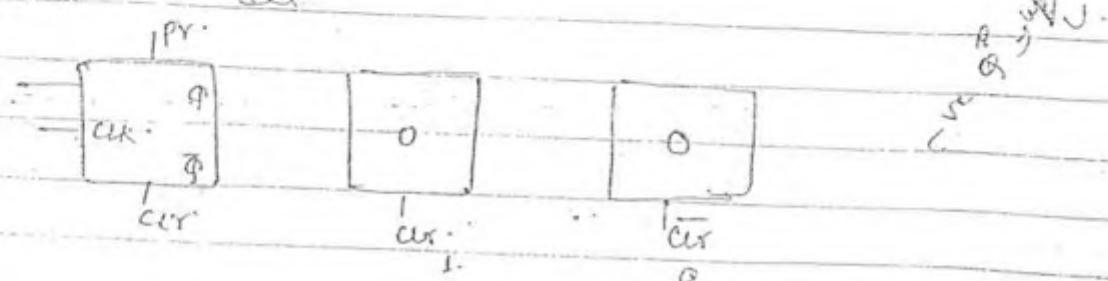
- Decoding errors are transient states representing ripple counter due to propagation delay.
- To avoid decoding error strobe signal are used.



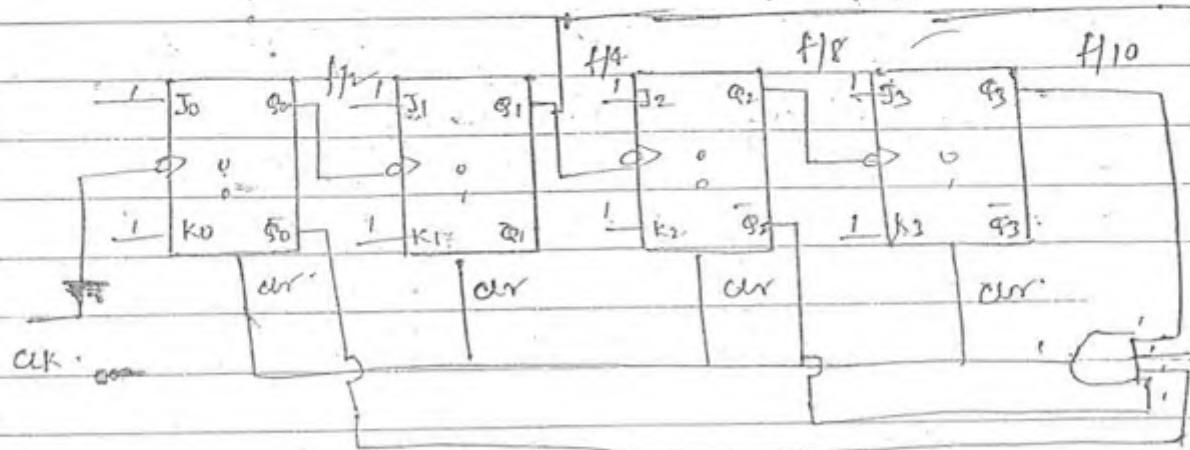
$$T_{clk} \geq n t_{pdff.} + T_S$$

- In ripple counter with n FF max no. possible states = 2^n .
- S, R, J, K, D, T \rightarrow Synchronous I/P.
- Clear, Preset \rightarrow Asynchronous I/P.
- Clear \rightarrow Reset.

Preset \rightarrow Set.



- * Non binary Ripple counter
- 2 Non binary Ripple counter.
- 3 BCD counter [Decade counter] :-



CLK $Q_3 \quad Q_2 \quad Q_1 \quad Q_0$

0 0 0 0 0

1 0 0 0 1

2 0 0 1 0

3 0 0 1 1

4 0 1 0 0

5 0 1 0 1

6 0 1 1 0

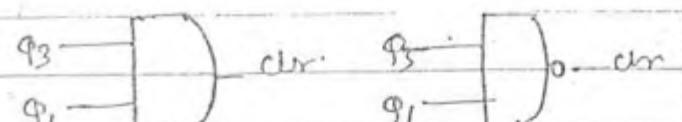
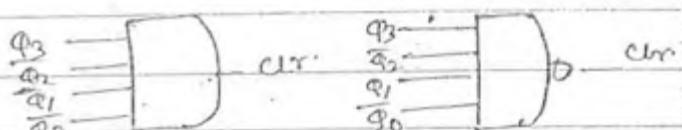
7 0 1 1 1

8 1 0 0 0

9 1 0 0 1

10 0 0 0 0 $\leftarrow 1010$

$Q_3 \bar{Q}_2 \bar{Q}_1 \bar{Q}_0$



→ All BCD counter are decade counter but decade counter is not necessarily vice versa.

WB.

$$15(a) \quad 8 \times 2 \times 5 = 60$$

$$\frac{12 \text{ M}2}{60} = 200 \text{ kHz}$$

16(b).

→ Asynchronous counter.

1) Toggle Trigger
 \rightarrow +ve
 \rightarrow -ve.

2) clock. \rightarrow Q
 \rightarrow \bar{Q} .

3) Counter \rightarrow up
 \rightarrow down.

4) Preset/clear.
 clear \rightarrow 000
 Preset \rightarrow 111

5) Decoding error.

W.B. 18)

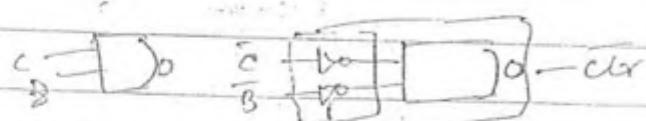
(a)	i) +ve edge.	111 ✓
	ii) Q as clock.	110 ✓
	iii) down.	101 ✓
	iv) preset=1111	101 ✓
	D10 ✓	111 ✓

111 \therefore mod 5 counter

22)

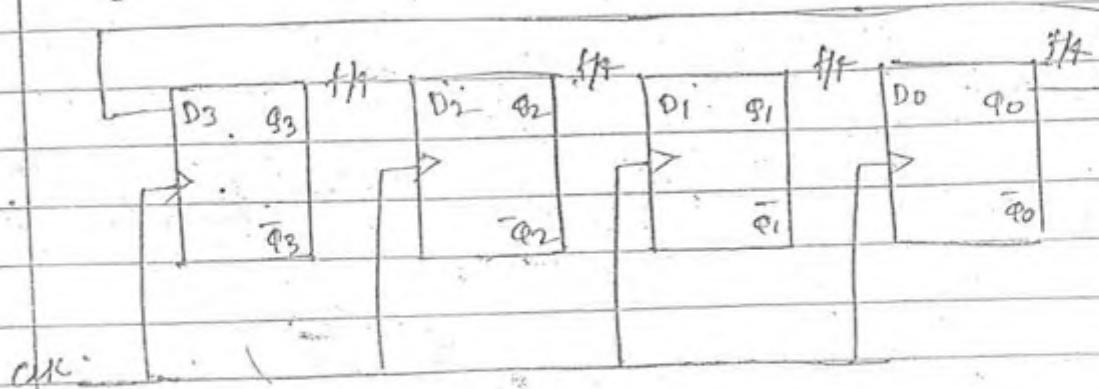
(c) 1110

23)

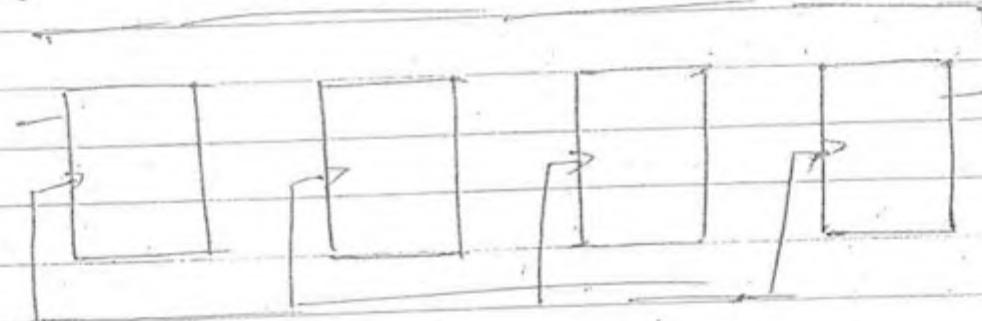


Bottled NAND gate DR gate.

3 Ring Counter : →



- It is a shift register
- In this last FF output is connected to the first FF input.
- In ring counter only one FF output is high & remaining FF outputs



Clock Q₃ Q₂ Q₁ Q₀

0 0 0 0 0

1 0 0 0 0

2 0 1 0 0

3 0 0 1 0

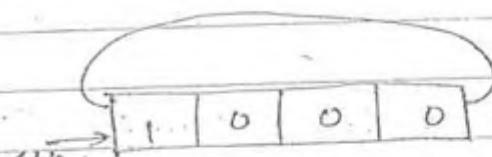
4 0 0 0 1

5 1 0 0 0

6 0 1 0 0

7 0 0 1 0

8 0 0 0 1



O/P

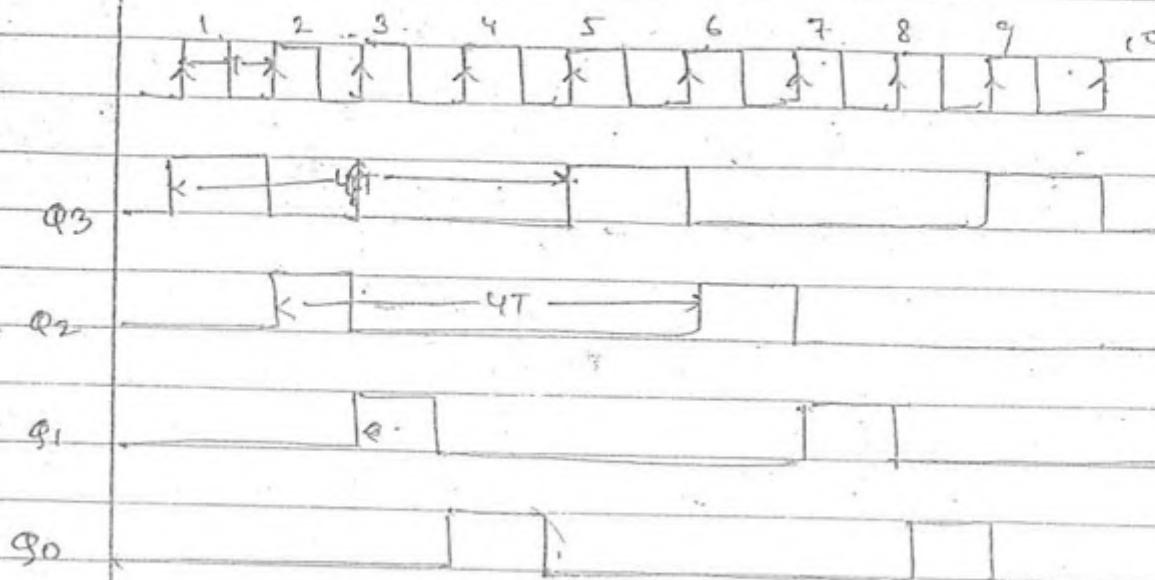
→ 4 bit ring counter = 4 State:

n bit → n State

f → f/n

[Unused state = $2^n - n$]

→ Timing diagram →



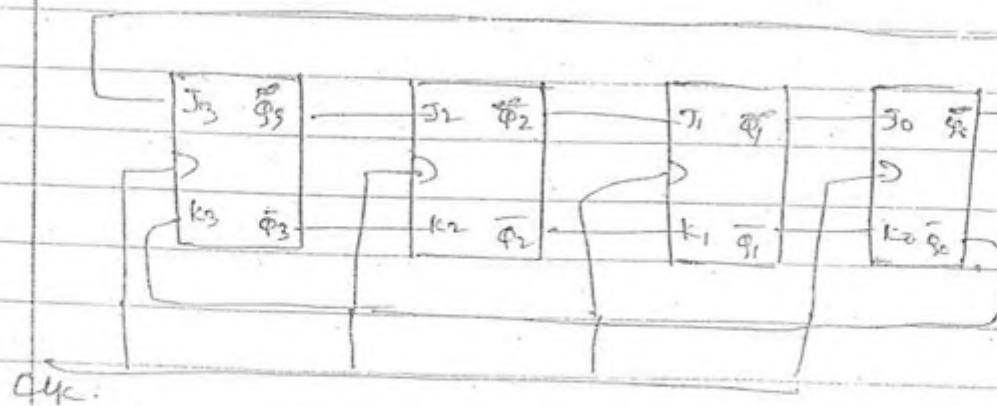
Phase shift b/w generated waveform = $\frac{360}{n}$

→ It is used in Stepper motor control

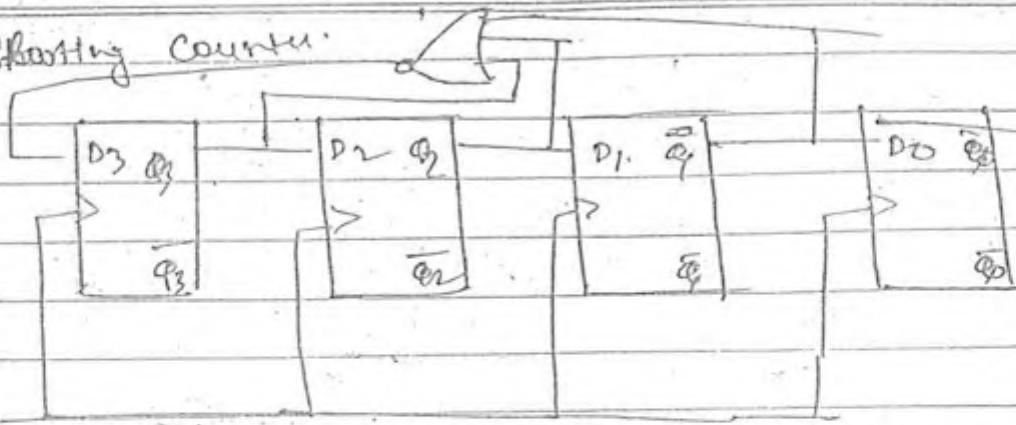
→ It is also used ADC

| no. of unused state = $2^n - n$ |

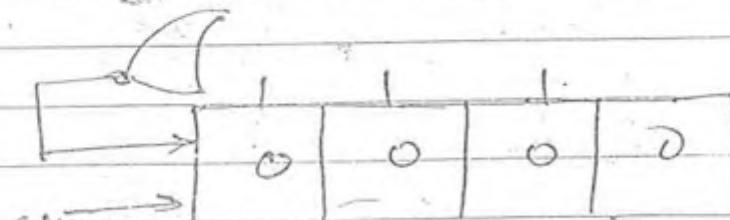
→ Ring Counter using J-K



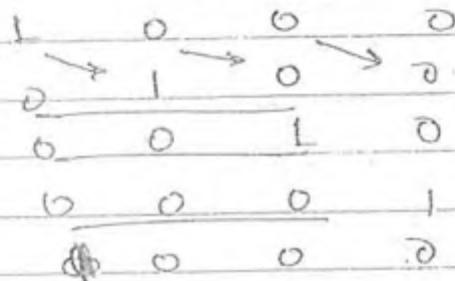
→ Self Shifting Counter



clk.



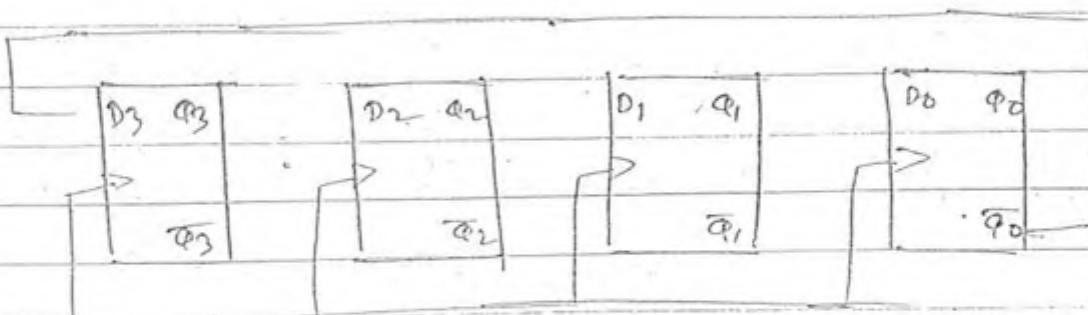
clk.



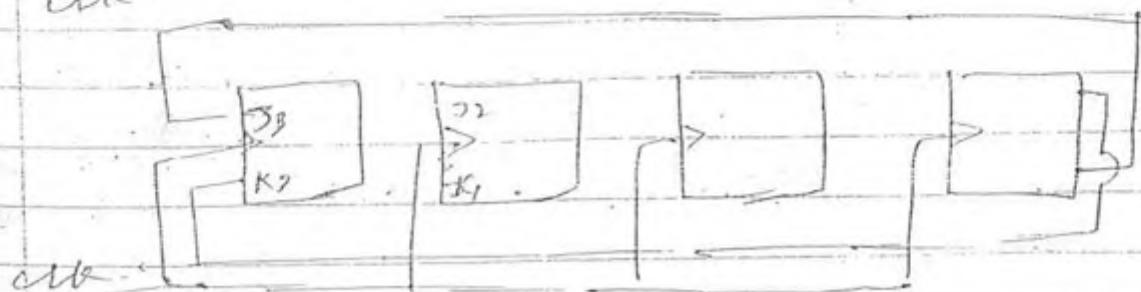
→ The advantage of ring counter is decoding is easy

→ To decode no logic gate is required

→ Johnson Counter:-



clk.



CK : $\begin{array}{|c|c|c|c|c|} \hline & 0 & 0 & 0 & 0 \\ \hline \end{array}$

1 0 0 0
1 1 0 0.
1 1 1 0.
1 1 1 1
0 1 1 1
0 0 1 1
0 0 0 1
1 0/0 0

4FF \rightarrow 8 · 1 1 0 0

nFF \rightarrow 2n

* Number System - Codes Data Representation:-

Various Number System

Arithmetic operation → Complement

Add, Sub

Various codes

Data representation → Unigned (+ve)

→ signed (+ve, -ve) → Sign magnitude

→ 1's.

→ 2's.

Number System And Code



Weighted

Additional Weightage:

Ex:-

③ ② ①

$10^2 \ 10^1 \ 10^0$

Binary

Octal

Decimal

Hexa

BCD code

unweighted

NO weightage

Ex - Gray code

Excess-3 code.

A number system with base α making 'Y' ^{contain} different digit
and they are from $(\alpha-1)$

Base

2

8

10

16

4

6

Different digit

0, 1

0, 1, ..., 7

0, 1, ..., 9

0, 1, ..., 9, A, B, C, D, E, F

0, ..., 3

0, ..., 5

12

0 ---- 9, A, B:

* Decimal to other conversion: →

$$(.)_{10} \rightarrow (.)_r$$

Where $r = 0, 1, 2, \dots, n$

Ex

$$(25.625)_{10} = (?)_r$$

To convert decimal no. into any other base r
 divide integer part and multiply fractional part
 with r.

$$(25.625)_{10} = (?)_2$$

$$\begin{array}{r} 2 | 25 \\ 2 | 12 - 1 \\ 2 | 6 - 0 \\ 2 | 3 - 0 \\ 2 | 1 - 1 \\ 0 - 1 \end{array} \quad (1+001)_2 \quad (11001.101)_2$$

$$0.625 \times 2 = 1.25 \Rightarrow 1$$

$$0.25 \times 2 = 0.5 = 0$$

$$0.5 \times 2 = 1.0 = 1$$

$$(25.625)_{10} = (?)_8$$

$$\begin{array}{r} 8 | 25 \\ 8 | 20 \\ 8 | 3 - 1 \\ 0 - 3 \end{array} \quad (25)_{10} = (31)_8$$

$$0.625 \times 8 = 5.0 = 5$$

$$\therefore (25.625)_{10} = (31.5)_8$$

$$(25.625)_{10} = (?)_{16}$$

$$\begin{array}{r} 16 \mid 25 \\ 16 \mid 1 - 9 \\ 0 - 1 \end{array} \quad 0.625 \times 16 = 10.000 \rightarrow A$$

$\therefore (19.A)_{16}$ Ans.

$(19)_{16}$

$$(254)_{10} = (?)_{16}$$

$$\begin{array}{r} 16 \mid 254 \\ 16 \mid 15 - E \uparrow \\ 0 - F \end{array} \quad (FE)_{16} \text{ Ans.}$$

$$(27.4)_{10} = (?)_4$$

$$\begin{array}{r} 4 \mid 27 \\ 4 \mid 6 \quad 3 \\ 4 \mid 1 \quad 2 \\ 0 \quad 1 \end{array} \quad \begin{array}{l} 0.4 \times 4 = 1.6 \rightarrow 1 \\ 0.6 \times 4 = 2.4 \rightarrow 2 \end{array} \quad \begin{array}{l} 0.4 \times 4 = 1.6 \rightarrow 1 \\ 0.6 \times 4 = 2.4 \end{array}$$

$\therefore (27.4) = (123.\overline{12})_4$

* Others to decimal number conversion:-

$$(y_3y_2y_1y_0.y_1y_2y_3)_{r} = (?)_{10}$$

To convert any other base r to decimal, multiply each digit with positional weightage and then add.

$$x_2r^2 + x_1r^1 + x_0r^0 + y_1r^{-1} + y_2r^{-2}$$

$$(10101 \cdot 11)_2 = (?)_{10}$$

16 8 4 2 1 $\frac{1}{2} \frac{1}{4}$

$$1 \times 16 + 0 \times 8 + 1 \times 4 + 0 \times 2 + 1 \times 1 + 1 \cdot \frac{1}{2} + 1 \cdot \frac{1}{4}$$

$$(21.75)_{10}$$

$$\rightarrow (57.4)_8 = (?)_{10}$$

~~8x~~

$$5 \times 8 + 7 \times \cancel{4} \frac{4}{8} = (47.5)_{10}$$

$$\rightarrow (57.4)_{16} = (?)_{10}$$

~~16x~~

$$57 \cdot 4$$

~~16x~~

$$80 + 7 \times 1 + 4 = (87.25)_{10}$$

$$\rightarrow (BAD)_{16} = (?)_{10}$$

$$16^2 \cdot 1$$

$$11 \times 16^2 + 10 \times 16^1 + 13 \times 16^0 = 28189$$

$$16^0 \rightarrow 1$$

$$16^1 \rightarrow 16$$

$$16^2 \rightarrow 256$$

$$16^3 \rightarrow 4096$$

$$\text{Ex } (35)_6 = (?)_{10}$$

~~6x~~

$$3 \times 6 + 5 \times 1 = 23$$

* Octal \leftrightarrow Binary

$$()_8 \rightarrow (?)_2$$

$$0 \rightarrow 000$$

$$1 \rightarrow 001$$

Ex $(37.45)_8 = (?)_2$

~~OCTAL~~ $011\ 111\ 8 \cdot 100\ 101$

* Hex \leftrightarrow Binary

Each digit is represented with 4 bit binary

$(259A)_6 = (?)_2$

↓ ↓ ↓ 4
0101 1001 1010

* Hex \leftrightarrow Binary

Ex $(CAD)_16 = (?)_8$

$(1100\ 1010\ 1101)_2 = (6255)_8$

* Arithmetic operations :-

Binary - Addition, Subtraction, Multiplication

Octal - Addition, Subtraction

Hex - Addition, Sub.

()_Y - Add, Sub.

→ Binary :-

i) Addition:-

$$\begin{array}{r} 110110 \\ + 101101 \\ \hline 1100011 \end{array}$$

~~Carry~~ ~~Sum~~

ii) Subtraction:-

$$\begin{array}{r} 100111 \\ - 10110 \\ \hline 001011 \end{array}$$

(c) Multiplication:-

$$\begin{array}{r} 10100101 \\ \times 101 \\ \hline 10100101 \end{array}$$

$$\underline{1010 \times 101}$$

$$\rightarrow (111)_2 \times (111)_2,$$

$$\begin{array}{r}
 1010 \\
 \times 101 \\
 \hline
 .1010 \\
 0.000 \\
 \hline
 1010 \\
 \hline
 1100.00
 \end{array}
 \quad
 \begin{array}{r}
 111 \\
 \times 111 \\
 \hline
 111 \\
 111 \\
 \hline
 1110
 \end{array}
 \quad
 \begin{array}{r}
 111 \\
 \times 111 \\
 \hline
 111 \\
 111 \\
 \hline
 1110
 \end{array}
 \rightarrow 4 \rightarrow 10$$

$$\begin{array}{r}
 111000.01 \\
 \hline
 6.100
 \end{array}$$

w.B.

$$(10111)_2 \times (15)_{10} = (101011001)_2$$

$$10111_2 \times 1111$$

$$\underline{\underline{0} \ 1 \ 1 \ 1 \ 1}$$

$$\begin{array}{r}
 10111_2 \times 1111 \\
 \hline
 10001_2 \\
 0001_2 \\
 1001_2 \\
 \hline
 10
 \end{array}$$

$$\begin{array}{r}
 2=1 \\
 w=1 \quad \left\{ \begin{array}{l} (0) \\ (1) \end{array} \right. \\
 y=1
 \end{array}$$

$$0.02$$

→ Octal : →

$$0+0=0$$

$$1+1=2$$

$$1+2=3$$

$$1+6=7$$

$$1+7=10$$

$$7+1=10$$

$$7+2=11$$

$$7+7=14$$

$$7+7=16$$

$$\begin{array}{r}
 8 \mid 18 \\
 8 \mid 1-0 \downarrow \\
 0-1
 \end{array}$$

$$\begin{array}{r}
 8 \mid 9 \\
 8 \mid 1-1 \downarrow \\
 0-1
 \end{array}$$

$$\begin{array}{r}
 8 \mid 19 \\
 8 \mid 1-6 \downarrow \\
 0-1
 \end{array}$$

→ 243

212

455

$$q. \quad \begin{array}{r} 567 \\ 243 \\ \hline 1032 \end{array}$$

$$\begin{array}{r} 8 | 11 \\ - 8 \\ \hline 3 \\ - 8 \\ \hline 0 \end{array}$$

Subtraction →

$$\begin{array}{r} 743 \\ - 564 \\ \hline 159 \end{array}$$

→ Hexadecimal System:-

i) Addition:-

$$1+1=2$$

$$1+2=3$$

⋮

$$1+9=A$$

$$1+A=B$$

$$1+B=C$$

$$A+A=14$$

$$10+10$$

$$\begin{array}{r} 16 | 20 \\ - 16 \\ \hline 0 \end{array} \quad \begin{array}{r} 16 | 21 \\ - 16 \\ \hline 0 \end{array}$$

$$A+B=15$$

10

$$q. \quad \begin{array}{r} 5689 \\ 4574 \\ \hline \end{array}$$

$$ADD \quad 26 \rightarrow 1A$$

$$\begin{array}{r} 16 | 06 \\ - 16 \\ \hline 0 \end{array}$$

$$4574$$

$$ADD \quad 24 \rightarrow 18$$

$$02$$

$$9BFD$$

$$188A$$

ii) Subtraction :-

$$\begin{array}{r} 16 | 216 \\ - 98 \\ \hline 128 \\ - 128 \\ \hline 0 \end{array} \quad \begin{array}{r} 16 | 19 \\ - 16 \\ \hline 3 \\ - 16 \\ \hline 13 \\ - 16 \\ \hline 7 \end{array}$$

$$3EC F$$

Complements: →

$$r \rightarrow (r-1)'s.$$

$\boxed{r}'s.$

$$B \rightarrow 1's.$$

\downarrow

$$\rightarrow 0's.$$

$$O \rightarrow 2's.$$

\Downarrow

$$8's$$

$$D \rightarrow 9's.$$

\Downarrow

$$16's$$

$$H \rightarrow F's.$$

$16's$

→ $(r-1)'s$ complement: →

To determine $(r-1)'s$ complement subtract given no. from max no. possible in the given base $(r^n - 1)$

$$1 \text{ bit} \rightarrow 2^1 - 1 =$$

→ 1's complement

$$\begin{array}{r} 1 \\ 0 \end{array}$$

$$0.1.0010$$

→ 7's complement: →

$$\begin{array}{r} 7 \\ 5 \\ 6 \\ 7 \\ 4 \end{array}$$

$$2103 \quad \underline{\text{10}}$$

→ 9's complement of decimal number: —

$$\begin{array}{r} 9 \\ 2 \\ 6 \\ 7 \\ 9 \end{array}$$

$$7920 \quad \underline{\text{10}}$$

PAGE NO.

DATE :

→ F's complement of hexadecimal no.

$$\begin{array}{r} \text{FFFF} \\ 2689 \end{array}$$

$$\underline{D.976}$$

→ 8's complement :-

To determine 8's complement first to write (r-1)'s complement
and then add 1 to LSB (Right-most)

Ex

$$\begin{array}{c}
 \text{2's complement} \rightarrow 10100 \\
 \text{1's complement} \rightarrow 01011 \\
 +1 \quad \cancel{+1} \\
 \hline
 01100
 \end{array}
 \qquad
 \begin{array}{c}
 1011011 \\
 0100100 \\
 +1 \quad \cancel{+1} \\
 \hline
 0100100
 \end{array}$$

8's complement

$$\begin{array}{r}
 2670 \\
 7777 \\
 \hline
 2670 \\
 \text{8's} \quad 510\cancel{7} \\
 +1 \\
 \hline
 5110
 \end{array}$$

10's complement:-

$$\begin{array}{r}
 5690 \\
 9999 \\
 \hline
 5690 \\
 -4809 \\
 +11 \\
 \hline
 438016
 \end{array}$$

16's Complement :-

$$\begin{array}{r}
 5289 \\
 F's \quad FFFF \\
 \underline{-} \quad \underline{5289} \\
 A\bar{D}76 \\
 + 1 \\
 \hline
 \cancel{A\bar{D}77} \quad \cancel{1}
 \end{array}$$

W.Soln $(11C.0)_{16} = ()_{10}$

$$1x2^9 + 1x2^8 + Cx2^7 + D \quad \text{numr=13.}$$

$$1x16^9 + 1x13 + Cx1 \neq D = 194 \quad (b)$$

2) (4) $(FE35)_{16} \text{ XOR } (CB15)_{16}$.

$$\begin{array}{r}
 FE35 \rightarrow 1111 \quad 1110 \quad 0011 \quad 0101 \\
 1100 \quad 1011 \quad 0001 \quad 0101 \\
 \hline
 0011 \quad 0101 \quad 0000 \quad 0000 \\
 3 \quad 5 \quad 2 \quad 0 \\
 3520 \quad \cancel{1} \quad (c)
 \end{array}$$

3) F's complement (C)

$$\begin{array}{r}
 FFFF \\
 2BFD \\
 \hline
 D402
 \end{array}$$

4) $b_{log_2 1's} = b$

$$3 \times 512 + 7 \times 64 + 5 \times 8 + 3$$

$$3753$$

$$0111101011 \rightarrow \circled{9}$$

Q) (d)

$$\begin{array}{r} 117316 \\ \times 200 \\ \hline 117 \\ \hline 0 E 3 \end{array}$$

Q) (g) $(4) \times 4096 + (9) \times 256 + (7) \times 16 + (5)$

$$4978$$

$$0100 \ 1001 \ 0111 \ 0101$$

8 62

(g) (a) 2-3

$$\begin{array}{r} 1 \cdot 2 \\ \hline 10 \cdot 1 \end{array}$$

$$\begin{array}{r} 4 \mid 5 \\ \hline 1 \ 1 \ 1 \uparrow \\ 0 \ - 1 \end{array}$$

$$\begin{array}{r} 4 \mid 4 \\ \hline 1 \ 0 \ 1 \uparrow \\ 0 \ - 1 \end{array}$$

$$11 \quad - 135$$

$$\begin{array}{r} 744 \\ \hline 323 \end{array}$$

$$\begin{array}{r} 6 \mid 9 \\ \hline 1 \ 3 \\ 6 \mid 0 \ - 1 \end{array}$$

20 (c)

$$21 (235)_{R_1} = (565)_{10}$$

$$(565)_{R_2} = (1065)_{R_2}$$

$$R_2 < 10$$

$$R_2 = 10$$

$$2 \times R_2^2 + 3 \times R_2 + 5 = 565$$

$$2 \times 256 + 3 \times 16 + 5 = 565 \checkmark$$

$$2 \times 144 + 3 \times 4 + 5 \neq 565$$

CODES

1) BCD code:-

2) Excess 3 code.

3) Gray code.

1) BCD [Binary Coded Decimal]:-

i) It is 4-bit code.

ii) Weighted code.

iii) 8421

iv) Each decimal digit is represented with 4 bit.

Decimal

B C D code

Excess 3 code

0

0 0 0 0

0 0 1 1

1

0 0 0 1

0 1 0 0

2

0 0 1 0

0 1 0 1

3

0 0 1 1

0 1 1 0

4

0 1 0 0

0 1 1 1

5

0 1 0 1

1 0 0 0

6

0 1 1 0

1 0 0 1

7

0 1 1 1

1 0 1 0

8

1 0 0 0

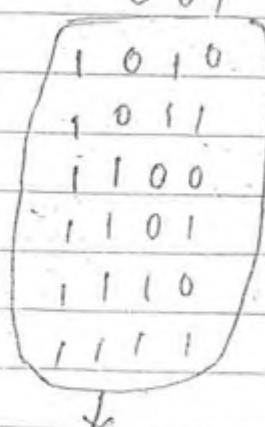
1 0 1 1

9

1 0 0 1

1 1 0 0

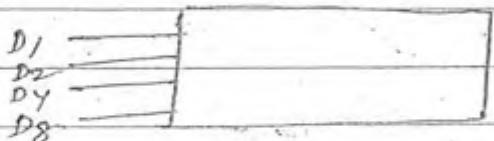
Self
complement
code



Invalid BCD code.

→ During arithmetic operation if invalid BCD is present then add 6 (0110) to take correct result.

Q) A combinational CKT is applied with 4-bit BCD code which is designated as D_8, D_7, D_6, D_5 . O/P is Y is 1 when I/P BCD is divisible by 3. Then the logical expression for Y is



$D_8 D_7$	$D_7 D_6$	$D_6 D_5$	$(D_8 D_7)$	$D_2 \bar{D}_1$
$D_8 D_7$	1		1	
$\bar{D}_8 \bar{D}_7$				0
$\bar{D}_8 D_7$	X	X	X	
$D_8 \bar{D}_7$	1	1		X

$$D_8 D_7 + D_7 D_6 + \bar{D}_8 D_7 D_6 + D_8 \bar{D}_7 D_6$$

(839),

1000 0011 1001

Q) Excess-3-code:-

- i) unweighted
- ii) 4 bit code.
- iii) BCD + 3 (0011)
- iv) Self Complement code

2421

3321

4311

5211

Self Complemented & Weighted code.

$$2+4+2+1=9$$

$$3+3+2+1=9$$

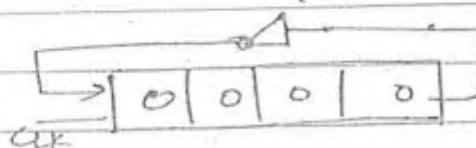
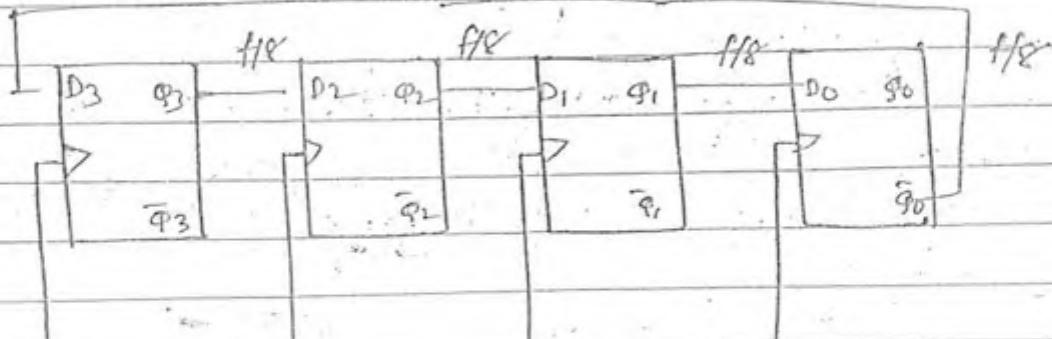
$$4+3+1+1=9$$

$$5+2+1+1=9$$

2421 code Decimal

0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
1 1 0 0	6
1 1 0 1	7
1 1 1 0	8
1 1 1 1	9

\Rightarrow Johnson Counter :- [Twisted counter or Möbius counter] :-
Creeping counter or walking counter or switch tail counter.



CLK	Q ₃	Q ₂	Q ₁	Q ₀	Decoding logic
0	0	0	0	0	$\bar{Q}_3 \bar{Q}_0 = Q_3 + Q_0$
1	1	0	0	0	$Q_3 \bar{Q}_2$ AND, NOR
2	1	1	0	0	$Q_2 \bar{Q}_1$
3	1	1	1	0	$Q_1 \bar{Q}_0$
4	0	1	1	0	$Q_3 Q_0$
5	0	1	1	1	$\bar{Q}_3 Q_2$
6	0	0	1	1	$\bar{Q}_2 Q_1$
7	0	0	0	1	$\bar{Q}_1 Q_0$
8	0	0	0	0	:

n FF $\rightarrow 2^n$ States.

No. of unused states $= 2^n - 2n$.

Other names of Johnson Counter:-

Twisted counter

Möbius counter

Creeping counter

Walking counter

Switch tail counter

- In Johnson counter to decode each state one two input AND gate / NOR gate.
- Disadvantage:-
- j) Lock out may occur when counter enters into unused state.
- In synchronous counter propagation delay of each FF is tpdff. Then:

$$T_{clk} \gg t_{pdff}$$

$$f_{clk} \leq \frac{1}{t_{pdff}}$$

$$f_{max} = \frac{1}{t_{pdff}}$$

W.B

②

$$(d) \quad 0 \rightarrow 01101$$

$$1 \rightarrow 0101$$

$$2 \rightarrow 0100$$

$$16 \rightarrow 0110$$

$$32 \rightarrow 0110$$

$$33 \rightarrow 0101$$

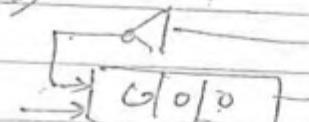
$$34 \rightarrow 0100$$

$$35 \rightarrow 0011$$

$$36 \rightarrow 0010$$

$$37 \rightarrow 0001$$

(3) (b)



$$0 \rightarrow 000$$

$$1 \rightarrow 100$$

$$2 \rightarrow 110$$

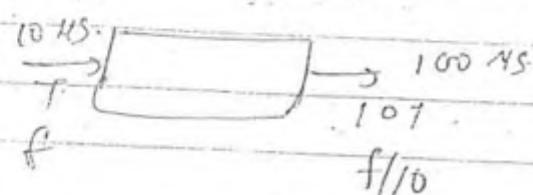
$$3 \rightarrow 111$$

$$4 \rightarrow 011$$

$$5 \rightarrow 001$$

$$6 \rightarrow 000$$

4) (c) ON & OFF Period same \rightarrow Symmetrical Square wave.



MOD5x MOD2

→ BCD counter can not use symmetrical count square wave.

15 (a)

17 (c)

11 (C) 4

13 (c)

13 (c)

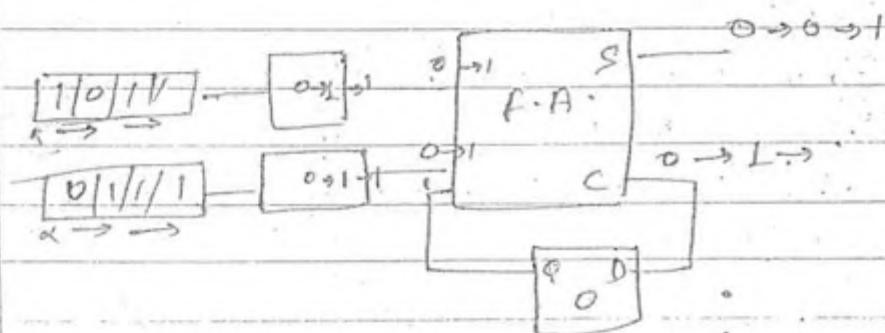
11 (c)

92) $R = \text{Max tpd}$

$S = tpd$

(b)

25

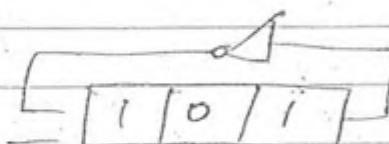


1 0 1 1

0 0 1 1

$$\begin{array}{r} 1 1 \\ 1 1 \\ \hline 1 1 0 \end{array} \quad S = 1$$

27 (d)



1 0 1

0 1 0

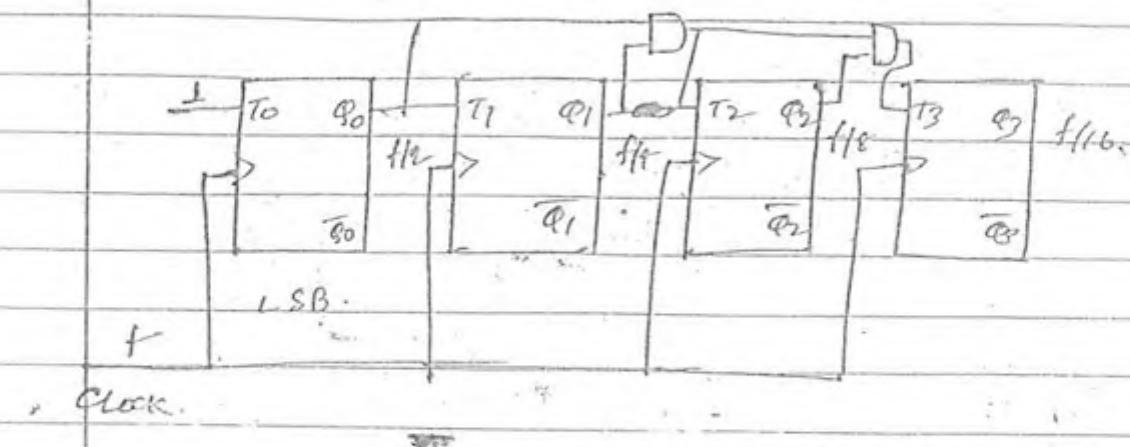
1 0 1

0 1 0

1 0 1

f/g

* Synchronous Series Carry Counter: →



- Ckt shown in figure is synchronous series carry up counter.
- In this Counter Q_0 toggles for every clock pulse
- Q_1 toggles when $Q_0 = 1$ & clock is applied
- Q_2 toggles when $Q_1, Q_0 = 1$ & clock is applied
- Q_3 toggles when $Q_2, Q_1, Q_0 = 1$ & clock is applied.

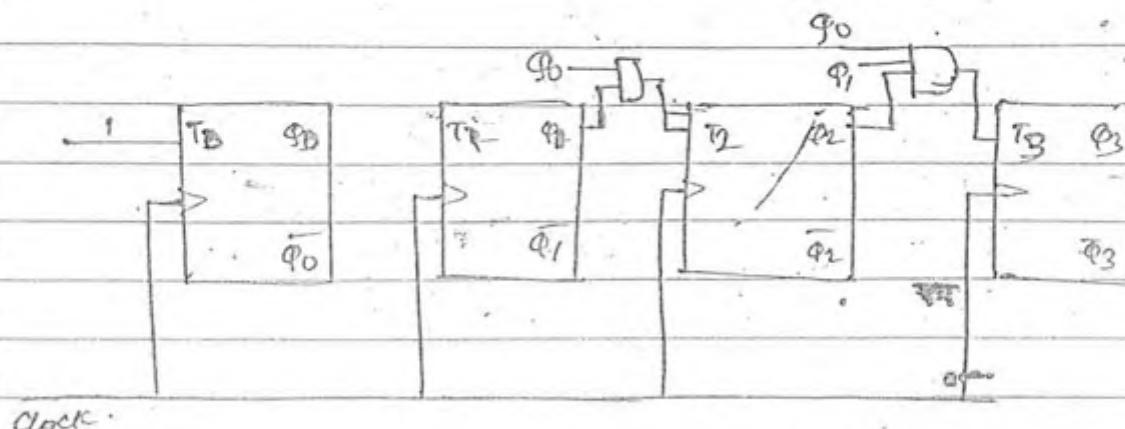
→ Truth table:

CLK	Q_3	Q_2	Q_1	Q_0	out	out
0	0	0	0	0	0	0
1	0	0	0	1	0	1
2	0	0	1	0	1	0
3	0	0	1	1	1	1
4	0	1	0	0	1	1
5	0	1	0	1	1	0
6	0	1	1	0	0	1
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	0	1
10	1	0	1	0	1	1
11	1	0	1	1	1	0
12	1	1	0	0	0	0
13	1	1	0	1	1	0
14	1	1	1	0	0	1

$$T_{ALK} \geq T_{pdFF} + (n-2) T_{pd\ AND}$$

→ To provide down counter use \bar{Q}_i off to the next stage S/P.

★ Synchronous parallel carry counter:



$$T_{clk} = t_{pdFF} + t_{pd\ AND}$$

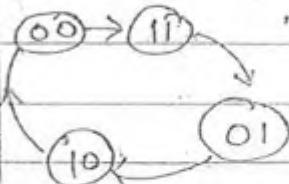
→ Synchronous parallel carry counter is faster than synchronous series carry counter.

→ Its operation is same as synchronous series counter.

★ Synchronous Counter Design for the Given Count Signal:-

Design a synchronous counter for the count signal

$0 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 0$ using +ve edge triggered DFF.



State diagram:

-89:

- 1) Identify no. of F.F & LIP & OIP.
- 2) Construct State table.
- 3) Write logical expression for LIP.
- 4) Minimize.
- 5) Implement.

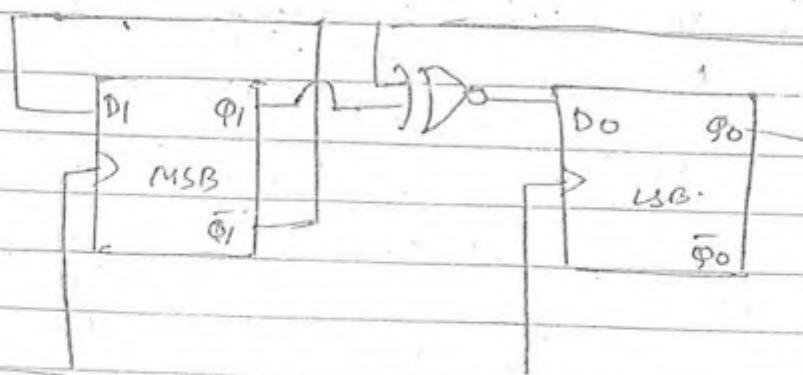
→ State table:

Present State		Next State		Excitation IP	
Q_1	Q_0	Q_1	Q_0	D_1	D_0
0	0	1	1	1	1
1	1	0	1	0	1
0	1	1	0	1	0
1	0	0	0	0	0

$$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0 \\ = \bar{Q}_1$$

$$D_0 = \bar{Q}_0 \bar{Q}_1 + Q_1 Q_0 \\ = Q_1 \bar{Q}_0$$

→ Implementation:-



Q1.

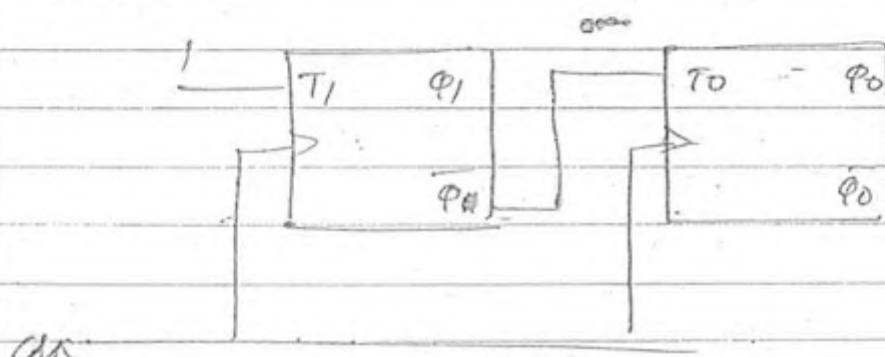
→ using T F.F :-

State table.		Next State.	
q_1	q_0	q_{1f}	q_{0f}
0	0	0	1
0	1	0	0
1	0	1	0
1	1	0	0

$$T_0 = \bar{\Phi}_1 \bar{\Phi}_0 + \bar{\Phi}_1 \Phi_0$$

$$= \bar{\Phi}_1$$

$$T_1 = 1$$



OK

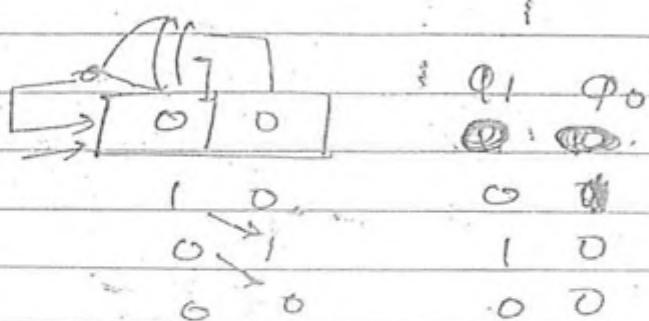
- Q) Design a synchronous counter for the count sequence
 $0 \rightarrow 2 \rightarrow 5 \rightarrow 3 \rightarrow 4 \rightarrow 7 \rightarrow 0$.

Sol: State table.

Present State	Next State
$q_2 q_1 q_0$	$q_{2f} q_{1f} q_{0f}$
0 0 0	0 1 0
0 1 0	1 0 1
1 0 1	0 1 1
0 1 1	1 0 0
1 0 0	1 1 1
1 1 1	0 0 0
0 0 1	0 0 0
1 1 0	0 0 0

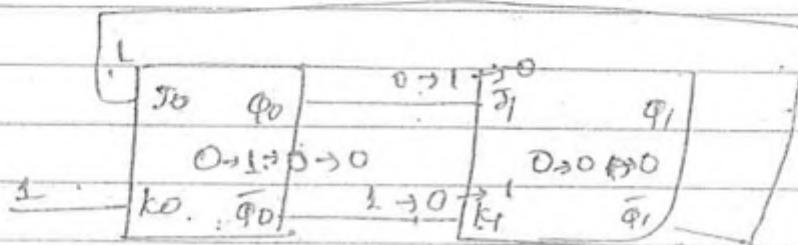
To avoid lock out change unused state to into one of used state in state table.

W.D.F



(b)

98



clk. Q0 Q1

0 0 0

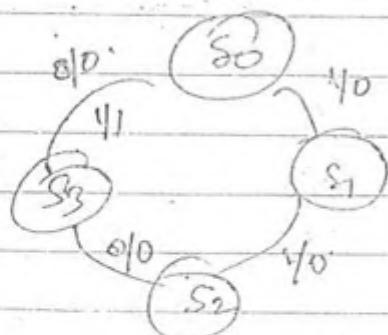
1 1 0

2 0 1

3 0 0

33 0 0

(c)



4-bit - 4 state

↑
2⁴

31

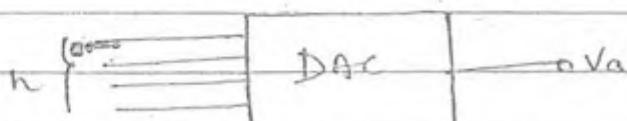
(d)

ADC / DACDAC

- 1) Weighted Resistor
- 2) R-2R Ladder

ADC

- 1) Counter type
- 2) SAR Type
- 3) Flash
- 4) Dual slope integrating type

★ Digital To Analog Converter (DAC):-

→ Characteristics :-

- 1) Resolution
- 2) Analog O/P voltage
- 3) Full Scale voltage
- 4) % Resolution ..
- 5) Accuracy
- 6) Linear
- 7) Monotonic

1. Resolution :-

Resolution of DAC correspond to change in analog voltage for one LSB increment at the I/P.

If reference voltage is given, then resolution of n-bit D/A converter is

$$\text{Resolution} = \frac{V_{ref}}{2^n - 1}$$

2) Analog O/P voltage :-

Analog O/P Voltage = Resolution \times Decimal equivalent of binary data.

- Q. In a 4 bit DAC, reference voltage is 5V and a binary data 1001 is applied then analog o/p voltage is

Sol:

$$V_a = \frac{5}{15} \times 9 = 3\text{ volt}$$

3) Full Scale Voltage :-

$V_{FS} = \text{Resolution} \times \text{Max}^m \text{ decimal}$

$$= \frac{V_{ref}}{2^{n-1}} \times 2^{n-1}$$

$$\Rightarrow V_{FS} = V_{ref}$$

4) % Resolution :-

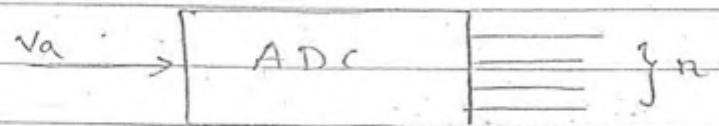
$$\% \text{ Resolution} = \frac{\text{Resolution} \times 100}{V_{FS}}$$

$$\% \text{ Resolution} = \frac{\frac{V_{ref}}{2^{n-1}} \times 100}{V_{ref}}$$

$$\% \text{ Resolution} = \frac{1}{2^{n-1}} \times 100$$

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~~★ ADC :-~~

$$\text{Resolution} = \frac{V_{\text{range}}}{2^n - 1}$$

$$V_{\text{range}} = V_{\text{max}} - V_{\text{min}}$$

5. Error Accuracy :-

Maximum error acceptable in ADC and DAC is equal to resolution or step size.

$$\text{Y. Resolution} = \frac{1}{2^n - 1} \times 100$$

$$\begin{aligned} \text{Dynamic Range} &= (6n + 1.76) \text{ dB} \\ &\approx 6n \text{ dB} \end{aligned}$$

Resolution

$$\frac{1}{2^{10}} = \frac{1}{1024} = 0.0009765625$$

57

$$VFS = 10.24$$

$$n = 10$$

$$\text{Resolution} = \frac{10.24}{n} = \frac{10.24}{2^{10}} = \frac{10.24}{1024} = 10 \text{ mV}$$

$$\text{error} = \pm 5 \text{ V}$$

$$0 \xrightarrow[25^\circ\text{C}]{+50^\circ} \pm 25 \rightarrow 5 \text{ mV}$$

$$1 \xrightarrow[25^\circ\text{C}]{+5^\circ} = 200 \text{ mV}$$

$$6) (a) Y. \text{ Resolution} = \frac{1}{2^{10}} \times 100 = 0.4$$

$$\frac{1}{2^{11}} \approx 0.004$$

$$\frac{1}{2^{11}} \times \frac{1}{250} \approx 0.004$$

\therefore 8 bit

$$8) (ii) n = 10$$

$$\text{range} = 5$$

$$\text{Resolution} = \frac{5}{1023} \approx \frac{5}{1000} \approx 5 \text{ mV}$$

$$16) (i) n = 12$$

$$7) \text{ Resolution} = \frac{1}{2^{12}} \times 100 = \frac{1}{4095} \times 100 \approx \frac{1}{4000} \times 100$$

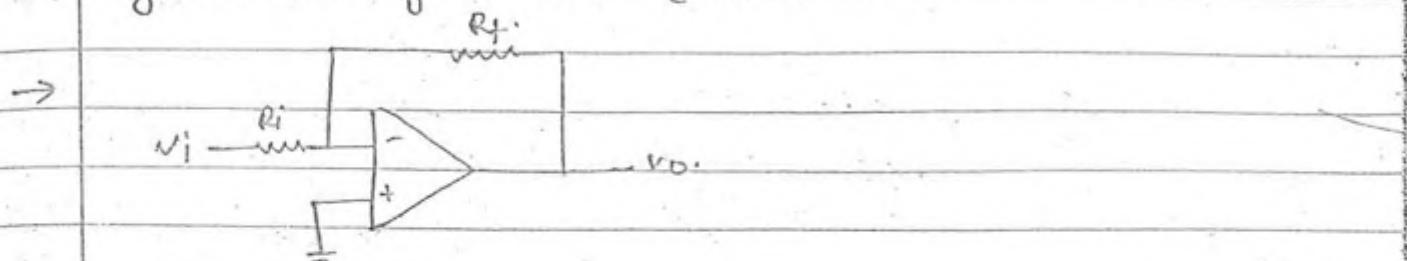
$$= 0.025$$

$$17) \text{ Accuracy (Resolution)} = 10 \text{ mV}$$

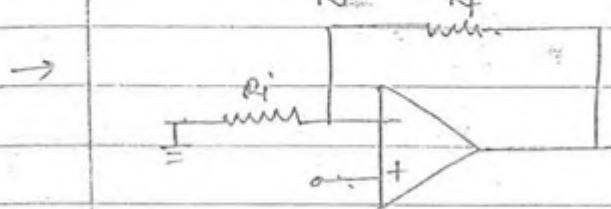
$$\frac{5}{2^{11}} = 10$$

$$n = 9, \frac{5}{2^{10}} = 10 \text{ mV}$$

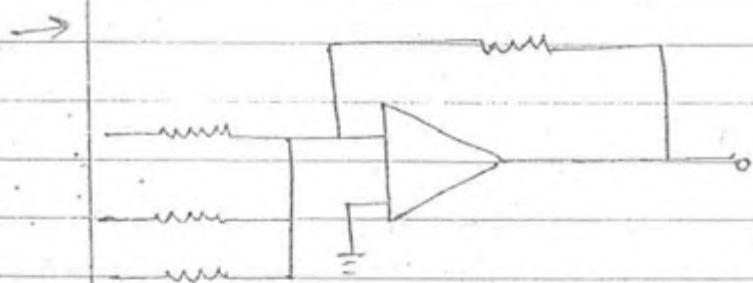
→ Digital to Analog converter (DAC) :-



$$V_o = -\frac{R_f}{R_i} V_i$$

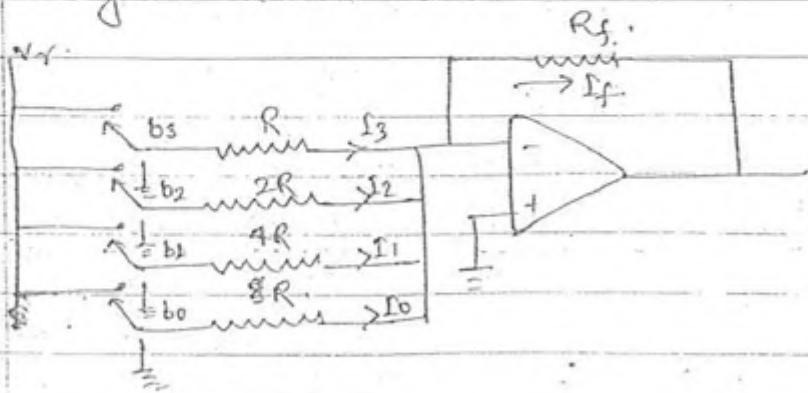


$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_i$$



$$V_o = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \dots \right)$$

→ Weighted Resistor DAC :-



$$I_3 = \frac{V_T}{R} \cdot b_3$$

$$I_2 = \frac{V_T}{2R} \cdot b_2$$

$$I_1 = \frac{V_T}{4R} \cdot b_1$$

$$I_0 = \frac{V_T}{8R} \cdot b_0$$

$$S_f = I_3 + I_2 + I_1 + I_0$$

$$V_o = -S_f \cdot R_f$$

L.S.B Resistance = (2^{n-1}) MSB Resistance

- Not popularly used.
- In weighted resistor DAC, accuracy is less due to use of different resistor. To avoid this R-2R ladder network is used.

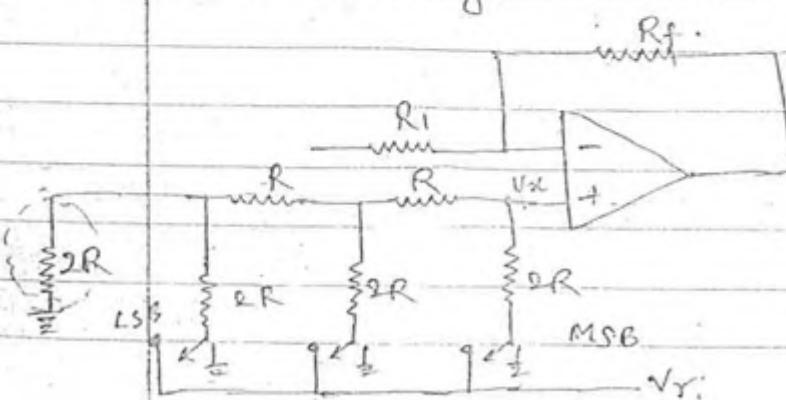
- R-2R Ladder Network :-

Normal Ladder

Inverted Ladder

- 1) Non Inverting
- 2) Inverting

- 3) Non Inverting R-2R Ladder :-



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$$V_o = \left(1 + \frac{R_f}{R_i} \right) V_{xi}$$

Where V_{xi} = Resolution \times Decimal equivalent of binary data.

$$= \frac{V_x}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i$$

$$V_o = \frac{V_x}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i \times \left[1 + \frac{R_f}{R_i} \right]$$

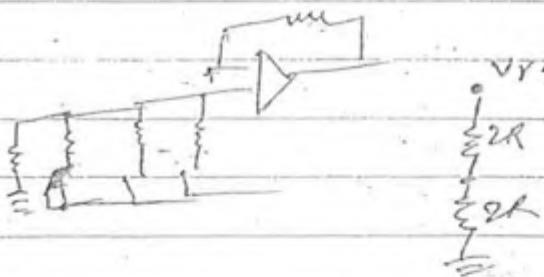
= Resolution \times decimal \times gain.

Note:-

$$b_2 \cdot 2^2 + b_1 \cdot 2^1 + b_0 \cdot 2^0 = \sum_{i=0}^{n-1} 2^i b_i$$

Applying Superposition theorem.

$$V_{xi} = \frac{V_x}{8}$$

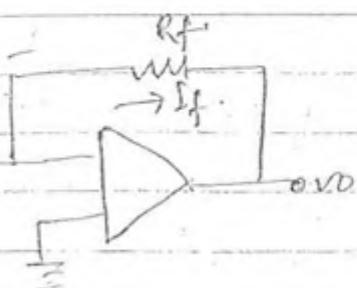
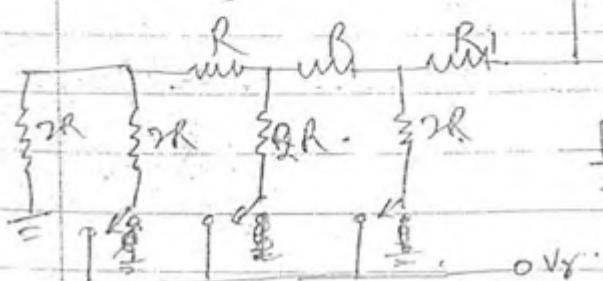


WB

$$\text{II } V_o = \frac{V_x}{2^4} \times 10 \times 8 \\ = 5V$$

Q) Invertin

2) Inverting R-2R Ladder:-



$$V_o = \frac{V_r}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i \times \left[\frac{-R_f}{R_1 + R} \right]$$

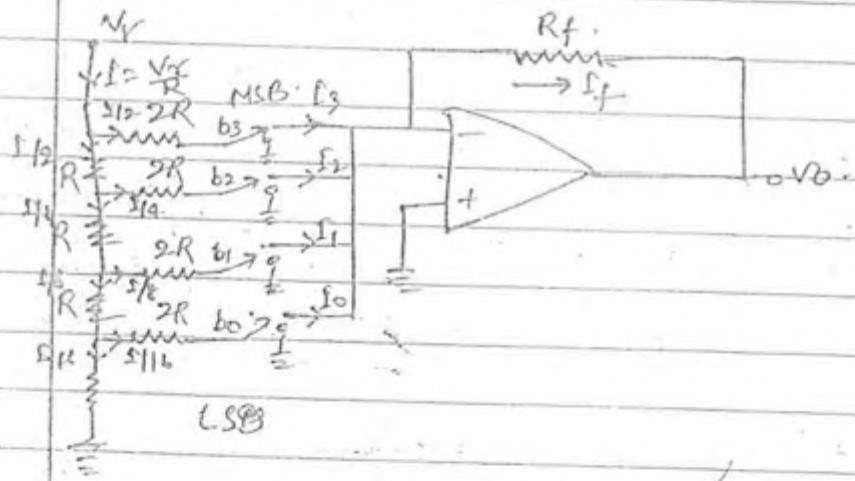
= Resolution \times Decimal \times gain.

$$I_f = \frac{V_r}{2^n} \left(\sum_{i=0}^{n-1} 2^i b_i \right) \times \frac{1}{R_1 + R}$$

P-49
Q22

$$I_o = \frac{V_r}{8/4} \times \frac{1}{3R} = \frac{V_r}{12R}$$

Inverted Ladder DAC :-



- Switch is always ground potential.
- There is no charging or discharging.

$$I_3 = \frac{I}{2} \times b_3 \quad I_1 = \frac{I}{8} \times b_1$$

$$I_2 = \frac{I}{4} \times b_2 \quad I_0 = \frac{I}{16} \times b_0$$

$$I_f = I_3 + I_2 + I_1 + I_0$$

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$$S_f = \frac{1}{2} b_3 + \frac{1}{4} b_2 + \frac{1}{8} b_1 + \frac{1}{16} b_0$$

$$= \frac{1}{16} [8b_3 + 4b_2 + 2b_1 + b_0]$$

$$S_f = \frac{1}{2^n} \sum_{i=0}^{n-1} 2^i b_i$$

$$S_f = \frac{V_r}{2^n} \sum_{i=0}^{n-1} 2^i b_i \cdot \frac{1}{R} \quad \left[\because S = \frac{V_r}{R} \right]$$

$$V_o = \frac{V_r}{2^n} \sum_{i=0}^{n-1} 2^i b_i \left[-\frac{R_f}{R_B} \right]$$

W.B
Q15
Wk 20

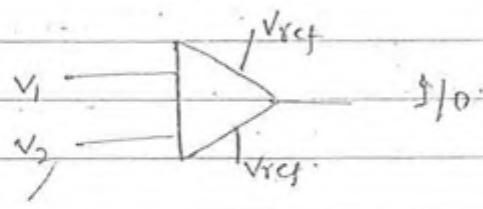
$$V_o = \frac{10}{16} \times 5 \times \left[-\frac{R_f}{R_B} \right] = -3.125$$

0101 = 5 ✓

$$2) V_A = \frac{4 \times 2}{8^4} = 1$$

★ Analog To Digital Converter :→

1) Counter Type ADC :→

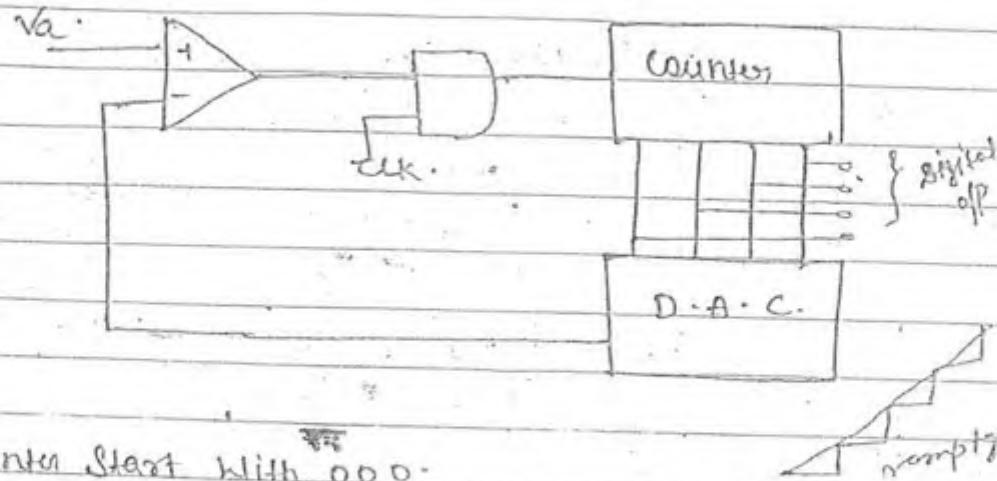


$$V_1 > V_2 \rightarrow +V_{ref} \rightarrow 1$$

$$V_1 < V_2 \rightarrow -V_{ref} \rightarrow 0$$

2) (a)

q)



- Counter starts with 000.
- In Counter-type ADC - a comparator is used at I/P stage to compare I/P Analog voltage with reference voltage provided by DAC feedback.
- A Counter is used to count no. of clk pulses applied.
- If analog voltage is greater than reference voltage then O/P of comparator of logic 1 & counter will continuously count clock pulse. If $V_a < V_r$, comparator O/P is 0 and counter will stop. At this time O/P of counter will provide binary O/P proportional to analog voltage (V_a).
- Maximum no. of clock pulses required for n-bit conversion is $2^n - 1$.
- Maximum conversion time = $(2^n - 1) T_{clk}$.
- Conversion time depends on I/P analog voltage.
- Counter-type ADC also known as ramp type ADC.

* Parallel Comparator Type:-

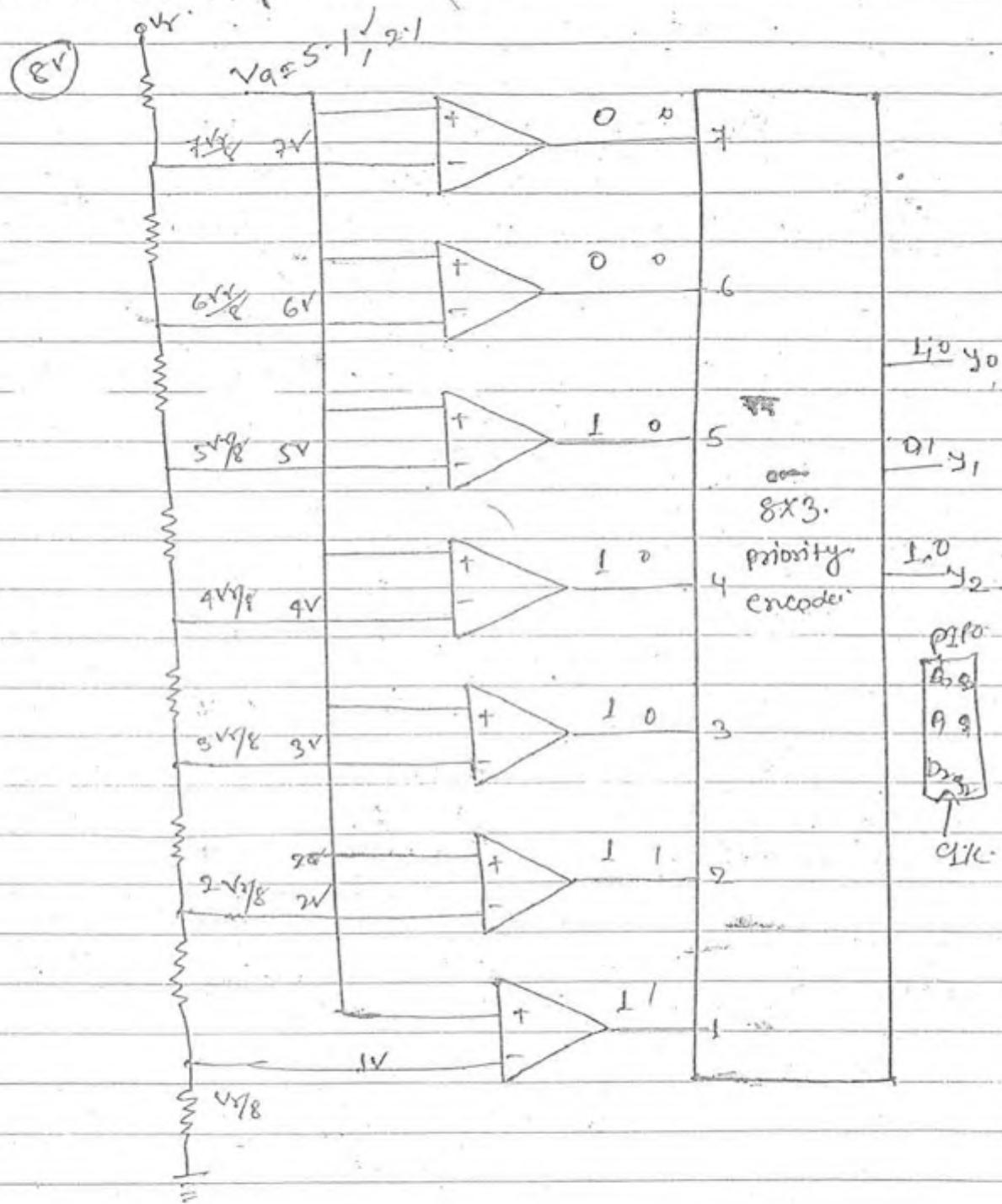
n bit $\rightarrow 2^n - 1$ comparators

Other require:-

2^n resistor

$2^n \times n$ priority encoder

3 bit Parallel Comparator ADC: →



Parallel comparator ADC is the fastest ADC among all.

Max^m no. of CLK pulse for n bit $\overset{\text{converted}}{=}$ 1 CLK pulse.

Range of Analog voltage
 $V_a > 7V_r/8$

Binary o/p:
 111

$$\frac{6V_r}{8} < V_a < \frac{7V_r}{8}$$

110

$$\frac{5V_r}{8} < V_a < \frac{6V_r}{8}$$

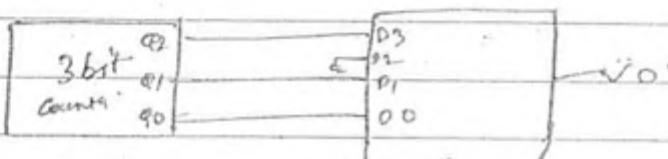
101

~~Range~~
 :

$$V_a < \frac{V_r}{8}$$

000

P_{Q14}⁹⁵

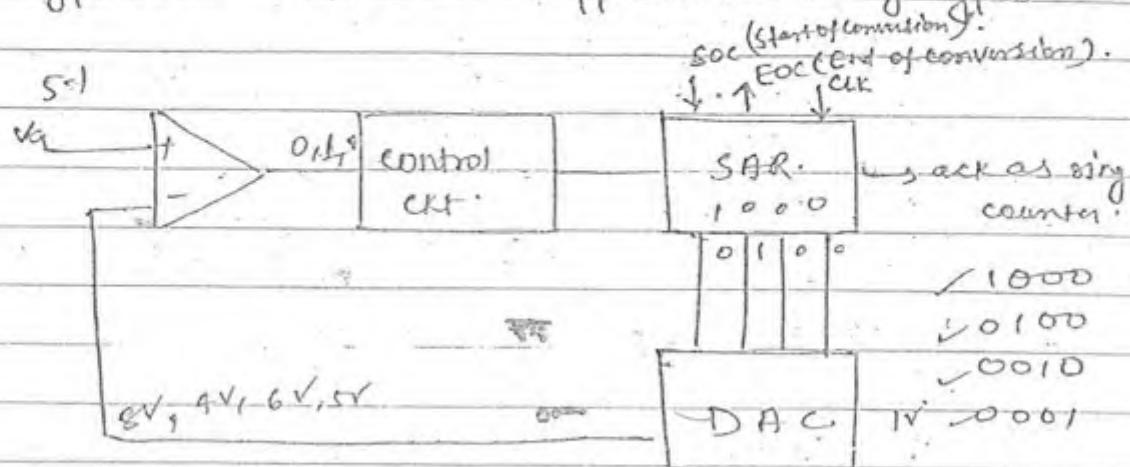


000	0000
001	0001
010	0010
011	0011
100	1000
101	1001
110	1010
111	1011



* SAR Type ADC (Successive)

* SAR Type ADC (Successive approximation reg. type) :-

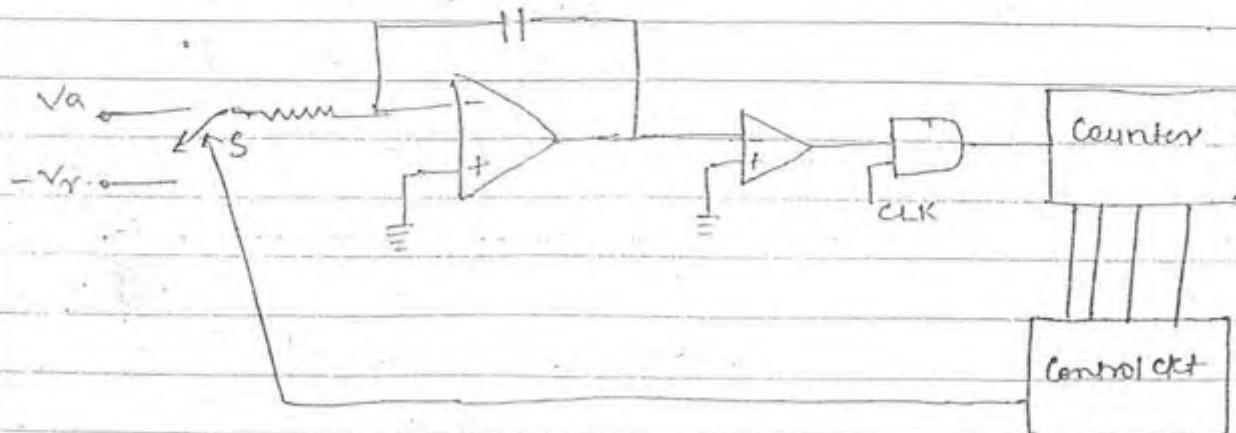


Ring Counter \rightarrow Set

Control ckt to reset ($V_a < V_r$)

- \rightarrow In SAR type ADC ring counter will present to successively to set the bit.
- \rightarrow Control ckt is used to reset previously set bit when $V_a < V_r$
- \rightarrow In SAR type ADC, n clk pulse required for n -bit conversion.
- \rightarrow Conversion time = $n T_{clk}$.
- \rightarrow In SAR type conversion time is uniform for any analog voltage (Independent of analog voltage)
- \rightarrow Mostly used in digital IC to provide interfacing with microprocessor

* Dual Slope Integrating Type ADC :-



Note:-

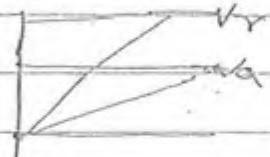
$$\rightarrow V_o = -\frac{1}{Rc} \int v_i dt$$

$$= -\frac{v_i}{Rc} \int dt$$

[$v_i = \text{const}$]

$$= -\frac{v_i}{Rc} \cdot t$$

$$\rightarrow |V_o| < |V_g|,]$$



→ In fast dual slope ADC a counter is used to count CLK pulses.

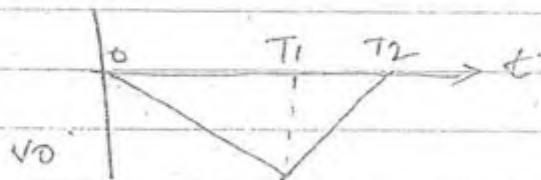
→ When conversion is started initially counter is reset to 0 and switch 'S' is connected to analog voltage V_g .

→ When integrator is integrating analog voltage off of integrator become -ve voltage. Due to this counter Comparator off is logic 1 & counter will continues CLK pulse.

→ After N^{th} CLK pulse again counter value becomes 0. At this time (T_1) Control CLK will connect switch S to reference voltage $-V_r$.

→ During reference voltage integration upto T_2 time O/P of integrator is -ve voltage due to this counter will again continues CLK pulse. At time T_2 O/P of integrator becomes +ve & Comparator o/p will become 0 due to this counter will stop.

→ Let N is the count when counter is stop.



$$T_1 = 2^{th} \text{ CLK}$$

$$T_2 - T_1 = N \text{ CLK}$$

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$$V_o = -\frac{V_a}{Rc} T_1 + \frac{V_r}{Rc} (T_2 - T_1) \quad \dots \text{(1)}$$

At time $t = T_2$

$$V_o = 0$$

∴ from Eqn (1)

$$0 = -\frac{V_a}{Rc} T_1 + \frac{V_r}{Rc} (T_2 - T_1)$$

$$\frac{V_a}{Rc} T_1 = \frac{V_r}{Rc} (T_2 - T_1)$$

$$V_a 2^n T_{clk} = V_r N T_{clk}$$

$$V_a = \left(\frac{V_r}{2^n} \right) N$$

$$\text{if } V_r = 2^n$$

$$V_a = N$$

Above all ADC, dual slope ADC is most accurate

$$\text{No. of CLK pulses} = 2^n + N$$

It is mostly used in digital voltmeter.

$$\text{Maximum No. of CLK} = 2^n + 2^n - 1$$

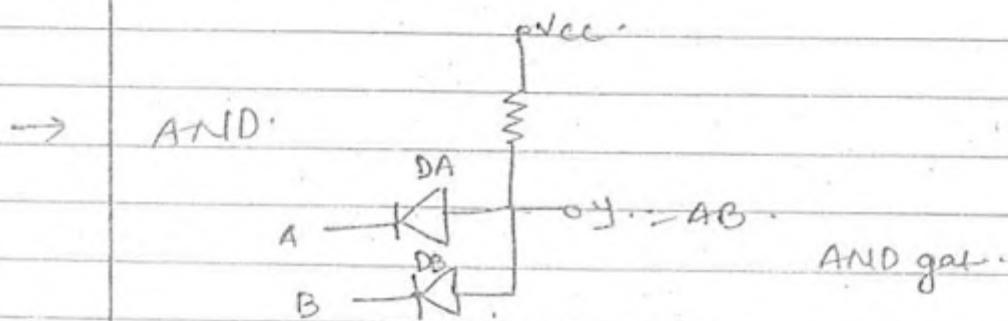
$$\approx 2^{n+1} - 1$$

So it is slowest ADC among all ADC.

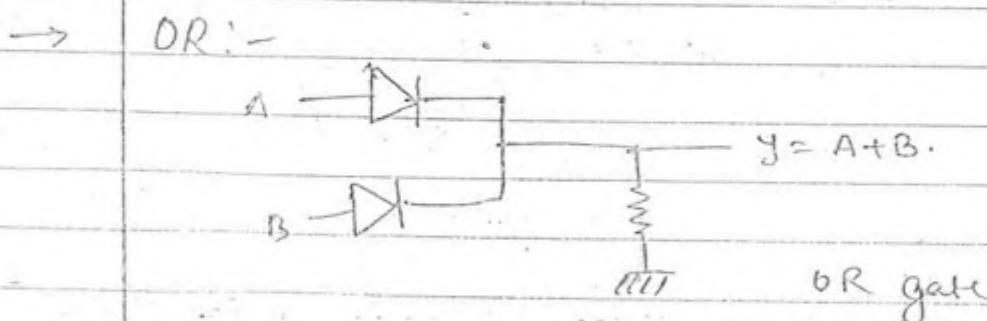
Counter type $\rightarrow 2^n - 1$ SAR $\rightarrow n$ flash $\rightarrow 1$ Dual $\rightarrow 2^{n+1}$

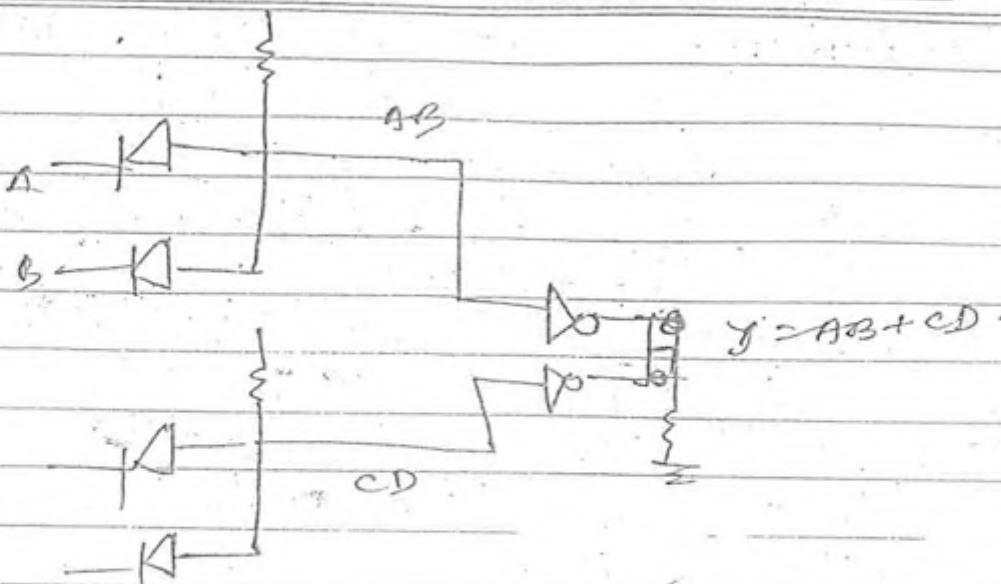
Logic families

- 1 DTI
- 2 TTL
- 3 ECL
- 4 NMOS
- 5 CMOS
- 6 RTL
- 7 DCTL
- 8 I²L
- 9 HTL
- 10 PMOS.

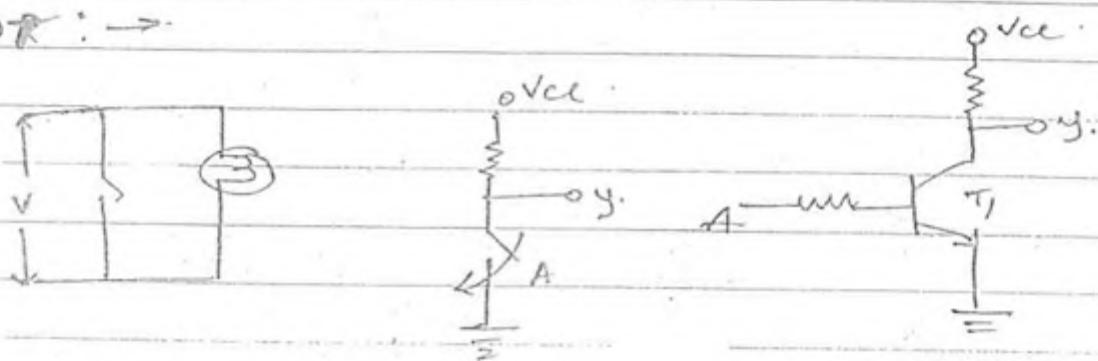


A	B	DA	DB	y
0	0	ON	ON	0
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	1 (Vcc)





→ NOR Gate :-



A y

0 1

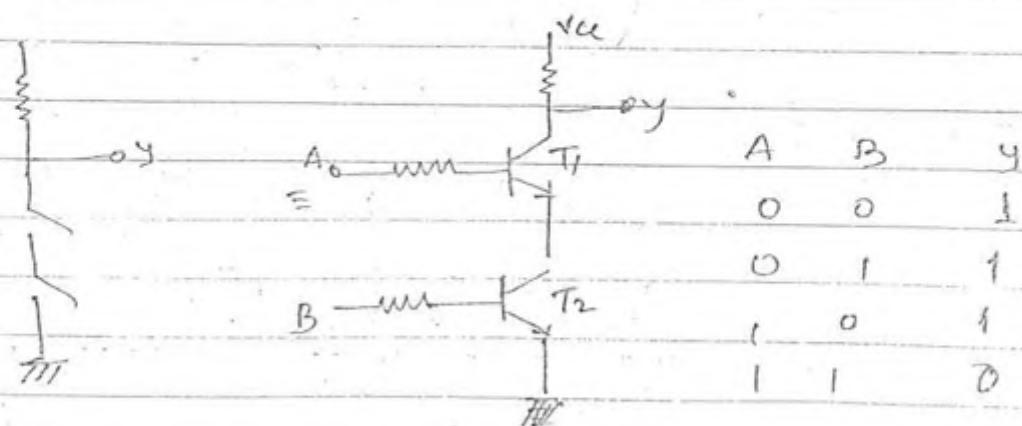
1 0

A T_1 y

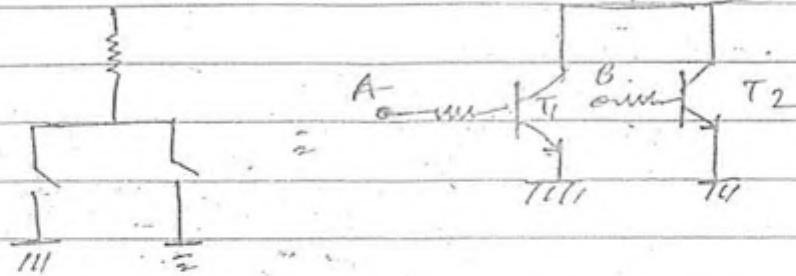
0 OF

1 ON

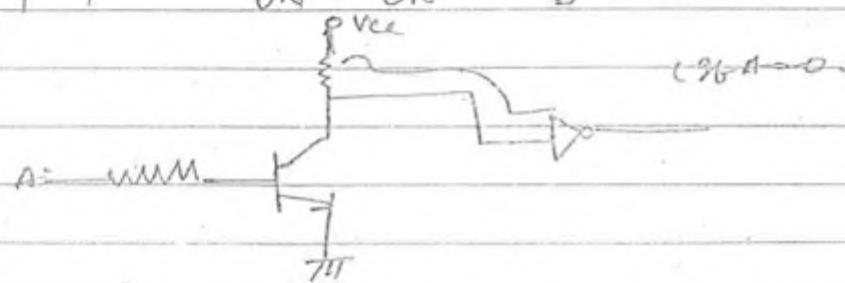
→ NAND Gate:-



→ NOR Gate :-



A	B	T ₁	T ₂	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0



→ When logic gate output is 1 (T₂ is OFF) it will act as current source.

→ When output is logic 0 (T₂ is ON) it will act as current sink.

→ Transistor:

J _{EB}	J _{CB}	
R.B	R.B	Cut-off
F.B	R.B	Active
R.B	F.B	Reverse active
F.B	F.B	Saturation

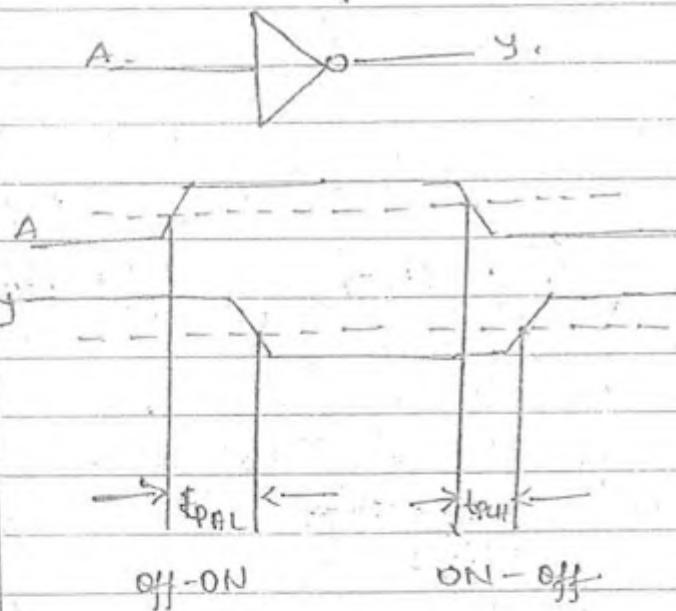
In Cut-off & Saturation region transistor act as a switch.

* Characteristics of logic family :-

- 1) t_{pd}
- 2) PDs.
- 3) figure of merit.
- 4) fan out.
- 5) Noise Margin.
- 6) Wired logic.
- 7) fan out.

1) Propagation Delay (t_{pd}) :-

It is measured in ns.



In transistor ON-OFF time is more compared to OFF-ON time due to saturation or storage time.

$$t_{pd} = \frac{t_{pd, off} + t_{pd, on}}{2} \text{ ns.}$$

2: Power Dissipation (P_{Diss}) :-

→ Power dissipation represent power dissipated open logic gate

→ 1st unit is mW.

$$P_{Diss} = V_{cc} \cdot I_{avg}$$

3: Figure of Merit :-

Product of propagation delay & power dissipation.

$$\text{figure of Merit} = P_{Diss} \cdot t_{pd}$$

mW x ns.

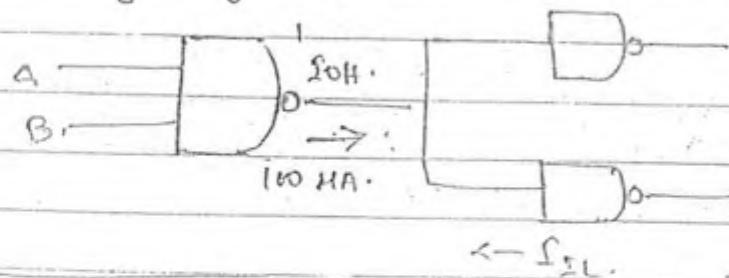
PJ:

1st unit is PJ.

~~I²L~~ has best figure of merit among all logic family.

4) fan-out :-

It is the max^m no. of logic gates that can be driven by logic off.



$$\text{fan out}_H = \frac{f_{OH}}{f_{IH}}$$

• Current source.
logic 1.

$$\text{fan out}_L = \frac{f_{OL}}{f_{IL}}$$

• Current sink.
logic 0.

fan out = (f_{outH} , f_{outL}) min.

Q. In TTL logic family.

$$I_{OH} = 400 \text{ mA}$$

$$I_{IH} = 40 \text{ mA}$$

$$I_{OL} = -16 \text{ mA}$$

$$I_{IL} = 1.6 \text{ mA}$$

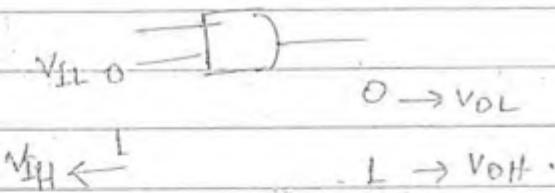
then fan out of logic family.

$$\text{Sol: } \frac{I_{OH}}{I_{OL}} = \frac{400}{16} = 10$$

$$\frac{I_{OL}}{I_{IL}} = \frac{16}{1.6} = 10$$

5) Noise Margin \rightarrow

It is the maximum noise voltage that can be added to a logic family without affect the O/P.



$$V_{OH} > V_{IH} > V_{IL} > V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

Ex. B

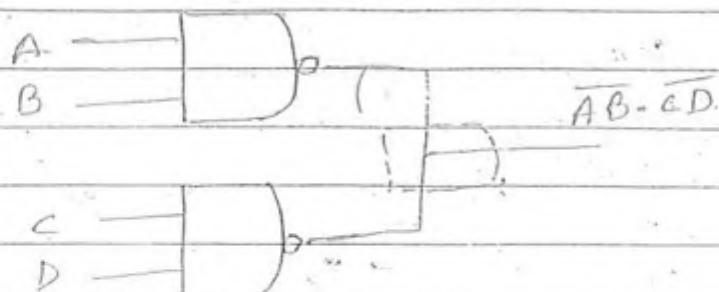
$$L(\Phi) 1/3 \quad V_{OH} = 3.8 \quad] 0.7V \rightarrow NM_H \\ V_{IH} = 3.1V$$

$$V_{IL} = 2.0 \quad] 0.7V \rightarrow NM_L \\ V_{OL} = 0.7$$

$$NM = (NM_L, NM_H)_{\min}$$

6>

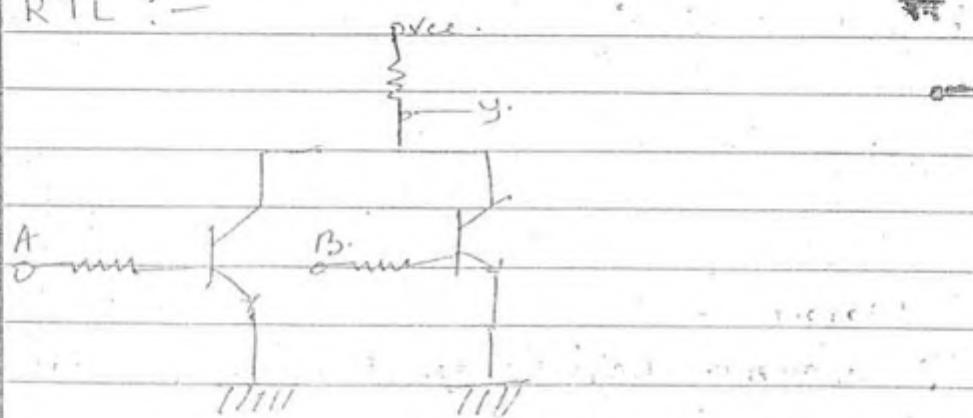
Wired logic:



[Wired AND]

* >

RTL :-

1> Basic gate : \rightarrow NOR2> $t_{pd} = 50\text{ ns}$.3> $P_{diss} = 10\text{ mW}$

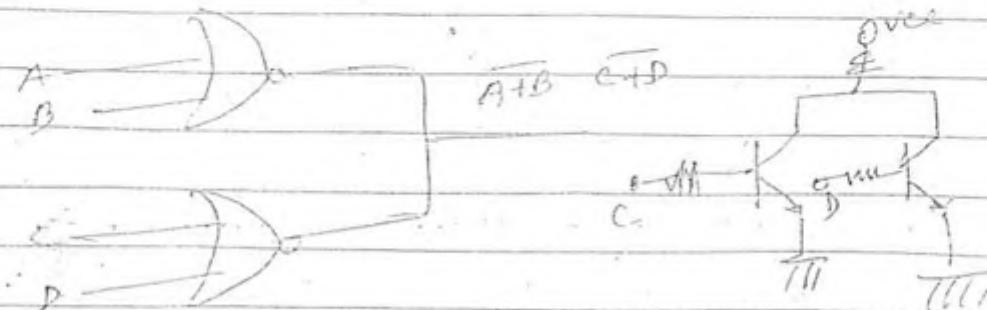
4> figure of Merit = 500PJ.

5> NM = 0.2V

6> fanout = 3

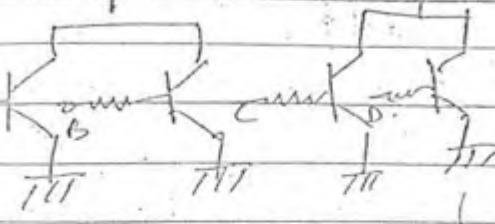
7> Wired AND

8>



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A	B	C	D	Y
0	0	0	0	1
0	0	1	0	0
0	0	1	1	0



Disadvantages of RTL :-

Low speed of operation.

Lower fan out.

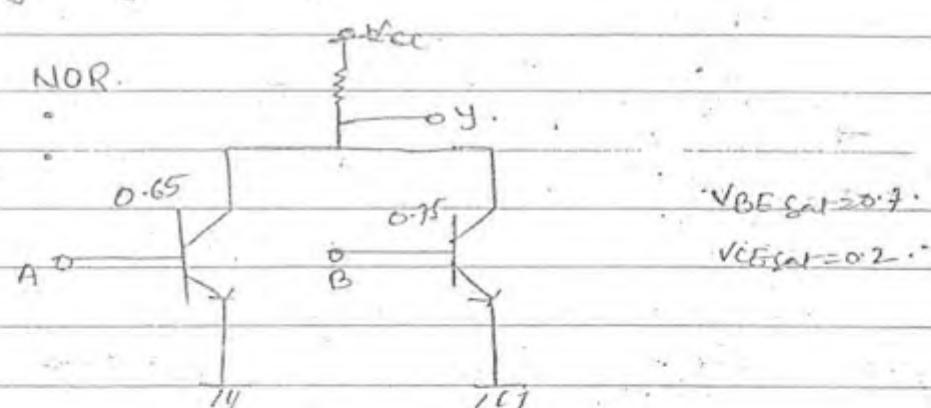
Low noise margin.

* DCTL (Direct Coupled Transistor Logic) :-

In RTL logic family if CCP transistor are removed then the resulting logic family is DCTL.

→ $t_{pd} = 40\text{ns}$

→ Basic gate \rightarrow NOR.



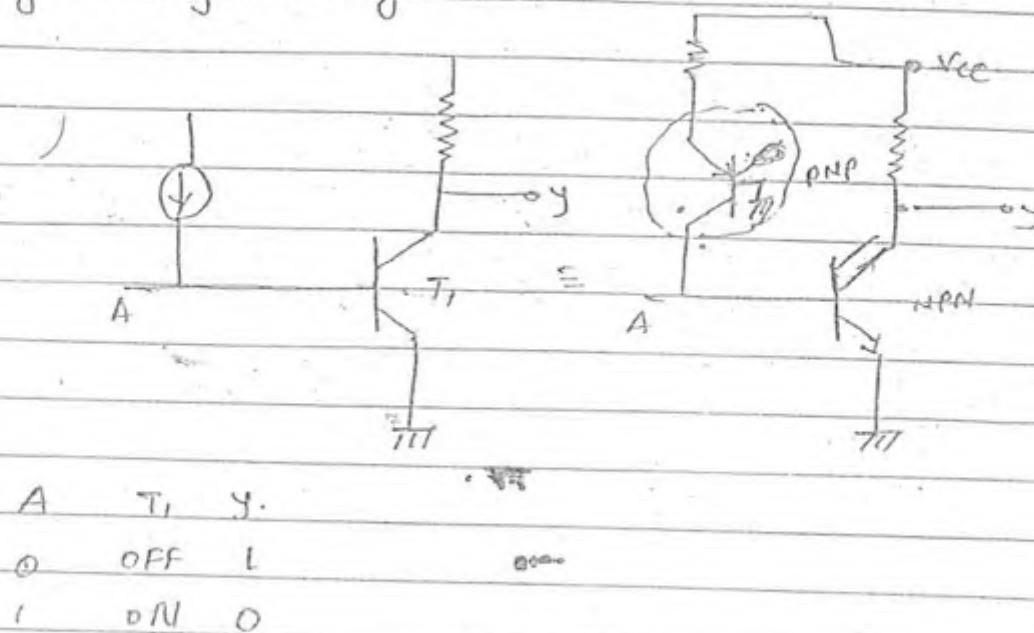
A	B	T ₁	T ₂	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	OFF	0

Disadvantages:-

→ Current fogging

In DCTL logic family if ~~TR have~~ different characteristic are used the TR have lower VBE_{sat} first become ON when it will not allow other TR to OFF. This is known as current fogging.

Integrated Injection Logic (I^2L): →



→ Fan out = 8 (due to multiple character)

→ $t_{pd} = 40\text{ ns}$.

→ Figure of Merit = $0.1P_J - 0.7P_J$.

→ Rate.

→ SST 1 to 12

MSS 13 to 99

LSS 100 - 1000

VLSI > 1000

→ In I^2L logic family due to integration of PNP & NPN tr it occupies less area. honey densities are more

→ It is mostly used in MSS & LSS logic family

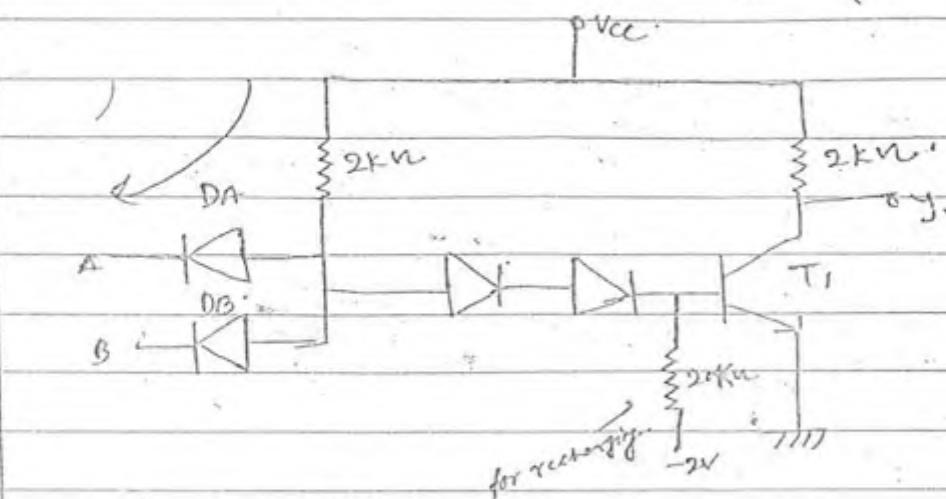
→ Due to use of multi character OIP fan out is increased.

→ MTL (Merged Transistor logic) - other name.

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A) DTI (Diode Transistor logic family 1) :-



A	B	T ₁	Y
0	0	OFF	1
0	1	OFF	1
1	0	OFF	1
1	1	ON	0

→ Operation :-

The ckt shown in fig is known as basic DTI gate. In this any I/P is low, all the I/P are low, Diode DA and DB will become forward bias while as D₁ & D₂ will become reverse bias due to this Tr T₁ is OFF & O/P is 1.

In them all the I/Ps as high DA & DB will become reverse bias & D₁ & D₂ will become forward bias & Tr T₁ is ON & O/P is low.

→ Basic gate - NAND

→ t_{pd} = 30ns.

→ P_{diss} = 8mW

→ Figur of Merit = 240 pJ

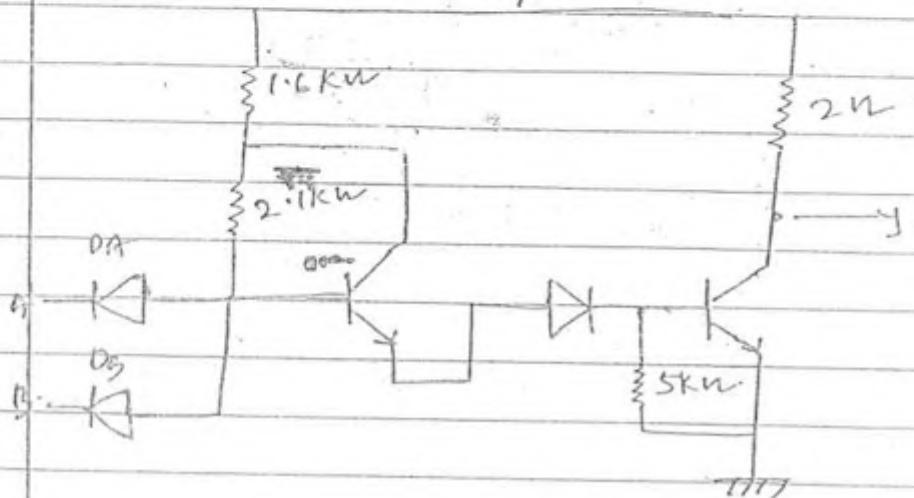
→ Noise Margin = 0.75V

→ fan out = 3 (low)

→ Wired AND

* Standard Diode Transistor logic

+ve p.v.c

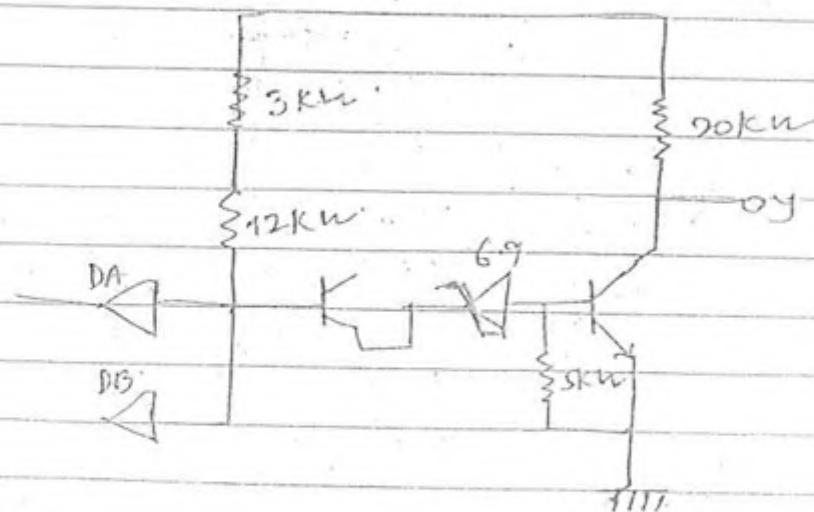


Fan out = 8

$$P_n = kTB$$

$$V_n = \sqrt{4kT_B}$$

* High Threshold Logic family (HTL) :-



Advantage

→ Noise margin $\rightarrow 4 - 5 V$ (highest)
logic

ii) logic 0 = 2V

logic 1 = 12V

iii) High voltage swing.

iv) $t_{pd} = 90\text{ ns}$

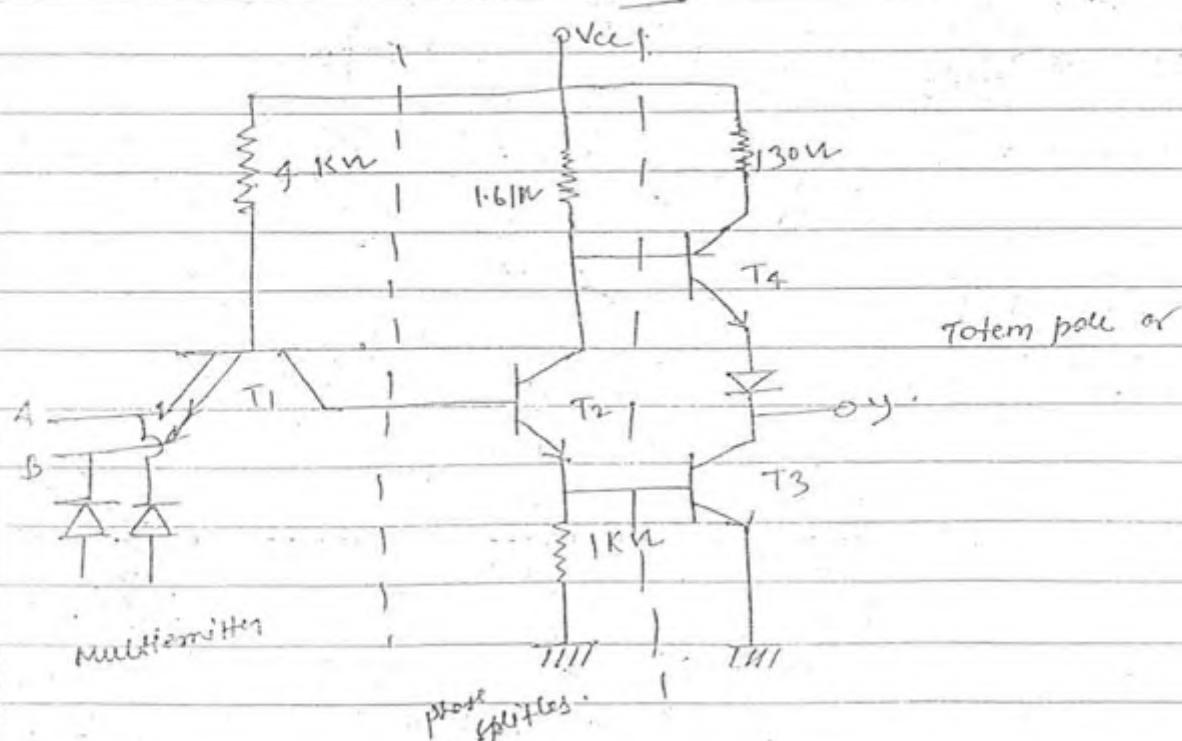
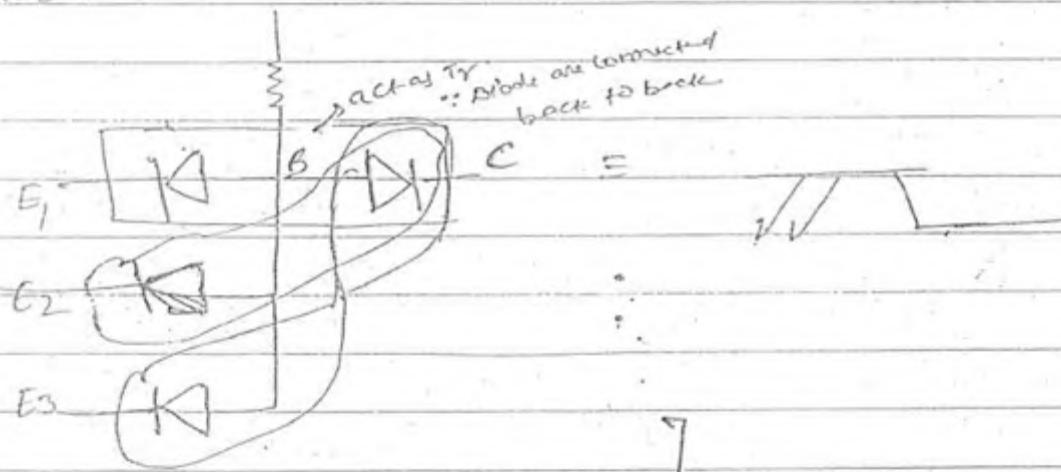
v) Power dissipation = 55 mW

vi) figure of Merit $\approx 5000 \text{ PJ}$.

vii) Fan-out = 10

* Transistor Transistor logic family (TTL)

[Note:-



A	B	T ₁	T ₂	T ₃	T ₄	Y
0	0	A	C	C	S	1
0	1	A	C	C	S	1
1	0	A	C	C	S	1
1	1	R	S	S	C	0

The CKT shown in fig. is Standard TTL. It basically have three states.

- 1) Multi Emitter IIP Stage.
- 2) Phase Splitter
- 3) Totem pole O/P stage or Active pulling O/P stage.

Operations:-

In this any IIP are low or all the IIPs are low then Emitter base junction of T₁ is forward biased & collector base junction of T₁ is reversed biased (Tr₁ is in active mode)

Due to this Tr₂ & Tr₃ is OFF while as Tr₄ is in saturation hence O/P is 1.

In them all the IIP are high then EB junction of T₁ is reversed biased while as C-B junction is forward biased (Mode \rightarrow Reverse active)

Due to this T₂ & T₃ are in saturation T₄ is in cut-off hence O/P is zero.

$$V_{IH} = 2.0 \text{ V}$$

$$V_{OH} = 2.4 \text{ V}$$

$$V_{SL} = 0.8$$

$$V_{PH} = 0.4$$

1) Fan out = 10

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- ii) $t_{pd} = 10 \text{ ns}$
- iii) $P_{diss} = 10 \text{ mW}$
- iv) figure of merit = 100 P.J
- v) Noise Margin = 0.4 V

Q8 (b)

→ Diode D is used to cut-off Transistor T₂ when T₁ is ON

→ Advantage of Totem pole:

- i) Lower Pdiss.
- ii) Highest speed of operation & higher fanout

Disadvantages:-

→ It is not used in wired logic.

→ To provide wired AND logic open collector configuration is used.



~~w.B.g~~ (a)

→ 300Ω Resistor is used in collector lead of ~~T₂~~ to reduce noise or generation of high freq. operation.

in O/P close

→ Clamping diodes are connected at S/P stage to protect T₁ during high freq. of operation (ringing).

* Different types of TTL :-

- 1) Standard TTL
- 2) High Speed
- 3) Low power
- 4) Schottky TTL.

2) High Speed TTL :-

In Standard TTL logic family if resistor values are reduced the propagation delay will reduce, then the resulting logic family is known as high speed TTL.

$$t_{pd} = 6 \text{ ns.}$$

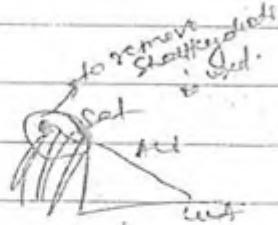
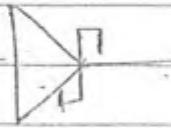
→ Disadvantages:-

Dissipation is increase.

3) Low Power TTL :-

In TTL logic family if resistor values are increased then power is reduced & resulting logic family is known as low power TTL.

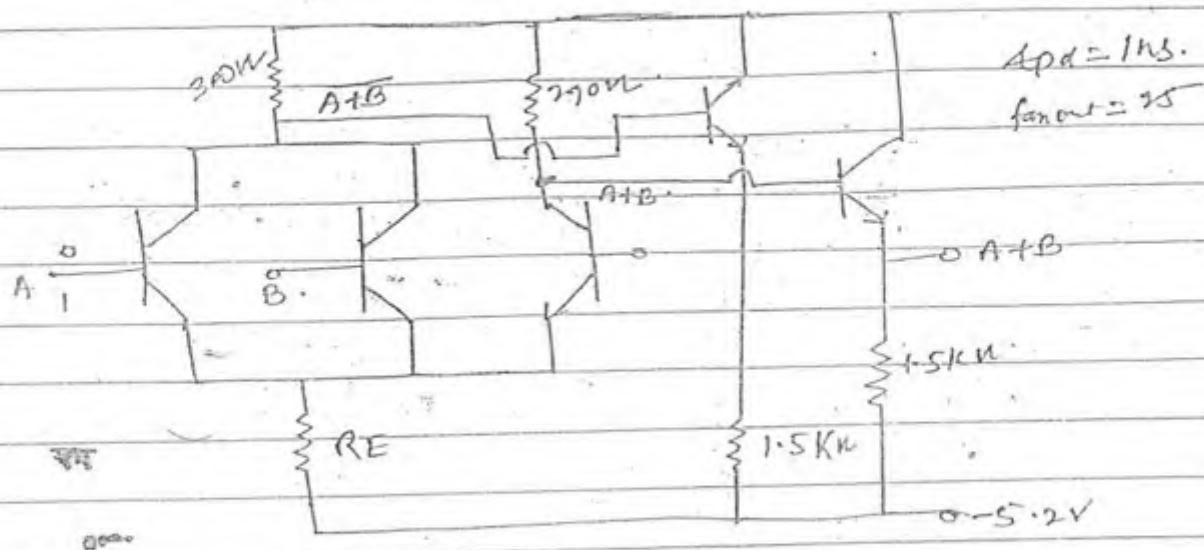
4) Schottky TTL :-



If Schottky diode is used b/w C-B region then it will remove storage time or saturation delay resultant logic family is known as Schottky TTL

$$t_{pd} = 2 \text{ ns.}$$

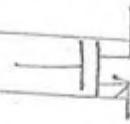
* Emitter Coupled Logic Family [ECL] :→



- i) It is the fastest logic family because it is non-saturated logic family.
- ii) In this Tr is operated in cut-off & active mode.
- iii) It basically contain two stage
- A) Differential Amplifier S/P Stage.
- B) Common collector emitter follower S/P Stage.
- iv) Due to use of differential amplifier complementary O/P are available in ECL family (NOR or OR gate)
- v) Due to use e-e stage in the S/P fan out is also high.
- vi) ECL logic family uses -ve power supply due to this any power supply spikes, blinks will not affect.
- vii) $P_{diss} = 50 \text{ mW}$.
- viii) $t_{pd} = 1 \text{ ns}$.
- ix) figure of Merit = 55 PJ.
- x) fan out = 25
- xi) Noise Margin = 0.3V
- xii) logic 0 → -1.7V
1 → -0.85V
- xiii) It will provide wired OR gate.

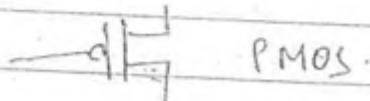
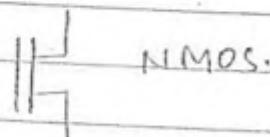
$$\begin{array}{c} A \\ \oplus \\ B \end{array} \rightarrow Y = \overline{A \oplus B} + \overline{B} \cdot D$$

* NMOS : →



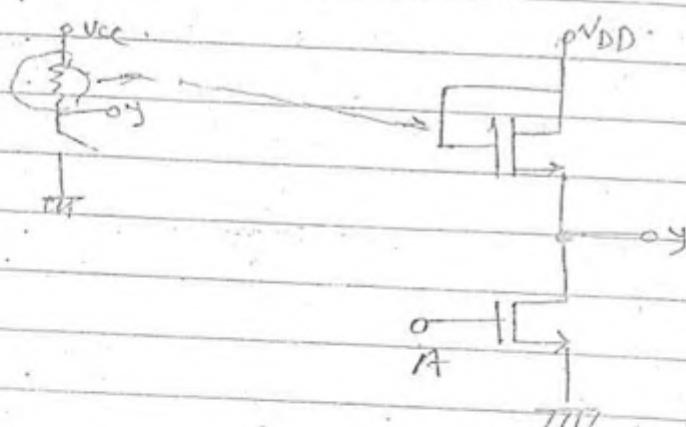
		T_r	P MOS.
a.	K _N Substrate.	0V → OFF	ON
		$V_{GS} \rightarrow ON$	OFF

In n-channel MOSFET logic 0 it is OFF & logic 1 is ON
In P-channel MOSFET logic 0 it is ON & logic 1 is OFF.



→ NMOS :

NOT :- (NMOS NOT)

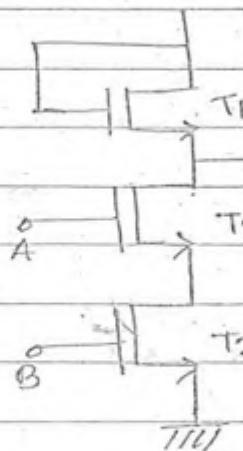


A ↑
Y ↓

0 OFF 1.

1 ON 0'

→ NMOS NAND



A	B	T _D	T ₃	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

$$\Sigma B \cdot D = (A \bar{B}) + (\bar{A}B) + (\bar{A}\bar{B}) = A(B+C) + DE$$

$$\rightarrow t_{pd} = 2.50 \text{ ns}$$

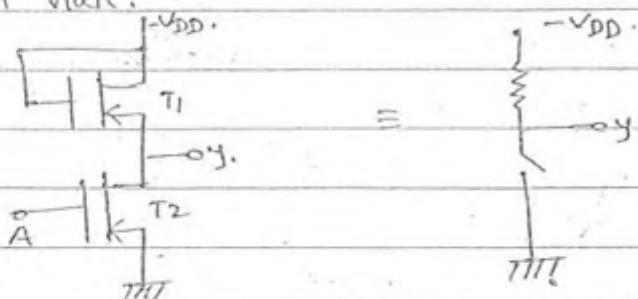
$$\rightarrow P_{diss} = 1 \text{ mW}$$

$$\rightarrow \text{figure of Merit} = 2.50 \text{ PS}$$

$$\rightarrow \text{Fanout} = 5$$

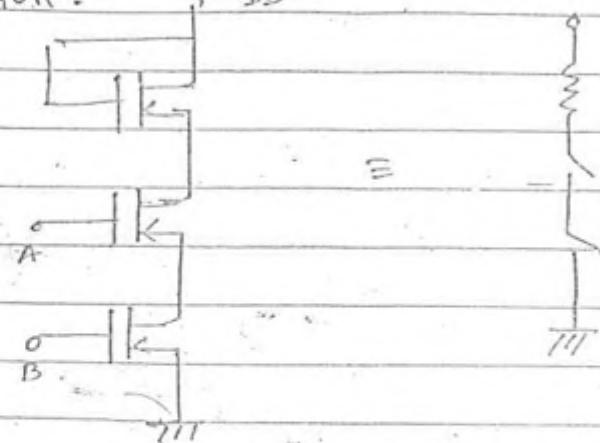
$$\rightarrow \text{Noise Margin} = 1.5V$$

★ PMOS NOT Gate:



A	T ₂	O/P voltage	Y
0	ON	GND	1
1	OFF	-V _{DD}	0

→ PMOS NOR :- V_{DD}



A B Y

0 0 1

0 1 0

1 0 0

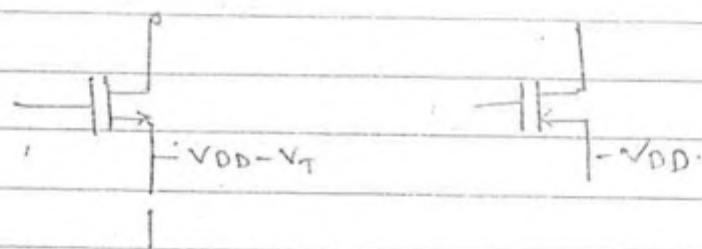
1 1 0

$t_{pd} = 300\text{ns}$

$P_{diss} = 0.2 \text{ mW}$

$f_{Figuresq_MHz} = 60 \text{ Pj}$

* CMOS



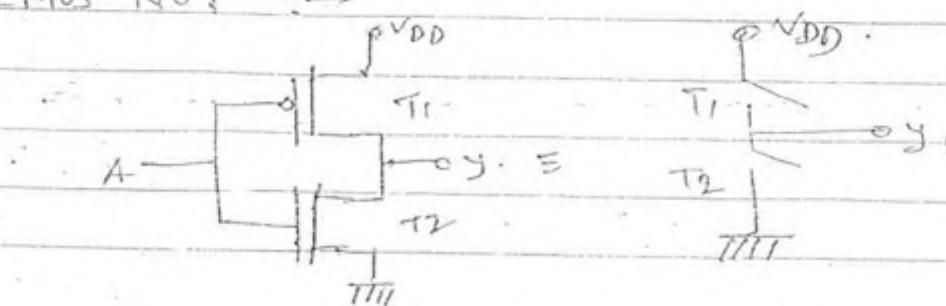
PMOS \rightarrow Strong $\rightarrow 1$

\rightarrow Weak $\rightarrow 0$

N MOS \rightarrow Strong $\rightarrow 0$

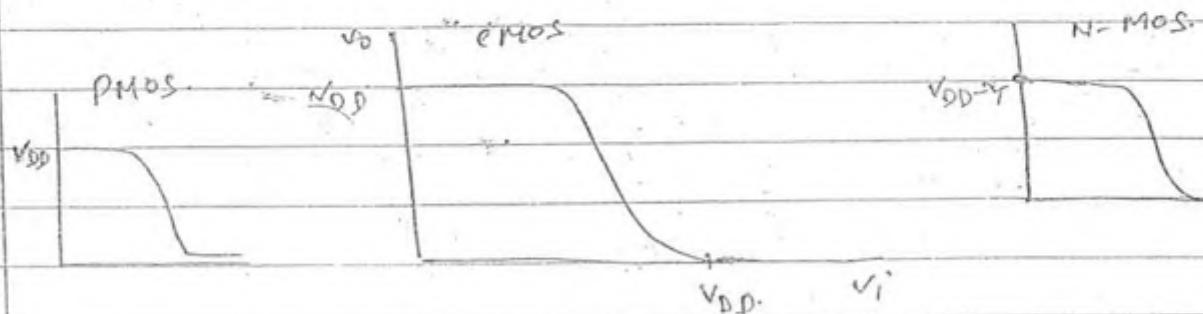
\rightarrow Weak $\rightarrow 1$

→ CMOS NOT \rightarrow



A	T ₁	T ₂	Y
0	ON	OFF	1
1	OFF	ON	0

→ Transfer characteristic :-



Advantages

Lowest Power dissipation

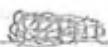
$$P_{diss} = 0.01 \text{ mW} \quad (\text{Station})$$

$$t_{pd} = 0.7 \text{ ns.}$$

$$\text{Figure of Merit} = 0.7 \text{ PJ.}$$

$$\text{Fanout} = 50 \quad (\text{High})$$

$$\text{Noise Margin} \approx \frac{V_{DD}}{2} \quad (\text{good})$$



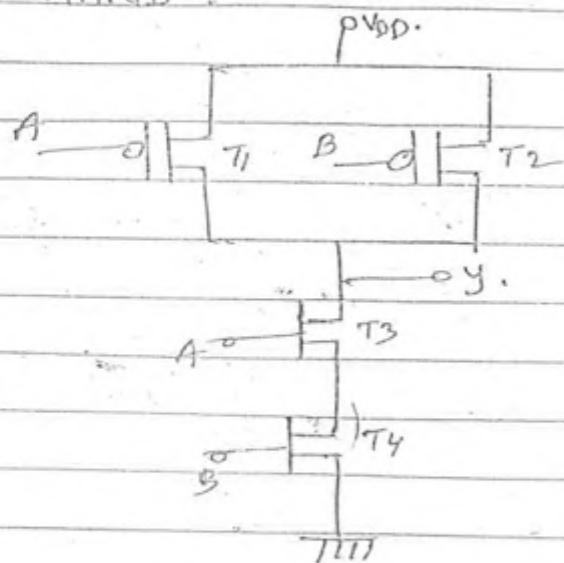
→ Power dissipation :-

1) Static → During logic 0 or logic 1.

2) Dynamic → $0 \rightarrow 1$ or $1 \rightarrow 0$

$$\propto C \cdot f^2 \cdot V_{DD}^2$$

→ CMOS NAND :-



A	B	T ₁	T ₂	T ₃	T ₄	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

(a) (b)

i) CMOS. $\rightarrow V_{DD}/2$

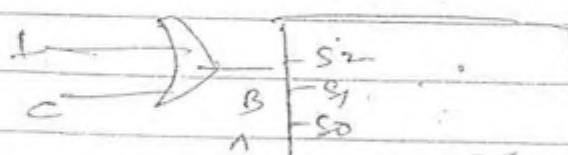
ii) DTC. $\rightarrow 0.75V$

iii) RTL. $\rightarrow 0.2V$

iv) ECL. $\rightarrow 0.3V$

q)

(b)



S₂ : S₁ : S₀

1	0	0	X ₄	0
1	0	1	X ₅	1
1	1	0	X ₆	1
1	1	1	X ₇	0

A ⊕ B

* Binary To Gray Code Conversion : →

* Gray code : →

→ Gray code is unweighted code.

→ Successive no. will differ by only 1 bit.

→ unidistance code (UDC)

→ Cyclic

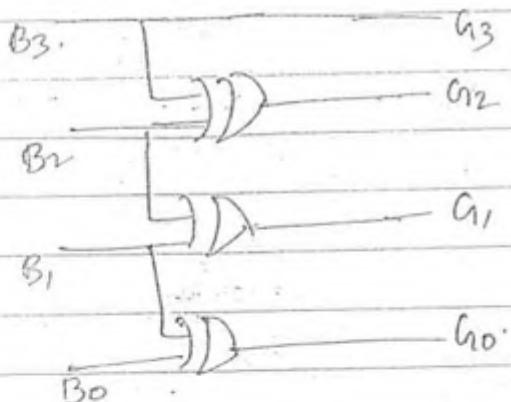
→ Repetitive

→ Minimum entropy code.

$B_3 \ B_2 \ B_1 \ B_0$

1 0 1 1
 ↗ ↗ ↗ ↗
 1 1 1 0

$G_3 \ G_2 \ G_1 \ G_0$

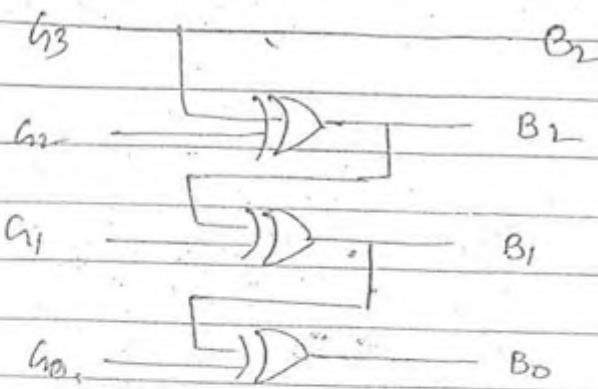


* Gray To Binary Conversion →

$G_3 \ G_2 \ G_1 \ G_0$

1 1 1 0
 ↘ ↘ ↘ ↘
 1 0 1 1

$B_3 \ B_2 \ B_1 \ B_0$



Data Representation

Magnitude

Signed

No. Signbit

↓
zero

+ve

unsigned
↓
+ve, -ve

Complement

1's

+ve, -ve

2's.

+ve, -ve

One extra bit \rightarrow sign.

Sign \rightarrow MSB.

MSB \rightarrow 0 \rightarrow +ve.

\rightarrow 1 \rightarrow -ve.

Ex :-

+6

110

0110

0110

0110

-6

X

1110

1001 · 1010

- In all representation +ve no. are represented in a similar way
- To represent -ve no. in sign magnitude only sign bit is changed. i.e.
- In 1's complement, to represent no. -ve no., first write +ve no. then 1's complement

5 (d)

6 (a)

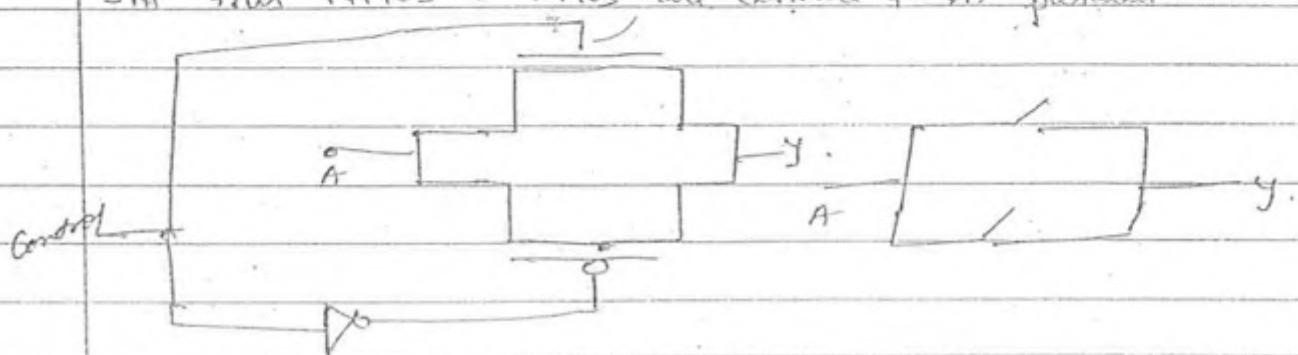
7 (d)

14) (d)

15 a

★ Transmission Gate :-

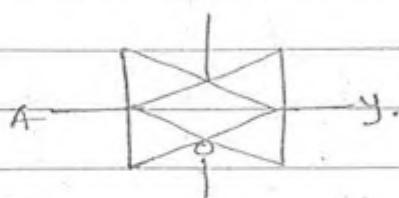
Q1) This NMOS & PMOS are connected in parallel.



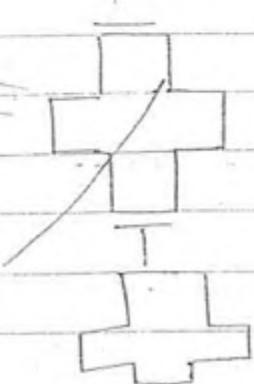
control	A	y.	High impedance
0	x	0	
1	0	0	
1	1	1	

control	y
0	high
1	A

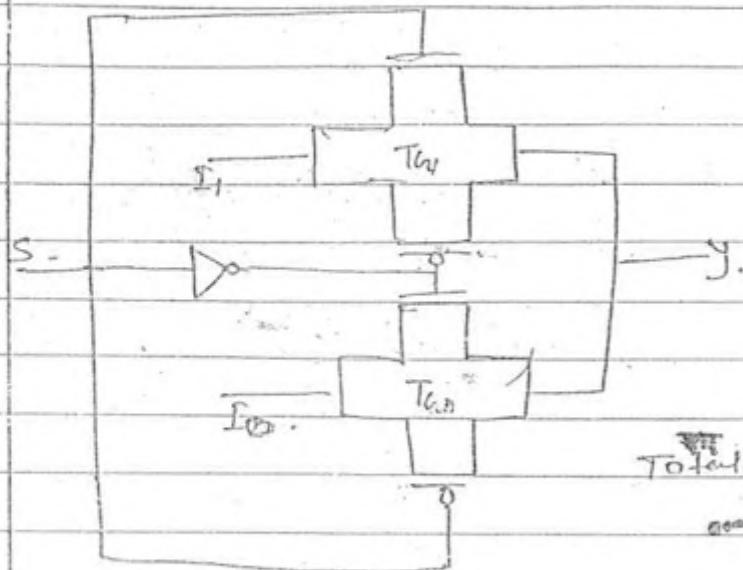
Symbol:-



2:1 Mux :-



→ 2:1 MUX using Transmission gate:-



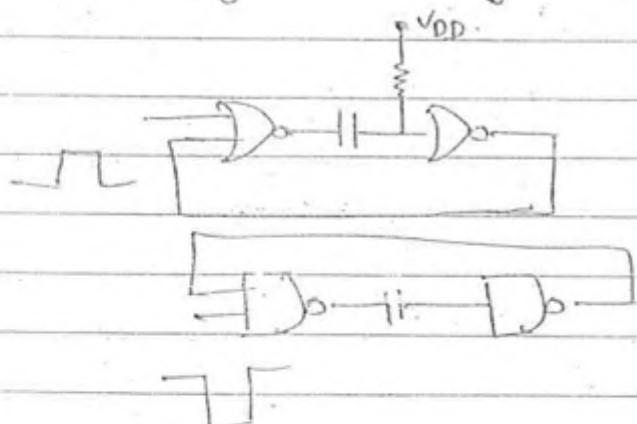
$$\text{Total no. of } T_g = 2 + 2 + 2 = 6$$

$S \quad Y$

0 I_1

1 I_2

→ CMOS NOR gate Monostable Multivibrator:-



- In 2's complement to represent -ve no. first write +ve no.
 Then complement to each (2's complement)
- A no. is represent in 2's complement to 011 the eq. decimal no.
 $1011 = 1101$
 $= -5$

$$\begin{array}{r} \text{Q. No. (d)} \quad 10011 \\ - (01101) \\ \hline -13 \end{array}$$

$$\begin{array}{r} \text{(10) (a)} \\ -127 \\ \swarrow \text{1's comp.} \rightarrow n \\ \searrow \text{2's comp.} \rightarrow m \end{array}$$

$$\begin{array}{r} 127 \rightarrow 0111111 \\ 1's \text{comp.} \xrightarrow{-127} 10000000 \quad n=1 \\ 2's -127 \quad 10000001 \quad m=2 \end{array}$$

$$m:n = 2:1$$

$$\begin{array}{r} \text{Q. No. (e) } 5-4 \\ 5+(-4) \\ +5 \rightarrow 01000 \\ -4 \rightarrow 1100 \\ \hline 0001 \end{array}$$

In 2's addition if any carry is present it is discarded.

17

$$\begin{array}{r} 1001 \leftarrow -7 \\ 11001 = -7 \\ 11001 - 7 \\ 101001 \end{array}$$

→ In 2's Complement to extend no. of bit copy
MSB bit.

	Binary	Sign Mag.	1's	2'sc
0	0000	+0	+0	+0
1	0001	+1	+1	+1
2	0010	+2	+2	+2
3	0011			
4	0100			
5	0101			
6	0110			
7	0111			
8	1000	-0	-7	-8
9	1001	-1	-6	-7
10	1010			
11	1011			
12	1100			
13	1101			
14	1110	-6	-1	-2
15	1111	-7	-0	-1

Range with sign magnitude.

4 bit

Sign mg → -7 to +7

1's → -7 to +7

2's → -8 to +7

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→ Sign magnitude, 1's.

$$\begin{aligned} n \text{ bit} &\rightarrow -(2^{n-1}) \text{ to } + (2^{n-1}) \\ &-(2^{n-1}-1) \text{ to } + (2^{n-1}) \\ &-7 \text{ to } +7 \end{aligned}$$

WB 16 (a) 19)

$$x = 01110$$

$$y = 11001$$

$$\begin{array}{r} \textcircled{1} & 110011 \\ \times & \underline{} \\ 0 & 00111 \\ \hline \text{Copy} & \text{Zero} \end{array}$$

→ +5, +4 using 1's complement

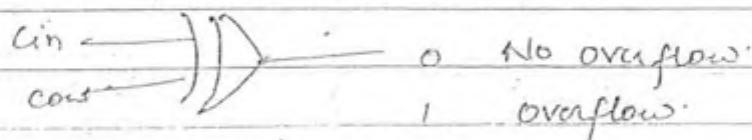
$$\begin{array}{r} +5 \rightarrow 10101 \\ +4 \rightarrow 0100 \\ \hline 10101 \\ \text{cout=0 overflow, Cin=1} \end{array}$$

Overflow may occur when two same sign are added in Signed representation.

Let x and y are sign bits of two no. & z is the resultant sign no. Then condition for overflow is

$$\bar{x}\bar{y}z + xy\bar{z}$$

Let Cin is carry into the MSB & $Cout$ is carry from MSB. for



MemoriesPrimary

RAM

1) RW

2) Random access.
(Same time)

3) Volatile

4) Storage of
Temporary data

ROM

Read only

Random access

Non volatile

Storage of
Permanent data

Ex BIOS / System prog.

Secondary

Semirandom

All discs

CD

DVD

H.D.

Serial access

Magnetic tape

Magnetic bubble

Ferrite core

CCIR

+
Charged Coupled Device

→ Ferrite Core → DRAM

★ In RAM : →

→ With n'bit address, max^m no. of memory location required = 2^n .→ In each memory location small m no. of bits are stored then memory capacity is $2^n \times m$.

Ex

$$\begin{array}{c} 4K \times 8 \\ 2^12 \quad 2^10 \rightarrow \text{Data} \\ 2^12. \end{array}$$

In 4Kx8

12 = Address line.

8 → Data line

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RAM

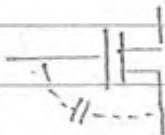
Static RAM

- 1) Stored like F.F.



Dynamic RAM

- 1) Data stored in MOS Capacitor
2) MOSFET



- 2) ~~BJT~~ MOSFET
3) Faster
4) Power dissipation more.
5) Densities less.
6) Cache memory.
7) No Refreshing

- 3) Slower
4) Less Power
5) Higher Densities
6) Main memory
7) Refreshing is required.

DIGITAL-ELECTRONICS