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KEC-101T / KEC-201T : EMERGING DOMAIN IN ELECTRONICS ENGINEERING

1

UNIT

Semiconductor Diode

CONTENTS

PART-1

Semiconductor Diode : Depletion Layer, V-I Characteristics, Ideal and Practical Diodes, Diode Equivalent Circuits.

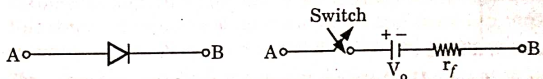
Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.1. **Explain semiconductor diode and also draw its equivalent circuit.**

Answer

1. A diode is an electrical device allowing current to flow only in one direction (forward bias) with far greater ease than in the other direction (reverse bias).
2. The most common type of diode in modern circuit design is the semiconductor diode (*p-n* junction).
3. A diode is a two-layer semiconductor consisting of *p*-type semiconductor material and *n*-type semiconductor material the equivalent circuit of diode is shown in Fig. 1.1.1.



Diode symbol Equivalent circuit

Fig. 1.1.1.

4. In an equilibrium, *p-n* junction, the free electrons from the *n*-type region will diffuse across the junction to the *p*-type side where they will recombine with some of the holes in the *p*-type material. Similarly, holes will diffuse across the junction in the opposite direction and recombine.
5. The recombination of free electrons and holes in the vicinity of the junction leaves a narrow region on either side of the junction that contains no mobile charge. This narrow region which has been depleted of mobile charge is called the depletion layer.
6. Diffusion of electrons into the *p*-region will leave positively charged ions (donors) in the *n*-region.
7. Similarly, diffusion of holes near the *p-n* interface in the *n*-type region leaves fixed ions (acceptors) with negative charge.

8. The regions nearby the *p-n* interfaces lose their neutrality and become charged, forming the space charge region or depletion layer.

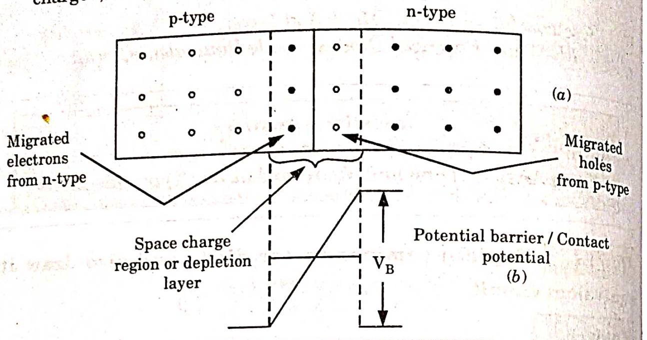


Fig. 1.1.2. *p-n* junction semiconductor.

9. This separation of charges causes an electric field to extend across the depletion layer. A potential difference must therefore exist across the depletion layer.

Que 1.2. **Explain the V-I characteristic of *p-n* junction diode. Draw well labelled characteristic.**

AKTU 2016-17, (Sem-I) Marks 05

Answer

i. **Forward bias :**

1. For the forward bias of a *p-n* junction, *p*-type is connected to the positive terminal while the *n*-type to negative terminal of battery.
2. The potential can be varied with potential divider. At some forward voltage (0.3 V for Ge and 0.7 V for Si) the potential barrier is eliminated and current starts flowing. This voltage is known as threshold or knee voltage (V_K).
3. As the forward voltage applied increases beyond threshold voltage, the forward current rises exponentially as shown in Fig. 1.2.1.
4. Beyond a certain safe value, it produces an extremely large current which may destroy the junction due to overheating.

ii. **Reverse bias :**

1. The *p*-type is connected to the negative terminal while *n*-type is connected to the positive terminal of a battery.
2. In this case, the junction resistance becomes very high and practically no current flows through the circuit.

3. In practical, a small current of the order of μA flows in the circuit due to minority carriers. This is known as reverse current. The reverse current is shown in Fig. 1.2.1.

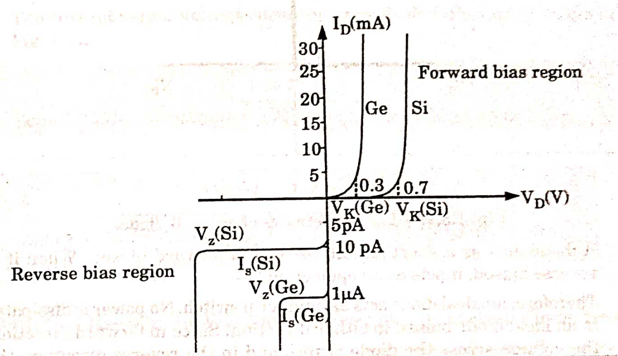


Fig. 1.2.1. Volt-ampere characteristics of *p-n* junction.

4. As the reverse bias is increased from zero, the reverse current quickly rises to its maximum or saturation value. The slight increase is due to impurities on the surface, which behaves as a resistor and hence obeys ohm's law. This gives rise to a current called surface leakage current.
5. If the reverse voltage is further increased, the kinetic energy of electrons becomes so high that they knock out from the semiconductor atoms. At this stage, breakdown of junction occurs and there is a sudden rise of reverse current. Now the junction is destroyed completely.
6. Thus, *p-n* junction diode is one-way device which offers a low resistance when forward biased and behaves like an insulator when reverse biased. Thus, it can be used as a rectifier *i.e.*, for converting alternating current into direct current.

Que 1.3. **Sketch and explain ideal and practical V-I characteristics of a *p-n* junction diode.**

Answer

A. **Ideal V-I characteristic :**

1. An ideal diode is perfect conductor in forward bias and a perfect resistor in reverse bias.
2. The current-voltage characteristic of the ideal diode is shown in Fig. 1.3.1.

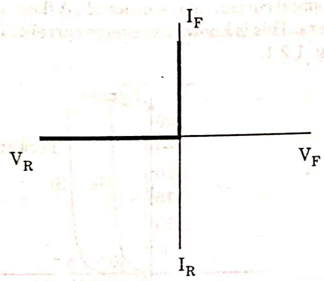


Fig. 1.3.1. V-I characteristics of an ideal diode.

3. A diode acts as a short circuit when it is forward biased. When it is reverse biased, it acts as an open circuit.
4. Therefore, an ideal diode acts as unilateral switch. No power is dissipated in an ideal diode biased in either direction. Since in forward direction, the voltage across the diode is zero and in the reverse direction, the current through the diode is zero as shown in Fig. 1.3.1.

B. Practical :

1. In practical, the battery introduced a small offset voltage (V_r) in forward biased. The value of the offset voltage is determined by the type of semiconductor used in a *p-n* junction but cannot be measured directly.

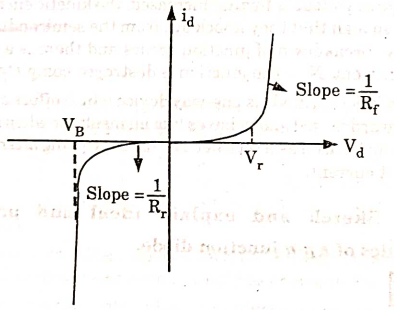


Fig. 1.3.2.

2. The resistor approximates the semiconductor resistance when diode is ON / OFF or forward bias / reverse bias.
3. A reverse biased diode conducts a very small amount of current called leakage current.

4. The ability of diode to withstand reverse-bias voltage is limited. If the applied reverse-bias voltage becomes too large diode will experience a heavy conduction known as breakdown, which is usually destructive.
5. The current versus voltage curve for a real diode looks like as shown in Fig. 1.3.2.

PART-2

Zener Diodes Breakdown Mechanism (Zener and Avalanche).

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.4. **Explain the V-I characteristic of *p-n* junction diode. How it is differ from zener diode ?** **AKTU 2016-17, (Sem-II) Marks 07**

OR

Explain input and output characteristics of zener diode. **AKTU 2015-16, (Sem-II) Marks 05**

Answer

A. V-I characteristic of *p-n* junction diode : Refer Q. 1.2, Page 1–3J, Unit-1.

B. Zener diode :

1. Zener diode is a reverse-biased heavily doped *p-n*-junction diode which is operated in the breakdown region. Fig. 1.4.1 shows the symbol of zener diode.

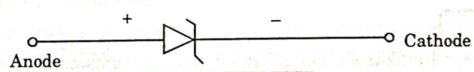


Fig. 1.4.1. Zener diode.

2. When a zener diode is forward biased, its characteristics are just same as the ordinary diode and it is shown in Fig. 1.4.2.
3. When zener diode is reverse biased then it gives constant current up to a certain voltage. When the reverse bias voltage is increased beyond that voltage, the current increased rapidly as shown in Fig. 1.4.2.

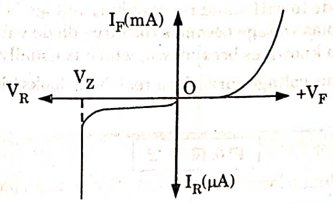


Fig. 1.4.2. V-I characteristic of zener diode.

4. The cut-off value of voltage beyond which zener diode reverse current increases rapidly is called zener voltage V_Z or breakdown voltage.
5. The breakdown or zener voltage depends upon the amount of doping.
6. A zener diode can be used as a voltage regulator to provide a constant voltage to a load.

C. Difference :

S. No	*p-n* junction diode	Zener diode
1.	The electricity flows in one direction.	The electricity flows in both the direction.
2.	The reverse bias permanently damages the depletion region.	The reverse bias makes the electricity flow in both the direction.
3.	The width of depletion region is large because the *p* and *n* region is lightly doped.	The width of depletion region is narrow because the *p* and *n* region is heavily doped.
4.	This is used for rectification.	This is used for voltage regulation.

Que 1.5. **Explain reverse breakdown of a diode.**

Answer

Reverse breakdown can occur by two mechanisms that are zener breakdown and avalanche breakdown.

i. Zener breakdown :

1. It takes place in very thin junction (*i.e.*, depletion layer is narrow due to heavily doped junctions on both sides).
2. When a small reverse bias voltage is applied, a very strong electric field (approximately 10^7 V/m) is set up across the thin depletion layer.
3. This field is enough to break the covalent bonds. This breaking of covalent bonds produces large number of electrons and holes which constitute the reverse saturation current (*i.e.*, zener current).

4. Zener current is independent of the applied voltage. It depends only on the external resistance.
5. This breakdown is called as zener breakdown as shown in Fig. 1.5.1. This breakdown occurs at low voltage.

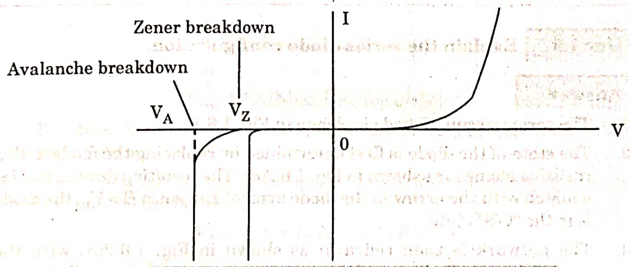


Fig. 1.5.1. The I-V characteristics comparison between zener and avalanche breakdown.

ii. Avalanche breakdown :

1. Avalanche breakdown takes place in slightly thick junction than the zener breakdown case. It means both sides of junction are lightly doped.
2. In this case, the electric field across the depletion region (layer) is not so strong to produce zener breakdown for the same applied voltage of zener breakdown case.
3. Here, the minority carriers accelerated by the field collide with the semiconductor atoms in the depletion region.
4. During collision the kinetic energy of electrons is transferred to other covalent bonds, thus the energy transferred to covalent bonds increases the band energy, hence covalent bonds are broken and electron-hole pairs are generated.
5. The newly generated carriers transfer their energy to other covalent bonds and break more bonds and thus extremely large numbers of carriers are generated due to cumulative process of avalanche multiplication.
6. This breakdown is called avalanche breakdown as shown in Fig. 1.9.1. This breakdown occurs at higher voltages.

PART-3

Diode Application : Diode Configuration, Half and Full Wave Rectification.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.6. **Explain the series diode configuration.**

Answer

1. The series circuit of diode is shown in Fig. 1.6.1.
2. The state of the diode is first determined by replacing the diode with a resistive element as shown in Fig. 1.6.2(*a*). The resulting direction of *I* is a match with the arrow in the diode symbol and since $E > V_K$, the diode is in the "ON" state.
3. The network is then redrawn as shown in Fig. 1.6.2(*b*) with the appropriate equivalent model for the forward biased silicon diode.

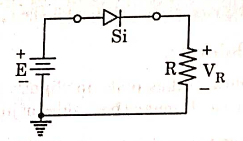


Fig. 1.6.1. Series diode configuration.

4. The resulting voltage and current level are the following :

$$V_D = V_K$$

$$V_R = E - V_K$$

$$I_D = I_R = \frac{V_R}{R}$$

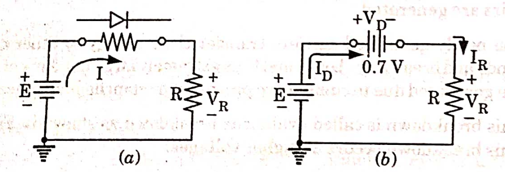


Fig. 1.6.2.

5. In Fig. 1.6.3 the diode is reversed. Replacing the diode with a resistor element as shown in Fig. 1.6.4 (*a*) will reveal that the resulting current direction does not match the arrow in the diode symbol.

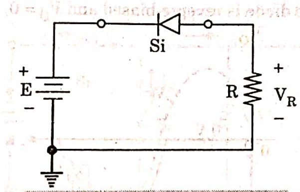


Fig. 1.6.3. Reversing the diode.

6. The diode is in the "OFF" state, resulting in the equivalent circuit of Fig. 1.6.4(*b*).
7. Due to open circuit, the diode current is 0 A and the voltage across the resistor *R* is the following :

$$V_R = I_R R = I_D R = (0\ \text{A})\, R = 0\ \text{V}$$

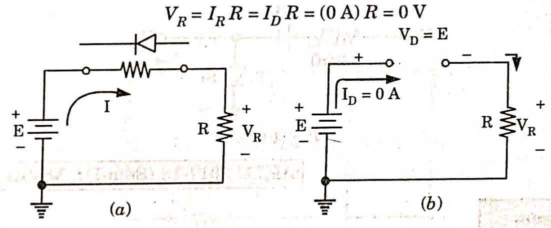


Fig. 1.6.4.

Que 1.7. **Determine V_O, and draw the output waveform of the given network of Fig. 1.7.1.**

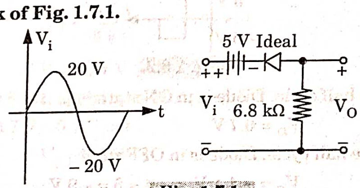


Fig. 1.7.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

1. For $V_i \leq 5$ V, the 5 V battery will ensure the diode is forward-biased and $V_O = V_i - 5$ V.
2. At $V_i = 5$ V
   $V_O = 5\text{ V} - 5\text{ V} = 0$ V
3. At $V_i = -20$ V
   $V_O = -20\text{ V} - 5\text{ V} = -25$ V

4. For $V_i > 5$ V, the diode is reverse-biased and $V_O = 0$.

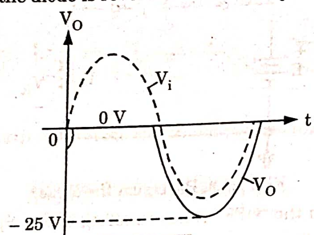


Fig. 1.7.2.

Que 1.8. **Sketch V_O for given circuit configuration (Fig. 1.8.1).**

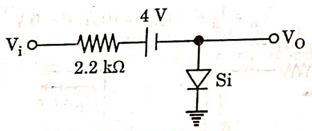


Fig. 1.8.1.

AKTU 2017-18 (Sem-II), Marks 3.5

Answer

1. Assume input waveform,

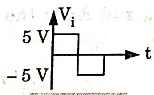


Fig. 1.8.2.

2. For positive half cycle. Diode is in ON state.

$\therefore$ $V_O = 0.7$ V

3. For negative half cycle. Diode is in OFF state.

$V_O = -4 + V_i = -4 - 5 = -9$ V

4. Output waveform as shown in Fig. 1.8.3.

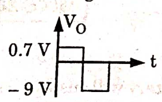


Fig. 1.8.3.

Que 1.9. **For the circuit shown in Fig. 1.9.1, determine I_1, I_2, I_3, I_4, V_O.**

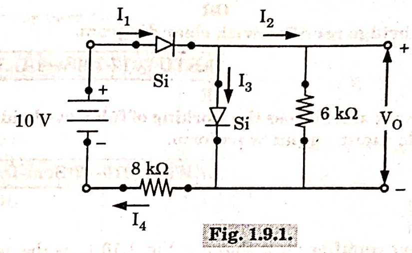


Fig. 1.9.1.

AKTU 2016-17(Sem-I), Marks 05

Answer

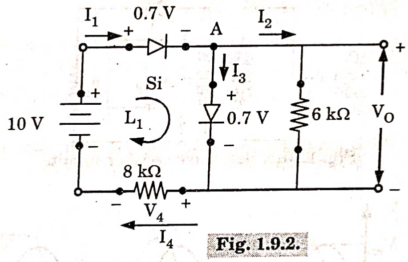


Fig. 1.9.2.

$$I_2 = \frac{0.7\text{ V}}{6\text{ k}\Omega} = 0.1167\text{ mA}$$

$$V_O = 0.7\text{ V}$$

Voltage across 8 kΩ, applying KVL in loop L_1,

$$-V_4 + 10\text{ V} - 0.7\text{ V} - 0.7\text{ V} = 0$$

$$V_4 = 8.6\text{ V}$$

We have, $$I_4 = \frac{V_4}{R} = \frac{8.6\text{ V}}{8\text{ k}\Omega} = 1.075\text{ mA}$$

$$I_4 = I_1 = 1.075\text{ mA}$$

Apply KCL at node A, $I_3 = I_1 - I_2 = 1.075\text{ mA} - 0.1167\text{ mA}$

$$I_3 = 0.96\text{ mA}$$

Que 1.10. **Explain the working of half wave and full wave bridge rectifier.**

OR

Explain the bridge rectifier with clear diagram.

AKTU 2017-18(Sem-I), Marks 3.5

OR

Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveform.

AKTU 2016-17(Sem-I), Marks 05

Answer

A. **Half wave rectifier :** It is shown in Fig. 1.10.1. As the name signifies only half portion of input is rectified (either positive half or negative half). Only single diode and a step down transformer are required for this circuit.

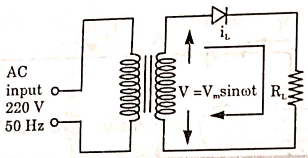


Fig. 1.10.1. Half wave rectifier circuit.

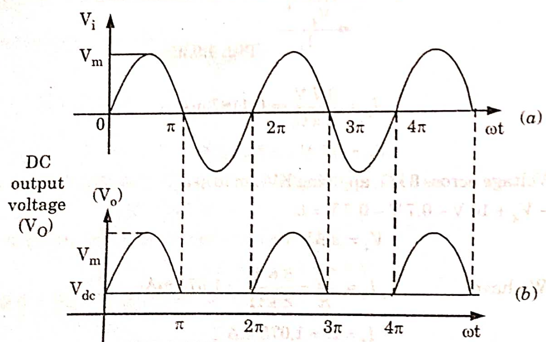


Fig. 1.10.2. (*a*) Input voltage (*b*) Output voltage.

B. **Full wave rectifier :** This circuit gives the output for full cycle (*i.e.*, for both positive and negative half cycles). There are two types of circuits used for it :

i. **Center-tap rectifier :**

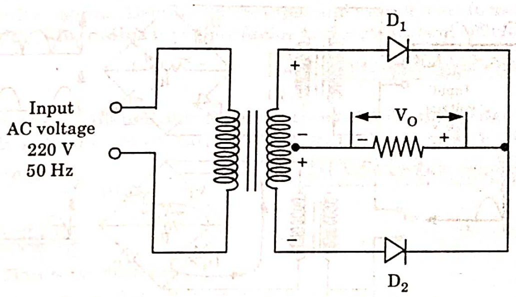


Fig. 1.10.3. Full wave rectifier.

1. In center-tap full wave rectifier circuit, diode D_1 will be ON for positive half cycle (*i.e.*, 0 to π) and the diode D_2 will be OFF during this cycle.
2. The diode D_2 will be ON for negative half cycle (*i.e.*, π to 2π) while the diode D_1 will be OFF during this cycle.
3. The input and output waveforms are shown in Fig. 1.10.4.

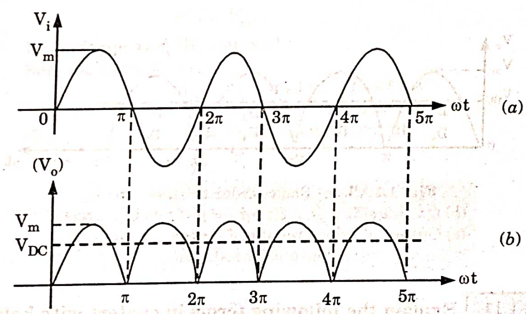


Fig. 1.10.4. (*a*) Input waveform (*b*) Output waveform.

ii. **Bridge rectifier :** As shown in Fig. 1.10.5(*b*) only diodes D_2 and D_4 are active during positive half cycle while diodes D_1 and D_3 are active for negative half cycle as shown in Fig. 1.10.5(*c*) and Fig. 2.10.5(*d*) shows the total output with the active diodes for a particular cycle.

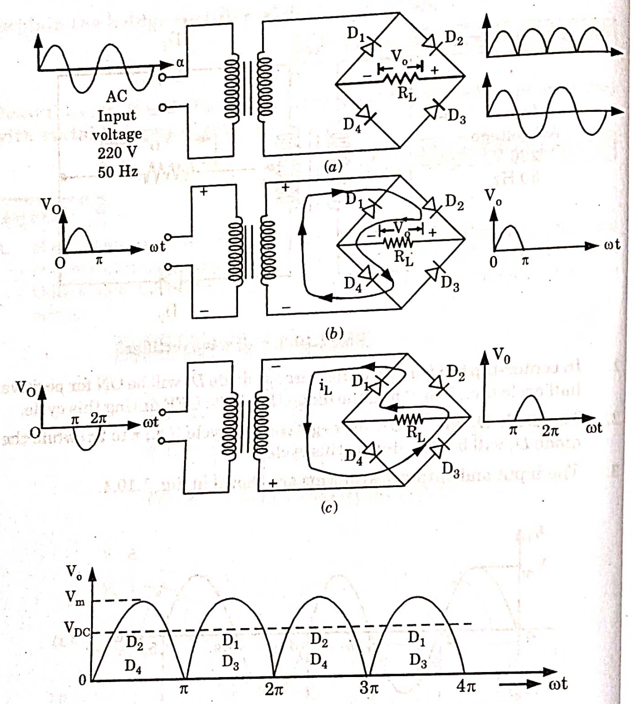


Fig. 1.10.5. (a) Basic bridge rectifier circuit
(b) Output of bridge rectifier for positive half cycle.
(c) Output of bridge rectifier for negative half cycle.
(d) Output for full cycle.

Que 1.11. **Explain the following terms in context with half wave rectifier and full wave rectifier :**
i. DC voltage and DC current
ii. RMS value of current

OR

For a half wave rectifier, derive an expression for ripple factor.

AKTU 2015-16(Sem-II), Marks 7.5

OR

Explain the operation of full wave bridge rectifier with the help of a circuit diagram. Also sketch the input and output waveforms. Define its PIV. Also derive its ripple factor and rectification efficiency.

AKTU 2017-18(Sem-II), Marks 07

OR

Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveforms. What is PIV of bridge rectifier ?

AKTU 2016-17(Sem-II), Marks 07

Answer

A. Half wave rectifier :

i. Operation : Refer Q. 1.10, Page 1–12J, Unit-1.

ii. PIV :

1. As we know during negative half cycle, diode will be reverse biased and there will be no output voltage.
2. In the negative half cycle the voltage across diode will be maximum when input reaches to its maximum value V_m. This maximum voltage during negative half cycle is called as the peak inverse voltage (PIV).
3. PIV for half wave rectifier is given by

$$\text{PIV} = V_m$$

iii. DC voltage and DC current :

Suppose current in load

$$i_L = I_m \sin \omega t \qquad 0 \le \omega t \le \pi \qquad \text{...(1.11.1)}$$
$$= 0 \qquad \pi \le \omega t \le 2\pi$$

Here, I_m = Peak value of current i_L

$$I_m = \frac{V_m}{R_L}$$

DC voltage for half wave rectifier, $V_{DC} = I_{DC} \times R_L$

$$V_{DC} = \frac{I_m}{\pi} \times R_L$$

$$V_{DC} = \frac{V_m}{\pi} \qquad \text{...(1.11.2)}$$

$$I_{DC} = \frac{I_m}{\pi} \qquad \text{...(1.11.3)}$$

iv. RMS value of current :

1. The rms value of the current flowing through the load is given as

$$I_{\text{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)}$$

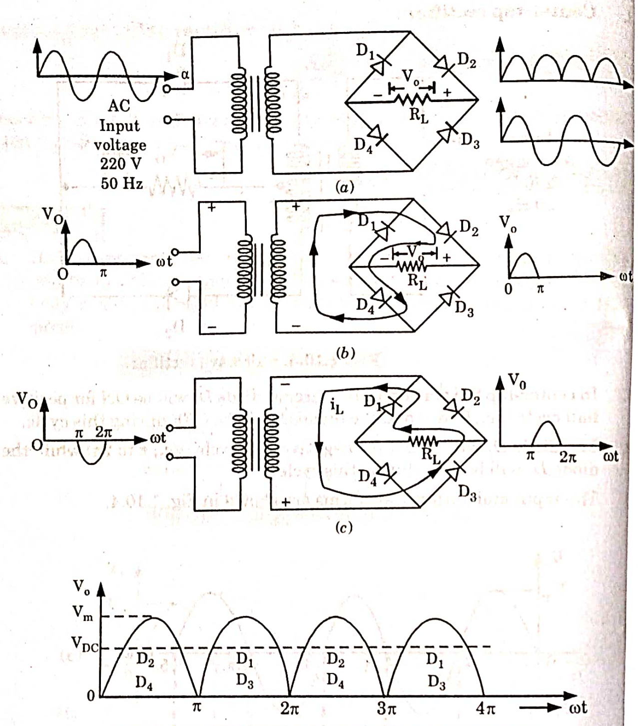


Fig. 1.10.5. *(a)* Basic bridge rectifier circuit
(b) Output of bridge rectifier for positive half cycle.
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Que 1.11. **Explain the following terms in context with half wa rectifier and full wave rectifier :**

i. DC voltage and DC current

ii. RMS value of current

OR

For a half wave rectifier, derive an expression for ripple factor.

AKTU 2015-16(Sem-II), Marks 7

OR

Explain the operation of full wave bridge rectifier with the help of a circuit diagram. Also sketch the input and output waveforms. Define its PIV. Also derive its ripple factor and rectification efficiency.

AKTU 2017-18(Sem-II), Marks 07

OR

Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveforms. What is PIV of bridge rectifier ?

AKTU 2016-17(Sem-II), Marks 07

Answer

A. Half wave rectifier :

i. Operation : Refer Q. 1.10, Page 1–12J, Unit-1.

ii. PIV :

1. As we know during negative half cycle, diode will be reverse biased and there will be no output voltage.
2. In the negative half cycle the voltage across diode will be maximum when input reaches to its maximum value V_m. This maximum voltage during negative half cycle is called as the peak inverse voltage (PIV).
3. PIV for half wave rectifier is given by

$$PIV = V_m$$

iii. DC voltage and DC current :

Suppose current in load

$$i_L = I_m \sin \omega t \qquad 0 \le \omega t \le \pi$$
$$= 0 \qquad \pi \le \omega t \le 2\pi \qquad \text{...(1.11.1)}$$

Here, I_m = Peak value of current i_L

$$I_m = \frac{V_m}{R_L}$$

DC voltage for half wave rectifier, $V_{DC} = I_{DC} \times R_L$

$$V_{DC} = \frac{I_m}{\pi} \times R_L$$

$$V_{DC} = \frac{V_m}{\pi} \qquad \text{...(1.11.2)}$$

$$I_{DC} = \frac{I_m}{\pi} \qquad \text{...(1.11.3)}$$

iv. RMS value of current :

1. The rms value of the current flowing through the load is given as

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)}$$

2. Replacing the value of i_L from eq. (1.11.1)

$$I_{rms} = \sqrt{\frac{1}{2\pi}\left[\int_0^{\pi} I_m^2 \cdot sin^2 \omega t \; d(\omega t) + \int_{\pi}^{2\pi} 0 \; d(\omega t)\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi}\frac{(1-\cos 2\omega t)}{2} . d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi \times 2}\left|\omega t - \frac{\sin 2\omega t}{2}\right|_0^{\pi}}$$

$$I_{rms} = \frac{I_m}{2} \quad ...(1.11.4)$$

3. Eq. (1.11.4) gives total current (AC and DC).
4. Thus instantaneous value of AC in output is,

$$i_{AC} = i_L - I_{DC}$$

$$(I_{AC})_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(i_L - I_{DC})^2 \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(i_L^2 + I_{DC}^2 - 2 i_L I_{DC}) \, d(\omega t)}$$

$$= \sqrt{I_{rms}^2 + I_{DC}^2 - 2\, I_{DC}^2}$$

$$(I_{AC})_{rms} = \sqrt{I_{rms}^2 - I_{DC}^2} \quad ...(1.11.5)$$

v. **Ripple factor :** The ripple factor is given as

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

Since, $I_{rms} = I_m/2$ and $I_{DC} = I_m/\pi$. So, $r = 1.21$

vi. **Rectification efficiency :** The efficiency is given as

$$\eta = \frac{\text{Output DC power}}{\text{Input AC power}} = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 \, R_L}{I_{rms}^2 \, (R_L + r_d)}$$

where, $R_L \rightarrow$ load resistance, $r_d \rightarrow$ diode resistance

$$= \frac{(I_m/\pi)^2 \, . \, R_L}{(I_m/2)^2 \, (r_d + R_L)}$$

$$\eta = 0.406 \quad (\because r_d << R_L)$$

$$\eta = 40.6 \%$$

B. **Full wave rectifiers :**

i. **Operation and waveforms of full wave bridge rectifier :** Refer Q. 1.10, Page 1–12J, Unit-1.

ii. **RMS value of current :**

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_L^2 \, d(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2 \sin^2 \omega t \; d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi}\frac{(1-\cos 2\omega t)}{2} d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi}\left|\omega t - \frac{\sin 2\omega t}{2}\right|_0^{\pi}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

iii. **PIV (Peak Inverse Voltage) :** It is same as the half wave rectifier, but the value of PIV is different for center-tap type full wave rectifier.

In centre-tap full wave rectifiers, PIV = $2V_m$

In bridge type full wave rectifiers, PIV = V_m

iv. **DC voltage and DC current :**

$$I_{DC} = \frac{1}{\pi}\int_0^{\pi} i_L \; d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_m \sin \omega t \; d(\omega t)$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$V_{DC} = I_{DC} \times R_L$$

$$V_{DC} = \frac{2I_m}{\pi} \times R_L = \frac{2V_m}{\pi}$$

v. **Ripple factor :**

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1}$$

$$r = 0.482$$

vi. **Rectification efficiency :**

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{(2I_m/\pi)^2 \, R_L}{(I_m/\sqrt{2})^2 (r_d + R_L)} \times 100 \%$$

$$= 81.2 \% \quad (\because r_d << R_L)$$

Que 1.12. **Differentiate between half wave and full wave rectifiers.**

AKTU 2015-16(Sem-I), Marks 05

Answer

S. No.	Full wave rectifier	Half wave rectifier
1.	Full wave rectifier is an electronic circuit which converts entire cycle of AC into pulsating DC.	A Half wave rectifier is an electronic circuit which converts only one-half of the AC cycle into pulsating DC.
2.	Full wave rectifier, is bi-directional, it conducts for positive half as well as negative half of the cycle.	The Half wave rectifier is unidirectional; it means it will allow the conduction in one direction only.
3.	Peak inverse voltage (PIV) is twice of the maximum value of supplied input.	Peak inverse voltage (PIV) is the maximum value of supplied input.
4.	Ripple factor is low.	Ripple factor is high.

Que 1.13. **Sketch V_O, V_{DC} for the network of Fig. 1.13.1, and determine the peak inverse voltage of each diode.**

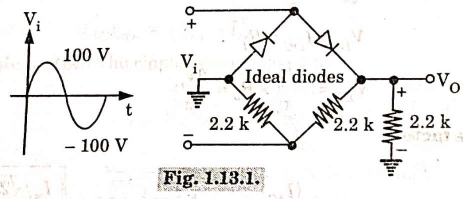

Fig. 1.13.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

For positive half-cycle of V_i :

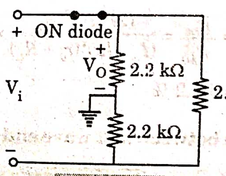

Fig. 1.13.2.

Using voltage divider rule and we get,

$$V_{Omax} = \frac{2.2\,\text{k}\Omega\,(V_{imax})}{2.2\,\text{k}\Omega + 2.2\,\text{k}\Omega}$$

$$= \frac{1}{2}(V_{imax}) = \frac{1}{2}\,(100\text{ V}) = 50\text{ V}$$

For negative half cycle of V_i :

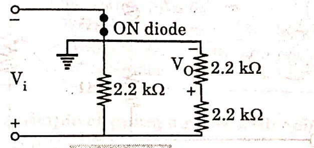

Fig. 1.13.3.

Polarity of V_O across the 2.2 kΩ resistor acting as a load is the same. Using voltage divider rule,

$$V_{Omax} = \frac{2.2\,\text{k}\Omega\,(V_{imax})}{2.2\,\text{k}\Omega + 2.2\,\text{k}\Omega}$$

$$= \frac{1}{2}(V_{i_{max}}) = \frac{1}{2}\,(100\text{ V}) = 50\text{ V}$$

$$V_{DC} = 0.636\,V_{Omax} = 0.636\,(50\text{ V}) = 31.8\text{ V}$$

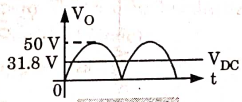

Fig. 1.13.4.

Peak inverse voltage of each diode = V_m = 100 V

Que 1.14. **Determine the output waveform for the given network as shown in Fig. 1.14.1. Determine the output DC level and compute PIV for each diode.**

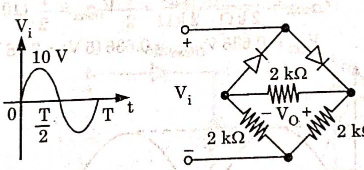

Fig. 1.14.1.

AKTU 2017-18(Sem-II), Marks 07

Answer

For positive half-cycle of V_i :

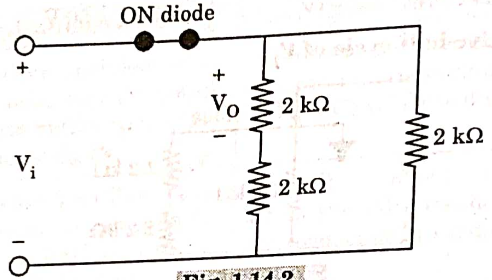

Fig. 1.14.2.

Using voltage divider rule,

$$V_{Omax} = \frac{2\,k\Omega\,(V_{imax})}{2\,k\Omega + 2\,k\Omega} = \frac{1}{2}\,(10\ V) = 5\ V$$

For negative half-cycle of V_i :

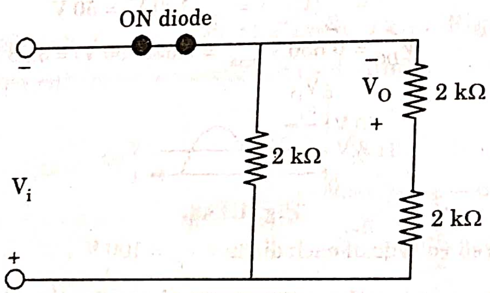

Fig. 1.14.3.

Using voltage divider rule,

$$V_{Omax} = \frac{2\,k\Omega\,(V_{imax})}{2\,k\Omega + 2\,k\Omega} = \frac{1}{2}\,V_{imax} = \frac{1}{2}\,(10) = 5\ V$$

$$V_{DC} = 0.636\ V_{Omax} = 0.636\ (5\ V) = 3.18\ V$$

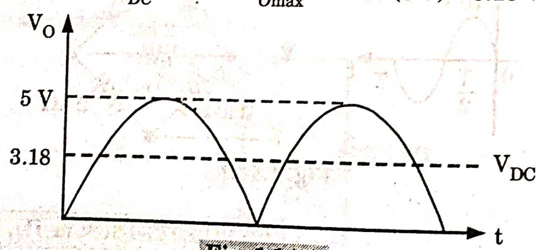

Fig. 1.14.4.

Peak inverse voltage of each diode = V_m = 10 V

PART-4
Clippers, Clampers.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.15. **Draw a simple clipping circuit with suitable waveform and explain types of clippers.**

Answer

A. **Clipping circuit :**

A wave shaping circuit which controls the shape of output waveform by removing (clipping) a portion of the applied wave is known as clipping circuit. For a clipping circuit at least one resistance and one diode are required.

B. **Types of clippers :** There are mainly two types of clippers *i.e.*, positive and negative clippers. They are further divided into two categories :

1. **Series clippers (for ideal diode) :**

a. **Simple series clippers :**

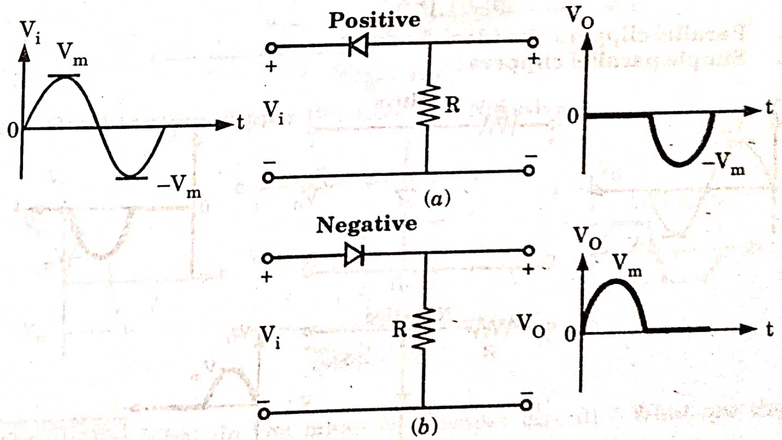

Fig. 1.15.1.

Answer

For positive half-cycle of V_i :

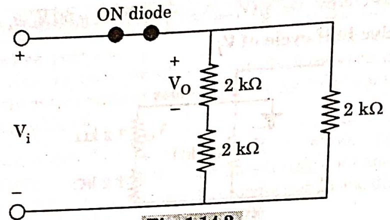

Fig. 1.14.2.

Using voltage divider rule,

$$V_{Omax} = \frac{2\,k\Omega\,(V_{imax})}{2\,k\Omega + 2\,k\Omega} = \frac{1}{2}\,(10\text{ V}) = 5\text{ V}$$

For negative half-cycle of V_i :

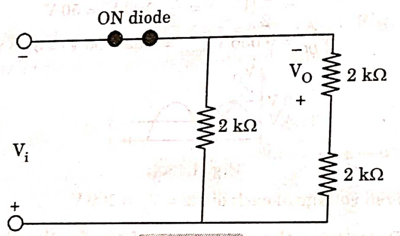

Fig. 1.14.3.

Using voltage divider rule,

$$V_{Omax} = \frac{2\,k\Omega\,(V_{imax})}{2\,k\Omega + 2\,k\Omega} = \frac{1}{2}\,V_{imax} = \frac{1}{2}\,(10) = 5\text{ V}$$

$$V_{DC} = 0.636\,V_{Omax} = 0.636\,(5\text{ V}) = 3.18\text{ V}$$

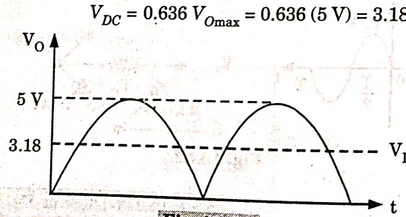

Fig. 1.14.4.

Peak inverse voltage of each diode = V_m = 10 V

PART-4

Clippers, Clampers.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.15. Draw a simple clipping circuit with suitable waveform and explain types of clippers.

Answer

A. **Clipping circuit :**

A wave shaping circuit which controls the shape of output waveform by removing (clipping) a portion of the applied wave is known as clipping circuit. For a clipping circuit at least one resistance and one diode are required.

B. **Types of clippers :** There are mainly two types of clippers *i.e.*, positive and negative clippers. They are further divided into two categories :

1. **Series clippers (for ideal diode) :**

a. **Simple series clippers :**

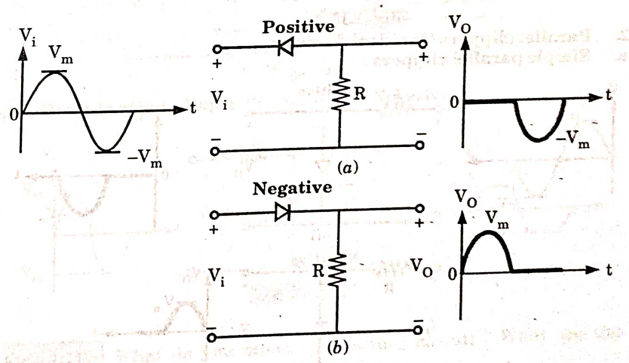

Fig. 1.15.1.

b. Biased series clippers :

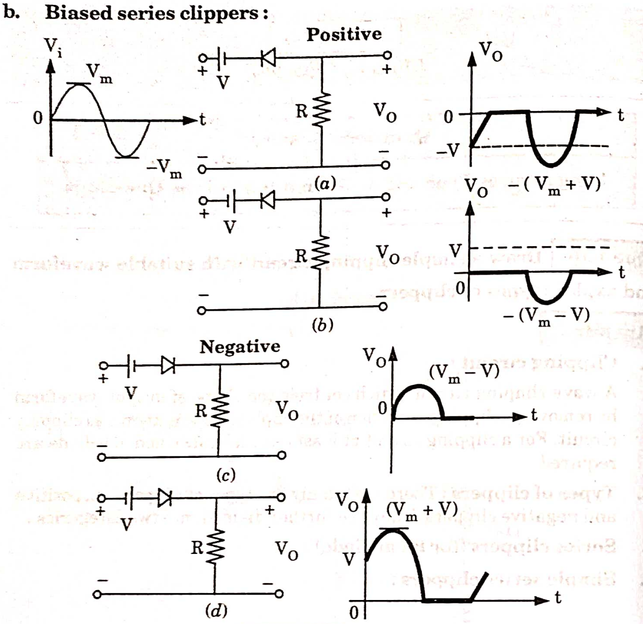

Fig. 1.15.2.

2. Parallel clippers (for ideal diodes) :

a. Simple parallel clippers :

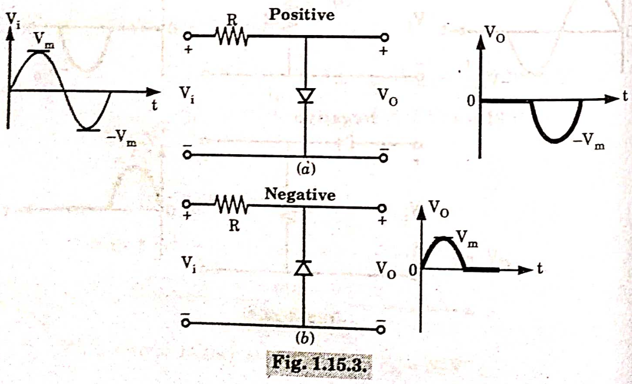

Fig. 1.15.3.

b. Biased parallel clippers :

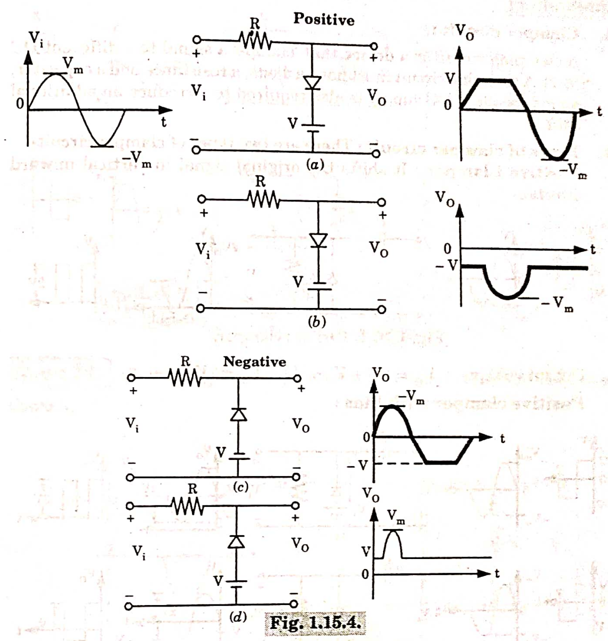

Fig. 1.15.4.

c. Combination clipper (Positive and Negative) :

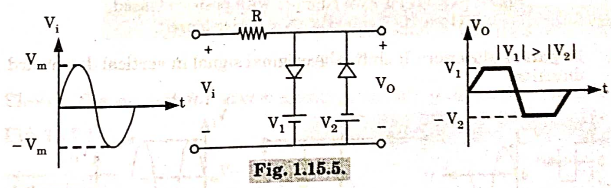

Fig. 1.15.5.

Que 1.16. What do you mean by clamper circuit ? What are the different types of clamper ciruits ?

Answer

A. Clamper circuit :

A clamping circuit is a device that 'clamps' a signal to a different DC level. A clamping circuit must have a diode, a resistance and a capacitor, an independent DC supply is also required to introduce an additional shift.

B. Types of clamper circuit : There are two types of clamper circuits.

1. **Positive Clamper :** It shifts the original signal in vertical upward direction.

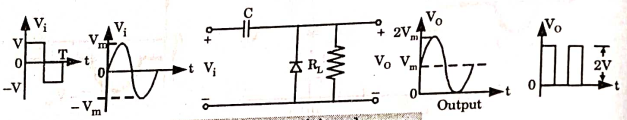

Fig. 1.16.1. Positive clamper.

Output voltage $V_O = V_m + V_c = V_m + V_m = 2V_m$

Positive clamper with bias :

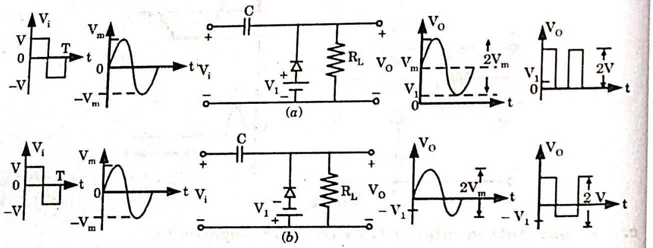

Fig. 1.16.2. (*a*) Positive clamper with positive biased, (*b*) Positive clamper with negative biased.

2. **Negative clamper :** It shifts the original signal in vertical downward direction.

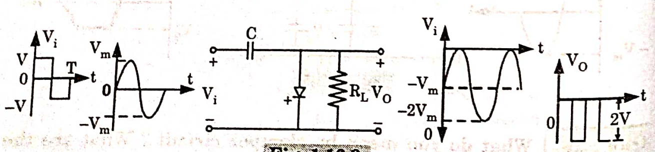

Fig. 1.16.3.

Negative clamper with bias

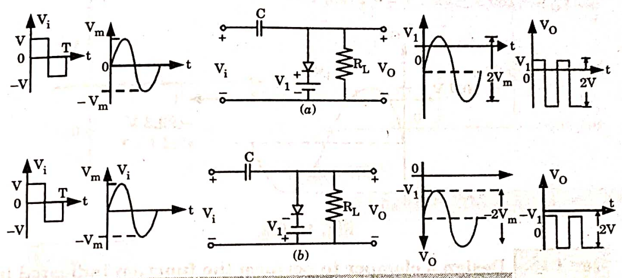

Fig. 1.16.4. (*a*) Negative clamper with positive bias, (*b*) Negative clamper with negative bias.

Que 1.17. **Sketch V_O for each network of Fig. 1.17.1, for the input shown.**

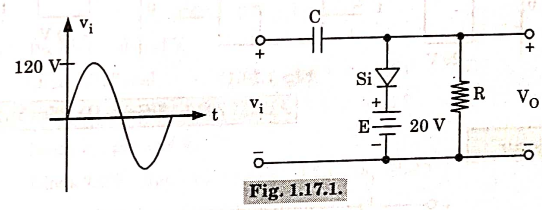

Fig. 1.17.1.

AKTU 2015-16(Sem-I), Marks 05

OR

Sketch the output for given clamper circuit with shown input in Fig. 1.17.1.

AKTU 2017-18(Sem-II), Marks 3.5

Answer

1. For positive half cycle capacitor charges to peak value of 120 V – 20 V – 0.7 V = 99.3 V with polarity (+ ⊣⊢ –). The output V_O = 20 V + 0.7 V = 20.7 V.

2. For next negative half cycle $V_O = V_i - 99.3$ V with negative peak value of $V_O = -120$ V $- 99.3$ V $= -219.3$ V.

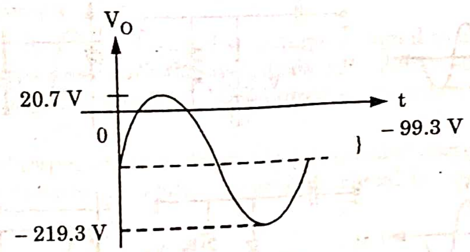

Fig. 1.17.2.

Que 1.18. Design a clamper to perform the function indicated in Fig. 1.18.1.

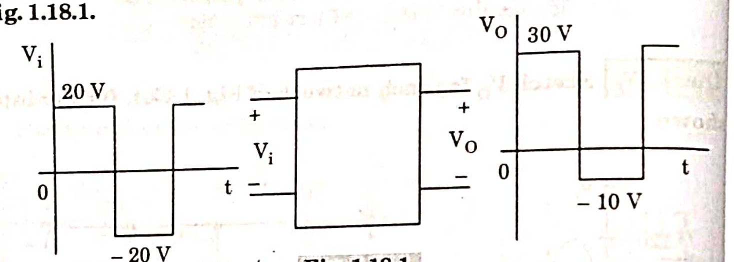

Fig. 1.18.1.

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Answer

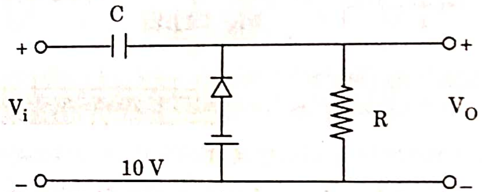


Fig. 1.18.2.

During positive half cycle :

$V_O = V_i + V_C + (-10) = V_m + V_m - 10 = 20 + 20 - 10 = 30$ V

During negative half cycle :

$V_O = -10$ V

Que 1.19. Determine v_O for the circuit shown in Fig. 1.19.1.

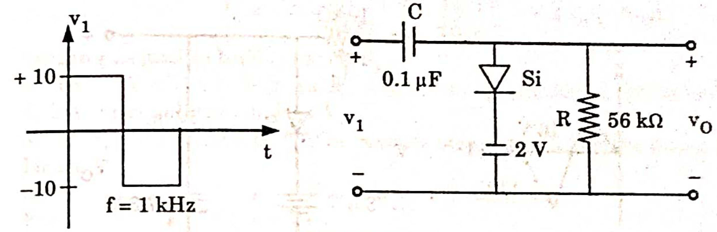


Fig. 1.19.1.

AKTU 2017-18 (Sem-I), Marks 3.5

Answer

i. $\tau = RC = (56\ \text{k}\Omega)(0.1\ \mu\text{F}) = 5.6$ ms

$5\tau = 28$ ms

ii. $5\tau = 28 \text{ ms} >> \dfrac{T}{2} = \dfrac{1\text{ms}}{2} = 0.5$ ms,

$$\frac{5\tau}{T/2} = \frac{28}{0.5} = \frac{56}{1} = 56:1$$

iii. Positive pulse of V_i

Diode 'ON' and $V_0 = -2\text{ V} + 0.7\text{ V} = -1.3$ V

Capacitor charge to 10 V + 2 V – 0.7 V= 11.3 V

Negative pulse of V_i

Diode 'OFF' and $V_0 = -10\text{ V} - 11.3\text{ V} = -21.3$ V

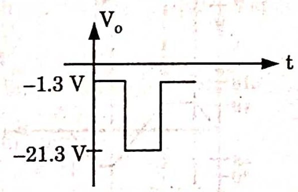


Fig. 1.19.2.

Que 1.20. Define clipper circuit. Sketch the output waveform for the circuit shown below given input.

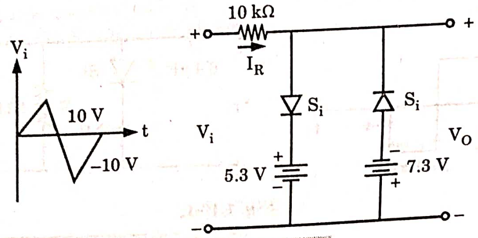


Fig. 1.20.1.

AKTU 2017-18(Sem-II), Marks 07

Answer

A. **Clipper :** Refer Q. 1.15, Page 1–22J, Unit-1.

B. **Numerial :**

i. **During positive half cycle of V_i :**

1. When $0 < V_i < 6$ V, then both diode D_1 and D_2 will be reverse biased and output will follow input voltage.

   i.e., $V_O = V_i$

2. When $V_i > 6$ V, then D_1 will be forward biased and D_2 will be reverse biased.

   So, $V_O = 0.7 + 5.3 = 6$ V (constant)

3. The current i_R will flow only when either of the two diodes will be forward biased.

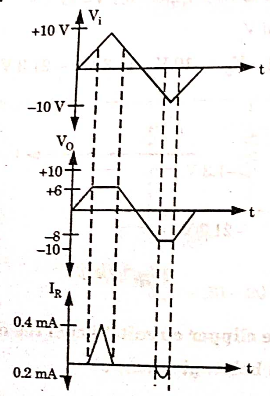


Fig. 1.20.2.

4. For $V_{in} = 10$ V

$$I_R = \frac{V_{in} - 0.7 - 5.3}{10\text{ k}\Omega} = \frac{10 - 6}{10\text{ k}\Omega} = 0.4\text{ mA (Peak)}.$$

ii. **During negative half cycle of V_i :**

1. When -7 V $< V_i < 0$, both diodes will be reverse biased so output will follow input voltage *i.e.,* $V_O = V_i$

2. When $V_i < -8$ V, then D_1 will be reverse biased and D_2 will be forward biased

   So, $V_O = -(0.7 + 6.3) = -8$ V (constant)

   For $V_{in} = -10$ V

   $$I_R = \frac{V_{in} + 0.7 + 7.3}{10\text{ k}\Omega} = \frac{-10 + 8}{10\text{ k}\Omega} = -0.2\text{ mA}.$$

3. The waveforms for V_o and I_R are shown in Fig. 1.20.2.

Que 1.21. **Explain the function of the circuit of Fig. 1.21.1 and draw the output waveform.**

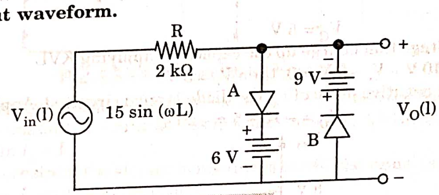


Fig. 1.21.1.

AKTU 2015-16(Sem-II), Marks 7.5

Answer

1. During positive half cycle :

i. **Case-1 :** When $V_{in} < 6$ V

   Diode *A* and *B*, both are reverse biased

   $V_O = V_{in}$

ii. **Case-2 :** When $V_{in} > 6$ V

   Diode *A* is forward biased, diode *B* is reverse biased

   $V_O = 6$ V

2. During negative half cycle :

i. **Case-1 :** When $V_{in} < -9$ V

   Diode *A* and *B*, both are reverse biased

   $V_O = V_{in}$

ii. **Case-2 :** When $V_{in} > -9$ V

   Diode *A* is reverse biased, diode *B* is forward biased

   $V_O = -9$ V

Que 1.22. **For the given clamper circuit shown in Fig. 1.22.1, determine the output voltage and also draw the waveform of output signal.**

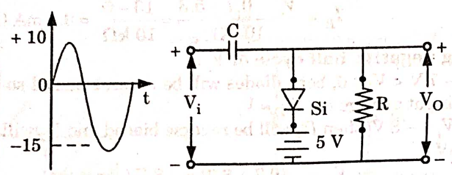


Fig. 1.22.1.

AKTU 2016-17(Sem-I), Marks 05

Answer

1. During positive pulse of V_i, the diode is short circuited. The voltage across R will be the same as across the battery (parallel).
   So,
   $$V_O = 5\text{ V}$$
2. The voltage that charge up the capacitor, applying KVL
   $$+10\text{ V} - V_c - 5\text{ V} = 0, \text{ then } V_c = 5\text{ V}$$
3. During negative pulse of V_i, the diode is open circuited. Applying KVL,
   $$V_O = -15 - 5 = -20\text{ V}$$

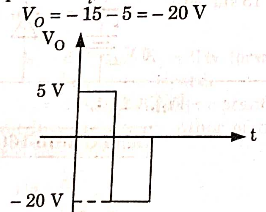


Fig. 1.22.2.

PART-5

Zener Diode as Shunt Regulator, Voltage-Multiplier Circuits.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.23. **How zener diode is used as shunt regulator ? Explain it.**

Answer

1. The circuit diagram for zener voltage/shunt regulator circuit is shown in Fig. 1.23.1.

2. The zener diode is selected with V_z equal to the voltage desired across the load.
3. Under reverse biased condition, voltage across zener diode practically remains constant, even if the current through it changes by a large extent.
4. Under normal conditions, the input current $I_i = I_L + I_z$ flows through resistor R. The input voltage V_i can be written as
   $$V_i = I_i R + V_z = (I_L + I_z) R + V_z$$

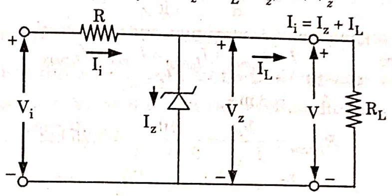


Fig. 1.23.1. Zener voltage regulator.

5. When the input voltage V_i increases, as the voltage across zener diode remains constant, the drop across R will increase with a corresponding increase in $I_L + I_z$.
6. As V_z is a constant, the voltage across the load will also remains constant and hence, I_L will be a constant.
7. Therefore, an increase in $I_L + I_z$ will result in an increase in I_z which will not alter the voltage across load. Thus, zener diode is used as a voltage regulator.
8. To operate zener diode as voltage regulator, the reverse voltage applied to zener diode never exceeds PIV of the diode and at the same time, the applied input voltage must be greater than the breakdown voltage of the zener diode.

Que 1.24.

i. **Find the range of R_L and I_L that will maintain a constant output of 10 V (Fig. 1.24.1).**

ii. **Also determine the maximum wattage rating of the zener diode for given circuit.**

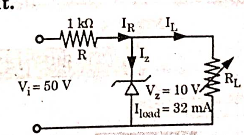


Fig. 1.24.1.

AKTU 2017-18(Sem-II), Marks 07

Answer

Given : $I_{z,max} = 32$ mA, $V_z = 10$ V
To Find : Range of I_L and R_L, maximum wattage.

1. From the circuit, $I = I_z + I_L$

   where, $I = \dfrac{V_i - V_z}{R} = \dfrac{50-10}{1\,k\Omega} = 40$ mA
2. When I_L is minimum, I_z is maximum and vice versa.
   Therefore, $I = I_{z,max} + I_{L,min} = I_{z,min} + I_{L,max}$
   $40 \times 10^{-3} = 32 \times 10^{-3} + I_{L,min}$
   $I_{L,min} = 8$ mA
3. Hence, $R_{L,max} = \dfrac{V_O}{I_{L,min}} = \dfrac{10}{8 \times 10^{-3}} = 1.25$ kΩ

   and $I = I_{z,min} + I_{L,max}$
4. Let $I_{z,min} = 5$ mA
   Therefore, $I_{L,max} = 40$ mA – 5 mA = 35 mA
   $R_{L,min} = \dfrac{V_O}{I_{L,max}} = \dfrac{10}{35\text{ mA}} = 285.72\ \Omega$
5. Hence, the range of I_L is between 8 mA and 35 mA while range of R_L is between 285.72 Ω and 1.25 kΩ.
6. Maximum wattage of zener diode is,
   $P_{zmax} = I_{zmax} V_z$
   $= 32 \text{ mA} \times 10 = 320 \times 10^{-3} = 0.32$ W

Que 1.25. **Determine the range of V_i for the Fig. 1.25.1, that will maintain the zener diode in "ON" state.**

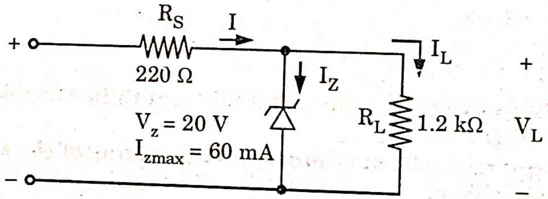


Fig. 1.25.1.

AKTU 2017-18 (Sem-I), Marks 3.5

Answer

Given : $R_S = 220\ \Omega$, $V_z = 20$ V, $I_{zmax} = 60$ mA, $R_L = 1.2$ kΩ, $V_L = V_z = 20$ V
To Find : Range of V_i.

1. We have $I_L = \dfrac{V_L}{R_L} = \dfrac{20}{1.2 \times 10^3} = 16.67$ mA
2. So, $V_{i\,min} = \dfrac{(R_S + R_L).V_z}{R_L} = \left(\dfrac{220+1200}{1200}\right) \times 20$
   $V_{i\,min} = 23.67$ V
3. Now, current through R_S
   $I = I_{zmax} + I_L = 60 + 16.67 = 76.67$ mA
4. So, $V_{i\,max} = I.R_S + V_Z = 76.67 \times 10^{-3} \times 220 + 20$
   $V_{i\,max} = 36.87$ V
   Hence, the range of V_i lies between 23.67 V and 36.87 V

Que 1.26. **For the network of Fig. 1.26.1, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the zener diode.**

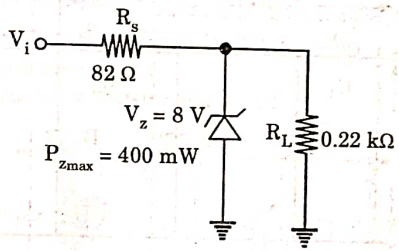


Fig. 1.26.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

The procedure is same as Q. 1.25, Page 1–33J, Unit-1.
Ans. Range is 10.98 V to 15.08 V.

Que 1.27. **Describe with the help of circuit diagram working of voltage tripler.**

AKTU 2015-16(Sem-I), Marks 05

OR

Explain with suitable circuit that how diode acts as a voltage multiplier ?

OR

Draw and discuss voltage tripler circuit.

AKTU 2016-17(Sem-I), Marks 05

Answer

1. Fig. 1.27.1 shows a circuit of general multiplier *i.e.*, this circuit can be used as a doubler, tripler and quadrupler.

2. Circuit-1 is a Doubler ($2V_m$).
   Circuit-2 is a Tripler ($3V_m$).
   Circuit-3 is a Quadrupler ($4V_m$).
3. During positive half cycle, the diode D_1 is ON and it charges capacitor C_1 to V_m.
4. In the first negative half cycle, the diode D_2 is ON and it charges C_2 to $2V_m$ ($V_{C2} = V_m + V_{C1} = 2V_m$). In this cycle the charge on capacitor C_1 starts discharging.
5. In the second positive half cycle the diode D_1 and D_3 are ON, the capacitor C_1 will be charged to V_m and the capacitor C_3 will be charged to

$$V_{C3} = V_i + (-V_{C1}) + V_{C2} = V_m - V_m + 2V_m$$
$$V_{C3} = 2V_m \text{ (Voltage across } C_3)$$

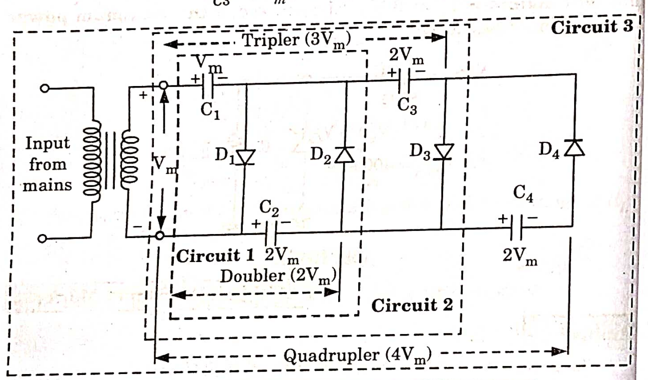


Fig. 1.27.1. General circuit diagram of multiplier.

6. During second negative half-cycle, the diode D_2 and diode D_4 are ON. The voltage across capacitor is given as :

$$V_{C4} = V_i + (V_{C2}) + V_{C3} + V_{C1} = V_m - 2V_m + 2V_m + V_m$$
$$V_{C4} = 2V_m$$

7. Now
   Voltage across $C_1 \rightarrow V_{C1} = V_m$
   Voltage across $C_2 \rightarrow V_{C2} = 2V_m$
   Voltage across $C_3 \rightarrow V_{C3} = 2V_m$
   Voltage across $C_4 \rightarrow V_{C4} = 2V_m$
8. **Voltage doubler :** Taking output across C_2.

$$V_O = V_{C2} = 2V_m$$

9. **Voltage tripler :** Taking output across C_3 and C_1.

$$V_1 = V_{C1} + V_{C3} = V_m + 2V_m = 3V_m$$

10. **Voltage quadrupler :** Taking output across C_2 and C_4

$$V_O = V_{C2} + V_{C4} = 2V_m + 2V_m = 4V_m$$

Que 1.28. What is voltage multiplier using *p-n* junction diode ? Explain the operation of voltage doublers.

OR

Explain full wave voltage doubler with clear diagram.

AKTU 2017-18(Sem-I), Marks 3.5

Answer

1. The circuit which produces a greater DC output voltage than AC input voltage using a rectifier circuit is called as voltage multiplier.
2. The output of voltage doubler is twice the peak input voltage.
3. There are two types of voltage doubler circuits :

i. Half wave voltage doubler :

1. The circuit diagram is shown in Fig. 1.28.1.

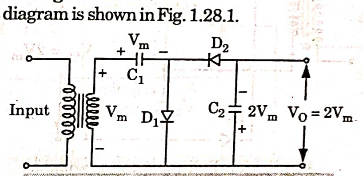


Fig. 1.28.1. Half wave voltage doubler.

2. During positive half-cycle of the input voltage, diode D_1 is forward biased (ON) and diode D_2 is reverse biased (OFF). Capacitor C_1 charges to the peak value of secondary voltage V_m with polarity.
3. During negative half-cycle, diode D_2 is ON while diode D_1 is OFF. Capacitor C_2 is charged up to a voltage *i.e.*, the sum of peak-supply voltage and the voltage across C_1.
4. During positive half-cycle : $V_{C1} = V_m$

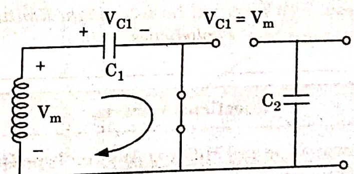


Fig. 1.28.2.

5. During negative half cycle :

$$-V_m - V_{C1} + V_{C2} = 0$$

$$-V_m - V_m + V_{C2} = 0$$
$$V_{C2} = 2V_m$$

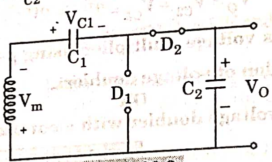


Fig. 1.28.3.

ii. Full wave voltage doubler :

1. The circuit diagram is shown in Fig. 1.28.4.
2. During positive half cycle, D_1 is ON and D_2 is OFF. Capacitor C_1 will be charged to a peak value V_m.

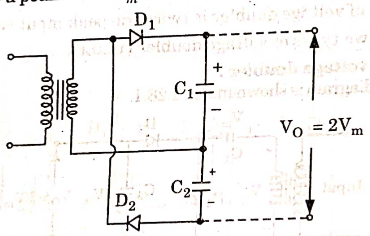


Fig. 1.28.4. Full wave voltage doubler.

$$V_{C1} = V_m$$

3. During negative half cycle, D_1 is OFF and D_2 is ON. Capacitor C_2 is charged to peak value V_m. Thus output voltage with no load connected :

$$V_O = V_{C1} + V_{C2}$$
$$V_O = 2V_m$$

PART-6

Special Purpose Two Terminal Devices : Light Emitting Diodes, Photodiodes.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.29. **What is LED ? Give its principle of working, construction and applications.**

Answer

A. LED : LED is a special type of semiconductor *p-n* junction that under forward bias emits external radiations in ultraviolet, visible and infrared regions of electromagnetic spectrum.

B. Construction of LED :

1. LED is just not an ordinary *p-n* junction diode where silicon is used. Here we use compound having elements like gallium, arsenic and phosphorus which are semitransparent unlike silicon which is opaque.
3. In all semiconductor *p-n* junctions, some of its energy will be given off as heat and some in the form of photons.
4. In the materials, such as gallium arsenide phosphide (GaAsP) or gallium phosphide (GaP), the number of photons of light energy emitted is sufficient to create a visible light source.

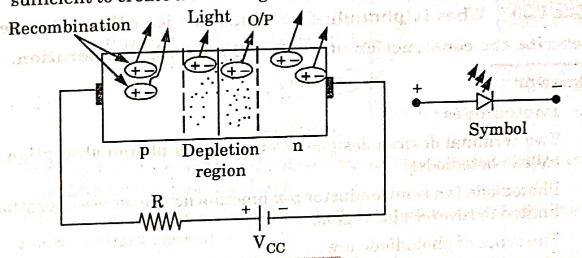


Fig. 1.29.1

C. Principle of LED :

1. The process involves :
   i. Generation of electron-hole pair (EHP) by excitation of semiconductor.
   ii. Recombination of EHP.
   iii. Extraction of photons from the semiconductor.
2. The characteristic for LED is given in Fig. 1.29.2.

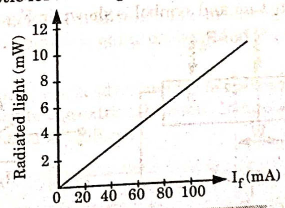


Fig. 1.29.2. Characteristics.

D. Working :

1. When LED is in forward bias condition, the electrons from *n*-type material cross the *p-n* junction and recombines with holes in the *p*-type material.
2. When recombination takes place, the recombining electrons release energy in the form of heat and light.
3. The emission depends upon the type of material, *i.e.*,
   GaAs → infrared radiation (invisible)
   GaP → red or green light (visible)
   GaAsP → red or yellow light (visible).

E. Applications :

1. Display LEDs like calculator, digital clocks etc.
2. Light source in optical fibre communication.
3. Light source in a source detector package like smoke detectors, tachometers, proximity detectors etc.

Que 1.30. **What is photodiode ? What are its different types ? Describe the construction of a photodiode with its operation.**

Answer

A. Photodiodes :

1. Two terminal devices designed to respond to photon absorption are called photodiodes.
2. Photodiode is a semiconductor *p-n* junction device whose operation is limited to reverse bias region.
3. The types of photodiode are :
   i. *p-n* diode
   ii. *p-i-n* diode
   iii. Avalanche diode
4. The output current of a reverse bias *p-n* junction changes when device is exposed to illumination.
5. The variation in the output current is linear with respect to luminous flux. The construction and symbol is shown in Fig. 1.30.1.

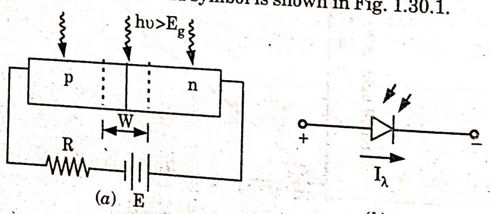


Fig. 1.30.1.

6. This diode is designed in such a manner that the rays are allowed to fall only on one surface across the junction. The remaining sides are restricted for the light to penetrate.
7. As the temperature due to illumination increases, more and more electron-hole pairs are generated and results in increasing the reverse saturation current.
8. When light rays fall on depletion width '*W*', it creates electron-hole pair and electrons are swept into *n*-region and holes into *p*-region very rapidly. This gives rise to a photo current. This is the basic principle of operation of photodiode.

B. Photodiode characteristics :

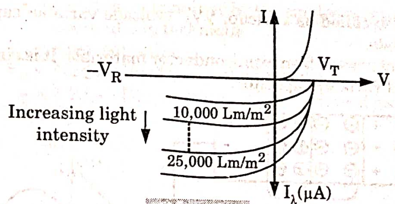


Fig. 1.30.2.

1. The Fig. 1.30.2 shows the *V-I* characteristics of *p-n* junction photodiode with different illumination level.
2. When no light ray is incident, the diode has a small reverse current I_λ known as dark current.
3. The dark current is that current which exists only with no applied illumination.
4. The increase in reverse voltage does not increase the reverse current significantly because all available charge carriers have already being swept across the junction.
5. The photodiode can also be used as a variable resistor controlled by light intensity.
6. Photodiode operates in quadrants, *i.e.*, in third quadrant, both *I* and *V* are negative and power is being delivered to the device from external circuit.
7. In fourth quadrant, *V* is positive and *I* is negative and power is delivered from the junction to the external circuit. In applications, usually third quadrant operation is preferred.

PART-7

Varacter Diodes, Tunnel Diodes, Liquid-Crystal Displays.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.31. **Explain input and output characteristics of varactor diode.** **AKTU 2015-16(Sem-II), Marks 05**

Answer

1. This is also called as varicap, VVC (voltage variable capacitance), or tuning diode.
2. This is constructed from semiconductor materials. It is simply a voltage dependent variable capacitor.

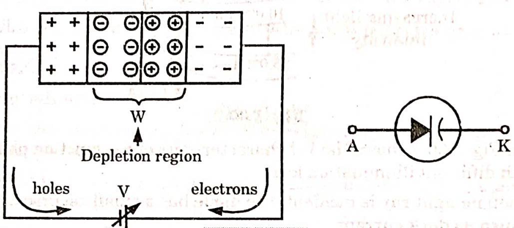


Fig. 1.31.1.

3. Fig. 1.31.1 shows the varactor diode in reverse-bias condition and symbol of varactor diodes.

   If $V \rightarrow$ larger, then $W \rightarrow$ wider
   $V \rightarrow$ smaller, then $W \rightarrow$ narrower
4. The depletion region W in this case acts like an insulator preventing the conduction between the n and p region of the diode, just like a dielectric which separates the two plates of a capacitor.
5. Let area of plates = A

   If distance between two capacitor plates = W

   then capacitance, $C = \in . \dfrac{A}{W}$

   where $\in$ = Permittivity of the semiconductor materials.

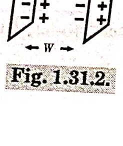


Fig. 1.31.2.

Varicap characteristics :

1. Fig. 1.32.3 shows the characteristics of a typical commercially available varicap diode.
2. We see that there is the initial sharp decline in C_T with increase in reverse bias.
3. The normal range of V_R for varactor diodes is limited to about 20 V.
4. In terms of the applied reverse bias, the transition capacitance is given approximately by

$$C_T = \frac{k}{(V_T + V_R)^n}$$

where k = Constant determined by the semiconductor material and construction technique

V_T = Knee potential

V_R = Magnitude of the applied reverse bias potential

n = 1/2 for alloy junction = 1/3 for diffused junction

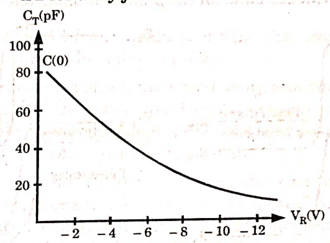


Fig. 1.31.3.

5. In terms of the capacitance at the zero-bias condition $C(0)$, the capacitance as a function of V_R is given by :

$$C_T(V_R) = \frac{C(0)}{(1 + |V_R / V_T|)^n}$$

Que 1.32. **Explain working and characteristics of Tunnel diode with the help of neat diagram.** **AKTU 2015-16(Sem-I), Marks 05**

OR

Discuss the construction and working of tunnel diode. Also sketch its I-V characteristics and explain. **AKTU 2017-18(Sem-II), Marks 07**

OR

Explain principle of operation and construction of tunnel diode. Draw its V-I characteristic. **AKTU 2016-17(Sem-II), Marks 5.25**

OR

Explain the V-I characteristic of tunnel diode.

AKTU 2016-17(Sem-I), Marks 05

OR

Explain tunnel diode. **AKTU 2017-18(Sem-I), Marks 3.5**

Answer

A. Principle of Operation of tunnel Diode :

i. In forward bias condition :

1. A small forward bias is applied across the junction.
2. Since, the potential of the p-side under this condition is higher than the potential of n-side, E_{Fp} will move below E_{Fn}, as shown in Fig. 1.32.1 (a) and the electrons in the conduction band on the n-side faces empty states in the valence band on the p-side, at same energy level.

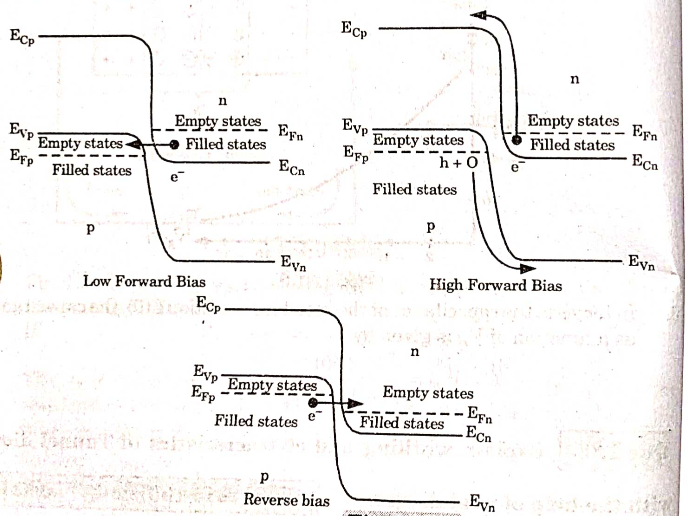


Fig. 1.32.1.

3. The thin barrier across the junction would permit tunneling of electrons from n-side to p-side, with the consequent current flowing from the p-side to n-side. Thus, I_D is positive for this case. As the forward bias is increased, more such filled states on the n-side would come opposite to the empty states.
4. With further increase in the forward bias, a specific condition would be reached when the maximum number of filled states in the conduction band on the n-side would face the maximum number of empty states in the valence band on the p-side. The tunneling current would reach a peak.

5. If the forward bias is increased further, then the conduction band of n-side would move away from the valence band of the p-side, and there would be no empty states on the p-side corresponding to the filled states on n-side.
6. Hence, tunneling current would go to zero and the normal diffusion component of current would dominate. This results in normal p-n junction diode characteristics.

ii. In reverse bias condition :

1. When negative voltage is applied to the p-side with respect to n-side, this would push E_{Fp} above E_{Fn} with their separation being equal to the applied voltage.
2. The filled states of the p-side are directly opposite to the empty states on the n-side across a very narrow barrier.
3. Thus, the electrons from p-side would easily tunnel through this thin barrier by the process of quantum mechanical tunneling and appear on the n-side.
4. Since, electrons travel from p-side to n-side, the actual direction of current is from n to p-side and is negative.
5. As the amount of reverse bias is increased, more number of filled states in the valence band of the p-side would appear opposite to the number of empty states in the conduction band of the n-side and the reverse current would keep on increasing with reverse voltage.

B. Characteristics : Due to heavy doping, the current in negative resistance region is suddenly increased with a small applied voltage. Due to this reduced depletion region the sudden increase in current (at small applied voltage) is called "carrier punching through" effect.

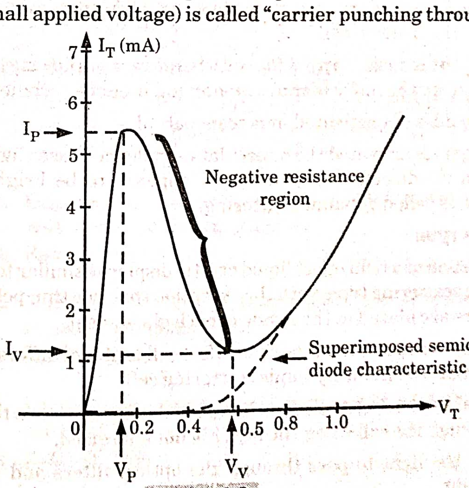


Fig. 1.32.2.

Que 1.33. Explain principle of operation of LCD.

AKTU 2016-17(Sem-I), Marks 05

Answer

1. Liquid crystal cell displays (LCDs) are used in similar applications where LEDs are used. These applications are display of numeric and alphanumeric characters in dot matrix and segmental displays.
2. The LCDs are of two types :
   a. **Dynamic scattering :**
   i. The construction of a dynamic scattering liquid crystal cell is shown in Fig. 1.33.1.

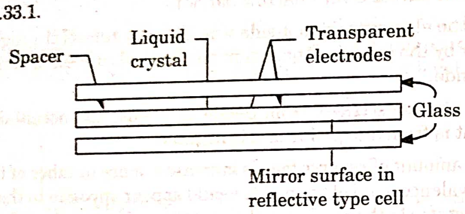


Fig. 1.33.1.

ii. The liquid crystal material may be one of the several organic compounds which exhibit optical properties of a crystal though they remain in liquid form.
iii. Liquid crystal is layered between glass sheets with transparent electrodes deposited on the inside faces.
iv. When a potential is applied across the cell, charge carriers flowing through the liquid disrupt the molecular alignment and produce turbulence.
v. When the liquid is not activated, it is transparent.
vi. When the liquid is activated the molecular turbulence causes light to be scattered in all directions and the cell appears to be bright. This phenomenon is called dynamic scattering.

b. **Field effect type :**
i. The construction of a field effect liquid crystal display is similar to that of the dynamic scattering type, with the exception that two thin polarizing optical filters are placed at the inside of each glass sheet.
ii. The liquid crystal material in the field effect cell is also of different type from that employed in the dynamic scattering cell.
iii. The material used is twisted nematic type and actually twists the light passing through the cell when the latter is not energized.
iv. This allows the light to pass through the optical filters and the cell appears bright.

v. When the cell is energised, no twisting of light takes place and the cell appears dull.

3. Liquid crystal cells are of two types :
   a. **Transmittive type :**
   i. In the transmittive type cell, both glass sheets are transparent, so that light from a rear source is scattered in the forward direction when the cell is activated.
   b. **Reflective type :**
   i. The reflective type cell has a reflecting surface on one side of glass sheets.
   ii. The incident light on the front surface of the cell is dynamically scattered by an activated cell.
   iii. Both types of cells appear quite bright when activated even under ambient light conditions.
4. The liquid crystals are light reflectors or transmitters and therefore they consume small amounts of energy (unlike light generators).
5. Considering the case of seven segment display the current is about 25 μA for dynamic scattering cells and 300 μA for field effect cells.
6. Unlike LEDs which can work on DC the LCDs require AC voltage supply.
7. A typical voltage supply to dynamic scattering LCD is 30 V peak to peak with 50 Hz.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Explain the V-I characteristic of *p-n* junction diode. Draw well labelled characteristic.

Ans. Refer Q. 1.2.

Q. 2. Explain the V-I characteristic of *p-n* junction diode. How it is differ from zener diode ?

Ans. Refer Q. 1.4.

Q. 3. Explain the working of half wave and full wave bridge rectifier.

Ans. Refer Q. 1.10.

Q. 4. For a half wave rectifier, derive an expression for ripple factor.

Ans. Refer Q. 1.11.

Q. 5. Differentiate between half wave and full wave rectifiers.

Ans. Refer Q. 1.12.

Q. 6. Sketch V_O for each network of Fig. 1, for the input shown.

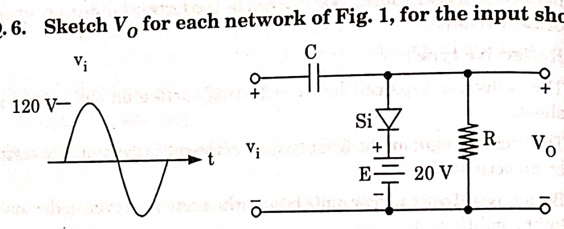


Fig. 1.

Ans. Refer Q. 1.17.

Q. 7. Describe with the help of circuit diagram working of voltage tripler.

Ans. Refer Q. 1.27.

Q. 8. What is voltage multiplier using *p-n* junction diode ? Explain the operation of voltage doublers.

Ans. Refer Q. 1.28.

Q. 9. Explain input and output characteristics of varactor diode.

Ans. Refer Q. 1.31.

Q. 10. Explain the V-I characteristic of tunnel diode.

2 UNIT

BJT and FET

CONTENTS

PART-1

Bipolar Junction Transistor : Transistor Construction, Operation, Amplification Action.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 2.1. **Explain BJT.**

Answer

1. A junction transistor is a three-layer semiconductor device, sandwich of one type of semiconductor material between two layers of the other type.
2. There are two types of transistors :
a. *npn* transistor and
b. *pnp* transistor.
3. When a layer of *p*-type material is sandwiched between two layers of *n*-type material, the transistor is known as *npn* as shown in Fig. 2.1.1(*a*).
4. Similarly, when a layer of *n*-type material is sandwiched between two layers of *p*-type material, the transistor is known as *pnp* transistor as shown in Fig. 2.1.1(*b*).
5. The transistors are made either from silicon or germanium crystal.
6. The symbols for *npn* and *pnp* transistors are also shown in Fig. 2.1.1.

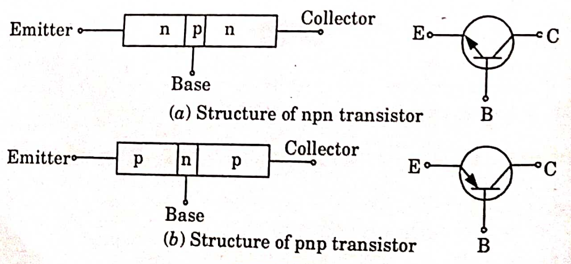


Fig. 2.1.1.

7. A transistor has three doped region :

a. **Emitter :**
i. This is the left hand section of the transistor.
ii. The main function of this region is to supply majority charge carriers (either holes or electrons) to the base and hence it is more heavily doped in comparison to other regions.

b. **Base :**
i. The middle section of the transistor is known as base.
ii. This is very lightly doped and is very thin (10^{-6} m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

c. **Collector :**
i. The right hand section of transistor is known as collector.
ii. The main function of the collector is to collect majority charge carriers through the base. This is moderately doped.

8. The arrow head direction indicates the conventional direction of current flow *i.e.*, in case of *npn* it is from base to emitter while in case of *pnp* it is from emitter to base.
9. In most of the cases the collector region is made large due to the fact that collector has to dissipate much greater power.
10. The junction between emitter and base may be called as emitter-base junction and junction between base and collector may be called as collector-base junction.
11. The emitter-base junction is always forward biased while the collector-base junction is reversed biased.
12. The resistance of emitter-base junction is very small as compared to collector-base junction.
13. So, forward bias applied to emitter-base junction is generally very small and reverse bias on collector-base junction is much higher.

Que 2.2. **Describe the operation of *pnp* transistor.**

Answer

1. *pnp* transistor with emitter base junction as forward bias and collector base junction as reversed biased is shown in Fig. 2.2.1.
2. The holes of *p*-region are repelled by positive terminal of battery V_{EE} towards the base.
3. The potential barrier at emitter base junction is reduced as it is forward bias and holes cross this junction and penetrate into *n*-region, constitute the emitter current I_E.
4. The width of base is very thin and only 5 % of holes recombine with the free electrons of *n*-region which constitutes the current I_B.

5. The remaining holes are able to drift across the base and enter into the collector region.
6. They are swept up by negative collector voltage V_{CC}. This constitutes the collector current I_C.

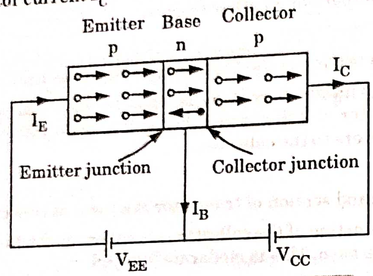


Fig. 2.2.1. Operation of pnp transistor.

7. As holes reach the collector, electrons are emitted from the negative terminal of battery and neutralize these holes.
8. Now a covalent bond near the emitter electrode breaks down. The liberated electron enters the positive terminal of battery V_{EE}. This process is repeated again and again.
9. As the width of the base region is very small, the ratio of hole current to electron current is very large so the electron current may be neglected.
10. Thus only the hole current plays the important role in the operation of *pnp* transistor.

Que 2.3. **Explain the operation of *npn* transistor.**

OR

Explain various current components in *npn* transistor with help of suitable diagram. **AKTU 2016-17(Sem-I), Marks 05**

Answer

1. The biasing of *npn* transistor is shown in Fig. 2.3.1.
2. The emitter base junction is forward biased because electrons are repelled from the negative terminal of battery V_{EE} towards the junction.
3. The collector base junction is reversed biased because electrons are flowing away from the collector junction towards the positive collector battery terminal V_{CC}.
4. The electrons in emitter region are repelled from the negative terminal of the battery towards the emitter junction.

5. Since the potential barrier at the junction is reduced due to forward bias and base region is very thin and lightly doped, electrons cross the *p*-type base region.
6. A few electrons combine with the holes in *p*-region and are lost as charge carrier.
7. Now electrons in *n*-region swept up by positive collector voltage V_{CC}. In this way electron conduction takes place, continuously so long as the two junctions are properly biased.
8. So the current conduction in *npn* transistor is carried out by the electrons.

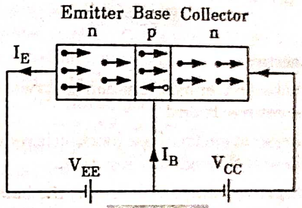


Fig. 2.3.1.

9. Applying Kirchhoff's current law,

$$I_E = I_C + I_B$$

10. The collector current has two components the majority and minority carriers. The minority current component is called leakage current (I_{CO}).

So, $$I_C = I_{C\,\text{majority}} + I_{CO\,\text{minority}}$$

Que 2.4. **Describe the biasing of BJT circuit.**

Answer

1. Biasing is necessary to establish the proper region of operation for AC amplification.
2. The emitter layer is heavily doped, base is lightly doped and collector is moderately doped.
3. This low doping level decreases the conductivity and hence increases the resistance of the material by limiting the number of "free" carriers.

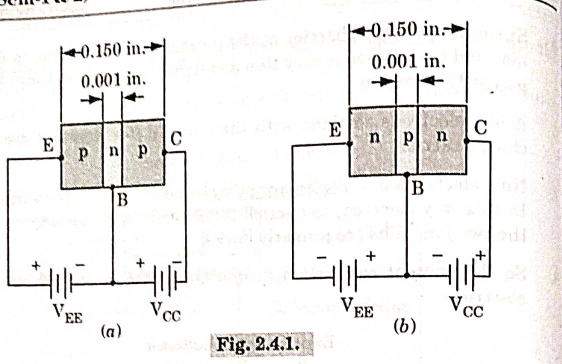


Fig. 2.4.1.

A. **For *pnp* transistor :**

i. *pnp* transistor with emitter base junction as forward bias and collector base junction as reverse biased.

ii. The potential barrier at emitter-base junction is reduced as it is forward biased and holes pass through this junction.

iii. By applying a negative voltage at collector, the holes are easily drifted across the collector-base junction to constitute a current I_C.

B. **For *npn* transistor :**

i. The emitter-base junction of *npn* is forward bias and the electron is repelled by a negative forward junction.

ii. The collector-base function is reverse bias because electrons flow toward positive collector battery terminal V_{CC} to constitute a current I_C.

Que 2.5. **Explain transistor as an amplifier in detail.**

Answer

1. The transistor has two *p-n* junctions *i.e.*, it is like two diodes. The junction between emitter and base may be called emitter-base diode or simply emitter diode. The junction between base and collector may be called as collector-base diode or collector diode. The basic circuit of a transistor amplifier is shown in Fig. 2.5.1.
2. The weak signal to be amplified is applied between emitter-base circuit and the output is taken across the load resistor R_L connected in the collector-base circuit.
3. Let us assume for instant V_{EE} is disconnected.
4. Now for negative peak of signal, the emitter base junction will be reversed bias, which is not desirable, because to achieve amplification, the input circuit should remain forward bias.

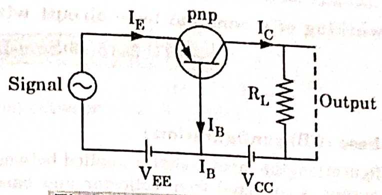


Fig. 2.5.1. Transistor as an amplifier.

5. A small change in signal voltage produces an appreciable change in emitter current because the input circuit has low resistance.
6. Due to transistor action, the change in emitter current causes almost the same change in collector current.
7. When the collector current flows through the load resistance R_L, a large voltage is developed across it.
8. In this way, a weak signal applied in the input circuit appears in the amplified form across the output circuit.
9. Let, small voltage change ΔV_i causes large emitter current change ΔI_E. We define it by the symbol α that fraction of this current change is collected and pass through R_L.

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad i.e., \Delta I_C = \alpha \Delta I_E$$

10. The change in output voltage across load resistor

$$\Delta V_O = R_L \times \Delta I_C$$
$$= R_L \times \alpha \times \Delta I_E$$

11. The voltage amplification

$$A = \frac{\Delta V_o}{\Delta V_i}$$

will be greater than unity and transistor acts as an amplifier.

PART-2

Common Base, Common Emitter, Common Collector Configuration.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 2.6. **Draw the basic structure of CB BJT and explain its principle of operation with in neat diagram along with its input and output characteristics.** AKTU 2017-18(Sem-II), Marks 07

OR

Explain the working of a common base circuit with its circuit diagram.

AKTU 2015-16(Sem-II), Marks 05

Answer

A. **Common-base (CB) configuration :**

1. In this configuration, the input signal is applied between emitter and base. The output is collected from collector and base as shown in Fig. 2.6.1.

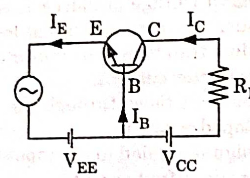


Fig. 2.6.1. Common-base *npn* transistor amplifier.

Current amplification factor (α) :

1. It is defined as the ratio of the collector current to the emitter current of a transistor when no signal is applied and is called DC alpha (α_{DC}).

$$\alpha_{DC} = \frac{I_C}{I_E}$$

2. Simply α_{DC} is α

Then $$\alpha = \frac{I_C}{I_E}$$

3. Higher the value of α better is the transistor in the sense that collector current approaches the emitter current.

$$I_C = \alpha I_E \text{ and } I_B = I_E - I_C$$
$$I_B = I_E - \alpha I_E = I_E(1-\alpha)$$

4. Now, when signal is applied, the ratio of change in collector to emitter current at constant collector base voltage is defined as current amplification factor.

$$\alpha_{AC} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$$

Practically $\alpha_{DC} = \alpha_{AC} = \alpha = 0.9$ to 0.99

5. Total collector current $I_C = \underbrace{\alpha I_E}_{\text{Majority}} + \underbrace{I_{CBO}}_{\text{Minority}}$

6. The collector current can also be expressed as

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

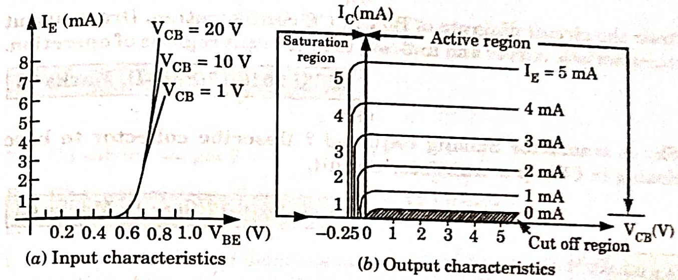
$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$

7. The relation between α and β is given by

$$\alpha = \frac{\beta}{1+\beta} \text{ or } 1-\alpha = \frac{1}{1+\beta}$$

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

B. **Characteristics of CB circuit :**



(*a*) Input characteristics (*b*) Output characteristics

Fig. 2.6.2.

a. **Input characteristics :**

i. There exists a cut in, offset or threshold voltage V_{BE} below which the current is very small.

ii. I_E increases rapidly with small increase in V_{BE} *i.e.*, input resistance is very small.

b. **Output characteristics :**

i. In active region, the collector current is independent of collector voltage and depends upon emitter current but if V_{CB} increases beyond a certain value, I_C increases rapidly due to avalanche breakdown.

In this region, the base emitter function is forward biased whereas collector base function is reversed biased.

ii. In cut off region, a small amount of collector current flows even when $I_E = 0$, *i.e.*, leakage current I_{CBO}.

Here emitter base and collector base junctions both are reversed biased.

iii. In saturation region, current I_C flows even if $V_{CB} \cong 0$.

Here collector and emitter junctions both are forward biased.

Que 2.7. **Draw and explain the input and output characteristics of common emitter configuration.**

AKTU 2015-16(Sem-I), Marks 05

OR

OR

Draw the common emitter circuit and sketch the input and output characteristics. Also explain active region, cut-off region and saturation region by indicating them on the characteristics curve.

AKTU 2017-18(Sem-I), Marks 07

OR

Draw the CE configuration circuit of BJT and explain its input and output characteristics.

AKTU 2015-16(Sem-II), Marks 7.5

OR

Draw the circuit diagram of BJT in CE configuration. Draw output characteristic curves and indicate the different regions of operation.

AKTU 2016-17(Sem-I), Marks 05

OR

Why is transistor biasing required ? Describe collector to base biasing in CE *n-p-n* transistor circuit.

AKTU 2016-17(Sem-I), Marks 05

Answer

A. **CE configuration :**

1. In CE configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter.
2. As emitter is common to input and output circuits, hence the name common emitter configuration and is shown in Fig. 2.7.1.

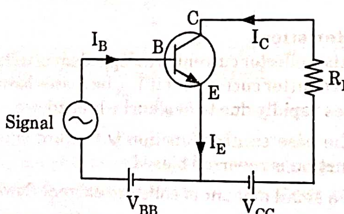


Fig. 2.7.1. Common-emitter *npn* transistor amplifier.

3. The base current amplification factor is the ratio of collector current to the base current and is also called DC beta (β_{DC}) of a transistor, when no signal is applied.

$$\beta_{DC} = \beta = \frac{I_C}{I_B}$$

4. When signal is applied, the ratio of change in collector current to the change in base current is defined as current amplification factor.

$$\beta_{AC} = \beta = \frac{\Delta I_C}{\Delta I_B}$$

$$I_C = \beta I_B$$

β is generally greater than 20 and ranges from 20 to 500. Hence, this configuration is frequently used when current gain as well as voltage gain is required.

5. Total collector current

$$I_C = \beta I_B + I_{CEO}$$

6. We know that $I_E = I_B + I_C$

$$I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

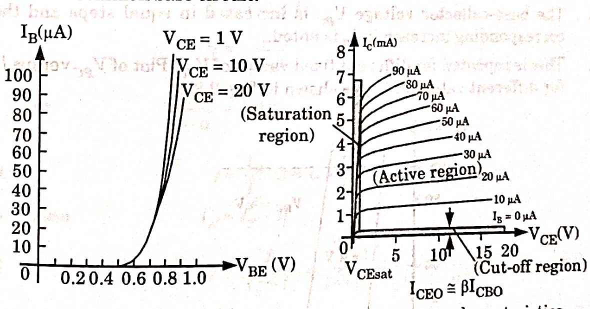
7. On solving we get $\beta = \dfrac{\alpha}{1-\alpha}$ and $I_{CEO} = \dfrac{1}{1-\alpha} I_{CBO}$

B. **Characteristics of common emitter circuit :**

a. **Input characteristic :**

i. The forward biased diode curve is expected because the base emitter section of transistor is a diode and it is forward biased.

ii. In this case, I_B increases less rapidly with V_{BE} as compared to common base configuration *i.e.*, input resistance of common emitter is higher than common base circuit.



(*a*) Input characteristics (*b*) Output characteristics

Fig. 2.7.2.

b. **Output characteristics :**

i. In active region, for small values of base current, the effect of collector voltage over collector current is small while for large base current values effect increases. Thus, the current gain of this configuration is greater than unity.

ii. When V_{CE} has very low value, the transistor is said to be saturated. The change in I_B does not produce a corresponding change in I_C.

iii. In cut-off region, a small amount of I_C flows even when $I_B = 0$. *i.e.*, I_{CEO} and the transistor is said to be cut-off.

C. **Transistor biasing :** Refer Q. 2.4, Page 2–5J, Unit-2.

Que 2.8. **Explain the operation of common collector configuration with suitable characteristics in detail.**

Answer

1. The circuit diagram for determining the static characteristics of an *npn* transistor in the common collector configuration is shown in Fig. 2.8.1.

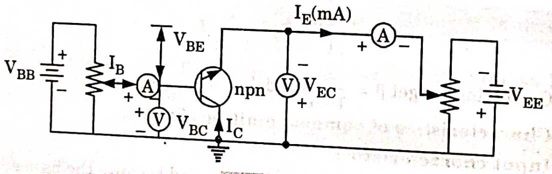


Fig. 2.8.1.

Input characteristics :

1. To determine the input characteristics, V_{EC} is kept at a suitable fixed value.
2. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted.
3. This is repeated for different fixed values of V_{EC}. Plot of V_{BC} versus I_B for different values of V_{EC} is shown in Fig. 2.8.2.

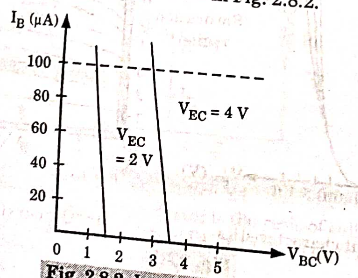


Fig. 2.8.2. Input characteristics.

Output characteristics :

1. The output characteristics shown in Fig. 2.8.3 are the plots of V_{EC} versus I_C for different values of I_B.

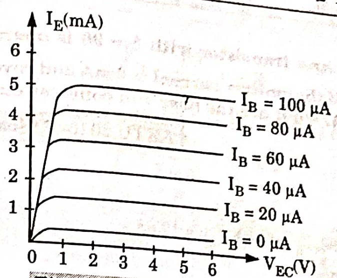


Fig. 2.8.3. Output characteristics.

Que 2.9. **Derive the relation between α, β and γ.**

Answer

1. We know, $\alpha = \dfrac{I_C}{I_E}$ and $\beta = \dfrac{I_C}{I_B}$

2. $$I_E = I_B + I_C,\ I_B = I_E - I_C$$

3. Now $$\beta = \frac{I_C}{I_E - I_C} = \frac{I_C / I_E}{1 - I_C / I_E} = \frac{\alpha}{1-\alpha}$$

$$\beta(1-\alpha) = \alpha \text{ or } \beta - \beta\alpha = \alpha$$

$$\beta = \alpha(1+\beta)$$

$\therefore$ $$\alpha = \frac{\beta}{1+\beta}$$

or $$\frac{1}{1-\alpha} = 1 + \beta$$

4. $$\gamma = \frac{I_E}{I_B} \text{ and } \alpha = \frac{I_C}{I_E}$$

5. Also $$I_B = I_E - I_C$$

6. $$\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1-(I_C/I_E)} = \frac{1}{1-\alpha} \quad ...(2.9.1)$$

7. We have, $$1 - \alpha = \frac{1}{1+\beta} \quad ...(2.9.2)$$

8. Put values of eq. (2.9.2) in eq. (2.9.1)

$$\gamma = \frac{1}{1-\alpha} = 1 + \beta$$

Que 2.10. An *npn* transistor with β = 98 is operated in the CE configuration, if the emitter current is 2 mA and reverse saturation current is 12 μA. What are the base and collector current ?

AKTU 2016-17(Sem-I), Marks 05

Answer

Given : $\beta = 98$, $I_E = 2$ mA, $I_{sat} = 12\ \mu$A
To Find : I_B, I_C

$$\alpha = \frac{\beta}{1+\beta} = \frac{98}{1+98} = 0.989$$

$\because$
$$\alpha = \frac{I_C}{I_E}$$

$\therefore$
$$I_C = \alpha I_E = 0.989 \times 2 = 1.978 \text{ mA}$$
$$I_B = I_E - I_C = 2 - 1.978 = 0.022 \text{ mA}$$

Que 2.11. For the network of Fig. 2.11.1

a. Determine R_B and R_E
b. Find V_B, V_{CE}, and V_{BC}

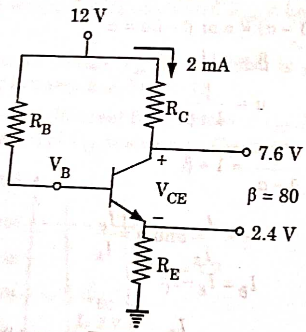


Fig. 2.11.1.

AKTU 2017-18(Sem-I), Marks 07

Answer

Given : $V_{CC} = 12$ V, $V_C = 7.6$ V, $V_E = 2.4$ V, $\beta = 80$
To Find : R_B, R_E, V_B, V_{CE}, V_{BC}

1. We have,
$$V_{CE} = V_C - V_E = 7.6\text{ V} - 2.4\text{ V} = 5.2\text{ V}$$

2. Now
$$\alpha = \frac{\beta}{\beta+1} = \frac{80}{80+1} = 0.98$$

So,
$$I_E = I_C/\alpha = 2 \text{ mA and } I_B = I_C/80 = 0.025 \text{ mA}$$
$$R_E = \frac{V_E}{I_E} = \frac{2.4\text{ V}}{2\text{ mA}} = 1.2\text{ k}\Omega$$

3. Now
$$V_{CC} = V_{CE} + I_C R_C + I_E R_E$$
$$12 = 5.2 + 2R_C + 1.2 \times 2$$
$$R_C = 2.2\text{ k}\Omega$$

and
$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$
$$12 = 0.025\text{ mA} \times R_B + 0.7\text{ V} + 1.2 \times 2$$
$$R_B = 356\text{ k}\Omega$$

Now,
$$V_B = V_E + V_{BE} = 2.4 + 0.7 = 3.1\text{ V}$$
$$V_{BC} = V_B - V_C$$
$$= 3.1 - 7.6 = -4.5\text{ V}$$

Que 2.12. For the voltage divider configuration of Fig. 2.12.1, determine r_e, A_v, Z_{in} and Z_O.

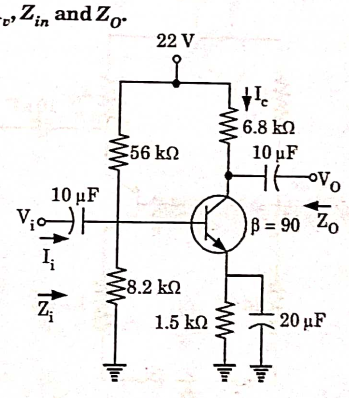


Fig. 2.12.1.

AKTU 2015-16(Sem-I), Marks 10

Answer

1. Using approximate approach,
$$V_B = \frac{8.2 \times 10^3 \times 22}{(56 + 8.2) \times 10^3} = 2.81\text{ V}$$

2.
$$V_E = V_B - V_{BE} = 2.81 - 0.7 = 2.11\text{ V}$$

3.
$$I_E = \frac{V_E}{R_E} = \frac{2.11}{1.5 \times 10^3} = 1.41\text{ mA}$$

4. $$r_e = \frac{V_T}{I_E} = \frac{26 \times 10^{-3}}{1.41 \times 10^{-3}} = 18.44\ \Omega$$

5. $$R' = (56\ \text{k}\Omega) \parallel (8.2\ \text{k}\Omega)$$
$$= \frac{56 \times 8.2 \times 10^3}{(56 + 8.2)} = 7.15\ \text{k}\Omega$$

6. $$Z_{in} = R' \parallel \beta r_e = (7.15\ \text{k}\Omega) \parallel (90)\,(18.44\ \Omega)$$
$$= 7.15\ \text{k}\Omega \parallel 1.659\ \text{k}\Omega$$
$$= \frac{7.15 \times 1.659 \times 10^3}{(7.15 + 1.66)} = 1.35\ \text{k}\Omega$$

7. $$A_v = -\frac{R_C}{r_e} = -\frac{6.8 \times 10^3}{18.44} = -368.76$$

8. $$Z_O = R_C = 6.8\ \text{k}\Omega$$

Que 2.13. Given that $I_{CQ} = 2$ mA and $V_{CEQ} = 10$ V, determine R_1 and R_C for the network of Fig. 2.13.1.

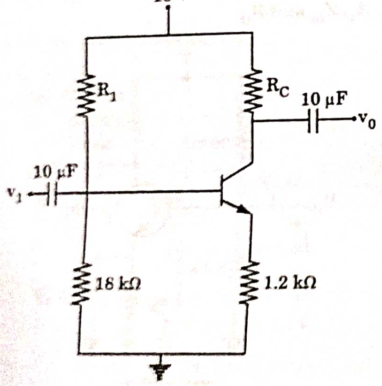


Fig. 2.13.1.

AKTU 2016-17(Sem-II), Marks 07

Answer

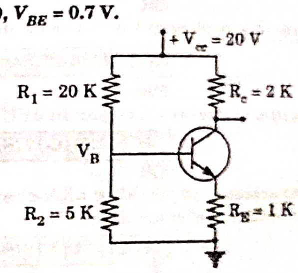
Given : $I_{CQ} = 2$ mA, $V_{CEQ} = 10$ V, $R_E = 1.2$ kΩ, $R_2 = 18$ kΩ
To Find : R_1, R_C.

1. $$V_B = \frac{18\ \text{k}\Omega}{R_1 + 18\ \text{k}\Omega} \times 18\ \text{V} = \frac{324 \times 10^3}{R_1 + 18 \times 10^3}\ \text{V} \quad ...(2.13.1)$$

2. $$I_C = I_E = \frac{V_B - V_{BE}}{R_E}$$
$$2 \times 10^{-3} = \frac{\dfrac{324 \times 10^3}{R_1 + 18 \times 10^3} - 0.7}{1.2 \times 10^3}$$
$$R_1 = 86.5\ \text{k}\Omega$$

3. $$V_{CE} = V_{CC} - I_C\,(R_C + R_E)$$
$$10 = 18 - 2 \times 10^{-3}\,(R_C + 1.2 \times 10^3)$$
$$R_C = 2.8\ \text{k}\Omega$$

Que 2.14. For the circuit shown in Fig. 2.14.1, determine V_B, I_C, V_C. Given that $\beta = 80$, $V_{BE} = 0.7$ V.



AKTU 2016-17(Sem-I), Marks 7.5

Answer

$$R_{th} = R_1 \| R_2 = \frac{20 \times 5}{20 + 5} = 4\ \text{K}$$

$$V_{th} = V_B = \frac{20 \times 5}{20 + 5} = 4\ \text{V}$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1 + \beta)R_E} = \frac{4 - 0.7}{4 + 81} = 0.0388\ \text{mA}$$

$$I_c = \beta . I_B = 80 \times 0.0388 = 3.11\ \text{mA}$$

$$V_c = V_{cc} - I_c R_c = 20 - (3.11 \times 2) = 13.8\ \text{V}$$

PART-3

Field Effect Transistor : Construction and Characteristics of JFETs, Transfer Characteristics.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 2.15. Explain the transconductance curve of a JFET.

AKTU 2015-16(Sem-II), Marks 05

OR

Draw the circuit and explain the drain characteristic fo N-channel JFET.

AKTU 2016-17(Sem-I), Marks 05

OR

Draw and explain the n-channel JFET and draw its transfe characteristics.

AKTU 2016-17(Sem-II), Marks 5.2

OR

Explain the formation of depletion region in JFET.

AKTU 2016-17(Sem-I), Marks 7.

OR

Explain the construction and working of N-channel JFET. Dra the drain characteristics and transfer curve.

AKTU 2017-18(Sem-I), Marks 3.

Answer

JFET (Junction Field Effect Transistor) :

A. **Basic construction :**

1. The structure of n-channel field effect transistor is shown in Fig. 2.15.1.

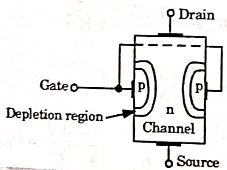


Fig. 2.15.1. Junction field-effect transistor (JFET).

2. For the fabrication of n-channel JFET, a narrow bar of n-typ semiconductor material is taken. Now on opposite sides of its midd part, two heavily doped p-type regions are formed by diffusion as show in Fig. 2.15.1.
3. The junctions form two p-n diodes or gates.
4. The area between the gates is called a channel.
5. Actually the two p-regions are internally connected and a single lead i taken out, which is called as gate junction.

6. Ohmic contacts are made at the two ends of n-type semiconductor bar.
7. One lead is called as source terminal S and the other as drain terminal D.
8. When a potential difference is established between source and drain, a current flows from one end to the other end in n-type material which forms a sort of channel. This current consists of majority carriers which in this case are electrons.

B. **Operation of n-channel FET :**

1. The operation of n-channel FET can be understood with the help of Fig. 2.15.2.
2. First suppose that the gate has been reversed biased by gate battery V_{GG} and drain battery is not connected. So that space charge region or depletion region on either side of a reverse biased p-n junction are formed.
3. Further consider effect of drain battery V_{DD} while V_{GG} is removed.
4. The voltage V_{DD} is dropped across the n-channel resistance (say R_{DS}) giving rise to a drain current.

$$I_D = V_{DD} / R_{DS}$$

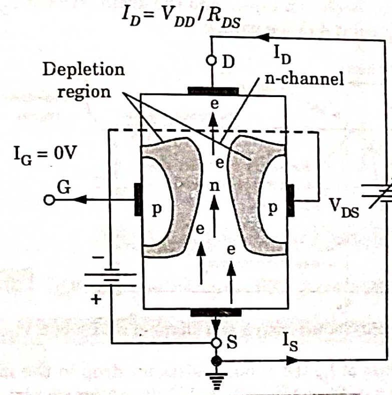


Fig. 2.15.2. Operation of FET.

5. Consider two points A and B in n-channel as shown in Fig. 2.15.3.
6. Let V_A and V_B be potential drop at these points. Certainly $V_A > V_B$, so due to progressive voltage drop, the reverse biasing effect is stronger near drain.

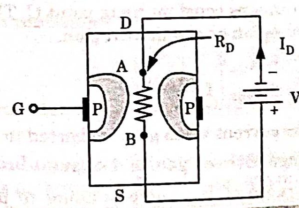


Fig. 2.15.3. Voltage drop across channel.

7. This explains why the depletion regions extend farther into the channel at point A than at point B.
8. This gate bias increases the depletion regions and thereby decreases the cross-section of n-channel due to which I_D decreases. Since negative gate voltage controls the drain current, FET is called a voltage controlled device.

C. Static Characteristics of FET (*V-I*) :

1. Static means I_D versus V_{DS} for different values of V_{GS}.
2. Let us consider the characteristics for $V_{GS} = 0$, the curve is shown in Fig. 2.15.4.
3. When $V_{DS} = 0$, there is no attracting potential at the drain and hence drain current $I_D = 0$, although the channel between the gates is fully open as $V_{GS} = 0$.
4. As V_{DS} is increased, the electrons flow from source to drain through channel between depletion layers and the drain current I_D increases linearly up to a point A (knee point).

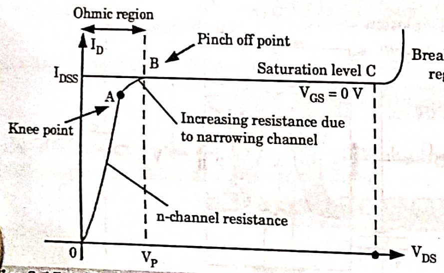


Fig. 2.15.4. Drain characteristics of n-channel FET when $V_{GS} = 0$.

With the increase of I_D, the ohmic resistance drop in the material of semiconductor bar. So as the voltage V_{DS} is progressively increased, the drain current I_D, from point A, increases at reverse square law rate up to point B which is called pinch-off point. The corresponding voltage is called pinch-off voltage and is denoted by V_P.

6. As V_{DS} is further increased, the channel resistance also increases in such a way, that I_D remains constant up to point C. The region BC is known as saturation region or amplifier region.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

where I_{DSS} = Drain current when gate is shorted to source, and V_{GS} = Voltage between gate and source.

7. With continued increase of V_{DS} corresponding to point C (called avalanche breakdown voltage V_A), eventually breakdown across the gate junction takes place and current I_D shoots to a high value.

D. Transfer characteristics :

1. The transfer characteristics is a plot of drain current I_D, versus voltage between gate and source V_{GS} for a constant value of voltage between drain and source V_{DS}. This is shown in Fig. 2.15.5.
2. When $V_{GS} = 0, I_D = I_{DSS}$

   and $I_D = 0, V_{GS} = V_P$
3. The transfer characteristic follows the equation

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS}\ (off)}\right)^2$$

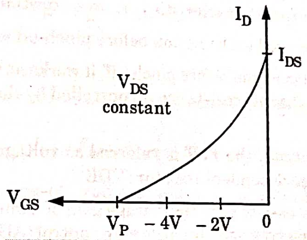


Fig. 2.15.5. Transfer characteristics.

Que 2.16. **Discuss the various FET parameters with respect to common source configuration.**

Answer

i. **DC drain resistance R_{DS} :** This is the static or ohmic resistance of the channel.

It is given by :

$$R_{DS} = \left[\frac{V_{DS}}{I_D}\right]$$

ii. **AC drain resistance :**

$$r_d = \left[\frac{\Delta V_{DS}}{\Delta I_D}\right] \quad V_{GS} \text{ held constant}$$

This is evaluated at $V_{GS} = 0$ *i.e.*, when FET is operating in the pinch-off region.

iii. **Transconductance :** The control that the gate voltage has over drain current is measured by forward transconductance g_{fs} and is similar to mutual conductance g_m. It is simply the slope of transfer characteristics.

$$g_{fs} = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) \quad V_{DS} \text{ held constant}$$

The unit of g_{fs} is siemens (mho).

iv. **Amplification factor :** The amplification factor μ is defined as

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) \quad I_D \text{ held constant}$$

Que 2.17. **Explain with the help of necessary diagrams, how FET can be used as (Voltage Controlled Resistor) VVR.**

Answer

1. In most of the linear applications, JFET is operated in constant current portion of its output characteristics *i.e.*, in saturation region.
2. FET can also be used in the region before pinch-off where V_{DD} is small.
3. FET when used in region before pinch-off, it works as variable resistance device *i.e.*, the channel resistance is controlled by the gate bias voltage (V_{GS}).
4. In such applications, the FET is referred as voltage variable resistor (VVR) or voltage dependent resistor (VDR).
5. The VVR can be used to vary the voltage gain of a multistage amplifier. This action is referred as automatic gain control (AGC).
6. If the signal is low then voltage gain of the stages can be increased and when becomes high, the gain can be reduced automatically. In this way, the general level of amplification is maintained fairly constant.
7. The circuit arrangement of AGC amplifier using the FET as voltage variable resistor is shown in Fig. 2.17.1.

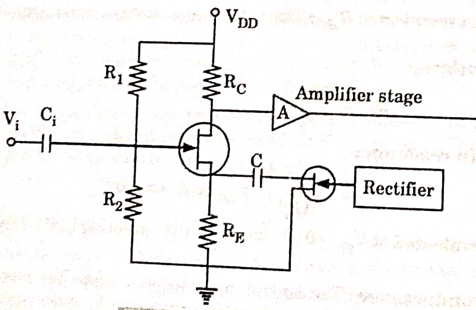


Fig. 2.17.1. FET as VVR.

8. The input signal V_i is amplified by amplifier.
9. It is then rectified and filtered to produce DC voltage proportional to output signal level. This voltage is applied to the gate of the FET so that the AC resistance between drain and source changes.
10. Capacitor '*C*' isolates the transistor from FET so that the bias conditions of transistor are not affected.
11. Thus, when output increases, V_{GS} also increases and R_{DS} changes so that the gain of the transistor decreases. Thus automatically the gain is controlled.

Que 2.18. **Show that the transconductance g_m of JFET is related to drain current I_{DS} by**

$$g_m = \frac{2}{V_P}\sqrt{I_{DSS} I_{DS}}$$

Answer

1. As we know, the saturation drain current, I_{DS} is given by

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad ...(2.18.1)$$

where V_P is pinch-off voltage and I_{DSS} is the value of I_{DS} when $V_{GS} = 0$.

2. Differentiating eq. (2.18.1) with respect to V_{GS}, we get

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

3. We know that, $g_m = \dfrac{\partial I_{DS}}{\partial V_{GS}}$, V_{DS} is constant

$$\therefore \quad g_m = -\frac{2 I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \quad ...(2.18.2)$$

4. From eq. (2.18.1), we have

$$\left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

5. Substituting this value in eq. (2.18.2), we get

$$g_m = \frac{-2 I_{DSS}}{V_P}\sqrt{\frac{I_{DS}}{I_{DSS}}}$$

$$g_m = \frac{-2}{V_P}\sqrt{\frac{(I_{DSS})^2 I_{DS}}{I_{DSS}}} = \frac{2}{|V_P|}\sqrt{I_{DSS}\, I_{DS}}$$

[∵ V_P may be positive or negative]

Que 2.19.

i. **Draw the schematic diagram of self-biasing JFET amplifier.**
ii. **Explain the CMOS inverter circuit working operation.**

AKTU 2015-16(Sem-II), Marks 10

OR

Draw the CE n-p-n BJT characteristics. Also explain the self bias configuration in DC bias configuration.

AKTU 2016-17(Sem-II), Marks 10

Answer

A. **CE characteristics :** Refer Q. 2.7, Page 2-9J, Unit-2.

B. **Self bias configuration :**

1. The self bias configuration eliminates the need of two DC supplies i.e., only drain supply is used and no gate supply is connected.
2. Fig. 2.19.1 shows the arrangement, a resistor R_S is connected in the source leg of the configuration. This is known as bias resistor.
3. The DC component of drain current I_D flowing through R_S makes a voltage drop across resistor R_S.
4. The capacitor C_S bypasses the AC component of drain current.

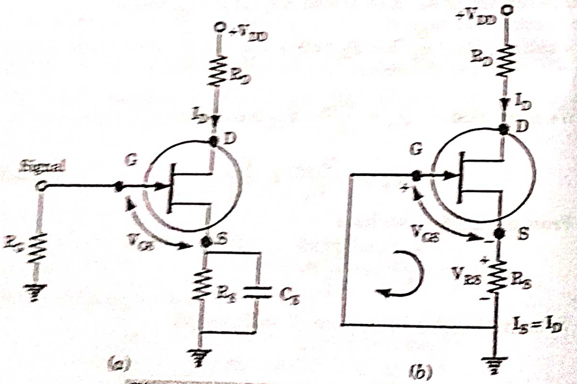


Fig. 2.19.1. Self bias configuration.

5. The addition of R_G in circuit does not upset the DC bias, but avoid the short-circuiting of the AC input voltage. Otherwise, the leakage current would build up static charge at the gate which could change the bias.
6. R_S also help to prevent any variation in FET drain current.

7. Let there be an increase in the drain current. This will increase the voltage drop across resistor R_S and this results in decrease of channel width. So, the drain current is reduced.
8. For DC analysis, the capacitors can be replaced by open circuit and the resistor R_G replaced by short-circuit equivalent. Since $I_G = 0$ A. The equivalent circuit is shown in Fig. 2.19.1(b).
9. For the indicated loop, we have

$$-V_{GS} - V_{RS} = 0$$
$$V_{GS} = -V_{RS}$$
$$V_{GS} = -I_D R_S$$

10. The gate is kept at this much negative potential with respect to ground.

but $\quad I_D = I_S$

and $\quad V_{DS} = V_{DD} - I_D(R_S + R_D)$

In addition $\quad V_S = I_D R_S,\ V_G = 0\text{ V}$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

C. **CMOS Inverter :**

1. An inverter is a logic element that "inverts" the applied signal. That is, if the logic level of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level 5 V, and vice versa.
2. In Fig. 2.19.2, both gates are connected to the applied signal and both drain to the output V_O.
3. The source of the p-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, whereas the source of the n-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output.
4. With 5 V at V_i (with respect to ground), $V_{GS_1} = V_i$, and Q_1 is ON, resulting in a relatively low resistance between drain and source as shown in Fig. 2.19.2.
5. Since V_i and V_{SS} are at 5 V, $V_{GS_2} = 0$ V, which is less that the required V_T for the device, resulting in an OFF state.
6. The resulting resistance level between drain and source is quite high for Q_2, as shown in Fig. 2.19.2.
7. A simple application of the voltage-divider rule will reveal that V_O is very close to 0 V, or the 0-state, establishing the desired inversion process.
8. For an applied voltage V_i of 0 V (0-state), $V_{GS_1} = 0$ V, and Q_1 will be OFF with $V_{SS_2} = -5$ V, turning on the p-channel MOSFET.
9. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_O = V_{SS} = 5$ V (the 1-state).

10. Since the drain current that flows for either case is limited by the OFF transistor to the leakage value, the power dissipated by the device in either state is very low.

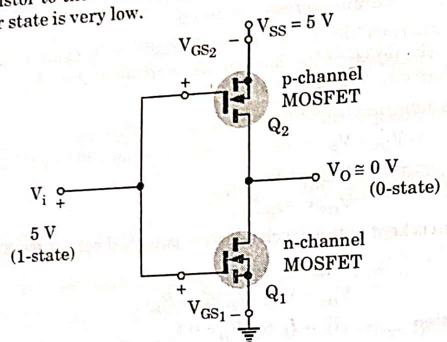


Fig. 2.19.2. CMOS inverter.

PART-4

MOSFET (Depletion and Enhancement)Type, Transfer Characteristic.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 2.20. **Draw the circuit of *n*-channel depletion type MOSFET and explain its operation. Also draw its drain and transfer characteristics.** **AKTU 2017-18(Sem-II), Marks 07**

OR

Describe the construction and basic connection of depletion MOSFET. **AKTU 2016-17(Sem-I), Marks 05**

OR

Explain construction and working of depletion MOSFET. **AKTU 2017-18(Sem-I), Marks 3.5**

Answer

1. For the depletion mode, the gate is maintained at negative potential while the drain is maintained at positive potential.

2. When voltage between gate and source is zero ($V_{GS} = 0$), as shown in the Fig. 2.20.1., significant current flows for a given V_{DS}, like a FET.

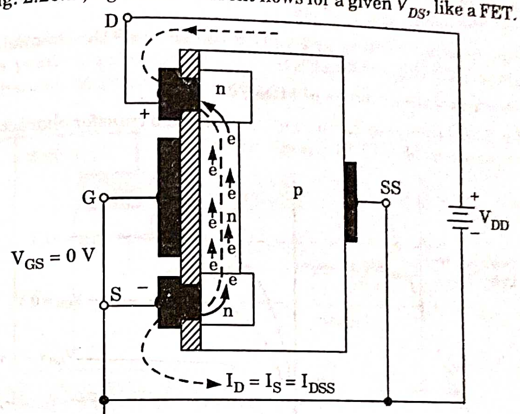


Fig. 2.20.1. Depletion mode MOSFET.

3. Let negative potential is applied at the gate. In such case positive charges are induced in *n*-channel through SiO_2 as shown in Fig. 2.20.2.

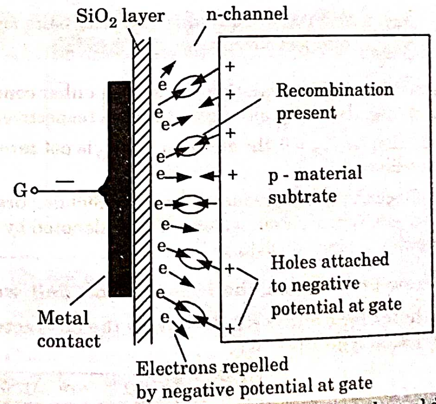


Fig. 2.20.2. Reduction in free carriers in a channel due to a negative potential at the gate terminal.

4. This mechanism depletes the channel from majority carriers *i.e.*, electrons, and hence conductivity decreases.

10. When a negative gate voltage is applied between gate to source, this negative gate voltage creates a hole accumulation layer as shown in Fig. 2.21.3.

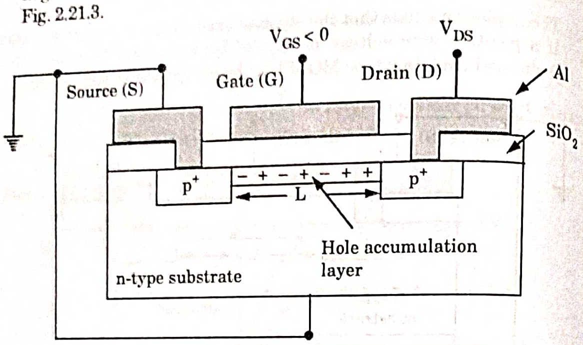
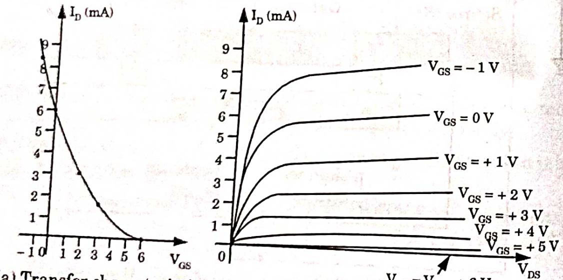


Fig. 2.21.3. Cross-section of a *p*-channel depletion MOSFET with $V_{GS} < 0$.

11. Due to accumulation of holes in the *p*-type channel, drain current increases.
12. The drain and transfer characteristics are shown in Fig. 2.21.4.



(a) Transfer characteristics (b) Drain characteristics

Fig. 2.21.4.

Que 2.22. **Describe the working operation of enhancement mode and depletion mode MOSFET. Also derive an expression for g_m of JFET configuration.**

AKTU 2015-16(Sem-II), Marks 7.5

Answer

A. **Depletion mode MOSFET :** Refer Q. 2.20, Page 2–26J, Unit-2.

B. **Expression for g_m :** Refer Q. 2.18, Page 2–23J, Unit-2.

C. **Enhancement MOSFET :**

1. Fig. 2.22.1 shows the cross-sectional view of *n*-channel enhancement MOSFET.

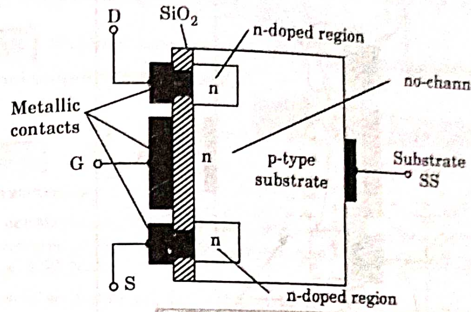


Fig. 2.22.1. Enhancement MOSFET.

2. It consists of a lightly doped *p*-type substrate into which two heavily doped n^+-regions are diffused. This n^+-regions act as source and drain respectively.
3. A thin layer of insulating SiO_2 is grown over the entire surface and holes are cut into the oxide layer through which metal contacts are to be made for source and drain terminals.
4. On SiO_2 layer, a conducting layer of aluminium overlaid, covering entire channel length from source to drain, constitute the gate.

Working of Enhancement MOSFET :

1. The channel, the insulating dielectric SiO_2 and metal layer of gate forms a parallel plate capacitor.
2. When a positive potential is applied at the gate with respect to substrate, negative charges are induced on semiconductor side.
3. These negative charges, induced on *p*-type substrate consist of electrons which forms an inversion layer as shown in Fig. 2.22.2.
4. The inversion layer forms an effective *n*-type channel.
5. When the positive potential at the gate is increased, the magnitude of the induced negative charges in semiconductor increases.
6. Thus, the conductivity of induced *n*-channel increases and results in increased drain current.
7. For a constant drain voltage, the drain current increases as the positive drain voltage increases *i.e.*, the drain current has been enhanced by the application of positive gate voltage. Such MOSFET is termed as an enhancement MOSFET.

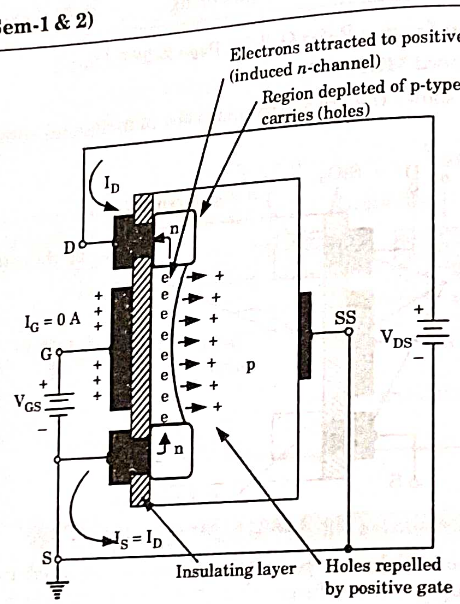


Fig. 2.22.2. Channel formation in the *n*-channel enhancement type MOSFET.

Characteristics curves of enhancement MOSFET :

1. Fig. 2.22.3 shows the static drain and transfer characteristics of *n*-channel enhancement MOSFET.
2. From Fig. 2.22.3, as V_{GS} is made positive, the drain current first increases slowly and then at relatively fast rate with increase of V_{GS}.

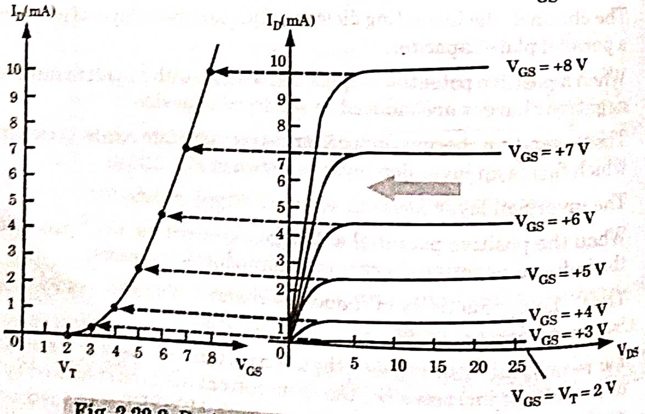


Fig. 2.22.3. Drain and transfer characteristics for an n-channel enhancement-type MOSFET.

3. The threshold voltage is defined as the gate voltage at which channel is induced to produce the flow of current I_D of prescribed value and is denoted by V_T. Such type of FET is very useful in switching applications, since no gate voltage is required to hold it off.

Que 2.23. **Explain construction, working and characteristics of *p*-channel enhancement MOSFET.**

AKTU 2015-16(Sem-I), Marks 05

Answer

A. Construction :

1. The construction of a *p*-channel enhancement type MOSFET is exactly the reverse of that *n*-channel enhancement type MOSFET. It is shown in Fig. 2.23.1(*a*).
2. There is an *n*-type substrate and *p*-doped regions under the drain and source connections.
3. The terminal remains as identified, but all the polarities and the current directions are reversed.

B. Operation :

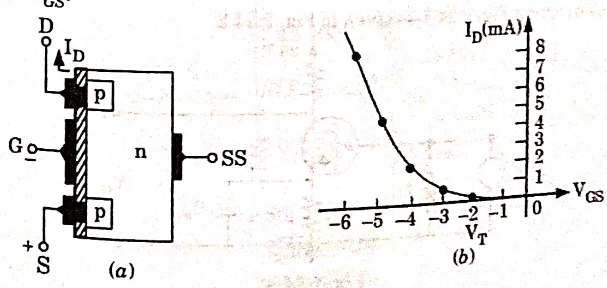
i. When $V_{SG} < |V_{tp}|$:
There is no channel and transistor operates in cut-off mode *i.e.*, $i_D = 0$.

ii. When $V_{DG} > |V_{tp}|$ or $V_{SD} < |V_{OV}|$:
The continuous channel is created and transistor operates in triode region.

iii. When $V_{DG} \le |V_{tp}|$ or $V_{SD} \ge |V_{OV}|$:
The channel is pinched-off and the transistor operates in saturation region.

C. Characteristics :

1. The drain characteristics will appear as shown in Fig 2.23.1(*b*), with increasing levels of current resulting from increasingly negative values of V_{GS}.



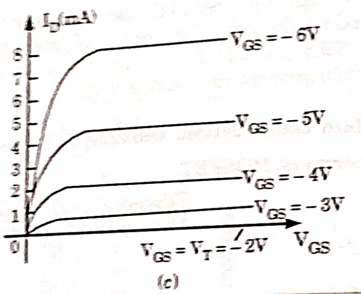


Fig. 2.23.1. *p*-channel enhancement-type MOSFET.

2. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of *n*-channel enhancement MOSFET.
3. The transfer curve is shown in Fig. 2.23.1(*c*), with I_D increasing with increasingly negative values of V_{GS} beyond V_T.

Que 2.24. **Determine Z_i, Z_o, V_o for the network of Fig. 2.24.1 if $V_i = 20$ mV.**

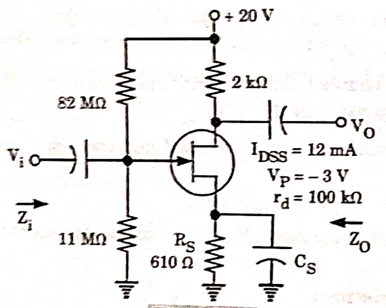


Fig. 2.24.1.

Answer

1. Converting Fig. 2.24.1 as given in Fig. 2.24.2.

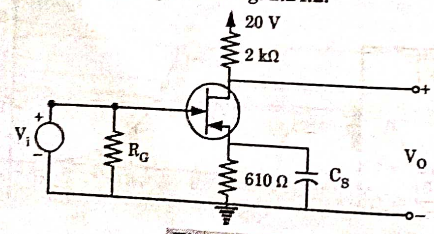


Fig. 2.24.2.

where, $R_G = 82\,M\Omega \,\|\, 11\,M\Omega$

2. $Z_i = R_G = 82\,M\Omega \,\|\, 11\,M\Omega = \dfrac{82 \times 11 \times 10^6}{82 + 11} = 9.698\,M\Omega$

3. $Z_O = r_d \,\|\, R_D$

$$= \frac{100 \times 10^3 \times 2 \times 10^3}{(100 + 2) \times 10^3} = 1.96\text{ k}\Omega$$

4. For V_{GS}, $\dfrac{20 \times 11}{82 + 11} = I_D \times 610$

$$I_D = 3.880\text{ mA}$$

5. $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$3.88 \times 10^{-3} = 12 \times 10^{-3}\left[1 - \frac{V_{GS}}{-3}\right]^2$$

$$\frac{3.88 \times 10^{-3}}{12 \times 10^{-3}} = \left[1 + \frac{V_{GS}}{3}\right]^2$$

$$V_{GS} = -1.294$$

6. We know that $g_m = \dfrac{-2\,I_{DSS}}{V_P}\left[1 - \dfrac{V_{GS}}{V_P}\right]$

$$g_m = \frac{-2 \times 12 \times 10^{-3}}{-3}\left(1 - \frac{(-1.294)}{(-3)}\right) = 4.55\text{ ms}$$

7. $V_{gs} = V_i = 20$ V

8. We know, $V_O = -g_m V_{gs}(r_d \,\|\, R_D)$

$$V_O = -4.55 \times 10^{-3}\left[\frac{100 \times 2 \times 10^3}{100 + 2}\right] = -8.92\text{ V}$$

Que 2.25. **Determine I_D, V_{GS}, V_D, V_S and V_{DS} for the given network as shown in Fig. 2.25.1.**

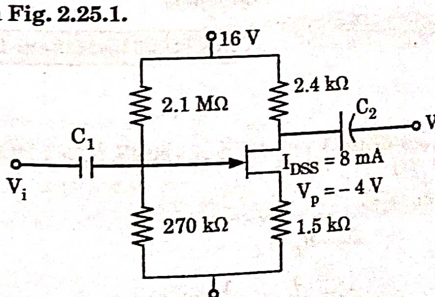


Fig. 2.25.1.

Answer

Given : $I_{DSS} = 8$ mA, $V_p = -4$ V
To Find : I_D, V_{GS}, V_D, V_S, V_{DS}

1. $$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{270 \times 16}{2100 + 270} = 1.82 \text{ V}$$
2. $$V_{GS} = V_G - I_D R_S = 1.82 - 1.5\, I_D$$
3. As, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
4. On solving, $I_{DQ} = 2.41$ mA
5. $V_{GSQ} = 1.82 - 2.41 \times 1.5 = -1.795$ V
6. $V_D = V_{DD} - I_D R_D = 16 - 2.41 \times 2.4 = 10.216$ V
7. $V_S = I_D R_S = 3.615$ V
8. $V_{DS} = V_D - V_S = 6.601$ V
9. $V_{DG} = V_D - V_G = 8.396$ V

Que 2.26. **Determine Z_i, Z_O and A_v for the network of Fig. 2.26.1, i $I_{DSS} = 12$ mA, $V_P = -6$ V, and $Y_{OS} = 40$ micro siemens.**

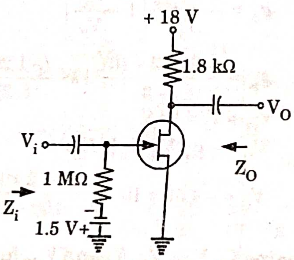


Fig. 2.26.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

Given : $I_{DSS} = 12$ mA, $V_P = -6$ V, $Y_{OS} = 40$ µS, $R_G = 1$ MΩ, $R_D = 1.8$ kΩ, $Z_i = R_G = 1$ MΩ
To Find : Z_i, Z_o, A_v

1. We have, $$Z_O = R_D \| r_d$$
2. $$r_d = \frac{1}{Y_{OS}} = \frac{1}{40 \text{ µS}} = 25 \text{ k}\Omega$$

3. $Z_O = (1.8 \text{ k}\Omega) \,||\, (25 \text{ k}\Omega) = 1.68$ kΩ
4. $$g_m = g_{mO}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$
5. $$g_{mO} = \frac{2\, I_{DSS}}{|V_P|} = \frac{2 \times 12 \times 10^{-3}}{6} = 4 \text{ mS}$$
6. $$g_m = 4 \times 10^{-3}\left(1 - \frac{(-1.5)}{(-6)}\right) = 3 \text{ mS}$$
7. $A_V = -g_{mO}(R_D \,||\, r_d)$
8. $A_V = -(3 \text{ mS})\,(1.8 \text{ k}\Omega \,\|\, 25 \text{ k}\Omega)$
   $A_V = -(3 \text{ mS}) \times (1.68 \text{ k}\Omega)$
   $A_V = -5.04$

Que 2.27. **For the voltage divider network shown in Fig. 2.27.1. Given $I_{DSS} = 10$ mA, $Vp = -3.5$ V, determine V_G, I_{DQ}, V_{GSQ}, V_D, V_S and V_{DSQ}.**

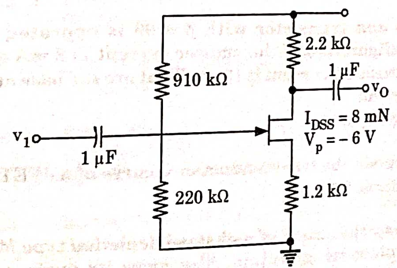


Fig. 2.27.1.

AKTU 2017-18(Sem-II), Marks 07

Answer

The procedure is same as Q. 2.25, Page 2–35J, Unit-2.

Ans. $V_G = 3.33$ V, $V_{GS} = V_{GSQ} = -1.662$ V, $V_{DSQ} = 3.188$ V, $V_D = 8.188$ V, $V_S = 5$ V, $I_{DQ} = 4.16$ mA

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Explain the operation of *npn* transistor.

Ans. Refer Q. 2.3.

Q. 2. Draw the basic structure of CB BJT and explain its principle of operation with in neat diagram along with its input and output characteristics.

Ans. Refer Q. 2.6.

Q. 3. Draw and explain the input and output characteristics of common emitter configuration.

Ans. Refer Q. 2.7.

Q. 4. An *npn* transistor with β = 98 is operated in the CB configuration, if the emitter current is 2 mA and reverse saturation current is 12 μA. What are the base and collector current ?

Ans. Refer Q. 2.10.

Q. 5. Explain the transconductance curve of a JFET.

Ans. Refer Q. 2.15.

Q. 6. Draw the circuit of *n*-channel depletion type MOSFET and explain its operation. Also draw its drain and transfer characteristics.

Ans. Refer Q. 2.20.

Q. 7. Describe the working operation of enhancement mode and depletion mode MOSFET. Also derive an expression for g_m of JFET configuration.

Ans. Refer Q. 2.22.

Q. 8. Explain construction, working and characteristics of *p*-channel enhancement MOSFET.

Ans. Refer Q. 2.23.

☺☺☺

3 UNIT

Operational Amplifiers and IoT

CONTENTS

PART-1

Operational Amplifier : Introduction, Op-Amp Basic.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 3.1. **Define Op-Amp with the help of block diagram. Also draw its equivalent circuit.**

Answer

1. Op-Amp is designed to perform various mathematical operations.
2. The Fig. 3.1.1 represents the block diagram approach of an operational amplifier.

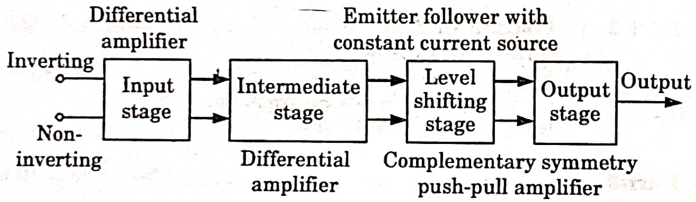


Fig. 3.1.1. Block diagram of Op-Amp.

3. It consists of two differential amplifiers followed by level shifter and an output stage.
4. The input stage is a dual input differential amplifier which provides most of the voltage gain to operational amplifier. It also provides high resistance to operational amplifier.
5. The intermediate stage is also dual input. This is driven by the output of first stage and is used to provide some additional gain. The DC level at the output of intermediate stage is well above the ground level.
6. The level shifter is an emitter follower using constant current source. The function of level shifter is to shift DC level at the output of intermediate stage downwards to zero volt with respect to ground.
7. The output stage is generally push-pull amplifier. Its function is to increase large output voltage swing capability and to provide low output resistance.
8. Fig. 3.1.2 shows the equivalent circuit of operational amplifier.
9. V_{id} is the difference of two input voltages *i.e.*, $(V_2 - V_1)$. R_i is the input resistance.

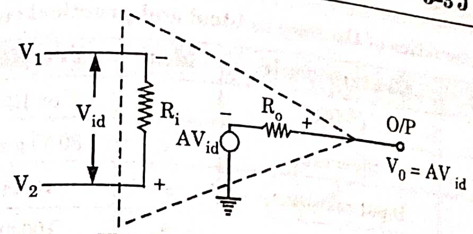


Fig. 3.1.2. Equivalent circuit.

10. R_o is the output resistance which is Thevenin's equivalent.
11. The voltage source AV_{id} is an equivalent Thevenin's voltage source.
12. The output voltage is directly proportional to the difference between the two input voltages.
13. It has open-loop voltage gain of 1,00,000, input impedance of 2 MΩ, and output impedance of 75 Ω.
14. Fig. 3.1.3 shows popular package style and the pin diagram.

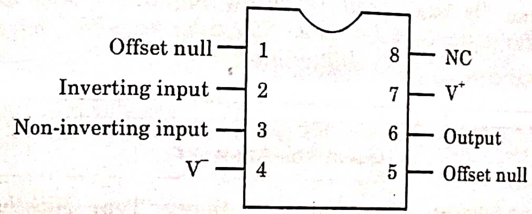


Fig. 3.1.3. Dual in line package.

Que 3.2. **Define Op-Amp with the help of block diagram. Also describe the equivalent circuit along with its ideal and practical characteristics.**

OR

Define Op-Amp with the help of block diagram. Also draw its equivalent circuit. List the ideal characteristics of Op-Amp.

AKTU 2017-18(Sem-II), Marks 07

OR

Draw the block diagram and equivalent circuit of an Op-Amp. Explain ideal characteristics of an Op-Amp.

AKTU 2015-16(Sem-II), Marks 7.5

Answer

A. **Op-Amp :** Refer Q. 3.1, Page 3–2J, Unit-3.

B. Characteristics of Op-Amp in ideal and practical cases :

S. No.	Characteristic	Ideal	Practical
1.	CMRR	∞	10^6 or 120 dB
2.	Slew rate	∞	80 V/ μ sec
3.	Input resistance	∞	$10^6 \Omega$
4.	Output resistance	0	100 Ω
5.	Voltage gain A_V	∞	10^6
6.	Bandwidth	∞	10^6 Hz
7.	Offset voltage	0	Negligible
8.	Offset current	0	Negligible

PART-2

Practical Op-Amp Circuits (Inverting Amplifier, Non-inverting Amplifier, Unity Gain Amplifier, Summing Amplifier, Integrator, Differentiator).

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 3.3. **Draw the circuit of an Op-Amp as voltage follower and find an expression for its voltage gain.**

OR

Draw and derive relationship for Op-Amp as closed loop non-inverting amplifier circuit. **AKTU 2016-17(Sem-I), Marks 05**

OR

Derive an expression for voltage gain of inverting and non-inverting ideal operational amplifier configurations.

AKTU 2017-18(Sem-I), Marks 07

Answer

A. Inverting Op-Amp :

1. Fig. 3.3.1 shows the basic inverting amplifier with input resistance R_1 and feedback resistance R_f.

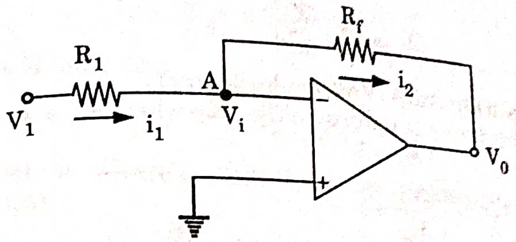


Fig. 3.3.1. Inverting amplifier.

2. The current i_1 flowing through R_1 is given by,

$$i_1 = \frac{V_1 - V_i}{R_1} = \frac{V_1}{R_1} \quad (\because V_i = 0 \text{ due to virtual ground})$$

and

$$i_2 = \frac{V_i - V_0}{R_f} = \frac{-V_0}{R_f}$$

3. At point A,

$$\frac{V_1}{R_1} = -\frac{V_0}{R_f}$$

$$A_v = \frac{V_0}{V_1} = -\frac{R_f}{R_1}$$

B. Non-inverting amplifier :

1. The circuit for non-inverting amplifier is shown in Fig. 3.3.2.

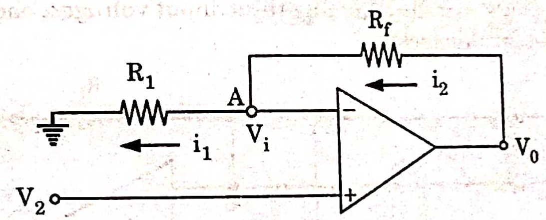


Fig. 3.3.2. Non-inverting amplifier.

2. The currents i_1 and i_2 are given as :

$$i_1 = \frac{V_2}{R_1} \text{ and } i_2 = \frac{V_0 - V_2}{R_f} \quad (\because V_i = V_2 \text{ due to virtual ground})$$

3. Applying KCL at point A,

$$(-i_1) + i_2 = 0 - \frac{V_2}{R_1} + \frac{V_0 - V_2}{R_f} = 0$$

$$\frac{V_0}{R_f} = \frac{V_2}{R_1} + \frac{V_2}{R_f} = V_2\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$\frac{V_0}{V_2} = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1}\right)$$

$$A_V = \left(1 + \frac{R_f}{R_1}\right)$$

C. Unity gain Op-Amp (Voltage Follower) :

1. Fig. 3.3.3 represents unity gain Op-Amp where $R_1 \to \infty$.

$$A_V = 1$$

$$\frac{V_0}{V_{in}} = 1$$

$$V_0 = V_{in}$$

2. The voltage gain is unity and the output voltage follows the input voltage.

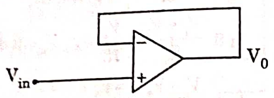


Fig. 3.3.3.

Que 3.4. **Explain summing amplifier using Op-Amp.**

AKTU 2015-16(Sem-II), Marks 03

Answer

1. Fig. 3.4.1 shows the three input summer circuit. This circuit provides a means of algebraically summing three input voltages, each multiplied by a constant gain factor.

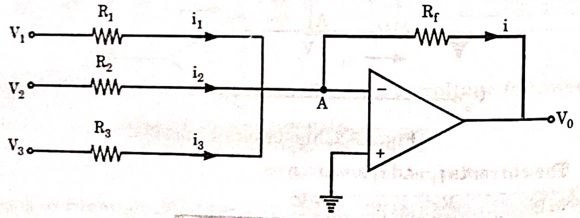


Fig. 3.4.1. Summer circuit.

2. At point A (virtual ground), the different currents are given as :

$$i_1 = \frac{V_1}{R_1}, i_2 = \frac{V_2}{R_2}, i_3 = \frac{V_3}{R_3} \text{ and } i = -\frac{V_0}{R_f}$$

3. Applying KCL at point A, we get,

$$i_1 + i_2 + i_3 - i = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_0}{R_f} = 0$$

$$V_0 = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

4. If $R_1 = R_2 = R_3 = R$, then

$$V_0 = -\frac{R_f}{R}[V_1 + V_2 + V_3]$$

5. Thus the output voltage is proportional to the algebraic sum of three input voltages.

Again, if $R_f = R$,

$$V_0 = -[V_1 + V_2 + V_3]$$

Que 3.5. **Calculate the output voltage for the circuit of Fig. 3.5.1 with inputs of V_1 = 40 mV rms and V_2 = 20 mV rms.**

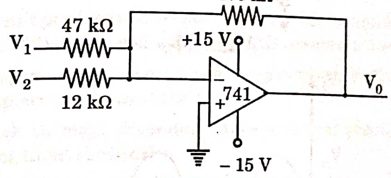


Fig. 3.5.1.

AKTU 2016-17(Sem-II), Marks 07

Answer

Given : V_1 = 40 mV rms, V_2 = 20 mV rms, R_1 = 47 kΩ, R_2 = 12 kΩ, R_f = 470 kΩ.

To Find : V_0.

$$V_0 = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right] = -\left[\frac{470}{47} \times 40 + \frac{470}{12} \times 20\right]$$

$$= -[400 + 783.3] = -1183.33 \text{ mV rms}$$

$$= -1.18 \text{ V rms}$$

Que 3.6. **Explain zero crossing detector using Op-Amp.**

AKTU 2015-16(Sem-II), Marks 03

Answer

1. The basic comparator can be used as a zero crossing detector when V_{ref} is set to zero.

2. An inverting zero-crossing detector is shown in Fig. 3.6.1 and the output waveform for a sinusoidal input signal is shown in Fig. 3.6.2. The circuit is also called a sine-to-square wave generator.

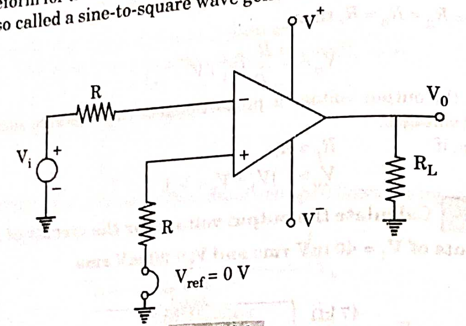


Fig. 3.6.1.

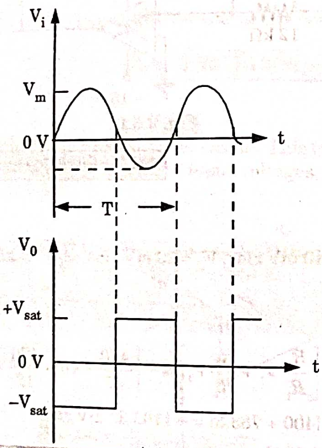


Fig. 3.6.2. Input and output waveforms.

Que 3.7. **Explain integrator circuit using Op-Amp.**

AKTU 2015-16(Sem-II), Marks 04

OR

Explain how Op-Amp can be used as

i. Integrator **ii. Inverting summer and**

iii. Voltage follower.

AKTU 2017-18(Sem-I), Marks 07

OR

Explain the operation of Op-Amp as integrator.

AKTU 2017-18(Sem-II), Marks 3.5

OR

Draw the circuit diagram of an integrator using Op-Amp and explain its working.

AKTU 2016-17(Sem-I), Marks 05

OR

Write a short note on differentiator.

Answer

A. **Integrator :**

1. The circuit of integrator is shown in Fig. 3.7.1.
2. This circuit produces an output voltage which is proportional to the time integral of the input voltage. Due to this reason it is known as integrator.
3. The integrator is an inverting Op-Amp in which feedback resistor R_f has been replaced by a capacitor C.
4. Feedback through capacitor forces a virtual ground to exist at the inverting input terminal.
5. The capacitive reactance X_c can be expressed as :

$$i_1 = \frac{V_1}{R_1} \text{ and } i_2 = \frac{d\,q_2}{dt} = C\frac{d(V_A - V_0)}{dt}$$

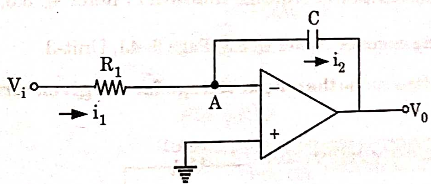


Fig. 3.7.1.

6. At point A :

$$i_1 = i_2$$

$$\frac{V_1}{R_1} = -C\frac{d\,V_0}{dt}$$

$$d\,V_0 = \frac{-1}{R_1 C} V_i\,dt$$

$$V_0(t) = -\frac{1}{R_1 C}\int V_1(t)\,dt$$

The above equation shows that the output is the integral of the input with an inversion and scale multiplier of $1/R_1C$.

B. Differentiator :

1. The function of a differentiator is to give an output voltage which is proportional to the rate of change of input voltage.
2. The circuit of a differentiator is shown in Fig. 3.7.2.

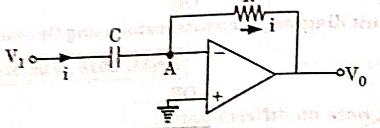


Fig. 3.7.2.

3. When we feed linearly increasing voltage to the differentiator, we get a constant DC output. So it is an inverse mathematical operation to that of an integrator.
4. At point A, $V_1 = \dfrac{q}{C}$

$$\frac{dV_1}{dt} = \frac{1}{C}\frac{dq}{dt} = \frac{i}{C} \quad \text{where } i = \frac{dq}{dt} \qquad \text{... (3.7.1)}$$

$$V_0 = -iR \qquad \text{...(3.7.2)}$$

5. Put the value of i from eq. (3.7.1) in eq. (3.7.2)

$$V_0 = -CR\frac{dV_1}{dt} \qquad \text{...(3.7.3)}$$

6. The eq. (3.7.3) shows that the output voltage V_0 is equal to a constant $(-CR)$ times the time derivative of the input voltage V_1.

C. Unity gain amplifier (voltage follower) : Refer Q. 3.3, Page 3–4J, Unit-3.

D. Inverting summer : Refer Q. 3.3, Page 3–4J, Unit-3.

Que 3.8. Determine the output voltage for the given circuit shown in Fig. 3.8.1.

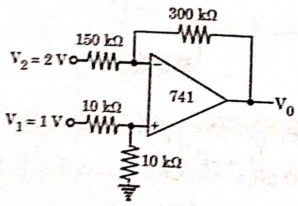


Fig. 3.8.1.

AKTU 2017-18(Sem-II), Marks 3.5

Answer

1. We can get V_0 by superposition method,

2. Let $V_1 = 1$ V and V_2 is at ground, so output due to V_1, V_{01}, will be due to input at non-inverting terminal,

$$\therefore \quad V_{01} = \left(1+\frac{300}{150}\right)\left(\frac{10}{(10+10)}\right) = \frac{1}{2}\times\frac{450}{150} = \frac{3}{2} = 1.5 \text{ V}$$

3. Let $V_2 = 2$ V and V_1 is at ground, so output due to V_2, V_{02} will be due to input at inverting terminal,

$$V_{02} = -\frac{300}{150} \times 2 = -4 \text{ V}$$

4. Now total output, $V_0 = V_{01} + V_{02}$

$$V_0 = +1.5 - 4 = -2.5 \text{ V}$$

Que 3.9. Find out the voltage V_2 and V_3 of the given network of Fig. 3.9.1.

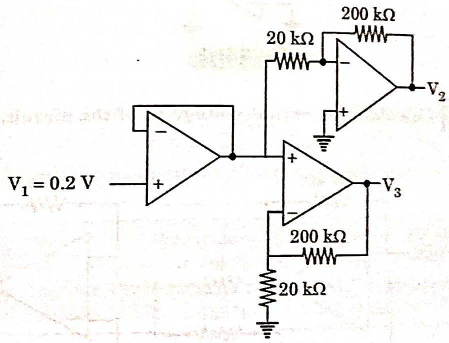


Fig. 3.9.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

1. Let V_A be the output of I[st] Op-Amp.
2. Thus, $V_A = 0.2$ V (∵ Unity gain follower)
3. $$V_2 = -\left(\frac{200\text{ k}\Omega}{20\text{ k}\Omega}\right)V_A = -10 \times 0.2 = -2 \text{ V}$$
4. $$V_3 = \left(1+\frac{200}{20}\right)V_A = 11 \times 0.2 = 2.2 \text{ V}$$

Que 3.10. Design and draw an inverting amplifier using Op-Amp with a gain of – 5 and R_i = 10 kΩ. **AKTU 2016-17(Sem-I), Marks 05**

Answer

Gain, $A_v = -5$

$R_i = 10\ \text{k}\Omega$

$\because \quad A_v = \dfrac{-R_f}{R_i} = -5$

$\therefore \quad R_f = 5 \times R_i = 5 \times 10 = 50\ \text{k}\Omega$

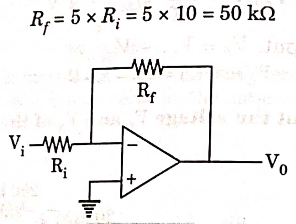


Fig. 3.10.1.

Que 3.11. **Calculate the output voltage V_0 of the circuit.**

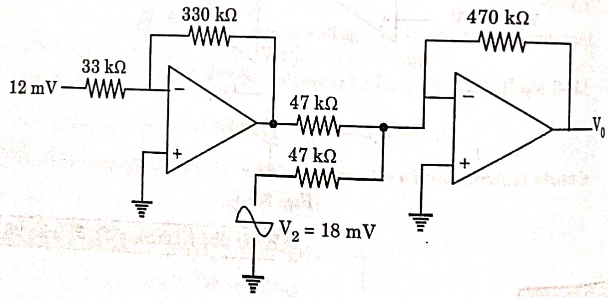


Fig. 3.11.1.

AKTU 2017-18(Sem-I), Marks 3.5

Answer

$$V_3 = -\left(\frac{R_2}{R_1}\right)V_1 = \frac{-330}{33} \times 12\ \text{mV} = -120\ \text{mV}$$

$$\text{Now } V_0 = -\left(\frac{R_5}{R_3}V_3 + \frac{R_5}{R_4}V_2\right)$$

$$= -\left[\frac{470}{47} \times (-120) + \frac{470}{47} \times 18\right]$$

$$= -[-1200 + 180] = 1020\ \text{mV}$$

$$V_0 = 1.02\ \text{V}$$

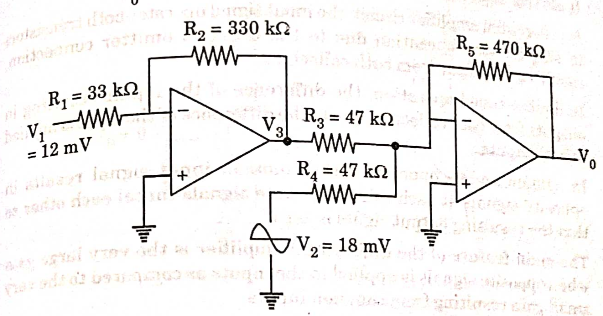


Fig. 3.11.2.

PART-3

Differential and Common-Mode Operation, Comparators.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 3.12. **Explain with the help of necessary diagram :**

a. **Inverting amplifier**

b. **Integrator**

c. **Differential amplifier in two modes of operation.**

AKTU 2015-16(Sem-I), Marks 10

OR

Analyse the differential amplifier with suitable circuit in two modes of operation.

Answer

A. **Inverting amplifier :** Refer Q. 3.3, Page 3–4J, Unit-3.

B. **Integrator :** Refer Q. 3.7, Page 3–8J, Unit-3.

C. Differential amplifier (in two modes of operation) :

1. The differential amplifier circuit has two separate inputs and two separate outputs and that the emitters are connected together.
2. It also consists of two separate voltage supplies.
3. In differential amplifier circuit, the input signal operates both transistors in single-ended operation due to the common emitter connection, resulting in output from both collectors.
4. In double-ended operation, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.
5. In common-mode operation, the common input signal results in opposite signals at each collector; these signals cancel each other so that the resulting output signal is zero.
6. The main feature of the differential amplifier is the very large gain when opposite signals is applied to the inputs as compared to the very small gain resulting from common inputs.
7. Let's consider DC bias operation of the differential amplifier circuit. With each base voltage at 0 V, the common emitter DC bias voltage is

$$V_E = 0\text{ V} - V_{BE} = -0.7\text{ V}$$

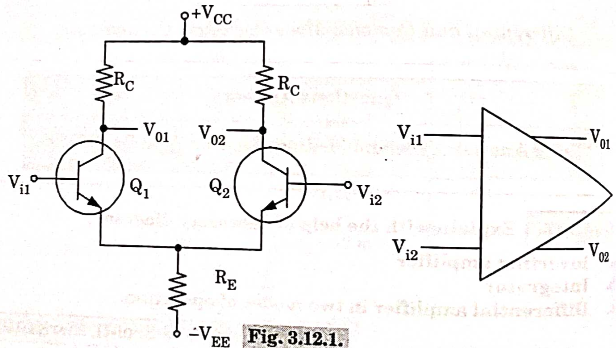


Fig. 3.12.1.

8. The emitter DC bias current is then,

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7\text{ V}}{R_E}$$

9. Assuming the transistors are well matched, we get

$$I_{C1} = I_{C2} = \frac{I_E}{2}$$

∴ Collector voltage,

$$V_{C1} = V_{C2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C$$

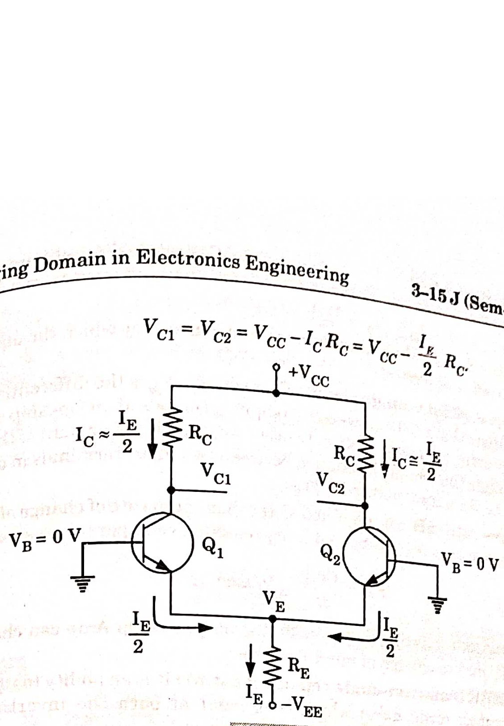


Fig. 3.12.2.

Que 3.13. Explain the basic parameters of Op-Amp.

OR

Explain the following characteristics of an Op-Amp :

i. CMRR

ii. Slew rate **AKTU 2017-18(Sem-I), Marks 3.5**

OR

Draw and explain the differential amplifier. Define CMRR and slew rate in Op-Amp. **AKTU 2016-17(Sem-II), Marks 5.25**

Answer

A. Differential amplifier : Refer Q. 3.12, Page 3–13J, Unit-3.

B. Basic parameters of Op-Amp :

1. **Input bias current :** The input bias currents I_{B1} and I_{B2} are the base bias currents of the two transistors in the input differential amplifier stage of the Op-Amp. An input bias current I_B is defined as the average of the two input bias currents I_{B1} and I_{B2} that is

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where, I_{B1} = DC bias current flowing into the inverting input,

I_{B2} = DC bias current flowing into the non-inverting input.

2. **Input offset current and voltage :**

i. **Input offset current :** The input offset current, I_{io} is defined as the algebraic difference between two input bias currents I_{B1} and I_{B2}

i.e., $I_{i0} = |I_{B1} - I_{B2}|$

The value of I_{io} indicates the maximum amount by which the input bias current may differ.

ii. **Input offset voltage :** Input offset voltage, V_{io} is the differential input voltage that exists between two input terminals of an Op-Amp without any external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero.

3. **Slew rate (SR) :** It is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per micro-second.

i.e.,
$$SR = \left.\frac{dv_o}{dt}\right|_{max} \text{ V/µsec}$$

Slew rate indicates how rapidly the output of Op-Amp can change in response to change in input frequency.

4. **CMRR (common-mode rejection ratio) :** It is an ability to reject the common mode noise which is present at both the inverting and non-inverting terminal.

$$CMRR = 20 \log \left|\frac{A_d}{A_{CM}}\right|$$

Que 3.14. **Determine the output voltage of an Op-Amp for input voltages of V_{i1} = 200 V and V_{i2} = 140 V. The amplifier has a differential gain of A_d = 6000 and the value of CMRR is :**

i. 200

ii. 10^5

AKTU 2015-16(Sem-I), Marks 05

Answer

Given : V_{i1} = 200 V, V_{i2} = 140 V, A_d = 6000

To Find : V_0.

i. For CMRR = 200 = A_d/A_{CM}

$$V_0 = A_d V_d + A_{CM} V_{CM} = A_d(V_{i_1} - V_{i_2}) + \frac{A_d}{CMRR}\left(\frac{V_{i_1} + V_{i_2}}{2}\right)$$

$$= 6000(200 - 140) + \frac{6000}{200}\left(\frac{200 + 140}{2}\right) = 365100 \text{ V}$$

$$= 36.51 \text{ kV}$$

ii. For CMRR = $10^5 = A_d/A_{CM}$

$$V_0 = A_d V_d + A_{CM} V_{CM}$$

$$= 6000(200 - 140) + \frac{6000}{10^5}\left(\frac{200 + 140}{2}\right) = 360010.2 \text{ V}$$

$$= 360 \text{ kV}$$

Que 3.15. **For an input of V_I = 50 mV in the circuit of Fig. 3.15.1, determine the maximum frequency that may be used. The Op-Amp slew rate SR = 0.4 V/s.**

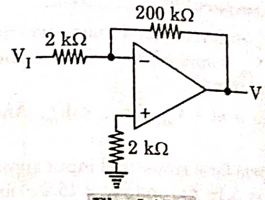


Fig. 3.15.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

Given : R_f = 200 kΩ, R_1 = 2 kΩ, V_I = 50 mV, SR = 0.4 V/s

To Find : f_{max}.

1. $$A_{CL} = \left|\frac{R_f}{R_1}\right| = \frac{200 \text{ k}\Omega}{2 \text{ k}\Omega} = 100$$

2. Output gain factor, $K = A_{CL} V_I = 100 \times 50 \times 10^{-3} = 5$ V

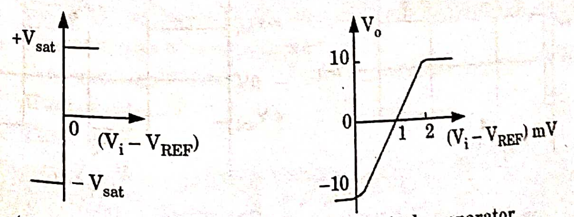
3. Maximum signal frequency = $\dfrac{SR}{2\pi K} = \dfrac{0.4}{2\pi(5)} = 0.012$ Hz

Que 3.16. **Write a short note on comparator and enlist its applications.**

Answer

A. **Comparator :**

1. A comparator is a circuit that is used for comparing a signal voltage applied at one input of Op-Amp with a known reference voltage at other input.



(*a*) Ideal comparator. (*b*) Practical comparator.

Fig. 3.16.1. The transfer characteristics.

2. It is basically an open-loop Op-Amp with output $\pm V_{sat} (= V_{CC})$ as shown in ideal transfer characteristics of Fig. 3.16.1(*a*).
3. There are basically two types of comparator :

i. Non-inverting comparator :

1. The circuit of Fig. 3.16.2(*a*) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (–ve) input and a time varying signal v_i is applied to (+ve) input.
2. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$. And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$.
3. The output waveform for a sinusoidal input signal applied to the (+ve) input is shown in Fig. 3.16.2(*b*) and Fig. 3.16.2(*c*) for positive and negative V_{ref} respectively.

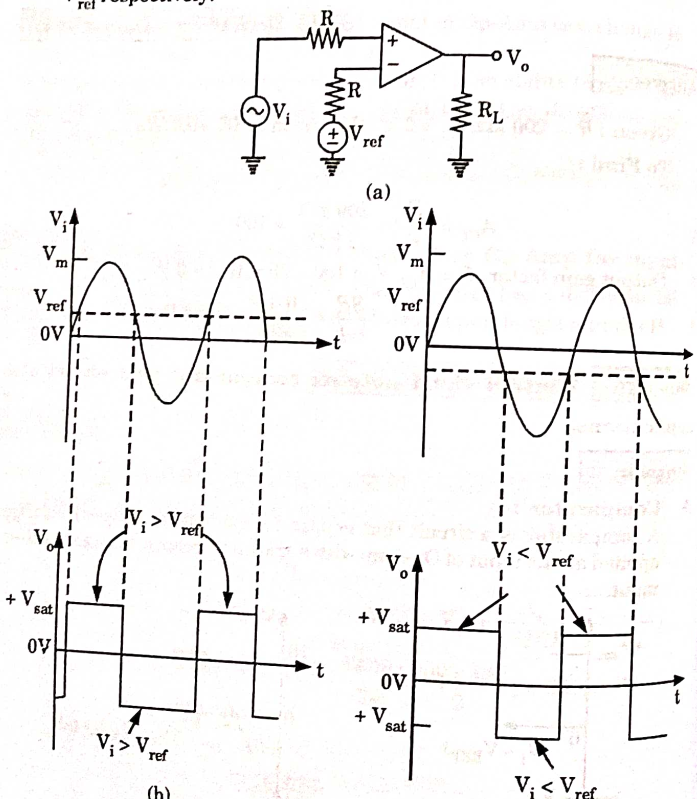


Fig. 3.16.2. (*a*) Non-inverting comparator. Input and output waveforms for (*b*) V_{ref} positive (*c*) V_{ref} negative.

ii. Inverting comparator :

In inverting comparator, fixed reference voltage V_{ref} is applied to (+ve) input and a time varying signal v_i is applied to (– ve) input.

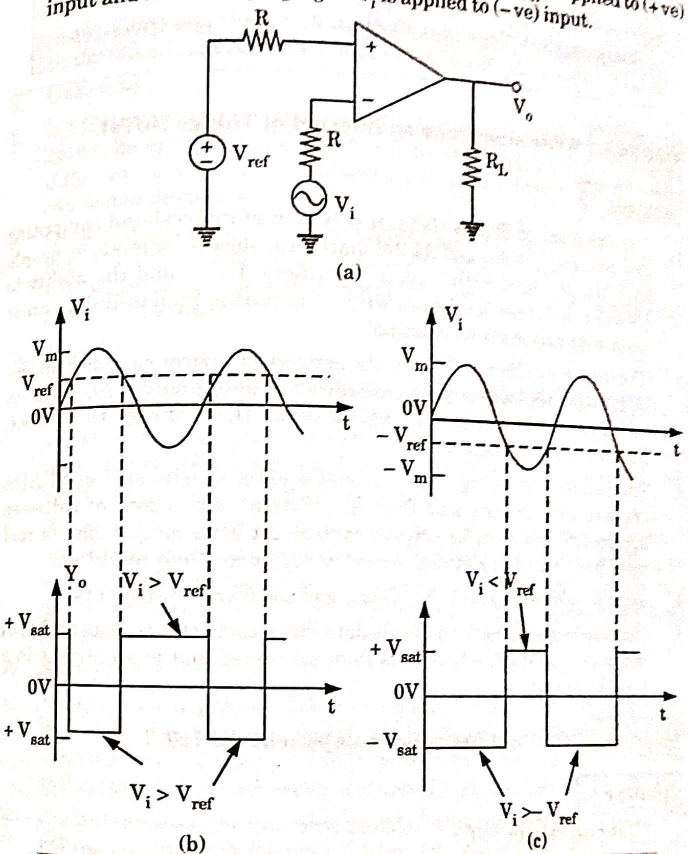


Fig. 3.16.3. (*a*) Inverting comparator. Input and output waveforms for (*b*) $V_{ref} > 0$ (*c*) $V_{ref} < 0$.

B. Applications of comparator :

i. Zero crossing detector
ii. Window detector
iii. Phase meter.

PART-4

Introduction of IoT System, Components of IoT System : Microprocessor and Microcontroller.

Que 3.19. **What is microcontroller and microprocessor ? Why microcontrollers are preferred for controlling operation ?**

Answer

A. Microcontroller :

1. A microcontroller contains a fixed amount of RAM, ROM, I/O ports and a timer all on a single chip.
2. The block diagram of microcontroller is shown in Fig. 3.19.1.

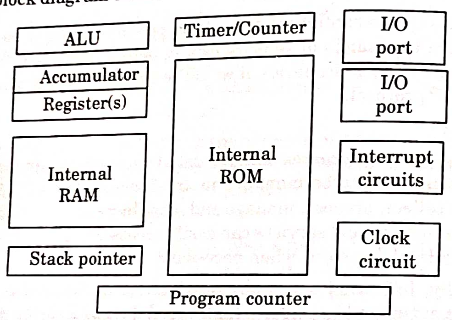


Fig. 3.19.1. Block diagram of a microcontroller.

3. Microcontrollers are intended to be special purpose digital computers.
4. Microcontroller is concerned with rapid movement of bits within the chip. It also consists of many bit-handling instructions.
5. Microcontrollers are normally less expensive than microprocessor.

B. Microprocessor :

1. Microprocessors contain no RAM, no ROM, and no I/O ports on the chip itself.
2. The block diagram of a microprocessor is shown in Fig. 3.19.2.

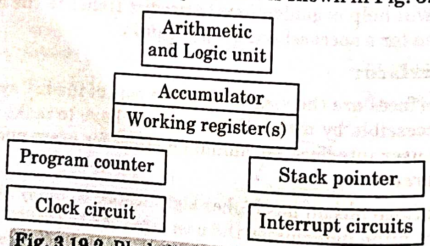


Fig. 3.19.2. Block diagram of a microprocessor.

3. Microprocessors are intended to be general purpose digital computers.

4. These processors are concerned with a rapid movement of the code and data from external addresses to the chip. It also has one or two types of bit-handling instructions.
5. Microprocessors are more expensive than microcontrollers because of addition of external RAM, ROM and I/O ports makes these system bulkier and more expensive.

C. Microcontrollers are preferred over microprocessors for controlling operations because :

i. They meet the computing needs of the task efficiently and cost effectively.
ii. Software development tools such as compilers, assemblers and debuggers are available for operations.
iii. Wide availability and reliable sources of the microcontroller.
iv. The power consumption of this device is also very low.

PART-5

Bluetooth Technology, WiFi Technology, Concept of Networking, Sensor Nodes, Concept of Cloud.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 3.20. **Explain in detail about the bluetooth and its application.**

Answer

1. Bluetooth was designed to be low powered, operate over a short range, and support both data and voice services.
2. Bluetooth enables peer-to-peer communications among all sorts of devices.
3. This system enables computing and communication devices to exchange information and work together for the benefit of the user.
4. Bluetooth and pervasive computing have much in common: Both aim to make computing and communications easier, more convenient, and more personal.
5. Both enable the use of a myriad of devices, especially small mobile devices, to accomplish these objectives. Thus, it appears evident that Bluetooth can be an excellent match with and a key element of pervasive computing.

6. Specifically, bluetooth has applications in at least three important pervasive computing domains: home networking, automobile network solutions, and mobile e-business.
7. The bluetooth standard aims to achieve interconnectivity between any bluetooth device regardless of brand or manufacturer. As a result, any bluetooth device anywhere in the world can connect to other similar devices within its range.
8. There are many other bluetooth usages, such as pervasive computing. Like wireless ethernet, bluetooth uses radio frequency-based data transmission.
9. The major difference between bluetooth and wireless ethernet is the concept of the piconet.
10. Bluetooth is based on the idea that devices that are within close range should establish a small network, allowing them to access each other's resources.
11. In contrast to wireless ethernet, which is based on more or less static IP (internet protocol) addresses, bluetooth enables a less restrictive, low-level communication; also, the usage of such as bluetooth enabled active tags referred to as BTnodes.
12. The main reason for using bluetooth as a communication standard for the active tags is that bluetooth modules are being integrated in an increasing number of consumer devices, such as mobile phones, PDAs, and digital cameras.

Bluetooth application :

1. Mobile e-business :
   i. pager
   ii. communicator
   iii. mobile phone.
2. Home networking :
   i. Fax
   ii. Bluetooth
   iii. Head phone.
3. Automobile network solution.

Que 3.21. **Give an overview of Wi-Fi network in IoT.**

Answer

1. The IEEE 802.11 standard extends the 802 network standards to the wireless medium by specifying the operation of wireless local area network (WLAN) communication within the ISM radio bands.
2. First version was published in 1997. The physical (PHY) and media access control (MAC) network layers are defined by 802.11.

3. The IEEE 802.11b/g standards use the 2.4 GHz frequency band, whereas 802.11a uses the 5 GHz band, and 802.11n uses a multiple input multiple output (MIMO) mechanism to utilize both the 2.4 GHz and 5 GHz bands.

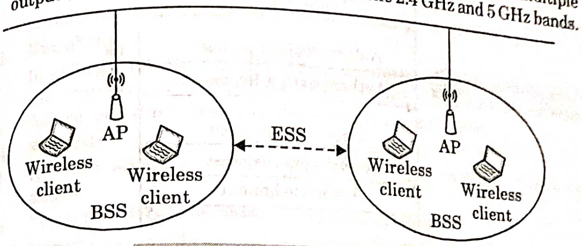


Fig. 3.21.1. Infrastructure WLAN.

4. The 802.11 wireless LAN standard operates in two modes, ad-hoc mode (peer-to-peer) or infrastructure mode (peer-to-AP).
5. In an infrastructure setup, wireless stations (STAs) connect to, or associate with an access point (AP).
6. This grouping of devices (STA(s) + AP) is called a basic service set (BSS) where each STA can connect to an outside network (the internet) via its associated AP.
7. A BSS uses a service set ID (SSID) to identify itself. Multiple APs can be connected via a wired distribution system (DS) where different BSSs are referred to as an extended service set (ESS).
8. In a scenario where BSSs use different SSIDs, a STA may change association however it must change its association to a different AP which causes a temporary loss of connection.
9. A basic service set ID (BSSID) is the media access control (MAC) address of an AP; this allows a STA to identify a unique BSS AP in an ESS. This research is carried out on an infrastructure WLAN within one BSS.
10. In order to associate with an AP, a STA must go through a three-phase setup process as illustrated in Fig. 3.21.2.
11. These phases are the scan, authentication, and association phases. On waking or power on, a STA must discover nearby APs by using a passive or an active scan.
12. A passive scan involves listening on each channel for broadcast beacons sent from APs. In an active scan, the STA 'actively' sends out a broadcast probe request frame one channel and then waits for a response from an AP on that channel.
13. After APs are discovered and one AP is selected, the STA starts the authentication process to authenticate itself with the AP.
14. The STA first sends out an authentication frame, to which the chosen AP responds with additional authentication frames.

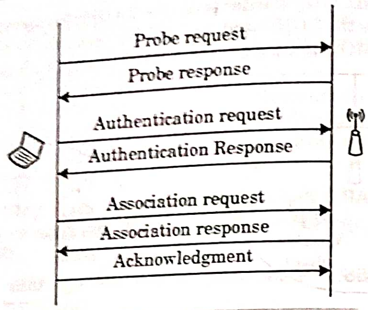


Fig. 3.21.2. Request-response process.

15. The authentication phase controls what nodes can access the AP. It is a network access control mechanism.
16. After successful authentication, the STA moves to associate with the AP by sending an association/re-association request frame to which the AP responds with an association/re-association response frame.
17. Finally, the STA sends an acknowledgement (ACK) frame to the AP. Once the AP receives this ACK frame, the STA is associated with the AP and a valid connection is established between the STA and the AP.
18. The infrastructure topology is sometime called an AP topology since the wireless network consists of at least an AP and a set of wireless devices.
19. In this topology, the system is divided into basic cells, where each cell is controlled by an AP. To extend the coverage area, multiple basic cells can be used.

Que 3.22. **What is network ? What are the criteria to be meet by a network ?**

Answer

A. **Network :**
1. A network is a set of devices (often referred to as nodes) connected by communication links.
2. A node can be a computer, printer, or any other device capable of sending and/or receiving data generated by other nodes on the network.

B. **Network criteria :**

A network must be able to meet a certain number of criteria. The most important of these are performance, reliability, and security.

i. **Performance :**
1. Performance can be measured in many ways, including transit time and response time.
2. Transit time is the amount of time required for a message to travel from one device to another.

3. Response time is the elapsed time between an inquiry and a response.
4. The performance of a network depends on a number of factors, including the number of users, the type of transmission medium, the capabilities of the connected hardware, and the efficiency of the software.

ii. **Reliability :**

In addition to accuracy of delivery, network reliability is measured by the frequency of failure, the time it takes a link to recover from a failure, and the network's robustness in a catastrophe.

iii. **Security :**
1. Network security issues include protecting data from unauthorized access.
2. Protecting data from damage and development.
3. Implementing policies and procedures for recovery from breaches and data losses.

Que 3.23. **Explain the components of sensor node.**

Answer

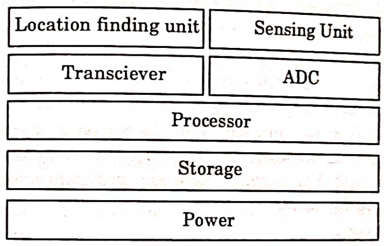


Fig. 3.23.1. Architecture of a sensor node.

Components of sensors node are :

1. **Location finding unit :**
a. Location finding unit contains a transceiver which transmits or receives data.
b. Sensor node often makes use of ISM band, which gives free radio, spectrum allocation and global availability. The possible choices of wireless transmission media are Radio Frequency (RF), optical communication (laser) and infrared.
c. Laser requires less energy, but need line-of-sight for communication and is sensitive to atmospheric conditions.

2. **Sensing unit :**
a. Sensors are used by wireless sensor nodes to capture data from their environment.
b. They are hardware devices that produce a measurable response to a change in a physical condition like temperature of pressure.

c. Sensors measure physical data of the parameter to be monitored and have specific characteristics such as accuracy, sensitivity etc.

3. **Transceiver :**

a. The functionality of both transmitter and receiver are combined into a single device known as a transceiver.

b. Transceivers often lack unique identifiers.

c. The operational states are transmit, receive, idle, and sleep. Current generation transceivers have built-in state machines that perform some operations automatically.

d. Most transceivers operating in idle mode have a power consumption almost equal to the power consumed in receive mode.

4. **Processor :**

a. The processor processes data and controls the functionality of other components in the sensor node.

b. While the most common processor is a microcontroller, other alternatives that can be used as a controller are a general purpose desktop microprocessor, digital signal processors etc.

c. A microcontroller is often used in many embedded system such as sensor node because of its low cost, flexibility to connect to other devices, ease of programming and low power consumption.

5. **Storage or External memory :**

a. Flash memories are used due to their cost and storage capacity. Memory requirements are very much application dependent.

b. Two categories of memory based on the purpose of storage are : user memory and program memory where user memory is used for storing application related or personal data and program memory is used for programming the device.

6. **Power source :**

a. A wireless sensor node is a popular solution when it is difficult or impossible to run a mains supply to the sensor node.

b. An important aspect in the development of a wireless sensor node is ensuring that there is always adequate energy available to power the system.

c. The sensor node consumes power for sensing, communicating and data processing.

d. Power is stored either in batteries or capacitors.

Que 3.24. **Explain briefly the term cloud.**

Answer

1. Cloud is an extension of the internet with some level of inherent discipline and ethics.

2. Cloud can be thought of unification of information technology with business intelligence.

3. Technology merges virtualization, grid functionalities and web standards as a single utility model which is delivered to the customers over the internet, whereas the business intelligence defines the best cost schemes leading to win-win situation for both the cloud service provider as well as the cloud service consumer.

4. Cloud brokers negotiate the best deals and relationships between the cloud consumers and cloud providers.

5. They can use specialized tools to identify the most appropriate cloud resource and map the requirements of the application to it.

6. Cloud broker services are mainly categorized into three groups :

a. Service intermediation broker provides a service to a consumer that enhances a given service by adding some value on top to increase some specific capability.

b. Service aggregation brokerage service combines and integrates into one or more services and ensures that data are modelled across all component services and movement, security of data between the service consumer and multiple providers.

c. Service arbitrage is similar to cloud service aggregation but services being aggregated are not fixed. In addition, these services provide flexibility and opportunity for the service aggregator.

Que 3.25. **What are the components of cloud ?**

Answer

Components of cloud :

1. **Cloud service consumer (or end user) :**

i. Cloud service consumers are the end users known as clients, which interact with the system and demand for services as per their requirement.

ii. The client can be categorized into the following three categories :

a. **Mobile clients :** Mobile clients run the application from laptops, PDAs and smart phones. This category of clients demands for higher speed and high level of security.

b. **Thin clients :** Thin clients neither have hard drives nor have DVD ROM drives, and largely depend on the server.

c. **Thick clients :** Thick clients are self-sufficient in terms of accessories.

2. **Cloud service provider :**

i. Cloud service providers are the agents which host the servers in the cloud and deliver service to the end users.

ii. The major cloud providers are Google, Amazon, Sales Force, IBM, Microsoft and Rackspace.

3. **Internet medium :** Internet medium is the communication channel between the consumer and provider where services are redirected.

4. **Datacentre :**

i. Datacentre is the collection of servers where the applications subscribed are housed.

ii. It consists of storage, network, and server.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Define Op-Amp with the help of block diagram. Also describe the equivalent circuit along with its ideal and practical characteristics.

Ans. Refer Q. 3.2.

Q. 2. Draw the circuit of an Op-Amp as voltage follower and find an expression for its voltage gain.

Ans. Refer Q. 3.3.

Q. 3. Calculate the output voltage for the circuit of Fig. 1 with inputs of V_1 = 40 mV rms and V_2 = 20 mV rms.

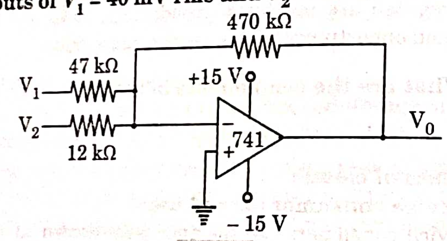


Fig. 1.

Ans. Refer Q. 3.5.

Q. 4. Explain integrator circuit using Op-Amp.

Ans. Refer Q. 3.7.

Q. 5. Design and draw an inverting amplifier using Op-Amp with a gain of – 5 and R_i = 10 kΩ.

Ans. Refer Q. 3.10.

Q. 6. Explain the basic parameters of Op-Amp.

Ans. Refer Q. 3.13.

Q. 7. What are the components of IoT ? Explain the basic parameters of Op-Amp.

Ans. Refer Q. 3.18.

Q. 8. What is network ? What are the criteria to be meet by a network ?

Ans. Refer Q. 3.22.

☺☺☺

4 UNIT

Digital Electronics and ICT

CONTENTS

PART-1

Digital Electronics : Number System and Representation, Introduction of Basic and Universal Gates.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 4.1. **Define number system and also define signed and unsigned binary number ?**

Answer

Number system : It is a language of digital systems consisting of a set of symbols called digits with rules defined for their addition, multiplication and other mathematical operations.

The classification of number system is as follows :

1. **Decimal number system :** It has 10 symbols, so the base or radix of this number system is 10. The 10 symbols are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.
2. **Binary number system :** It is a base 2 number system. The two binary digits are 1 and 0.
3. **Octal number system :** It has a base of 8, it has eight possible digits 0, 1, 2, 3, 4, 5, 6 and 7.
4. **Hexadecimal number system :** It is a base 16 number system. It has digits from 0 to 9, *A, B, C, D, E* and *F*.
5. **Complements :** These are used in digital computers to simplify the subtraction operation and for logical manipulation.
6. **Signed binary number :** Binary number that carry identification as to their polarity is called signed binary number. Plus (+) and minus (–) signs for positive and negative numbers can be represented in a digital format. The three major signed binary notations are : Sign magnitude notation, 1's complement notation and 2's complement notation.
7. **Unsigned binary number :** In these type of numbers we do not consider the (+) or (–) sign and concentrate only on the magnitude (absolute value) of numbers.

Que 4.2. **Convert the following :**

i. $(62.7)_8 = (\ )_{16} = (\ )_2$

ii. $(BC\ 6)_{16} = (\ )_{10} = (\ )_2$

Answer

i. $(62.7)_8 = (\ )_{16} = (\ )_2$

$$\begin{matrix} 110 & 010 & .111 \\ 6 & 2 & 7 \end{matrix} \rightarrow 0011\ 0010\ .1110 \Rightarrow (32.E)_{16}$$

$\therefore$ $(62.7)_8 = (32.E)_{16} = (00110010.1110)_2$

ii. $(BC6)_{16} = (\ )_{10} = (\ )_2$

$$(BC6)_{16} = 11 \times 16^2 + 12 \times 16^1 + 6 \times 16^0 = (3014)_{10}$$

$$(3014)_{10} = (101111000110)_2$$

Que 4.3. **The solution to the quadratic equation $x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$. What is the base of the number system used ?**

Answer

1. Suppose the base of the number is b. The given quadratic equation is
$$(x^2 - 11x + 22)_b = 0 \quad ...(4.3.1)$$
2. The solution of quadratic equation is,
$$x = 3 \text{ and } x = 6$$
3. The quadratic equation formed with these roots is
$$(x - 3)(x - 6) = x^2 - (6 + 3)x + (6 \times 3) \quad ...(4.3.2)$$
4. Comparing eq. (4.3.2) with the given quadratic eq. (4.3.1)
$$(9)_{10} = (11)_b$$
$$b^1 \times 1 + b^0 \times 1 = 9$$
$$b + 1 = 9, \quad b = 8$$
also,
$$(18)_{10} = (22)_b$$
$$b^1 \times 2 + b^0 \times 2 = 18$$
$$2(b + 1) = 18, \quad b = 8$$

Hence, the base of the number system is 8.

Que 4.4. **What are the logic gates ? Explain each of them.**

Answer

There are three logic gates :

i. **AND gate :**

1. An AND gate will produce a HIGH output when all inputs are HIGH, otherwise the output of AND gate is LOW. Fig. 4.4.1 shows the symbol of AND gate.

Fig. 4.4.1.

2. Table 4.4.1 gives truth table for the two input AND gate. The inputs of AND gate is *A* and *B*, the output of gate is *Y*.

Table 4.4.1.

Input		Output
A	*B*	*Y* = *A* . *B*
0	0	0
0	1	0
1	0	0
1	1	1

ii. **OR gate :**

1. An OR gate produces a HIGH output when any one of the inputs is HIGH. It produces a LOW output when all the inputs are LOW. Fig 4.4.2 shows the logic symbol of 2 input OR gate.

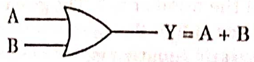


Fig. 4.4.2.

2. Table 4.4.2 gives the truth table for the two input OR gate. The input and output variables are represented in the binary form.

Table 4.4.2.

Input		Output
A	*B*	*Y* = *A* + *B*
0	0	0
0	1	1
1	0	1
1	1	1

iii. **NOT gate :**

1. The NOT gate is also called as an inverter. The output of NOT gate is also called as inverse input or complement of input.
2. Fig. 4.4.3 shows the logic symbol of NOT gate and Table 4.4.3 shows the truth table of NOT gate.
3. The NOT gate produces HIGH output when the input is LOW and the NOT gate output is LOW when the input is HIGH.

Fig. 4.4.3.

Table 4.4.3.

Input	Output
A	$Y = \overline{A}$
0	1
1	0

Que 4.5. **Explain universal gates.**

Answer

NAND and NOR gates are universal gates.

i. **NAND gate :**

1. NAND gate is a combination of AND gate followed by NOT gate. The output of NAND gate is inverse of AND gate output.
2. Fig. 4.5.1 shows the logic symbol of a NAND gate. Table 4.5.1, shows the truth table of NAND gate. NAND gate produce HIGH output when any one of the input in LOW.

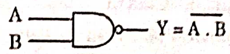


Fig. 4.5.1.

Table 4.5.1.

Input		Output
A	*B*	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

ii. **NOR gate :**

1. NOR gate is combination of OR gate followed by NOT gate, so the output of NOR gate is inverse of OR gate output.
2. Fig. 4.5.2 shows the logic symbol of NOR gate and table 4.5.2, shows the truth table of NOR gate. The NOR gate gives a LOW output when any one of the input is HIGH otherwise the output is HIGH.

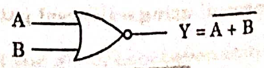


Fig. 4.5.2.

Table 4.5.2.

Input		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

PART-2

Using Boolean Algebra Simplification of Boolean Function, K-Map Minimization Upto 6 Variable.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 4.6. **State De Morgan's theorem.**

Answer

First De Morgan theorem : It states, complement of two or more variables and then AND operation on these is equivalent to NOR operation on these variables. (NOR means complement of two or more variables OR).

$$\overline{A_1 + A_2} = \overline{A_1} \,.\, \overline{A_2}$$

Second De Morgan theorem : It states that complement of two or more variables and then OR operation on these is equivalent to a NAND operation on these variables (NAND means complement of two or more variables AND).

$$\overline{A_1 A_2 A_3} = \overline{A_1} + \overline{A_2} + \overline{A_3} \ldots$$

Que 4.7. **Simplify the following expression as much as possible:**

$$F(w, x, y, z) = \bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}xy\bar{z} + wy\bar{z}$$

and implement your result using universal gates only.

Answer

$$F(w, x, y, z) = \bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}\, xy\bar{z} + wy\bar{z}$$

$$= \bar{y}\bar{z} + wy\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}xy\bar{z}$$

$$= \bar{z}\,(\bar{y} + wy) + \overline{wz}\,(\bar{x} + xy)$$

$$= \bar{z}\,(\bar{y} + w) + \overline{wz}\,(\bar{x} + y) \qquad [\because \bar{A} + AB = \bar{A} + \bar{B}]$$

$$= \bar{y}\bar{z} + w\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}y\bar{z}$$

$$= \bar{y}\bar{z} + \bar{w}y\bar{z} + w\bar{z} + \bar{w}\bar{x}\bar{z}$$

$$= \bar{z}\,(\bar{y} + \bar{w}y) + \bar{z}\,(w + \overline{wx})$$

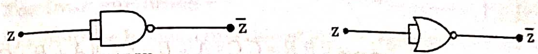
$$= \bar{z}\,(\bar{y} + \bar{w}) + \bar{z}\,(w + \bar{x})$$

$$= \bar{z}\,(\bar{y} + \bar{w} + w + \bar{x})$$

$$= \bar{z}\,(\bar{y} + 1 + \bar{x}) \qquad [\because 1 + A = 1]$$

$$= \bar{z}\,(\bar{y} + 1) \qquad [\because 1 + \bar{A} = 1]$$

$$= \bar{z}$$



Using NAND gate (*a*) Using NOR gate (*b*)

Fig. 4.7.1.

Que 4.8. **Simplify the following boolean expression to a minimum number of literals.**

i. $\bar{A}\bar{C} + ABC + A\bar{C} + A\bar{B}$

ii. $(\bar{x}\,\bar{y} + z) + z + xy + wz$

Answer

i. $\bar{A}\bar{C} + ABC + A\bar{C} + A\bar{B}$:

Let

$$Y = \bar{A}\bar{C} + A\bar{C} + A\bar{B} + ABC$$

$$= \bar{C}\,(\bar{A} + A) + A\,(\bar{B} + BC)$$

$$= \bar{C} + A(\bar{B} + C) \qquad [\because A + \bar{A} = 1]$$

$$= \bar{C} + AC + A\bar{B} \qquad [\because \bar{C} + AC = (\bar{C} + A)(\bar{C} + C)]$$

$$= \bar{C} + A + A\bar{B}$$

$$= \bar{C} + A(1 + \bar{B})$$

$$= A + \bar{C}$$

ii. $(\bar{x}\,\bar{y} + z) + z + xy + wz$

Let

$$Y = (\bar{x}\,\bar{y} + z) + z + xy + wz$$

$$= \bar{x}\,\bar{y} + z + xy + wz$$

$$= \bar{x}\,\bar{y} + xy + z\,(1 + w)$$

$$= \bar{x}\,\bar{y} + xy + z = x \odot y + z \qquad [\because 1 + w = 1]$$

Que 4.9. **Convert the given expression into canonical SOP form**

$$Y = A + AB + BC$$

Answer

$$Y = A(B + \overline{B})(C + \overline{C}) + AB(C + \overline{C}) + BC(A + \overline{A})$$

$$Y = (AB + A\overline{B})(C + \overline{C}) + ABC + AB\overline{C} + ABC + \overline{A}BC$$

$$= ABC + AB\overline{C} + A\overline{B}C + A\overline{B}\,\overline{C} + ABC + AB\overline{C} + ABC + \overline{A}BC$$

$$= ABC + AB\overline{C} + A\overline{B}C + A\overline{B}\,\overline{C} + \overline{A}BC$$

$[\because A + A = A]$

Que 4.10. **Convert the given expression into canonical POS form**

$$Y = A(A + \overline{B})(A + B + \overline{C})$$

Answer

$$Y = (A + B\overline{B} + C\overline{C})(A + \overline{B} + C\overline{C})(A + B + \overline{C})$$

$$= (A + B\overline{B} + C)(A + B\overline{B} + \overline{C})(A + \overline{B} + C)(A + \overline{B} + \overline{C})\ (A + B + \overline{C})$$

$$= (A + B + C)(A + \overline{B} + C)(A + B + \overline{C})(A + \overline{B} + \overline{C})$$

$$(A + \overline{B} + C)(A + \overline{B} + \overline{C})(A + B + \overline{C})$$

$$Y = (A + B + C)(A + \overline{B} + C)(A + B + \overline{C})(A + \overline{B} + \overline{C})$$

Que 4.11. **Write a short note on Karnaugh map. Also show the reduction of boolean expression and how to mark pairs. How gate-level minimization is implemented ?**

Answer

1. Karnaugh map is another way of presenting the information given by a truth table. These maps are also known by the name *K*-map. Let us consider the map for two variables. There may be four possible combinations within four squares.
2. Each square represents unique minterms as shown in Fig. 4.11.1 :

A \ B	$\overline{B}$	B
$\overline{A}$	$\overline{A}\,\overline{B}$ (0)	$\overline{A}B$ (1)
A	$A\overline{B}$ (2)	AB (3)

OR

A \ B	0	1
0	00 (0)	01 (1)
1	10 (2)	11 (3)

Fig. 4.11.1.

For three variables :

1. There are eight minterms for three binary variables. Hence the *K*-map consists of eight squares.

2. The *K*-map drawn in Fig. 4.11.2, for three variables is marked with numbers in each row and each column to show the relationship between the squares and the three variables.

A \ BC	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	m_0	m_1	m_3	m_2
A	m_4	m_5	m_7	m_6

OR

A \ BC	00	01	11	10
0	000 (0)	001 (1)	011 (3)	010 (2)
1	100 (4)	101 (5)	111 (7)	110 (6)

Fig. 4.11.2.

3. For example, the square assigned to m_5, which corresponds to row 1 and column 01. When these two numbers reconsidered, they give the binary number 101, whose decimal equivalent is 5.

For four variables :

1. The map for boolean function of four binary variables require sixteen minterms, hence the map consists of sixteen squares.
2. The listed terms are from 0 to 15, *i.e.*, 16 minterms. The map shows the relationship with the four variables.
3. In every square the numbers are written. The number denotes that this square corresponds to that number's minterm.

AB \ CD	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	m_0	m_1	m_3	m_2
$\overline{A}B$	m_4	m_5	m_7	m_6
AB	m_{12}	m_{13}	m_{15}	m_{14}
$A\overline{B}$	m_8	m_9	m_{11}	m_{10}

OR

AB \ CD	00	01	11	10
00	0000 (0)	0001 (1)	0011 (3)	0010 (2)
01	0100 (4)	0101 (5)	0111 (7)	0110 (6)
11	1100 (12)	1101 (13)	1111 (15)	1110 (14)
10	1000 (8)	1001 (9)	1011 (11)	1010 (10)

Fig. 4.11.3.

Que 4.12. **Simplify the boolean function.**

$$F(w, x, y, z) = \Sigma m(1, 3, 7, 11, 15)$$

which has the don't care conditions

$$d(w, x, y, z) = \Sigma d(0, 2, 5)$$

Answer

1. Given, $F(w, x, y, z) = \Sigma m(1, 3, 7, 11, 15)$ and don't care conditions

$$d(w, x, y, z) = \Sigma d(0, 2, 5)$$

2. The minterms of F are the variable combinations that make the function equal to 1. The minterms of d are the don't care minterms that may be either 0 or 1.
3. The K-map simplification is shown in Fig. 4.12.1.

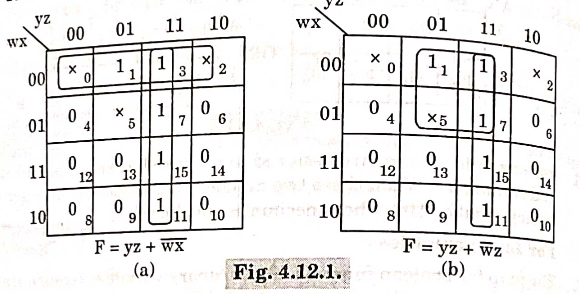


Fig. 4.12.1.

4. The minterms of F are marked by 1's, those of d are marked by $\times$'s and the remaining is filled with 0's.
5. To get the simplified expression in SOP form, we must include all five 1's in the map, but we may or may not include any of the $\times$'s, depending on the way the function is simplified.
6. In Fig. 4.12.1(a), don't care minterms 0 and 2 are included with the 1's, resulting as

$$F = yz + \bar{w}\bar{x}$$

7. In Fig. 4.12.1(b), don't care minterm 5 is included with the 1's, resulting as

$$F = yz + \bar{w}z$$

8. The K-map in Fig. 4.12.1(b) is more feasible because, we have to use the minimum don't care.

Que 4.13. **Simplify the following expression into product of sum (POS) form**

i. $AB\bar{C} + A\bar{B}D + BCD$

ii. $AC\bar{D} + \bar{C}D + A\bar{B} + ABCD$

Answer

i. $AB\bar{C} + A\bar{B}D + BCD$

1. Let

$$Y = AB\bar{C} + A\bar{B}D + BCD$$
$$= AB\bar{C}(D + \bar{D}) + A\bar{B}(C + \bar{C})D + (A + \bar{A})BCD$$
$$= AB\bar{C}D + AB\bar{C}\bar{D} + A\bar{B}CD + A\bar{B}\bar{C}D + ABCD + \bar{A}BCD$$
$$Y = \Sigma m(7, 9, 11, 12, 13, 15)$$

2. Now for POS form we will take complement function,

$$\bar{Y} = \Pi M(0, 1, 2, 3, 4, 5, 6, 8, 10, 14)$$

3. Minimization through K-map is shown in Fig. 4.13.1.

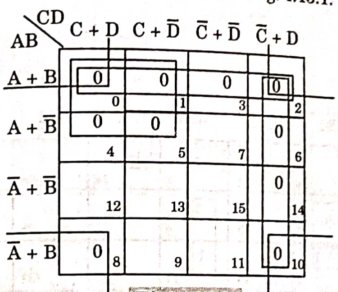


Fig. 4.13.1.

$$\therefore \bar{Y} = (A + B)(A + C)(\bar{C} + D)(B + D)$$

ii. $AC\bar{D} + \bar{C}D + A\bar{B} + ABCD$

1. Let, $Y = AC\bar{D} + \bar{C}D + A\bar{B} + ABCD$

$$= A(B+\bar{B})C\bar{D} + (A+\bar{A})(B+\bar{B})\bar{C}D + A\bar{B}(C+\bar{C})(D+\bar{D}) + ABCD$$
$$= A(B+\bar{B})C\bar{D} + (A+\bar{A})(B+\bar{B})\bar{C}D + A\bar{B}(C+\bar{C})(D+\bar{D}) + ABCD$$
$$= ABC\bar{D} + A\bar{B}C\bar{D} + AB\bar{C}D + A\bar{B}\bar{C}D + \bar{A}B\bar{C}D + \bar{A}\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}\bar{C}\bar{D} + ABCD$$
$$Y = \Sigma m(1, 5, 8, 9, 10, 11, 13, 14, 15)$$

2. Now for POS form, we have to take complement function,

$$\bar{Y} = \Pi M(0, 2, 3, 4, 6, 7, 12)$$

3. Minimization through K-map is shown in Fig. 4.13.2.

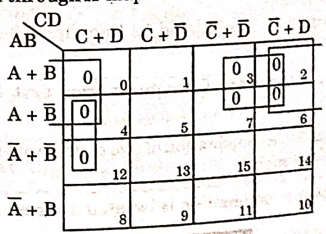


Fig. 4.13.2.

$$\bar{Y} = (A + D)(A + \bar{C})(\bar{B} + C + D)$$

Que 4.14. Simplify the following Boolean function using K-map
$Y = \Sigma m(0, 1, 3, 5, 6, 7, 9, 11, 16, 18, 19, 20, 21, 22, 24, 26)$

Answer

K-map :

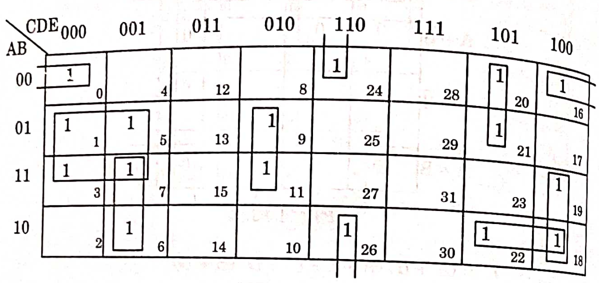


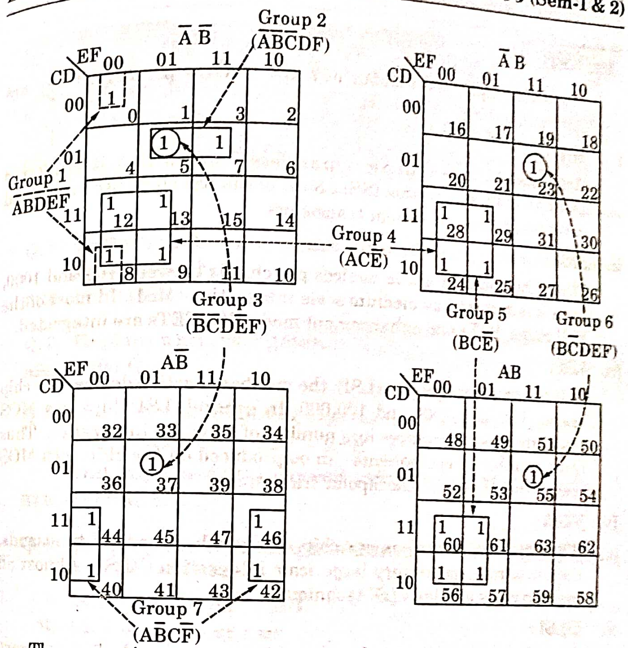
Fig. 4.14.1.

$$Y = \bar{D}\bar{E}\bar{A}\bar{B} + \bar{C}\bar{D}B + \bar{A}\bar{C}\bar{D}E + C\bar{D}A\bar{B} + \bar{C}D\bar{E}B + CD\bar{E}\bar{B} + C\bar{D}E\bar{A} + C\bar{D}\bar{E}A$$
$$= \bar{D}\bar{B}(\bar{E}\bar{A} + CA) + \bar{C}B(\bar{D} + D\bar{E}) + \bar{D}E(A\bar{C} + \bar{A}C) + C\bar{E}(D\bar{B} + \bar{D}A)$$
$$= \bar{D}\bar{B}(\bar{E}\bar{A} + CA) + \bar{C}B(\bar{D} + \bar{E}) + \bar{D}E(A \oplus C) + C\bar{E}(D\bar{B} + \bar{D}A)$$

Que 4.15. Simplify the Boolean function
$F(A, B, C, D, E, F) = \Sigma m(0, 5, 7, 8, 9, 12, 13, 23, 24, 25, 28, 29, 37, 40, 42, 44, 46, 55, 56, 57, 60, 61)$

Answer

1. Group 1 and group 2 are two pairs of 1's in the first 16-cell map.
2. Group 3 is formed by two isolated 1's from first 16-cell map and third 16-cell map.
3. Group 4 is a combination of two quads from first 16-cell and second 16-cell map.
4. Similarly group 5 is a combination of two quads from second 16-cell map and fourth 16-cell map.
5. Group 6 is again a combination is isolated 1's from second and fourth 16-cell maps.
6. Finally group 7 is a quad within the third 16-cell map.



The expression is,

$$F = \bar{A}\bar{B}\bar{D}\bar{E}\bar{F} + \bar{A}\bar{B}\bar{C}DF + \bar{B}\bar{C}D\bar{E}\bar{F} + \bar{A}C\bar{E} + BC\bar{E} + B\bar{C}DEF + A\bar{B}C\bar{F}$$

PART-3

Introduction to IC Technology : SSI, MSI, LSI, VLSI Integrated Circuits.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 4.16. Define the term : SSI, MSI, LSI and VLSI.

Answer

Depending upon the number of active devices per chip, there are different levels of integration :

i. **SSI :**

When the active devices per chip are less than 100, then it is referred as small scale integration (SSI). Most of the SSI chips use integrated resistors, diodes and bipolar transistors.

ii. **MSI :**

When the count of active devices per chip is between 100 and 1000, then it is referred as medium scale integration (MSI). In most of the MSI chips, BJTs and enhancement mode MOSFETs are integrated.

iii. **LSI :**

In large scale integration (LSI), the number of active devices per chip ranges between 1000 and 100,000. In general, LSI chips use MOS transistors; as it requires less number of steps for integration. Thus more number of components can be produced on the chip with MOS transistors than with the bipolar transistors.

iv. **VLSI :**

When the active devices per chip are over hundreds of thousands, then it is referred as very large scale integration (VLSI). Almost all modern chips employ VLSI technique.

v. **ULSI :**

Recently a new level of integration has been introduced which is known as ultra large scale integration (ULSI). In ULSI technique, more than one million active devices are integrated on a single chip. Pentium microprocessors use ULSI technology.

Table 4.16.1.

S. No.	Level of integration	Number of active devices per chip
1.	Small scale integration (SSI)	less than 100
2.	Medium scale integration (MSI)	100 - 10000
3.	Large scale integration (LSI)	1000 - 100000
4.	Very large scale integration (VLSI)	Over 100000
5.	Ultra large scale integration (ULSI)	Over 1 million

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Define number system and also define signed and unsigned binary number ?

Ans. Refer Q. 4.1.

Q. 2. Explain universal gates.

Ans. Refer Q. 4.5.

Q. 3. Simplify the following expression as much as possible :

$$F(w, x, y, z) = \bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}xy\bar{z} + wy\bar{z}$$

and implement your result using universal gates only.

Ans. Refer Q. 4.7.

Q. 4. Simplify the following boolean expression to a minimum number of literals.

i. $\bar{A}\bar{C} + ABC + A\bar{C} + A\bar{B}$

ii. $(\bar{x}\,\bar{y} + z) + z + xy + wz$

Ans. Refer Q. 4.8.

Q. 5. Simplify the boolean function.

$$F(w, x, y, z) = \Sigma m(1, 3, 7, 11, 15)$$

which has the don't care conditions

$$d(w, x, y, z) = \Sigma d(0, 2, 5)$$

Ans. Refer Q. 4.12.

☺☺☺

5 UNIT

Fundamentals of Communication Engineering

CONTENTS

PART-1

Fundamentals of Communication Engineering : Basics of Signal Representation and Analysis.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.1. **What do you understand by signal ? Define various types of signals with suitable examples.**

Answer

A. **Signal :** A signal is defined as a physical quantity that varies with time, space or any other independent variable. The representation of a signal by mathematical expression is known as signal modeling.

B. **Types of signals :**

i. **Deterministic and Random Signals :**

1. Deterministic signals can be completely specified in time.
2. The pattern of this signal is regular and can be characterized mathematically. So, its future value at any instant can be determined easily. For example, $y(t) = b\sin(\pi t)$, $y(t) = ax(t)$.
3. Random signals take random values at any given time.
4. The pattern of this signal is irregular and it cannot be defined mathematically.
5. So, future value of the signals at any instant cannot be predicted. For example : Noise.

ii. **Even and Odd Signals :**

A signal $x(t)$ or $x[n]$ is referred to as symmetric or even signal if,

$$x(-t) = x(t) \text{ or } x[-n] = x[n]$$

and referred to as non-symmetric or odd signal if

$$x(-t) = -x(t) \text{ or } x[-n] = -x[n]$$

iii. **Energy and Power Signals :**

a. **Power signal :** A power signal is defined as a signal having finite average power and infinite energy *i.e.*, $0 < P < \infty$ and $E = \infty$.

b. **Energy signal :** The energy signal is one that has a finite energy and zero average power *i.e.*, $0 < E < \infty$ and $P = 0$.

Que 5.2. Sketch and explain the basic signals used as building blocks for the modeling of more complex signals.

Answer

Building blocks :

1. **Unit Step Function :**
If a step function has unity magnitude then it is called unit step function

$$u(t) = 1 \text{ for } t \geq 0$$
$$= 0 \text{ for } t < 0$$

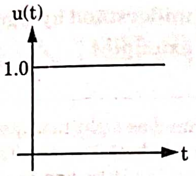


Fig. 5.2.1.

2. **Unit Ramp Function :**
It is defined as

$$r(t) = t \text{ for } t \geq 0$$
$$= 0 \text{ for } t < 0$$

or $r(t) = t\,u(t)$

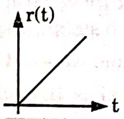


Fig. 5.2.2.

3. **Unit Parabolic Function :**
It is given by

$$p(t) = \frac{t^2}{2} \text{ for } t \geq 0$$
$$= 0 \text{ for } t < 0$$

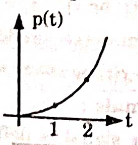


Fig. 5.2.3.

4. **Impulse Function :**
It is defined as

$$\int_{-\infty}^{\infty} \delta(t)\,dt = 1$$

and $\delta(t) = 0$ for $t \neq 0$

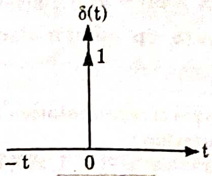


Fig. 5.2.4.

5. **Rectangular Pulse Function :**
It is defined as

$$\pi(t) = 1 \text{ for } |t| < 1/2$$
$$= 0 \text{ otherwise}$$

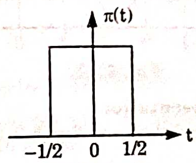


Fig. 5.2.5.

6. **Triangular Pulse Function :**
It is defined as

$$\Delta_a(t) = \begin{cases} 1 - \frac{|t|}{a}, & |t| \leq a \\ 0, & |t| > a \end{cases}$$

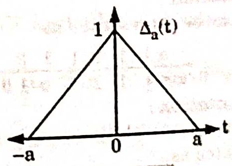


Fig. 5.2.6.

7. **Signum Function :**
It is defined as

$$\text{sgn}(t) = \begin{cases} 1 & t > 0 \\ -1 & t < 0 \end{cases}$$

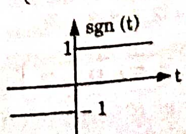


Fig. 5.2.7.

Que 5.3. **How can we represent a signal with different ways ? Show at least four ways to represent a discrete time signal.**

Answer

There are different types of representation for discrete time signals.

i. **Graphical representation :**
Let a signal $x[n]$ with values $x[-1] = 1$, $x[0] = 2$, $x[1] = 2$, $x[2] = 0$ and $x[3] = 1.5$, it can be shown as

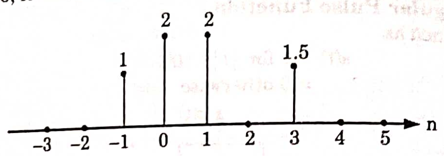


Fig. 5.3.1.

ii. **Fundamental representation :**
The discrete time signal shown in Fig. 5.3.1 can be represented using functional form as.

$$x[n] = \begin{cases} 1 & \text{for} \quad n = -1 \\ 2 & \text{for} \quad n = 0,1 \\ 0 & \text{for} \quad n = 2 \\ 1.5 & \text{for} \quad n = 3 \\ 0 & \quad \text{otherwise} \end{cases}$$

iii. **Tabular representation :**
In tabular term, it can be represented as

n	–1	0	1	2	3
x(n)	1	2	2	0	1.5

iv. **Sequence representation :**

1. A finite duration sequence with time origin ($n = 0$) indicated by the symbol ↑ is represented as,
$$x[n] = \{1, \underset{\uparrow}{2}, 2, 0, 1.5\}$$
2. A finite duration sequence can be represented as,
$$x[n] = \{... \ 0.2, 1, -1, 3, 2, ...\}$$
3. A finite duration sequence that satisfies the condition $x[n] = 0$, for $n < 0$ can be represented as,
$$x[n] = \{2, 4, 6, 8, -3\}$$

PART-2

Electromagnetic Spectrum, Elements of a Communication System, Need of Modulation and Typical Application.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.4. **Explain the applications of electromagnetic spectrum. Also classify it further for Radio and Optical spectrum respectively.**

Answer

Electromagnetic spectrum is the orderly distribution of electromagnetic radiations in accordance with their wavelength or frequency. It is classified as :

i. **Radio waves :**

1. These were discovered by Hertz in 1887.
2. The electromagnetic waves with the lowest frequencies and longest wavelengths are Radio waves.
3. Their frequencies may be as low as 10 Hz and their wavelengths can go upto millions of meters long.
4. Therefore, radio waves can be of extremely high frequency (EHF), super high frequency (SHF), ultra high frequency (UHF), very high frequency (VHF), high frequency (HF), medium frequency (MF), low frequency (LF), very low frequency (VLF), extremely low frequency (ELF).
5. Surface wave EHF and SHF are used for radar and space communication.
6. UHF and VHF are used in TV transmission and line of sight communication.
7. Sky wave HF and ground wave MF have applications in radio communication.
8. Surface wave LF and VLF are also used in radio navigation and ELF has application in sub-surface communication.

ii. **Microwaves :**

1. Radio waves with wavelengths ranging from a few tenths to about one thousandth of a meter are known as Microwaves.
2. These are produced by specially designed oscillators.
3. This is also for radar and TV communications.

iii. **Infrared (IR) :**

1. Infrared frequencies are intermediate between those of microwaves and red visible light.
2. We sense infrared light as heat.

3. Infrared radiation can affect photographic plate coated with special chemicals.

iv. Visible light waves :

1. The next band of frequencies in the electromagnetic spectrum is visible light.
2. Visible light occupies only a small part of this spectrum and it produces the sensation of vision.
3. White light is composed of a mixture of many different wavelengths each of which can be seen on its own by the human eye as a colour.
4. It consists of different colours, they are violet, blue, green, yellow, orange, red.
5. When ordinary white light is passed through a prism, it is separated into the rainbow of colours known as visible spectrum.

v. Ultraviolet light (UV) :

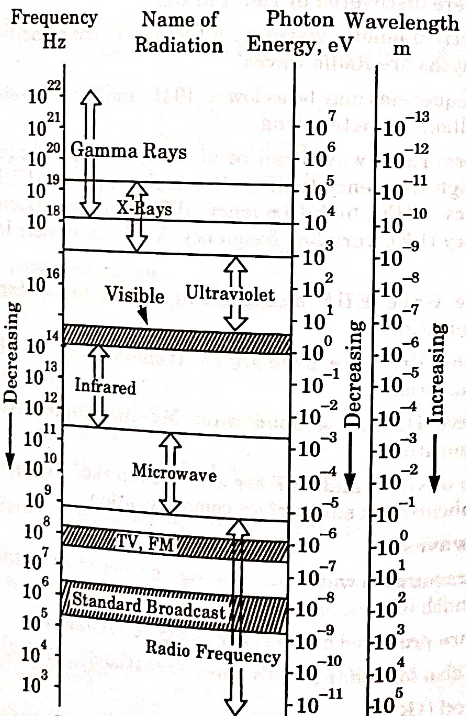


Fig. 5.4.1. Electromagnetic spectrum.

1. Just above visible light in the electromagnetic spectrum is ultraviolet light (UV).

2. This invisible light can be detected by photographic plate.
3. Ultraviolet radiation is very useful in medical science as it is producing chemical effect on our body.

vi. X-rays :

1. Frequencies higher than UV are X-ray.
2. This radiation was discovered by Rontgen in 1895.
3. These rays find several applications in medical science and industry.

vii. Gamma ray (γ) :

1. Frequencies higher than X-rays are Gamma rays.
2. These rays can affect photographic plates and cause ionization.
3. The sources of gamma rays are nuclear transitions involving decays.
4. X-rays are produced through electronic transitions deep in the electronic structure of the atom.
5. Also ultraviolet (UV) waves, visible radiation and infrared (IR) radiation result from electronic transitions of different energy ranges.
6. Microwaves and radio waves are produced by various types of electronic oscillations.

Que 5.5. **Explain with the help of block diagram the elements of communication systems.**

Answer

1. A modern communication system is first concerned with the processing and storing of information before its transmission.
2. The basic communication system consists of transmitter, channel and receiver. The input and output of communication system comes from information source and destination respectively.

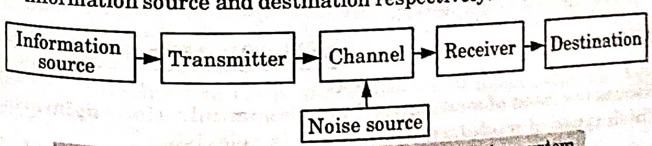


Fig. 5.5.1. Block diagram of basic communication system.

i. Information source :

1. The communication system exists to convey a message. This message comes from the information source.
2. Information may be words, groups of words, code symbols or any prearranged units.
3. The amount of information contained in any given message can be measured in bits or dits.

$$\text{Information} = \log_2\left(\frac{1}{P_i}\right) \text{ bits}$$

$$= \log_{10}\left(\frac{1}{P_i}\right) \text{ dits}$$

where P_i is the probability of occurrence. It must be realized that no real information is conveyed by a redundant message.

ii. **Transmitter :** In transmitter the message from information source is superimposed on some high frequency wave with certain rule to have a coded form of the original message. This process is known as modulation.

iii. **Channel :**

1. Channels are the medium to transmit information from source to destination.
2. It should be noted that the term channel is often used to refer to the frequency range allocated to a particular service or transmission, such as a television channel.
3. Noise may interfere with signal at any point in the communication system, but it will have its greatest effect when signal is weakest. It means the noise in the channel or at the input to the receiver is the most noticeable.

iv. **Receiver :**

1. Receiver does the opposite process that of transmitter.
2. Here demodulation of the wave coming from the receiver through channel is done to get original information.
3. The output of receiver may be fed to a loudspeaker or video display.

Que 5.6. **Explain the need of modulation in communication system.**

AKTU 2015-16(Sem-I), Marks 05

OR

Discuss the need of modulation in the communication engineering. Which types of modulations are used in television ?

AKTU 2016-17(Sem-II), Marks 5.25

Answer

A. **Need of modulation :**

Modulation is needed in communication system to achieve some basic needs :

i. **Multiplexing :**

1. Simultaneous transmission of multiple messages over a channel is known as multiplexing.

2. If transmitted without modulation, the different message signals over a single channel will interfere with one another.
3. Different message signals can be transmitted over a single channel without interference using multiplexing technique.

ii. **Practicability of Antennas :**

1. The antenna radiates effectively when its height is of the order of the wavelength of the signal being transmitted.
2. In broadcast system the maximum audio frequency transmitted from a radio station is of the order of 5 kHz.
3. The height of antenna

$$= \frac{\lambda}{2} = \frac{c}{2f} = \frac{3 \times 10^8}{2 \times 5 \times 10^3} = 30{,}000 \text{ m} = 30 \text{ km}$$

Practically, such height of antenna is not possible.

4. Therefore, modulation is used by which frequency increases and thus, height of antenna decreases.

B. Television systems use vestigial sideband modulation, a form of amplitude modulation in which one sideband is partially removed. This reduces the bandwidth of the transmitted signal, enabling narrower channels to be used.

PART-3

Fundamental of Amplitude Modulation and Demodulation Technique.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.7. **Define the term modulation and demodulation. Also classify the modulation.**

Answer

A. **Modulation :**

1. Modulation is defined as the process by which some characteristic of a signal called carrier is varied in accordance with the instantaneous value of baseband or modulating signal.
2. The signal resulting from the process of modulation is called modulated signal.

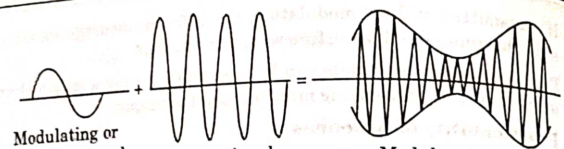


Fig. 5.7.1. Process of Modulation.

B. Classification of Modulation :

- Modulation
  - Analog Modulation
    - Amplitude
    - Frequency
    - Phase
  - Pulse Modulation
    - Pulse position
    - Pulse amplitude
    - Pulse width
  - Digital Modulation
    - Pulse code
    - ASK
    - FSK, PSK

C. Demodulation :

1. The receiver recreates the original message signal from a degraded version of transmitted signal after propagation through the channel.
2. This recreation is accomplished by using a process called demodulation.

Que 5.8. **Define Amplitude Modulation. Derive an expression for amplitude modulated wave.**

AKTU 2017-18(Sem-II), Marks 3.5

OR

Define amplitude modulation. Derive the expression for AM modulated waveform. Define modulation index of AM.

AKTU 2016-17(Sem-I), Marks 10

AKTU 2017-18(Sem-I), Marks 07

OR

Derive the expression for AM modulated waveform. Also derive the expression for modulation index.

AKTU 2016-17(Sem-II), Marks 07

Answer

1. Amplitude Modulation (AM) is defined as a system of modulation in which the amplitude of the carrier is made proportional to the instantaneous amplitude of the modulating voltage keeping frequency of the carrier constant.

2. Baseband or modulating signal is generally low frequency audio signal and carrier is high frequency RF-signal.
3. Let the carrier voltage (v_c) and modulating voltage (v_m) respectively given as:

$$v_c = V_c \sin \omega_c t \quad ...(5.8.1)$$

$$v_m = V_m \sin \omega_m t \quad ...(5.8.2)$$

where V_c is the maximum amplitude of carrier wave and V_m is the maximum amplitude of modulating wave.

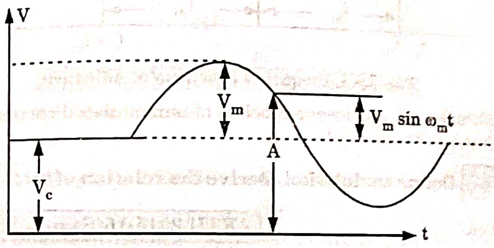


Fig. 5.8.1.

4. From the Fig. 5.8.1, it is clear that amplitude of AM wave A is given as :

$$A = V_C + v_m \quad ...(5.8.3)$$

From eq. (5.8.2), we have

$$A = V_C + V_m \sin \omega_m t$$

$$A = V_C\left(1 + \frac{V_m}{V_C} \sin \omega_m t\right) \quad ...(5.8.4)$$

5. The ratio V_m/V_c is known as modulation index (m_a).
6. The modulation index is a number lying between 0 and 1, and it is often expressed as a percentage and called the percentage modulation.
7. So, from eq. (5.8.4), we have amplitude of amplitude modulated wave

$$A = V_c (1 + m_a \sin \omega_m t) \quad ...(5.8.5)$$

8. So the instantaneous voltage of amplitude modulated wave is given as :

$$V_{AM} = A \sin \omega_c t \quad \text{(since frequency is constant)}$$

9. From eq. (5.8.5), we have

$$V_{AM} = V_c (1 + m_a \sin \omega_m t) \sin \omega_c t \quad ...(5.8.6)$$

This is the complete equation of AM-wave.

10. Now expanding eq. (5.8.6) we have

$$V_{AM} = V_c \sin\omega_c t + \frac{m_a V_c}{2} (2 \sin \omega_m t \sin \omega_c t)$$

$$V_{AM} = \underbrace{V_c \sin\omega_c t}_{Carrier} + \underbrace{\frac{m_a V_c}{2}\cos(\omega_c - \omega_m)t}_{LSB} - \underbrace{\frac{m_a V_c}{2}\cos(\omega_c + \omega_m)t}_{USB}$$

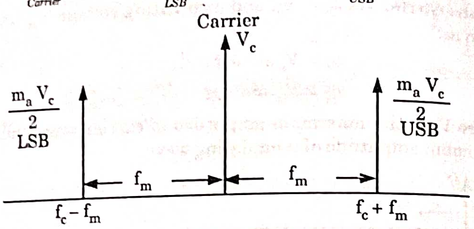


Fig. 5.8.2. Frequency spectrum of AM-wave.

11. Amplitude modulated wave consists of unmodulated carrier and two sidebands LSB and USB.

Que 5.9. **Define modulation. Derive the relation of total power of AM waves.**

AKTU 2015-16(Sem-I), Marks 05

Answer

A. **Modulation :** Refer Q. 5.7, Page 5–10J, Unit-5.

B. **Power of AM waves :**

1. We can write AM-wave equation as below :

$$v = \underbrace{V_c \sin\omega_c t}_{Carrier} + \underbrace{\frac{mV_c}{2}\cos(\omega_c - \omega_m)t}_{LSB} - \underbrace{\frac{mV_c}{2}\cos(\omega_c + \omega_m)t}_{USB} \quad ...(5.9.1)$$

2. The total power in modulated wave,
P_t = Power in carrier + Power in two sidebands

$$P_t = P_c + P_{LSB} + P_{USB} \quad ...(5.9.2)$$

3. The different power can be written as

$$P_c = \frac{\left(\frac{V_c}{\sqrt{2}}\right)^2}{R} = \frac{V_c^2}{2R} \quad ...(5.9.3)$$

$$P_{LSB} = P_{USB} = \frac{V_{SB}^2}{R} = \frac{\left(\frac{mV_c}{2\sqrt{2}}\right)^2}{R} = \frac{m^2V_c^2}{8R}$$

$$P_{LSB} = P_{USB} = \frac{m^2}{4}\left(\frac{V_c^2}{2R}\right) \quad ...(5.9.4)$$

where R is resistance.

4. Now from eq. (5.9.2), (5.9.3) and (5.9.4),

$$P_t = \left(\frac{V_c^2}{2R}\right) + \frac{m^2}{4}\left(\frac{V_c^2}{2R}\right) + \frac{m^2}{4}\left(\frac{V_c^2}{2R}\right)$$

$$P_t = \frac{V_c^2}{2R}\left(1 + \frac{m^2}{4} + \frac{m^2}{4}\right) c$$

$$P_t = \frac{V_c^2}{2R}\left(1 + \frac{m^2}{2}\right)$$

We know that

$$P_c = \frac{V_c^2}{2R}$$

$$P_t = P_c\left(1 + \frac{m^2}{2}\right)$$

where P_c is unmodulated carrier power and m is modulation index in AM.

Que 5.10. **Explain DSB-SC modulation and demodulator.**

OR

Explain Double Sideband Suppressed Carrier (DSB-SC) Techniques.

AKTU 2017-18(Sem-II), Marks 3.5

Answer

A. **DSB-SC Modulator :**

1. A DSB-SC modulator can be designed by using a mixer that generates the sidebands as well as carrier signal and the baseband message signal. For DSB-SC modulator only the base band message is to be filtered out.
2. Let us consider a simple switching modulator circuit with only one diode.

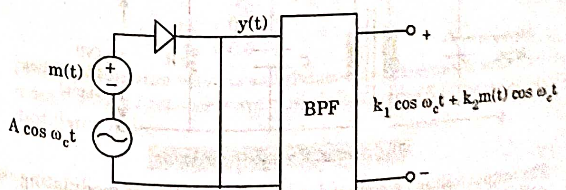


Fig. 5.10.1. An AM (DSB-SC) modulator.

3. The BPF passes frequency $\omega_c \pm \omega_m$ where ω_m is maximum frequency of message signal, carrier is represented by $A \cos \omega_c t$.
4. The switching action can be approximated by a pulse train as

$$s(t) = \frac{1}{2}+\frac{2}{\pi}\left[\cos \omega_c t - \frac{1}{3}\cos 3\omega_c t + \frac{1}{5}\cos 5\omega_c t - \frac{1}{7}\cos 7\omega_c t + ...\right] \quad ...(5.10.1)$$

5. Now the combined signal message $m(t) + A \cos \omega_c t$ will appear at the output when the diode is switched ON and otherwise not.

$$y(t) = [m(t) + A \cos \omega_c t]\ s(t)$$
$$= [m(t) + A \cos \omega_c t]$$
$$\left[\frac{1}{2}+\frac{2}{\pi}\left(\cos \omega_c t - \frac{1}{3}\cos 3\omega_c t + \frac{1}{5}\cos 5\omega_c t - \frac{1}{7}\cos 7\omega_c t + ...\right)\right]$$
$$y(t) = \frac{m(t)}{2}+\frac{A}{2}\cos \omega_c t + \frac{2}{\pi}m(t)\cos \omega_c t + \frac{2A}{\pi}\cos^2 \omega_c t + ...$$

6. The BPF passes $\omega_c \pm \omega_m$ and bring out $\frac{2}{\pi}m(t)\ \cos \omega_c t$ and the carrier component $\frac{A}{2}\cos \omega_c t$ which clearly is an AM or DSB-SC signal.

B. DSB-SC Demodulator :

1. Envelope detector can be used to detect the original message signal from the modulated signal.
2. This detector uses linear characteristics of diode.
3. In the circuit, C is a small capacitance and R is large resistance.
4. The parallel combination of R and C is the load resistance across which the rectified output voltage V_0 is developed.
5. At each positive peak of the RF cycle, C charges up to a potential almost equal to the peak signal voltage.

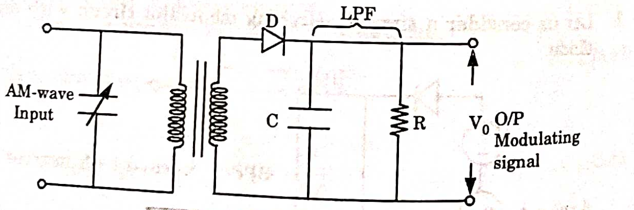


Fig. 5.10.2. Envelope detector.

6. The output voltage developed across R is replica of modulating signal with some ripples.

$$V_0 = A_c\,(1 + m_a \cos \omega_m t)$$
$$\frac{1}{RC} \geq m_a\,\omega_m$$

This is the condition for satisfactory detection of AM-wave.

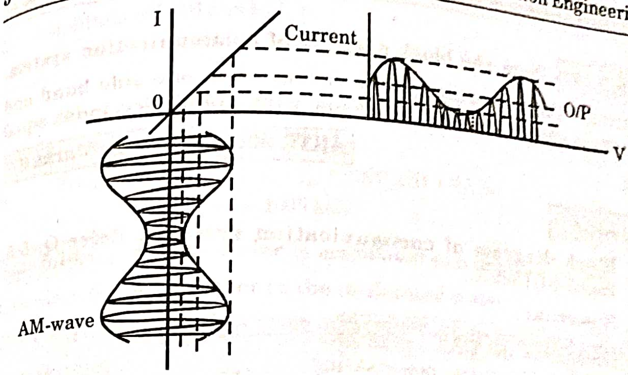


Fig. 5.10.3. Waveform representation of detector of AM-wave.

Que 5.11. **A certain AM transmitter radiates 9 kW with the carrier unmodulated and 10.125 kW when the carrier is modulated. Calculate the modulation index. If another sine wave is simultaneously transmitted with the modulation index 0.4, determine the total radiated power.**

AKTU 2017-18(Sem-I), Marks 07

Answer

Given : P_C = 9 kW, P_t = 10.125 kW, Modulation index, m_2 = 0.4
To Find : Modulation index, total radiated power.

1. We know,

$$P_t = P_C\left[\frac{m^2}{2}+1\right]$$
$$\frac{m^2}{2} = \frac{P_t}{P_C} - 1 = \frac{10.125}{9} - 1 = 0.125$$
$$m^2 = 0.25$$
$$\therefore \quad m = 0.5$$

2. Now, another sine wave is simultaneously transmitted with modulated index 0.4 with first sine wave of modulated index 0.5, therefore resultant modulated index,

$$m_t = \sqrt{m_1^2 + m_2^2}$$
$$\Rightarrow \quad m_t = \sqrt{0.5^2 + 0.4^2} = 0.64$$

3. $\therefore$
$$P_t = P_C\left[1+\frac{m_t^2}{2}\right] = 9\left[1+\frac{0.64^2}{2}\right] = 10.84 \text{ kW}$$

Que 5.12. **Draw the block diagram of communication system. Calculate the percentage power saving when one side band and carrier is suppressed in an AM signal with modulation index equal to 1.**

AKTU 2017-18(Sem-I), Marks 07

Answer

A. **Block diagram of communication system :** Refer Q. 5.5, Page 5–8J, Unit-5.

B. **Numerical :**

Given : $m = 100\ \% = 1$
To Find : Percentage power saving

1. We have,
$$P_T = P_C + \frac{m^2 P_C}{4} + \frac{m^2 P_C}{4} = P_C + \frac{P_C}{4} + \frac{P_C}{4}$$
$$= \frac{3}{2} P_C = 1.5\ P_C$$

2. When carrier and one sideband are suppressed
$$P_T = P_{USB} = \frac{P_C}{4}$$

3. Power saved $= P_C + \frac{P_C}{4} = \frac{5}{4} P_C = 1.25\ P_C$

4. % of power saved $= \frac{1.25 P_C}{1.5 P_C} \times 100 = 83.33\ \%$

Que 5.13. **A sinusoidal carrier of 1 MHz and amplitude 100 V is amplitude modulated by a sinusoidal modulating signal of frequency 5 kHz providing 50 % modulation. Calculate the frequency and amplitude of USB and LSB.**

AKTU 2017-18(Sem-II), Marks 3.5

Answer

Given : $f_c = 1$ MHz, $V_a = 100$ V, $f_m = 5$ kHz, m = 0.5
To Find : Amplitude and frequency of USB and LSB.

1. We have modulation index,
$$m = \frac{V_a}{V_c}$$
$$0.5 = \frac{100}{V_c}$$
$$V_c = 200\text{ V}$$

2. Amplitude of USB and LSB is,
$$\frac{mV_c}{2} = \frac{0.5 \times 200}{2} = 50\text{ V}$$

3. Frequency of LSB $= f_c - f_m = 1000$ kHz $- 5$ kHz
$= 995$ kHz

4. Frequency of USB $= f_c + f_m = 1000$ kHz $+ 5$ kHz
$= 1005$ kHz

Que 5.14. **A 460 W carrier is modulated to a depth of 65 percent. Calculate the total power in the modulated wave.**

AKTU 2015-16(Sem-I), Marks 05

Answer

Given : $P_C = 460$ W, $m = 65\ \% = 0.65$
To Find : Total power.

We know,
$$P_t = P_C\left(1 + \frac{m^2}{2}\right) = 460\left(1 + \frac{(0.65)^2}{2}\right)$$
$$P_t = 557.175\text{ W}$$

Que 5.15. **A 500 W carrier is modulated to a depth of 60%. Calculate the total power in amplitude modulated wave.**

AKTU 2016-17(Sem-I), Marks 05

Answer

Given : $P_c = 500$ W, $m = 60\ \% = 0.6$
To Find : Total power.

We know,
$$P_t = P_c\left(1 + \frac{m^2}{2}\right) = 500\left(1 + \frac{(0.6)^2}{2}\right)$$
$$T_t = 590\text{ W}$$

Que 5.16. **Compare Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM).**

AKTU 2017-18(Sem-II), Marks 3.5

Answer

S. No.	AM	FM	PM
1.	Amplitude of carrier is varied according to amplitude of modulating signal.	Frequency of carrier is varied according to amplitude of modulating signal.	Phase of carrier is varied according to amplitude of modulating signal.
2.	Modulation index does not greater than 1.	Modulation index may be greater than 1.	Modulation index may be greater than 1.
3.	AM is most commonly used for transmitting information via a radio carrier wave.	FM is commonly used at VHF radio frequencies for high-fidelity broadcasts of music and speech.	Phase modulation is widely used for transmitting radio waves.

Que 5.17. **If a FM wave is represented by the equation :**

$$V = 8 \sin (6 \times 10^8 + 3 \sin 2000t)$$

Calculate :

i. **Carrier frequency**

ii. **Modulating frequency**

iii. **Modulation index.**

AKTU 2016-17(Sem-I), Marks 05

Answer

1. Given, $V = 8 \sin (6 \times 10^8 t + 3 \sin 2000t)$ ...(5.17.1)
2. The equation of FM wave is given by

$$V = A \sin \left(\omega_c t + \frac{\Delta\omega}{\omega_m} \sin \omega_m t \right) \quad ...(5.17.2)$$

3. Compare eq. (5.17.1) with eq. (5.17.2)

i. Carrier frequency = $\omega_c = 6 \times 10^8$ rad/sec.

ii. Modulating frequency = $\omega_m = 2000$ rad/sec.

iii. Modulation index = $\dfrac{\Delta\omega}{\omega_m} = 3$

PART-4

Introduction to Data Communications : Goals and Applications of Networks.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.18. **Describe the goals and applications of network.**

Answer

A. **Goals of network are :**

1. Cost reduction by sharing hardware and software resources.
2. High reliability by having multiple sources of supply.
3. Greater flexibility because of possibility to connect devices.
4. Increase productivity by making it easier to access data by the several users.
5. To increase the systems performance, as the work load increases, by just adding more processors.
6. Computer networks provide a powerful communication medium.

B. **Applications of network are :**

i. **Marketing and sales :**

1. Marketing professional use to collect, exchange and analyze data relating to customer needs and product development cycles.
2. Sales application includes teleshopping, which uses order entry computers or telephone connected to an order processing network, and online reservation services for railways, hotels, airlines, restaurants, theatre etc.

ii. **Financial services :** It include credit history searches, foreign exchange and investment services and Electronic Fund Transfer (EFT), which allow a user to transfer money without going to bank.

iii. **Electronic messaging :**

1. Emails transfer the messages between two and more users in a network.
2. With this application user can transfer the information in the form of text, picture and voice.

iv. **Directory services :** It allows list of files to be stored in central location to speed up the world wide search operation.

v. **Information services :**

1. It includes bulletin boards and data bank.
2. A 'www' site offering the technical specification for a new product in an information services.

PART-5

General Model of Wireless Communication : Evolution of Mobile Radio Communication Fundamental, GPRS, GSM, CDMA.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.19. **Explain the term evolution of mobile radio communication fundamentals.**

Answer

1. In the year 1887 Heinrich Hertz proves existence of EM waves. Gugliemo Marconi developed the world's first commercial radio service in 1897.
2. It was the first ship-to-shore communication system and provided information about incoming ships.
3. The first human voice transmission via radio was accomplished by Reginald Fessenden in 1900.
4. The first use of mobile radio in an automobile was in 1921. Early radio telephone systems could be carried on ships but were too large to carry in cars.
5. The key technological breakthrough came in 1935, when scientist Edwin Armstrong introduced frequency modulation (FM) to improve radio broadcasting.
6. This technology reduced the required bulk of radio equipment and improved transmission quality.
7. In 1946, Bell telephone labs inaugurated the first mobile system for public, the system was known as mobile telephone service (MTS). But MTS offered only one way communication at a time.
8. In 1965, Bell system introduced improved version of MTS known as improved mobile telephone service (IMTS), which was the first automatic mobile system and full duplex in nature.

9. The ability to provide wireless communication to an entire population was not even imaginable until Bell laboratories developed the cellular concept in 1960s and 1970s.
10. With the development of highly reliable, miniature, solid state radio frequency hardware in the 1970s, the wireless communication era was born.

Que 5.20. **What is GSM ? Mention the GSM services and features.**

Answer

A. **GSM :**

1. Global system for mobile (GSM) is a second generation cellular system standard that was developed to solve the fragmentation problems of the first generation cellular systems in Europe.
2. GSM was the world's first cellular system to specify digital modulation and network level architectures and services, and is the world's most popular 2G technology.
3. GSM was originally developed to serve as the pan-European cellular service and promised a wide range of network services through the use of ISDN.
4. In 1992, GSM changed its name to the global system for mobile communications for marketing reasons.

B. **GSM services and features :**

1. GSM services follow ISDN guidelines and are classified as either teleservices or data services.
2. Teleservices include standard mobile telephony and mobile originated or base originated traffic.
3. Data services include computer-to-computer communication and packet switched traffic. User services may be divided into three major categories:

i. **Telephone services :** It includes emergency calling and facsimile. GSM also supports videotex and teletex, though they are not integral parts of GSM standard.

ii. **Bearer service or data services :** These are limited to layer 1, 2 and 3 of the open system interconnection (OSI) reference model. Supported services include packet switched protocols and data rates from 300 bps to 9.6 kbps. Data may be transmitted using either a transparent mode or non-transparent mode.

iii. **Supplementary ISDN services :**

a. They are digital in nature, and include call diversion, closed user groups and caller identification, and are not available in analog mobile networks.

b. Supplementary services also include the short messaging service (SMS) which allows GSM subscriber and base stations to transmit alphanumeric pages of limited length while simultaneously carrying normal voice traffic.

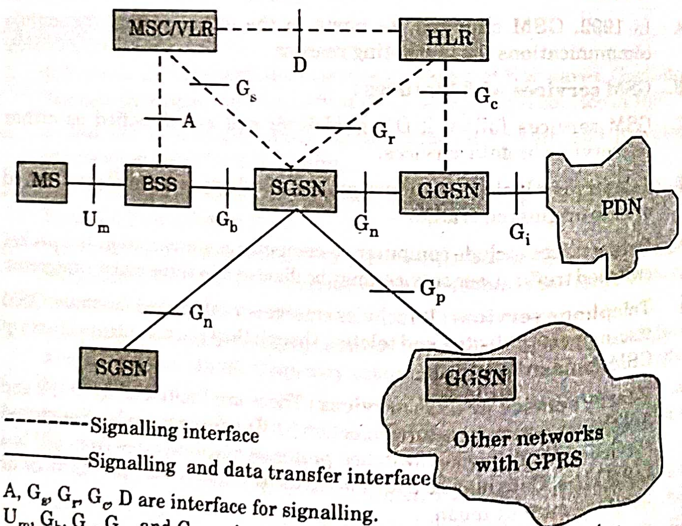
4. From the user's point of view, one of the most remarkable features of GSM is the subscriber identity module (SIM), which is a memory device that stores information such as the subscriber's identification number, the networks and countries where the subscriber is entitled to service, privacy keys and other user specific information.

5. A second remarkable feature of GSM is the on-the-air privacy which is provided by the system.

Que 5.21. **Explain GPRS architecture.**

Answer

1. The GSM technology was developed for voice services, but it did not have the capability to provide data services.
2. To develop a higher data rate capability and to enhance the services the GPRS protocol was developed on the GSM platform. The scenario and GPRS architecture are shown in Fig. 5.21.1.



--------Signalling interface

———Signalling and data transfer interface

A, G_s, G_r, G_c, D are interface for signalling.

U_m, G_b, G_n, G_p, and G_i are interfaces for signalling and transmission.

Fig. 5.21.1. GPRS architecture with modifications in the GSM, including additional GPRS components.

3. GPRS could offer data rates up to 115 kbps, which allowed web browsing and other services requiring data transfer. GGSN-gateway GPRS support node; SGSN-serving GPRS support node; PDN-packet data network.
4. GPRS uses packet-switched data rather than circuit-switched data, which is much more efficient for using the available capacity. This is because data transfer takes place in a bursty manner.
5. The transfer occurs in short peaks, followed by breaks when there is little or no activity. Packet switching permits sharing the overall capacity among several users.
6. The data is split into packets and then tags are inserted into each packet to mark its destination address. Packets from several sources can then be transmitted over the link. It is unlikely that the data burst for all the users will occur at the same time, so sharing the overall resource in this fashion makes the system efficient.
7. For GPRS, the data from the BSC is routed through the serving GPRS support node (SGSN).
8. This forms the gateway to the services within the network and then a gateway GPRS support node (GGSN), which forms the gateway to the outside world.

a. **SGSN function :** It enables authentication and then tracks the location of a mobile within a network. It also ensures that the quality of service (QoS) is at the required level.

b. **GGSN function :** It appears as a data gateway to the public packet network and provides identity to the mobiles for internet access as follows :

i. The network protocols used and supported by GPRS are X.25 and IP.

ii. In operation, the protocols assign addresses (packet data protocol or PDP addresses) to the devices in the network for routing the data through the system.

iii. A GPRS mobile must attach itself to the SGSN and activate its PDP address. This address is supplied by the GGSN, which is associated with the SGSN.

iv. As a result, a mobile can be attached to only one SGSN, although once its address is assigned, it can receive data from multiple GGSNs using multiple PDP addresses.

Que 5.22. **Explain forward and reverse IS-95 channel modulation process.**

Answer

A. **IS-95 forward channel :**

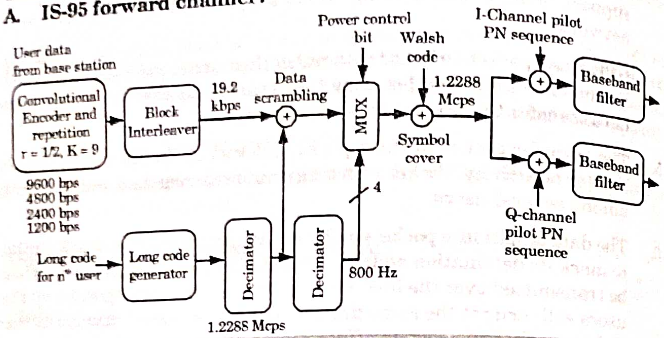


Fig. 5.22.1. Forward CDMA channel modulation process.

1. For voice traffic the speech is encoded at a data rate of 9.6 kbps including error detection bits. During quiet periods the data rate is lowered to 1200 bps.
2. The 2400 bps is used to transmit transient in the background noise. 4800 bps is used to mix digitized speech signaling data.
3. The data or digitized speech is transmitted in 20 ms blocks will forward error correction provided by convolutional encoder with rate 1/2, thus doubling the effective data rate to 19.2 kbps rate.
4. For lower data rates, the encoder O/P bits are replicated to yield 19.2 kbps rate.
5. The data are then interleaved in blocks to reduce the effects of errors by spreading them out.
6. Following the interleaver, the data bits are scrambled. The purpose of this is to serve as privacy mask and also to prevent sending of repetitive patterns.
7. The scrambling is accomplished by means of a long code that is generated as a pseudo random number from a 42-bit long shift register.
8. The shift register is initialised with the user's electronic serial number. The output of long code generator is at a rate of 1.2288 Mcps.
9. The decimator keeps only the first chip out of every 64 consecutive PN chips. The O/P of decimator is at 19.2 kbps.
10. The data scrambling is performed by modulo-2 addition of the interleaver O/P with the decimator O/P.
11. The next step in the processing inserts power control bits at a rate of 800 bps by replacing some of the traffic channel bits, using the long code generator to encode the bits.

12. The next step in the DSSS function spreads the 19.2 kbps to a rate of 1.2288 Mbps (Mcps) using one row of 64 × 64 Walsh matrix. One row of the matrix is assigned to a MS during call set up.
13. After this bits are spread in quadrature. Two separate bit stream (I and Q), data are split in I and Q channels.
14. Data in each channel XORed with a unique short-code. The short-binary spreading sequence, period $2^{15}-1$, chips is generated from a 15 bit long shift register. Thus data is transmitted using QPSK modulation.
15. A pilot code on the forward link is also transmitted simultaneously and at a higher power level thereby allowing all mobiles to use coherent detection while estimating the channel conditions.

B. **IS - 95 reverse channel :**

1. First few steps are same as forward channel. Data rate tripled here to 28.8 kbps, then block interleaved. The next step is spreading of the data using Walsh matrix. In the reverse channel the data coming out of the block interleaver are grouped into units of 6 bits.
2. Each 6 bit unit serves as a index to select a row of 64 × 64 Walsh matrix ($2^6 = 64$) and that row is substituted for the input. Thus, the data row is expanded by a factor of 64/6 to 307.2 kbps.
3. The purpose of this encoding is to improve the reception at the BS, because the 64 possible coding are orthogonal, the coding enhances decision making at receiver.
4. We can view this Walsh modulation as a form of block error correcting code with $(n, k) = (64, 6)$ and $d_{min} = 32$ (all distances are 32).
5. The data burst randomizer is used to help to reduce interference from other mobile stations. The operation involves using the long code mask to smooth the data out over each 20 ms frame.

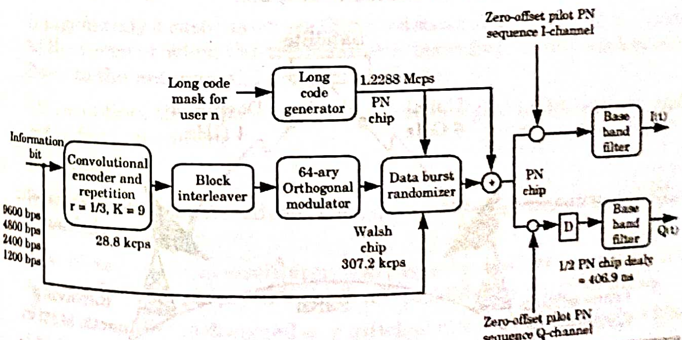


Fig. 5.22.2. Reverse IS-95 channel modulation process for a single user.

6. The next step in the process is DSSS function in case of reverse channel, the long code unique to mobile is XORed with the output of randomizer to produce 1.2288 Mcps final data stream.
7. The digital bit stream is then modulated on to a corner using an offset QPSK modulation.
8. The reason the modulators are different is that in forward channel, the spreading codes are orthogonal, all coming from Walsh matrix, whereas in reverse channel, orthgonality of the spreading code is not guaranteed.

PART-6

Elements of Satellite & Radar Communication.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.23. **What are the elements of satellite communication ? Explain each of them with a suitable block diagram.**

Answer

1. The basic elements of satellite communication are users, earth station transmitter, satellite and earth station receivers.
2. Fig. 5.23.1 shows the basic block diagram of the satellite communication system. It consists of many earth stations on the ground and these stations are linked with a satellite in space.

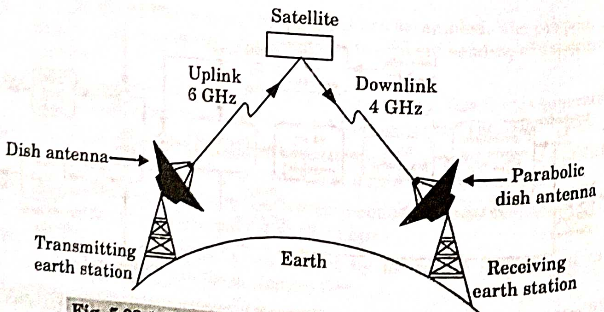


Fig. 5.23.1. Basic element of satellite communication system.

3. The user is connected to the earth station through a terrestrial network, and this network may be a telephone switch or dedicated link to a earth station.
4. The user generates a baseband signal that gets processed through the terrestrial network and transmitted to a satellite by the earth station.
5. The satellite consists of a large number of repeaters, that receives the modulated radio frequency carrier in its uplink frequency spectrum from all the earth stations in the network, amplifies these carriers, then retransmits them back to the earth station in the downlink frequency spectrum.
6. To avoid the interference, downlink and uplink frequency spectrum should have different frequencies.
7. The signal at the receiving earth station is processed to get back the base band signal, then it is sent to the user through a terrestrial network.

Que 5.24. **Explain the block diagram of radar.**

Answer

1. The block diagram of radar is shown in Fig. 5.24.1. In the block diagram the radar signal is produced at low power by a waveform generator, which is the input of power amplifier which acts as a transmitter.
2. When a power oscillator is used, it is also turned on and off by a pulse modulator to generate a pulse waveform.
3. The output of the transmitter is delivered to the antenna by a waveguide or transmission line.

i. **Duplexer :**

1. It allows a single antenna to be used for both transmitting and receiving.
2. It is generally a gaseous device that produces a short circuit at the input to the receiver when the transmitter is operating, so that high power flows to the antenna and not to the receiver.
3. On reception, the duplexer directs the echo signal to the receiver and not to the transmitter.

ii. **Receiver :**

1. It is always superheterodyne. The input or RF stage can be a low noise transistor amplifier.
2. The mixer or local oscillator (LO) convert the RF signal to an intermediate frequency (IF) where it is amplified by the IF amplifier.
3. The IF amplifier is designed as a matched filter, which maximizes the output peak-signal-to-mean-noise ratio.
4. Thus, the matched filter maximizes the detectability of weak echo signals and attenuated unwanted signals.

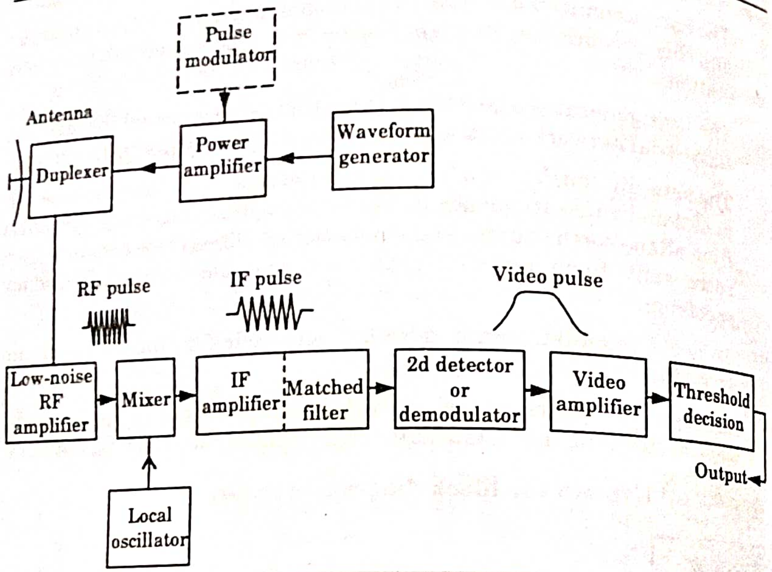


Fig. 5.24.1. Block diagram of a radar.

iii. 2d detector or demodulator :

1. Its purpose is to assist in extracting the signal modulation from the carrier.
2. The combination of IF amplifier, second detector and video amplifier acts as an envelope detector to pass the pulse modulation and reject the carrier frequency.
3. At the output of the receiver a decision is made whether a target is present or not.
4. The decision is based on the magnitude of the receiver output.
5. If the output is larger than the threshold level then target is present. If it does not cross the threshold, noise is present.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. What do you understand by signal ? Define various types of signals with suitable examples.

Ans. Refer Q. 5.1.

Q. 2. Explain the applications of electromagnetic spectrum. Also classify it further for Radio and Optical spectrum respectively.

Ans. Refer Q. 5.4.

Q. 3. Explain the need of modulation in communication system.

Ans. Refer Q. 5.6.

Q. 4. Define Amplitude Modulation. Derive an expression for amplitude modulated wave.

Ans. Refer Q. 5.8.

Q. 5. A certain AM transmitter radiates 9 kW with the carrier unmodulated and 10.125 kW when the carrier is modulated. Calculate the modulation index. If another sine wave is simultaneously transmitted with the modulation index 0.4, determine the total radiated power.

Ans. Refer Q. 5.11.

Q. 6. A sinusoidal carrier of 1 MHz and amplitude 100 V is amplitude modulated by a sinusoidal modulating signal of frequency 5 kHz providing 50 % modulation. Calculate the frequency and amplitude of USB and LSB.

Ans. Refer Q. 5.13.

Q. 7. Explain the term evolution of mobile radio communication fundamentals.

Ans. Refer Q. 5.19.

Q. 8. Explain forward and reverse IS-95 channel modulation process.

Ans. Refer Q. 5.22.

☺☺☺

1 UNIT

Semiconductor Diode (2 Marks Questions)

1.1. Why Si is preferred over Ge for manufacturing of electronics devices ?

AKTU 2015-16(Sem-I), Marks 02

Ans. Si is preferred over Ge for manufacturing of electronic devices due to following reasons :

i. Silicon is available in plenty amount on the surface of earth. This is the main reason why silicon is very much used by semiconductor device manufacturers.
ii. Cheaper.
iii. Smaller leakage current.
iv. Suitable for low power and high power applications.

1.2. Compare the properties of Si and Ge Semiconductors.

AKTU 2015-16(Sem-II), Marks 02

Ans.

S. No.	Properties	Si	Ge
1.	Conductivity	Comparatively low.	Conductivity is comparatively higher.
2.	Atomic radius	Has a smaller atomic radius than germanium.	Has comparatively a larger atomic radius.

1.3. Explain the effect of temperature on conductivity of a semiconductor.

AKTU 2015-16(Sem-I), Marks 02

Ans. In intrinsic semiconductor, as temperature increases the mobility of charge carrier reduces and this will reduce the conductivity by a smaller value and at the same time, a large number of covalent bond will be broken and a large number of electrons and holes are created and this will increase the conductivity by a large value.

1.4. Distinguish between avalanche and zener breakdown.

AKTU 2016-17(Sem-I), Marks 02

Ans.

S. No.	Zener breakdown mechanism	Avalanche breakdown mechanism
1.	This breakdown mechanism occurs in very thin junction.	This breakdown mechanism occurs in slightly thick junction.
2.	Zener current is independent of applied voltage.	Avalanche breakdown occurs at high voltages.
3.	Temperature coefficient is negative *i.e.*, – 1.4 mV/°C.	Temperature coefficient is positive *i.e.*, 2mV/°C.

1.5. Define depletion layer in a diode.

AKTU 2015-16(Sem-II), Marks 02

OR

Define depletion layer of *pn* junction diode.

AKTU 2015-16(Sem-I), Marks 02

Ans. The region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region.

1.6. Define bulk resistance of the diode.

AKTU 2015-16(Sem-II), Marks 02

Ans. Bulk resistance of diode depends on how it is biased. It is the approximate resistance of diode when it is forward biased.

1.7. Draw the double ended diode clipper circuit.

AKTU 2015-16(Sem-II), Marks 02

Ans.

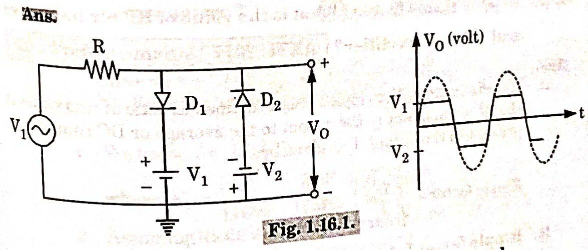


Fig. 1.16.1.

1.8. Classify the materials with help of energy band.

AKTU 2016-17(Sem-II), Marks 02

Ans. On the basis of energy band diagram, materials are classified into three types :

1. **Insulators :** In insulators, valence band is full and conduction band is empty. The energy gap between valence and conduction band is very large.
2. **Conductors :** In case of conductors, the valence and conduction bands overlap each other.
3. **Semiconductors :** In case of semiconductors, the valence band is almost full and conduction band is almost empty, also the energy gap between valence and conduction band is very small.

1.9. Draw a neat diagram of a full wave rectifier bridge circuit using diode.

Ans.

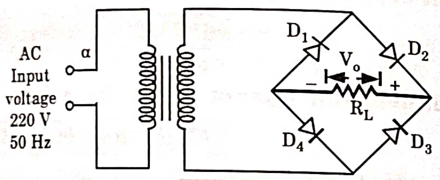


Fig. 1.9.1.

1.10. What are the PIV for full wave center tapped rectifier and bridge rectifier respectively ?

Ans. In center tap full wave rectifier, PIV = $2V_m$
In bridge type full wave rectifier, PIV = V_m

1.11. What is the voltage multiplier ?

Ans. Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

1.12. What is ripple factor ? What is the value of RF for half wave and full wave rectifier ? **AKTU 2017-18(Sem-I), Marks 02**

Ans.

A. **Ripple factor :** The ripple factor is defined as ratio of rms value of the AC component in the output to the average or DC component present in the output. It is given by,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_{rms}}{I_{DC}}\right]^2 - 1}$$

B. **Ripple factor for half wave rectifier :**

1. The ripple factor is given as

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

Since, $I_{rms} = I_m/2$ and $I_{DC} = I_m/\pi$. So, $r = 1.21$

C. **Ripple factor of full wave rectifier :**

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1}$$

$r = 0.482$

1.13. Explain the principle of operation of LED.

AKTU 2017-18(Sem-II), Marks 02

AKTU 2016-17(Sem-II), Marks 02

AKTU 2016-17(Sem-I), Marks 02

Ans.

i. Generation of electron-hole pair (EHP) by excitation of semiconductor.
ii. Recombination of EHP.
iii. Extraction of photons from the semiconductor.

1.14. What is photodiode ? Also write its uses.

Ans. Two-terminal devices designed to respond to photon absorption are called photodiodes.

Photodiodes are used primarily for two classes of application :

i. For detection of light, particularly very weak light.
ii. For power generation.

1.15. Calculate the dynamic forward resistance of *p-n* junction diode when applied voltage is 0.80 V at temperature of 43 degree Celsius and reverse saturation current is 8 microampere ? **AKTU 2016-17(Sem-I), Marks 02**

Ans.

Given : $V = 0.80\text{V}$, $T = 43\ °\text{C} = 316\ \text{K}$, $I_0 = 8\ \mu\text{A}$
To Find : Dynamic forward resistance.

1. We know, $I = I_0(e^{V/\eta V_T} - 1)$ ...(1.15.1)

where, $V_T = \dfrac{T}{11600} = \dfrac{316}{11600} = 36.7\ \text{mV}$

2. Assuming diode is a germanium diode, therefore $\eta = 1$
3. Putting all given values in eq. (1.15.1).

$$I = 8 \times 10^{-6}\left(e^{\frac{0.80}{1 \times 36.7 \times 10^{-3}}} - 1\right) = 2.34 \times 10^4\ \text{A}$$

4. Dynamic forward resistance, $r_f = \frac{nV_T}{I}$

$$= \frac{1 \times 36.7 \times 10^{-3}}{2.34 \times 10^{4}} = 1.56 \times 10^{-8}\,\Omega$$

1.16. The reverse saturation current of a silicon *p-n* junction diode is 10 μA at the temperature 300 K. Determine the forward bias voltage to be applied across the *p-n* junction to obtain a current of around 100 mA.

AKTU 2017-18(Sem-II), Marks 02

Ans.

Given : I_0 =10 μA, η = 2 (for Si), T = 300 K, I = 100 mA
To Find : Forward bias voltage.

We know, $I = I_0(e^{V/\eta V_T} - 1)$

$$100 \times 10^{-3} = 10 \times 10^{-6} (e^{V/2 \times 0.0259} - 1)$$

$$10001 = e^{V/0.0518}$$

Taking ln both sides,

$$9.21 = \frac{V}{0.0518}$$

$$V = 0.47 \text{ V}$$

1.17. Consider a constant voltage source with 10 V and series internal resistance of 100 ohm. Calculate its equivalent to a current source.

AKTU 2015-16(Sem-II), Marks 02

Ans. Equivalent current source $= \frac{V}{R} = \frac{10}{100} = 0.1$ A

☺☺☺

2 UNIT

BJT and FET (2 Marks Questions)

2.1. What are the various operating modes of transistor ?

Ans. There are 4 different modes of transistor :

S. No.	Mode	BE	CB
1.	Active	Forward bias	Reverse bias
2.	Saturation	Forward bias	Forward bias
3.	Cut-off	Reverse bias	Reverse bias
4.	Inverse active	Reverse bias	Forward bias

2.2. Why BJT is called current controlled device ?

AKTU 2017-18(Sem-I), Marks 02

Ans. A BJT is called current control device because the base current controls the current flow from emitter to collector.

2.3. Derive the relation between α and β for BJT.

AKTU 2017-18(Sem-II), Marks 02

AKTU 2016-17(Sem-II), Marks 02

AKTU 2016-17(Sem-I), Marks 02

Ans. We know that, $I_E = I_C + I_B$ ...(2.3.1)

Dividing eq. (2.3.1) both sides by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

But we know that $\beta = \frac{I_C}{I_B}$ and $\alpha = \frac{I_C}{I_E}$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} = \frac{\beta+1}{\beta}$$

$$\alpha = \frac{\beta}{\beta+1}$$

2.4. The thickness of base is typically smaller than emitter and collector. Why ? **AKTU 2016-17(Sem-I), Marks 02**

Ans. Base is very highly doped and is very thin (10^{-6} m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

2.5. Explain with proper reason the use of emitter follower. **AKTU 2015-16(Sem-I), Marks 02**

Ans. The emitter follower is used as a voltage buffer for connecting a high resistance source to a low resistance load.

2.6. Enlist the difference between JFET and BJT.

Ans.

S. No.	JFET	BJT
1.	Its operation depends only on majority carriers, so it is a unipolar device.	Its operation depends on both majority and minority carriers, so it is a bipolar device.
2.	It is a voltage controlled device.	It is a current controlled device.
3.	It has high input impedance.	It has low input impedance.
4.	Small in size, therefore space requirement on board is small.	Large in size, therefore space requirement on board is large.

2.7. Enlist the differences between JFET and MOSFET.

Ans.

S. No.	JFET	MOSFET
1.	JFET has lower input resistance than MOSFET.	MOSFET have much higher input resistance than JFET.
2.	JFET can operate in depletion mode.	MOSFET can operate in enhancement as well as depletion mode.

2.8. Mention the differences between *p*-channel and *n*-channel MOSFET.

Ans.

S. No.	*p*-channel MOSFET	*n*-channel MOSFET
1.	The current carriers are holes.	The current carriers are electrons.
2.	Transconductance is less in *p*-channel than *n*-channel.	Transconductance is more in *n*-channel than *p*-channel.
3.	Due to lower mobility of holes *p*-channel is not as fast as *n*-channel.	Due to higher mobility of electrons, *n*-channel MOSFET is faster.

2.9. Write down the constructional difference between depletion type and enhancement type MOSFET. **AKTU 2016-17(Sem-II), Marks 02**

Ans. The main constructional difference is the absence of continuous channel between the source and drain of enhancement MOSFET but it is present in case of depletion MOSFET.

2.10. Describe how FET can be used as voltage variable resistor. **AKTU 2017-18(Sem-II), Marks 02**

OR

Explain FET as voltage variable resistor. **AKTU 2016-17(Sem-I), Marks 02** **AKTU 2015-16(Sem-I), Marks 02**

Ans. FET when used in the region before pinch-off, it works as variable resistance device *i.e.*, the channel resistance is controlled by the gate bias voltage (V_{GS}).
In such applications FET is referred as voltage variable resistor (VVR).

2.11. Define ohmic region in FET. **AKTU 2015-16(Sem-II), Marks 02**

Ans.
1. In the ohmic region, FET works as a linear device, *i.e.*, a resistor. For example, voltage-variable resistor (VVR) and voltage-dependent resistor (VDR).
2. In the ohmic region, FET will work as a voltage-variable resistor by varying V_{GS}.

2.12. Why are FET called unipolar device ?

AKTU 2016-17(Sem-II), Marks 02

Ans. In FET, current conduction depends only on one type of carriers (majority carriers) either electrons or holes, so it is a unipolar device.

2.13. What is trans-conductance in FET ? What is the relationship between g_m and g_{mo} ?

AKTU 2017-18(Sem-I), Marks 02

Ans. The control that the gate voltage has over drain current is measured by transconductance g_m. It is simply the slope of transfer characteristics.

$$g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) V_{DS} \text{ held constant}$$

The unit of g_m is siemens (mho).

$$g_m = g_{mo}\sqrt{I_{DQ}/I_{DSS}}$$

2.14. In JFET, I_{DSS} = 8 mA, V_P = – 4 V biased at V_{GS} = – 1.8 V. Determine the value of g_m.

AKTU 2015-16(Sem-I), Marks 02

Ans. Given, I_{DSS} = 8 mA, V_P = – 4 V, V_{GS} = – 1.8 V

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1-\frac{V_{GS}}{V_P}\right] = \frac{2\times 8}{4}\left[1-\frac{1.8}{4}\right] = 2.2 \text{ mS}$$

2.15. If α of a transistor changes from 0.981 to 0.987, find the percentage change in β.

AKTU 2015-16(Sem-II), Marks 02

Ans. Here,

$$\beta_1 = \frac{\alpha_1}{1-\alpha_1} = \frac{0.981}{1-0.981} = 51.632$$

$$\beta_2 = \frac{\alpha_2}{1-\alpha_2} = \frac{0.987}{1-0.987} = 75.92$$

$$\% \text{ change in } \beta = \frac{\beta_2-\beta_1}{\beta_1} = \frac{75.92-51.632}{51.632} = 47\ \%$$

☺☺☺

3 UNIT

Operational Amplifiers and IoT (2 Marks Questions)

3.1. Define Op-Amp and draw its block diagram.

AKTU 2015-16(Sem-I), Marks 02

Ans. Op-Amp : Operational amplifier is designed to perform various mathematical operations such as addition, subtraction, integration, differentiation etc.

Block diagram :

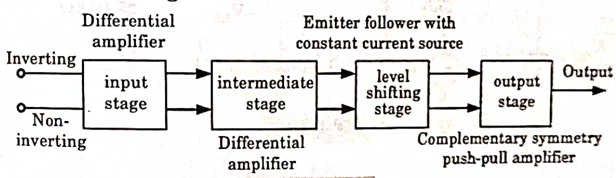


Fig. 3.1.1.

3.2. List of ideal characteristics of Op-Amp.

AKTU 2017-18(Sem-I), Marks 02

OR

Write the characteristics of an ideal Op-Amp.

AKTU 2016-17(Sem-I), Marks 02

Ans.

1. Input impedance is infinite.
2. Output impedance is zero.
3. Infinite CMRR.
4. Bandwidth is infinite.
5. Open loop gain is infinite.

3.3. Define CMRR, slew rate of Op-Amp.

AKTU 2015-16(Sem-I), Marks 02

Ans.

1. **CMRR :** CMRR is defined as the ratio of the differential voltage gain A_d to the common mode voltage gain A_{cm}.

i.e., $$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right|$$

2. **Slew rate (SR) :** It is defined as the maximum rate of change of output voltage per unit time and is expressed in volts per micro-second

i.e., $$SR = \left.\frac{dV_0}{dt}\right|_{max} \text{ V/}\mu\text{s}$$

3.4. Draw the output waveform that will appear across R_L.

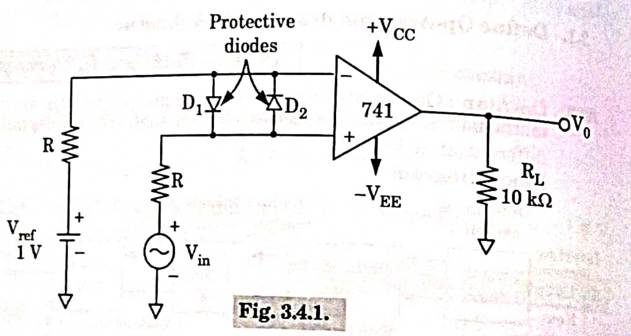


Fig. 3.4.1.

AKTU 2015-16(Sem-II), Marks 02

Ans.

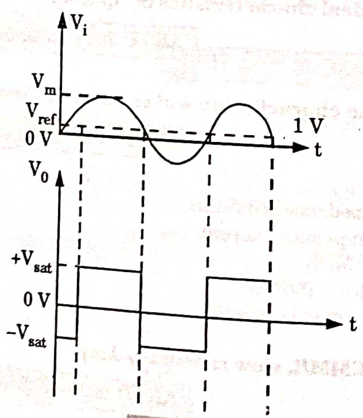


Fig. 3.4.2.

3.5. Sketch the circuit of Op-Amp as an integrator and differentiator.

AKTU 2017-18(Sem-II), Marks 02

OR

Derive the circuit of integrator using an ideal Op-Amp.

AKTU 2016-17(Sem-II), Marks 02

Ans. **Integrator :**

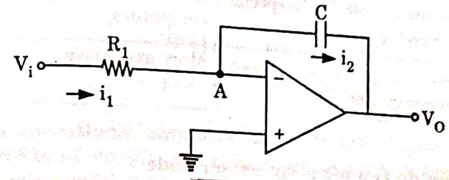


Fig. 3.5.1.

Differentiator :

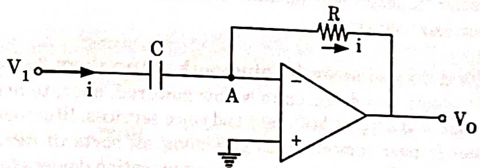


Fig. 3.5.2.

3.6. What do you mean by IoT ?

Ans. Internet of Things (IoT) is a concept and a paradigm that considers pervasive presence in the environment of a variety of things/objects that through wireless and wired connections and unique addressing schemes are able to interact with each other and co-operate with other things/objects to create new applications/services and reach common goals.

3.7. State the goals of IoT.

Ans. The goal of the Internet of Things is to enable things to be connected anytime, anyplace, with anything and anyone ideally using any path/network and any service.

3.8. What is the difference between a microcontroller and microprocessor ?

i.e., $\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right|$

2. **Slew rate (SR) :** It is defined as the maximum rate of change of output voltage per unit time and is expressed in volts per micro-second

i.e., $\text{SR} = \left.\frac{dV_0}{dt}\right|_{max}$ V/μs

3.4. Draw the output waveform that will appear across R_L.

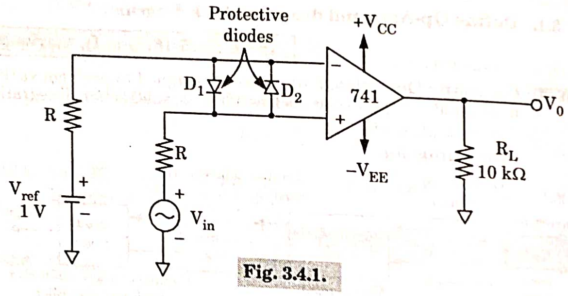


Fig. 3.4.1.

AKTU 2015-16(Sem-II), Marks 02

Ans.

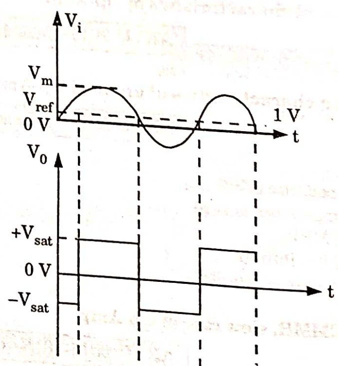


Fig. 3.4.2.

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AKTU 2017-18(Sem-II), Marks 02

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Derive the circuit of integrator using an ideal Op-Amp.

AKTU 2016-17(Sem-II), Marks 02

Ans. **Integrator :**

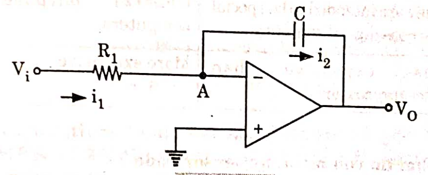
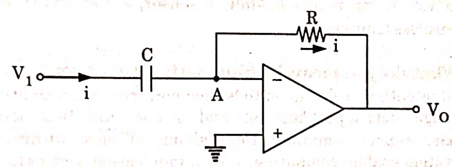


Fig. 3.5.1.

Differentiator :



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3.7. State the goals of IoT.

Ans. The goal of the Internet of Things is to enable things to be connected anytime, anyplace, with anything and anyone ideally using any path/network and any service.

3.8. What is the difference between a microcontroller and microprocessor ?

Ans.

S. No.	Microcontroller	Microprocessor
1.	It contains a fixed amount of RAM, ROM, I/O ports and a timer all on a single chip.	It does not contain ROM, RAM and I/O ports on the chip itself.
2.	They are intended to be special purpose digital computers.	General purpose digital computers.
3.	Less expensive than microprocessor.	More expensive.

3.9. What do you mean by sensor node ?

Ans. The sensor node is one of the main parts of a WSN. The hardware of a sensor node generally includes four parts : the power and power management module, a sensor, a microcontroller, and a wireless transceiver.

3.10. What do you mean by bluetooth technology ?

Ans. Bluetooth was designed to be low powered, operate over a short range, and support both data and voice services. Bluetooth enables peer-to-peer communications among all sorts of devices. This system enables computing and communication devices to exchange information and work together for the benefit of the user.

3.11. What are the various applications of bluetooth ?

Ans. Bluetooth application :

1. Mobile e-business :
   a. Pager b. Communicator
   c. Mobile phone.
2. Home networking :
   a. Fax b. Bluetooth
   c. Headphone.
3. Automobile network solution.

3.12. An operational amplifier has a differential gain of 10^3 and a CMRR of 100, input voltages are 120 μV and 80 μV. Determine the output voltage.

AKTU 2017-18(Sem-I), Marks 02

Ans.

Given : CMRR = 100, $A_d = 10^3$, $V_1 = 120$ μV, $V_2 = 80$ μV
To Find : V_O.

1. We know, $\text{CMRR} = \dfrac{A_d}{A_{cm}}$

$$A_{cm} = \frac{10^3}{100} = 10$$

2. Output voltage $= A_d V_d + A_{cm} V_c$

$$= 10^3 (V_1 - V_2) + 10 \left(\frac{V_1 + V_2}{2}\right)$$

$$= 10^3 (120 - 80) \times 10^{-6} + 10\left(\frac{120 + 80}{2}\right) \times 10^{-6}$$

$$= 40 \times 10^{-3} + 10^{-3} = 41 \text{ mV}$$

3.13. An operational amplifier has differential gain of 10^2 and CMRR of 80 dB, input voltage are 100 microvolt and 60 microvolt. Determine output voltage.

AKTU 2016-17(Sem-I), Marks 02

Ans.

Given : CMRR = 80 dB, $A_d = 10^2$, $V_1 = 100$ μV, $V_2 = 60$ μV
To Find : V_o

1. We know, $\text{CMRR} = 20 \log \left|\dfrac{A_d}{A_{cm}}\right|$

$$80 \text{ dB} = 20 \log \left|\frac{10^2}{A_{cm}}\right|$$

$$4 = \log \left|\frac{10^2}{A_{cm}}\right|$$

2. Taking antilog and we get,

$$10^4 = 10^2 / A_{cm}$$

$$A_{cm} = 10^{-2}$$

3. Output voltage $= A_d V_d + A_{cm} V_c$

$$= 10^2 (V_1 - V_2) + 10^{-2} \left(\frac{V_1 + V_2}{2}\right)$$

$$= 10^2 (100 - 60) \times 10^{-6} + 10^{-2} \left(\frac{100 + 60}{2}\right) \times 10^{-6}$$

$$= 10^2 \times 40 \times 10^{-6} + 80 \times 10^{-8}$$

$$= 4 \text{ mV}$$

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4 UNIT

Digital Electronics and ICT (2 Marks Questions)

4.1. What is number system ?

Ans. It is a language of digital systems consisting of a set of symbols called digits with rules defined for their addition, multiplication and other mathematical operations.

4.2. Classify number systems.

Ans. The number systems are as follows :

i. Decimal number system.
ii. Binary number system.
iii. Octal number system.
iv. Hexadecimal number system.

4.3. Write four advantages of digital systems over analog system.

Ans.

1. Digital communication system is more robust than analog system because it can resist the corruption of signal much better in presence of channel noise.
2. Implementation of digital hardware in digital communication system is flexible and permits the use of microprocessor, digital switching etc.
3. In digital system, it is possible to multiplex several digital signals that offer more efficient use of available bandwidth.
4. In digital system, it is easy to store large quantities of information.

4.4. Convert $(153.513)_{10}$ to an octal number ?

Ans.

$(153)_{10}$ to octal :

8	153	1
8	19	3
8	2	2
	0	

$(0.513)_{10}$ to octal :

$0.513 \times 8 = 4.104$
$0.104 \times 8 = 0.832$
$0.832 \times 8 = 6.656$
$0.656 \times 8 = 5.248$
$0.248 \times 8 = 1.984$
$0.984 \times 8 = 7.872$

$(153)_{10} = (231)_8$, $(0.513)_{10} = (0.406517......)_8$

So, $(153.513)_{10} = (231.406517)_8$

4.5. Convert the decimal number 32.57 in binary and Gray.

Ans. **For binary :**

2	32	0
2	16	0
2	8	0
2	4	0
2	2	0
2	1	1
	0	

For Gray :

$\oplus$ $\oplus$ $\oplus$ $\oplus$ $\oplus$ $\oplus$ $\oplus$

1 0 0 0 0 0 1 0

1 1 0 0 0 0 1 1

$32 = (100000)_2$

and $.57 = .57 \times 2 = 1.14$

$0.14 \times 2 = 0.28$

Hence, $(32.57)_{10} = (100000.10)_2$

Hence, $(32.57)_{10} = (110000.11)_{Gray}$

4.6. Convert the following :

i. $(562.13)_7 = (?)_{10}$

ii. $(467.342)_8 = (?)_{10}$

Ans.

i. $(562.13)_7 = 5 \times 7^2 + 6 \times 7^1 + 2 \times 7^0 + 1 \times 7^{-1} + 3 \times 7^{-2}$
$= (289.20)_{10}$

ii. $(467.342)_8 = 4 \times 8^2 + 6 \times 8^1 + 7 \times 8^0 + 3 \times 8^{-1} + 4 \times 8^{-2} + 2 \times 8^{-3}$
$= (311.441)_{10}$

4.7. Determine the value of base x, if $(193)_x = (623)_8$.

Ans.

$$(193)_x = (623)_8$$

$$1 \times x^2 + 9 \times x + 3 \times x^0 = 6 \times 8^2 + 2 \times 8^1 + 3 \times 8^0$$

$$x^2 + 9x + 3 = 403$$

$$x^2 + 9x - 400 = 0$$

$$x^2 + 25x - 16x - 400 = 0$$

$$(x + 25)(x - 16) = 0$$

$x \neq -25$ ($\because$ Base can't be negative)

$\therefore$ $x = 16$

4.8. Convert the following expression into canonical POS form

$$Y = (A + B)(B + C)(A + C)$$

Ans. Given,

$$Y = (A + B)(B + C)(A + C)$$

$$= (A + B + C\bar{C})(B + C + A\bar{A})(A + C + B\bar{B})$$

Canonical form,

$$Y = (A + B + C)(A + B + \bar{C})(A + B + C)(\bar{A} + B + C)(A + B + C)(A + \bar{B} + C)$$

$$= (A + B + C)(A + B + \bar{C})(\bar{A} + B + C)(A + \bar{B} + C)$$

4.9. Simplify the following boolean expression to a minimum number of literals : $(x'y' + z')' + z + xy + wz$

Ans.

Given, $(x'y' + z')' + z + xy + wz$

Using De-Morgan's theorem

$$(x'y' + z')' = (x + y)\, z$$

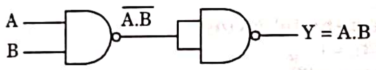
$$(x'y' + z')' + z + xy + wz = (x + y)\, z + z + xy + wz$$
$$= z[1 + (x + y)] + xy + wz = z + xy + wz$$
$$= z[1 + w] + xy = z + xy$$

4.10. What are the universal gates and why we call them as universal ?

Ans. NAND and NOR gates are universal gates, these are called universal because it is possible to implement any logic gate or expression using only NAND or only NOR gates.

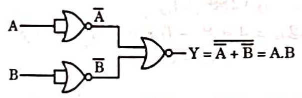
4.11. Implement two input AND gate using NAND gate.

Ans.



4.12. Implement two input AND gate using NOR gate.

Ans.



4.13. Define small scale integration.

Ans. When the active devices per chip are less than 100, then it is referred as small scale integration (SSI). Most of the SSI chips use integrated resistors, diodes and bipolar transistors.

4.14. What do you mean by LSI ?

Ans. In large scale integration (LSI), the number of active devices per chip ranges between 1000 and 100000. In general, LSI chips use MOS transistors; as it requires less number of steps for integration.

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5 UNIT

Fundamental of Communication Engineering (2 Marks Questions)

5.1. Define signal. Name various types of signal.

AKTU 2015-16(Sem-I), Marks 02

Ans. **Signal :** A signal is defined as a physical quantity that varies with time, space or any other independent variable.

Types :

i. Deterministic and Radom signals.
ii. Even and Odd signals.
iii. Energy and Power signals.

5.2. What do you mean by even and odd signals ?

Ans. A signal $x(t)$ or $x[n]$ is referred to as symmetric or even signal if,

$$x(-t) = x(t) \text{ or } x[-n] = x[n]$$

and referred to as non-symmetric or odd signal if

$$x(-t) = -x(t) \text{ or } x[-n] = -x[n]$$

5.3. What are energy and power signals ?

Ans. **Power signal :** A power signal is defined as a signal having finite average power and infinite energy *i.e.*, $0 < P < \infty$ and $E = \infty$.

Energy signal : The energy signal is one that has a finite energy and zero average power *i.e.*, $0 < E < \infty$ and $P = 0$.

5.4. What do you mean by periodic and non-periodic signals ?

Ans. A signal $f(t)$ is called periodic if there exist constant T, such that

$$f(t) = f(t + T) \quad \text{for } -\infty < t < \infty$$

T is called the period of the signal, and signal $f(t)$ repeats after every T. Those signals that do not satisfy the above condition are called as non-periodic signals.

5.5. Define modulation and give its types.

Ans. **Modulation :** Modulation is defined as the process by which some characteristic of a signal called carrier is varied in accordance with the instantaneous value of baseband or modulating signal. The signal resulting from the process of modulation is called modulated signal.

Types :

i. Analog modulation
ii. Pulse modulation
iii. Digital modulation

5.6. What is modulation index ? Draw the amplitude spectrum of AM wave. **AKTU 2017-18(Sem-I), Marks 02**

Ans. **Modulation index :** The modulation index or depth of modulation is the measure of the extent to which the amplitude of carrier wave is change by the signal.

Amplitude spectrum of AM wave :

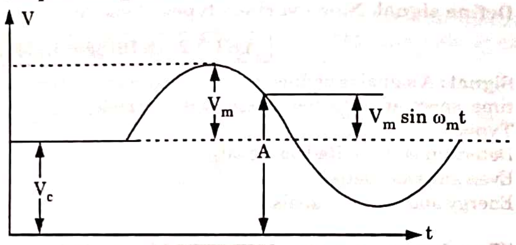

Fig. 5.6.1.

5.7. Define amplitude modulation

Ans. Amplitude Modulation (AM) is defined as a system of modulation in which the amplitude of the carrier is made proportional to the instantaneous amplitude of the modulating voltage keeping frequency of the carrier constant.

5.8. Give advantages of FM over AM. **AKTU 2016-17(Sem-I), Marks 02**

Ans. The main advantages of FM over AM are :

1. Improved signal to noise ratio with respect to manmade interference.
2. Less radiative power.
3. Smaller geographical interference between neighbouring stations.
4. Well-defined service area for given transmitter power.

5.9. Briefly discuss the need of modulation in communication engineering. **AKTU 2016-17(Sem-II), Marks 02**

Ans. Modulation is needed in communication system to achieve some basic needs :

i. **Multiplexing :**

1. Simultaneous transmission of multiple messages over a channel is known as multiplexing.

2. If transmitted without modulation, the different message signals over a single channel will interfere with one another.
3. Different message signals can be transmitted over a single channel without interference using multiplexing technique.

ii. **Practicability of Antennas :**

1. The antenna radiates effectively when its height is of the order of the wavelength of the signal being transmitted.
2. In broadcast system the maximum audio frequency transmitted from a radio station is of the order of 5 kHz.
3. The height of antenna

$$= \frac{\lambda}{2} = \frac{c}{2f} = \frac{3 \times 10^8}{2 \times 5 \times 10^3} = 30{,}000 \text{ m} = 30 \text{ km}$$

Practically, such height of antenna is not possible.

4. Therefore, modulation is used by which frequency increases and thus, height of antenna decreases.

5.10. What are the goals of the network ?

Ans.

1. Cost reduction by sharing hardware and software resources.
2. High reliability by having multiple sources of supply.
3. Greater flexibility because of possibility to connect devices.
4. Computer networks provide a powerful communication medium.

5.11. What is GSM ?

Ans. Global system for mobile (GSM) is a second generation cellular system standard that was developed to solve the fragmentation problems of the first cellular systems in Europe.

5.12. Name the services provided by GSM.

Ans. User services may be divided into three categories :

i. Telephone services.
ii. Bearer services or data services.
iii. Supplementary ISDN services.

5.13. What are the basic elements of satellite communication ?

Ans.

1. Users.
2. Earth station transmitter.
3. Satellite.
4. Earth station receiver.

5.14. What is radar ?

Ans. Radar is an electromagnetic system for the detection and location of reflecting objects such as aircrafts, ships, spacecrafts, vehicles, people and the natural environment.

5.15. The unmodulated rms current of an AM wave is 8.93 A and it increase to 11.25 A with modulation. Determine the modulation index. **AKTU 2017-18(Sem-II), Marks 02**

Ans. Given, $I_c = 8.93$ A

$I = 11.25$ A

We know, $I^2 = I_c^2\left(1+\frac{\mu^2}{2}\right)$

$$(11.25)^2 = (8.93)^2\left(1+\frac{\mu^2}{2}\right)$$

$$\mu^2 = 1.17$$

$$\mu = 1.08$$

5.16. A 320 W carrier is simultaneously modulated by two audio waves with modulation % of 45 and 60 respectively. What is the side band power radiated ?

AKTU 2015-16(Sem-I), Marks 02

Ans. Given, $P_c = 320$ W, $m_1 = 45$ %, $m_2 = 60$ %

$$P_c = \frac{A^2}{2} = 320$$

$$A^2 = 640$$

$$A = 25.29 \text{ V}$$

Sideband power,

$$P_{SB} = \frac{A^2}{4}\ (m_1{}^2 + m_2{}^2)$$

$$= \frac{640}{4}\ ((0.45)^2 + (0.6)^2)$$

$$= 90 \text{ W}$$

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B.Tech.
(SEM. I) ODD SEMESTER THEORY EXAMINATION, 2015-16
ELECTRONICS ENGINEERING

Time : 3 Hours **Total Marks : 100**

SECTION – A

1. Attempt **all** parts. All sections carry equal marks. Write answer of each part in short : **(2 × 10 = 20)**

a. **Explain the effect of temperature on conductivity of a semiconductor.**

Ans. Refer Q. 1.2, Page SQ–1J, Unit-1, 2 Marks Questions.

b. **Define CMRR, slew rate of Op-Amp.**

Ans. Refer Q. 3.3, Page SQ–10J, Unit-3, 2 Marks Questions.

c. **A 320 W carrier is simultaneously modulated by two audio waves with modulation % of 45 and 60 respectively. What is the side band power radiated ?**

Ans. Refer Q. 5.16, Page SQ–21J, Unit-5, 2 Marks Questions.

d. **Define signal. Name various types of signal.**

Ans. Refer Q. 5.1, Page SQ–18J, Unit-5, 2 Marks Questions.

e. **Why Si is preferred over Ge for manufacturing of electronics devices ?**

Ans. Refer Q. 1.1, Page SQ–1J, Unit-1, 2 Marks Questions.

f. **In JFET I_{DSS} = 8 mA, V_p = –4 V biased at V_{GS} = –1.8 V. Determine the value of g_m.**

Ans. Refer Q. 2.14, Page SQ–9J, Unit-2, 2 Marks Questions.

g. **Define Op-Amp and draw its block diagram.**

Ans. Refer Q. 3.1, Page SQ–10J, Unit-3, 2 Marks Questions.

h. **Explain FET as voltage variable resistor.**

Ans. Refer Q. 2.10, Page SQ–8J, Unit-2, 2 Marks Questions.

i. **Explain with proper reason the use of emitter follower.**

Ans. Refer Q. 2.5, Page SQ–7J, Unit-2, 2 Marks Questions.

j. Define depletion layer of *pn* junction diode.

Ans. Refer Q. 1.5, Page SQ–2J, Unit-1, 2 Marks Questions.

SECTION – B

2. Attempt any five questions from this section. (10 × 5 = 50)

a. Determine V_O, and draw the output waveform of the given network of Fig. 1.

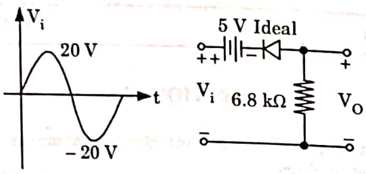

Fig. 1.

Ans. Refer Q. 1.7, Page 1–10J, Unit-1.

b. For the network of Fig. 2, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the zener diode.

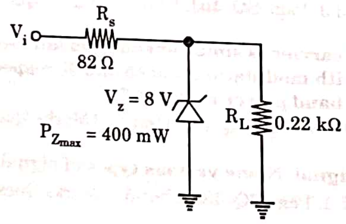

Fig. 2.

Ans. Refer Q. 1.26, Page 1–34J, Unit-1.

3. a. Sketch V_O, V_{DC} for the network of Fig. 3, and determine the peak inverse voltage of each diode.

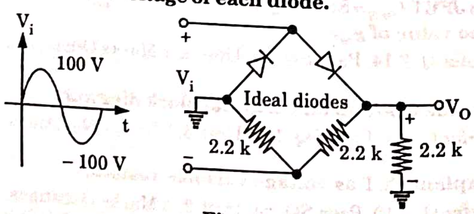

Fig. 3.

Ans. Refer Q. 1.13, Page 1–19J, Unit-1.

b. Sketch V_O for each network of Fig. 4, for the input shown.

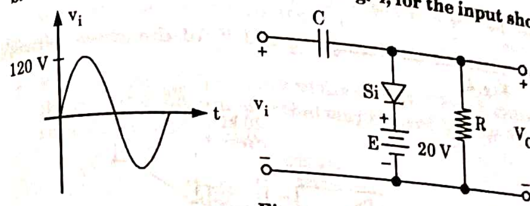

Fig. 4.

Ans. Refer Q. 1.17, Page 1–26J, Unit-1.

4. Explain with the help of necessary diagram :

a. Inverting Amplifier

b. Integrator

c. Differential amplifier in two modes of operation.

Ans. Refer Q. 3.12, Page 3–13J, Unit-3.

5. Define modulation. Derive the relation of total power of AM waves.

Ans. Refer Q. 5.9, Page 5–13J, Unit-5.

6. For the voltage divider configuration of Fig. 5, determine r_e, A_v, Z_{in} and Z_O.

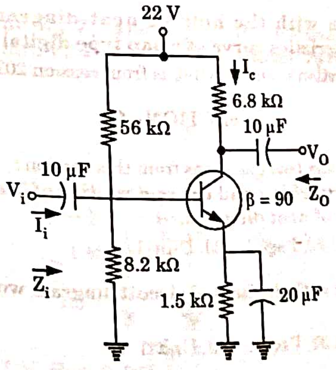

Fig. 5.

Ans. Refer Q. 2.12, Page 2–15J, Unit-2.

7. a. Determine the output voltage of an Op-Amp for input voltages of V_{i1} = 200 V and V_{i2} = 140 V. The amplifier has a differential gain of A_d = 6000 and the value of CMRR is :

i. 200

ii. 10^5

Ans. Refer Q. 3.14, Page 3–16J, Unit-3.

b. Find out the voltage V_2 and V_3 of the given network of Fig. 6.

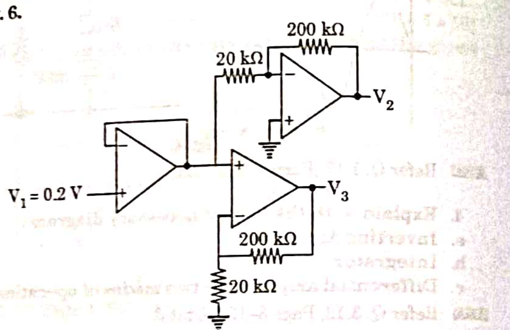

Fig. 6.

Ans. Refer Q. 3.9, Page 3–11J, Unit-3.

8. **With the help of neat block diagram explain the working of a CRO.**

Ans. This question is out of syllabus from session 2020-21.

9. **Explain with the help of neat diagram working and characteristics curve of ramp type digital voltmeter.**

Ans. This question is out of syllabus from session 2020-21.

SECTION – C

3. Attempt any two questions from this section : (15 × 2 = 30)

10. a. **Explain working and characteristics of Tunnel diode with the help of neat diagram.**

Ans. Refer Q. 1.32, Page 1–42J, Unit-1.

b. **Describe with the help of circuit diagram working of voltage tripler.**

Ans. Refer Q. 1.27, Page 1–34J, Unit-1.

c. **Differentiate between half wave and full wave rectifiers.**

Ans. Refer Q. 1.12, Page 1–18J, Unit-1.

11. a. **Explain construction, working and characteristics of p-channel Enhancement MOSFET.**

Ans. Refer Q. 2.23, Page 2–33J, Unit-2.

b. **Draw and explain the input and output characteristics of common emitter configuration.**

Ans. Refer Q. 2.7, Page 2–9J, Unit-2.

c. **For an input of V_I = 50 mV in the circuit of Fig. 7, determine the maximum frequency that may be used. The op-amp slew rate SR = 0.4 V/s.**

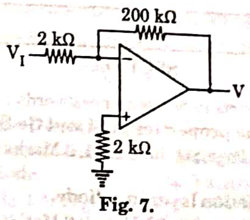

Fig. 7.

Ans. Refer Q. 3.15, Page 3–17J, Unit-3.

12. a. **Explain the need of modulation in communication system.**

Ans. Refer Q. 5.6, Page 5–9J, Unit-5.

b. **A 460 W carrier is modulated to a depth of 65 percent. Calculate the total power in the modulated wave.**

Ans. Refer Q. 5.14, Page 5–18J, Unit-5.

c. **Determine Z_i, Z_O and A_v for the network of Fig. 8, if I_{DSS} = 12 mA, V_P = – 6 V, and Y_{OS} = 40 micro Siemen.**

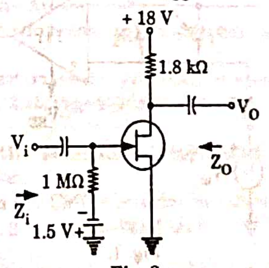

Fig. 8.

Ans. Refer Q. 2.26, Page 2–36J, Unit-1.

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B.Tech.

(SEM. II) ODD SEMESTER THEORY EXAMINATION, 2015-16

ELECTRONICS ENGINEERING

Time : 3 Hours **Max. Marks : 100**

SECTION-A

1. Answer **all** parts in few sentences/words : **(2 × 10 = 20)**

a. Compare the properties of Si and Ge Semiconductors.

Ans. Refer Q. 1.2, Page SQ–1J, Unit-1, 2 Marks Questions.

b. Define depletion layer in a diode.

Ans. Refer Q. 1.5, Page SQ–2J, Unit-1, 2 Marks Questions.

c. Define bulk resistance of the diode.

Ans. Refer Q. 1.6, Page SQ–2J, Unit-1, 2 Marks Questions.

d. Draw the double ended diode clipper circuit.

Ans. Refer Q. 1.7, Page SQ–2J, Unit-1, 2 Marks Questions.

e. Draw the output waveform that will appear across R_L.

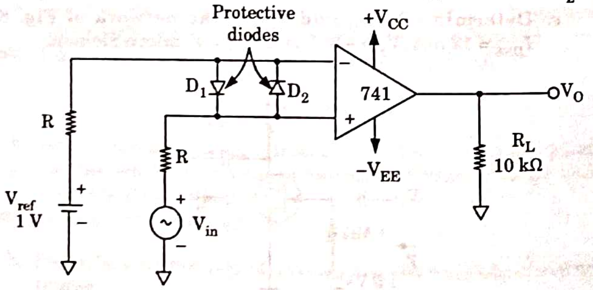

Fig. 1.

Ans. Refer Q. 3.4, Page SQ–11J, Unit-3, 2 Marks Questions.

f. Consider a constant voltage source with 10 V and series internal resistance of 100 ohm. Calculate its equivalent to a current source.

Ans. Refer Q. 1.17, Page SQ–5J, Unit-1, 2 Marks Questions.

g. Define ohmic region in FET.

Ans. Refer Q. 2.11, Page SQ–8J, Unit-2, 2 Marks Questions.

h. If α of a transistor changes from 0.981 to 0.987, find the percentage change in β.

Ans. Refer Q. 2.15, Page SQ–9J, Unit-2, 2 Marks Questions.

i. Why triggering circuit is needed in CRO ?

Ans. This question is out of syllabus from session 2020-21.

j. List the four specifications of unregulated power supply.

Ans. This question is out of syllabus from session 2020-21.

SECTION-B

2. Answer any **five** questions : **(10 × 5 = 50)**

a. Explain input and output characteristics of the following :

i. Zener Diode **ii. Varactor Diode**

Ans. i. Refer Q. 1.4, Page 1–6J, Unit-1.
ii. Refer Q. 1.31, Page 1–41J, Unit-1.

b. i. Explain the working of a common base circuit with its circuit diagram.

Ans. Refer Q. 2.6, Page 2–7J, Unit-2.

ii. What is a well-designed voltage divider biasing (VDB) circuit ?

Ans. This question is out of syllabus from session 2020-21.

c. i. Explain how the input impedance of an amplifier can load down the AC source ?

ii. Explain the transconductance curve of a JFET.

Ans.
i. This question is out of syllabus from session 2020-21.
ii. Refer Q. 2.15, Page 2–17J, Unit-2.

d. i. Draw the schematic diagram of self-biasing JFEFT amplifier.

ii. Explain the CMOS inverter circuit working operation.

Ans. Refer Q. 2.19, Page 2–24J, Unit-2.

e. Explain

i. Integrator circuit using Op-Amp

ii. Summing amplifier using Op-Amp

iii. Zero crossing detector using Op-Amp

Ans.
i. Refer Q. 3.7, Page 3–8J, Unit-3.
ii. Refer Q. 3.4, Page 3–6J, Unit-3.
iii. Refer Q. 3.6, Page 3–7J, Unit-3.

f. **Explain and calculate the voltage gain, input impedance and bandwidth for an inverting negative feedback amplifier.**

Ans. This question is out of syllabus from session 2020-21.

g. **Explain the characteristics of digital voltmeter system.**

Ans. This question is out of syllabus from session 2020-21.

h.
i. **Explain all oscilloscope controls with one example.**
ii. **How do you measure power supply performance ? Explain.**

Ans. This question is out of syllabus from session 2020-21.

SECTION-C

Note : Answer any two questions of the following : **(15 × 2 = 30)**

3. i. For a half wave rectifier, derive an expression for ripple factor.

ii. Explain the function of the circuit of Fig. 2 and draw the output waveform.

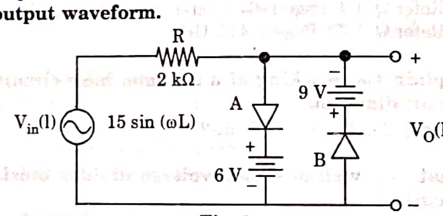

Fig. 2.

Ans.
i. Refer Q. 1.11, Page 1–15J, Unit-1.
ii. Refer Q. 1.21, Page 1–30J, Unit-1.

4. i. Draw the CE configuration circuit of BJT and explain its input and output characteristics.

ii. Describe the working operation of enhancement mode and depletion mode MOSFET. Also derive an expression for g_m of JFET configuration.

Ans.
i. Refer Q. 2.7, Page 2–9J, Unit-2.
ii. Refer Q. 2.22, Page 2–30J, Unit-2.

5. i. Draw the block diagram and equivalent circuit of an Op-Amp. Explain ideal characteristics of an Op-Amp.

ii. Explain briefly functions of the following blocks in CRO :
a. Deflection amplifier
b. Cathode Ray Tube

Ans.
i. Refer Q. 3.2, Page 3–3J, Unit-3.
ii. This question is out of syllabus from session 2020-21.

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B.Tech.
(SEM. I) ODD SEMESTER THEORY EXAMINATION, 2016-17
BASIC ELECTRONICS

Time : 3 Hours **Total Marks : 100**

Section-A

1. Attempt **all** parts. All parts carry equal marks. Write answer of each part in short. **(2 × 10 = 20)**

a. **Distinguish between avalanche and zener breakdown.**

Ans. Refer Q. 1.4, SQ–1J, Unit-1, 2 Marks Questions.

b. **Calculate the dynamic forward resistance of *p-n* junction diode when applied voltage is 0.80 V at temperature of 43 degree Celsius and reverse saturation current is 8 microampere ?**

Ans. Refer Q. 1.15, Page SQ–4J, Unit-1, 2 Marks Questions.

c. **Explain the principle of operation of LED.**

Ans. Refer Q. 1.13, Page SQ–4J, Unit-1, 2 Marks Questions.

d. **Derive the relationship between α and β.**

Ans. Refer Q. 2.3, Page SQ–6J, Unit-2, 2 Marks Questions.

e. **The thickness of base is typically smaller than emitter and collector. Why ?**

Ans. Refer Q. 2.4, Page SQ–7J, Unit-2, 2 Marks Questions.

f. **Explain FET as voltage variable resistor.**

Ans. Refer Q. 2.10, Page SQ–8J, Unit-2, 2 Marks Questions.

g. **An operational amplifier has differential gain of 10^3 and CMRR of 80 dB, input voltage are 100 microampere and 60 microampere. Determine output voltage.**

Ans. Refer Q. 3.13, Page SQ–14J, Unit-3, 2 Marks Questions.

h. **Write the characteristics of an ideal op-amp.**

Ans. Refer Q. 3.2, Page SQ–10J, Unit-3, 2 Marks Questions.

i. **State the advantages of digital instruments over analog instruments.**

Ans. This question is out of syllabus from session 2020-21.

j. Give advantages of FM over AM.

Ans. Refer Q. 5.8, Page SQ–19J, Unit-5, 2 Marks Questions.

Section-B

Attempt any **five** questions from this section **(10 × 5 = 50)**

2. a. Explain the *V-I* characteristic of *p-n* junction diode. Draw well labelled characteristic.

Ans. Refer Q. 1.2, Page 1–3J, Unit-1.

b. Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveform.

Ans. Refer Q. 1.10, Page 1–12J, Unit-1.

3. a. For the given clamper circuit shown in Fig. 1, determine the output voltage and also draw the waveform of output signal.

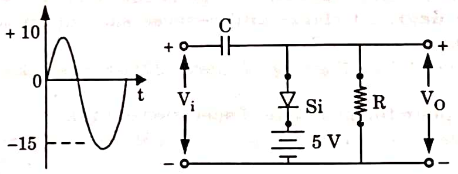

Fig. 1.

Ans. Refer Q. 1.22, Page 1–30J, Unit-1.

b. Explain the *V-I* characteristic of tunnel diode.

Ans. Refer Q. 1.32, Page 1–42J, Unit-1.

4. a. Draw the circuit diagram of BJT in CE configuration. Draw output characteristic curves and indicate the different regions of operation.

Ans. Refer Q. 2.7, Page 2–9J, Unit-2.

b. An *npn* transistor with $\beta = 98$ is operated in the CB configuration, if the emitter current is 2 mA and reverse saturation current is 12 μA. What are the base and collector current ?

Ans. Refer Q. 2.10, Page 2–14J, Unit-2.

5. a. Why is transistor biasing required ? Describe collector to base biasing in CE *n-p-n* transistor circuit.

Ans. Refer Q. 2.7, Page 2–9J, Unit-2.

b. Explain various current components in *n-p-n* transistor with help of suitable diagram.

Ans. Refer Q. 2.3, Page 2–4J, Unit-2.

6. a. Draw the circuit and explain the drain characteristic for *N*-channel JFET.

Ans. Refer Q. 2.15, Page 2–18J, Unit-2.

b. Describe the construction and basic connection of depletion MOSFET.

Ans. Refer Q. 2.20, Page 2–26J, Unit-2.

7. a. Draw the circuit diagram of an integrator using Op-Amp and explain its working.

Ans. Refer Q. 3.7, Page 3–8J, Unit-3.

b. Design and draw an inverting amplifier using Op-Amp with a gain of – 5 and R_i = 10 kΩ.

Ans. Refer Q. 3.10, Page 3–11J, Unit-3.

8. a. Explain how unknown signal frequency is measured using CRO ?

Ans. This question is out of syllabus from session 2020-21.

b. Explain the basic principle of a digital multimeter.

Ans. This question is out of syllabus from session 2020-21.

9. Define amplitude modulation. Derive the expression for AM modulated waveform. Define modulation index of AM.

Ans. Refer Q. 5.8, Page 5–11J, Unit-5.

Section - C

Attempt any **two** questions from this section. **(15 × 2 = 30)**

10. a. For the circuit shown in Fig. 4, determine I_1, I_2, I_3, I_4, V_O.

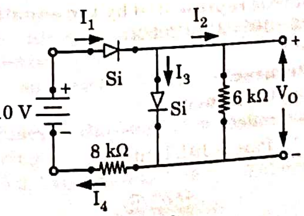

Fig. 2.

Ans. Refer Q. 1.9, Page 1–11J, Unit-1.

b. **Draw and discuss voltage tripler circuit.**

Ans. Refer Q. 1.27, Page 1–34J, Unit-1.

c. **Explain principle of operation of LCD.**

Ans. Refer Q. 1.33, Page 1–45J, Unit-4.

11. a. **Discuss AC equivalent model of voltage divider biased amplifier in CE configuration.**

Ans. This question is out of syllabus from session 2020-21.

b. **For the circuit shown in Fig. 3, determine V_B, I_C, V_C. Given that β = 80, V_{BE} = 0.7 V.**

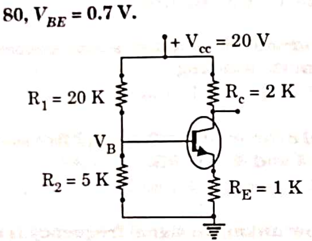

Fig. 3.

Ans. Refer Q. 2.14, Page 2–17J, Unit-2.

c. **Explain the formation of depletion region in JFET.**

Ans. Refer Q. 2.15, Page 2–18J, Unit-2.

12. a. **Draw and derive relationship for Op-Amp as closed loop non-inverting amplifier circuit.**

Ans. Refer Q. 3.3, Page 3–4J, Unit-3.

b. **A 500 W carrier is modulated to a depth of 60 %. Calculate the total power in amplitude modulated wave.**

Ans. Refer Q. 5.15, Page 5–18J, Unit-5.

c. **If a FM wave is represented by the equation :**
$V = 8 \sin(6 \times 10^8 + 3 \sin 2000t)$
Calculate :
i. **Carrier frequency**
ii. **Modulating frequency**
iii. **Modulation index.**

Ans. Refer Q. 5.17, Page 5–19J, Unit-5.

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B.Tech.

(SEM. II) EVEN SEMESTER THEORY EXAMINATION, 2016-17

BASIC ELECTRONICS

Time : 3 Hours **Total Marks : 70**

Note : Be precise in your answer. In case of numerical problem assume data wherever not provided.

SECTION-A

1. Attempt any **seven** of the following : **(2 × 7 = 14)**

a. **Classify the materials with help of energy band.**

Ans. Refer Q. 1.8, Page SQ–2J, Unit-1, 2 Marks Questions.

b. **Explain the principle of operation of LED.**

Ans. Refer Q. 1.13, Page SQ–4J, Unit-1, 2 Marks Questions.

c. **Derive the relationship between α and β.**

Ans. Refer Q. 2.3, Page SQ–6J, Unit-2, 2 Marks Questions.

d. **Why are FET called unipolar device ?**

Ans. Refer Q. 2.12, Page SQ–9J, Unit-2, 2 Marks Questions.

e. **Write down the constructional difference between depletion type and enhancement type MOSFET.**

Ans. Refer Q. 2.9, Page SQ–8J, Unit-2, 2 Marks Questions.

f. **Derive the circuit of integrator using an ideal op-amp.**

Ans. Refer Q. 3.5, Page SQ–12J, Unit-3, 2 Marks Questions.

g. **State the advantages of digital instruments over analog instruments.**

Ans. This question is out of syllabus from session 2020-21.

h. **Briefly discuss the need of modulation in communication engineering.**

Ans. Refer Q. 5.9, Page SQ–19J, Unit-5, 2 Marks Questions.

SECTION-B

2. Attempt any **five** of the following questions : **(7 × 5 = 35)**

a. Explain the *V-I* characteristic of *p-n* junction diode. How it is differ from zener diode ?

Ans. Refer Q. 1.4, Page 1–6J, Unit-1.

b. Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveforms. What is PIV of bridge rectifier ?

Ans. Refer Q. 1.11, Page 1–15J, Unit-1.

c. Draw and explain the construction and working of *p*-channel depletion type MOSFET. Also draw the characteristics of *p*-channel depletion type MOSFET.

Ans. Refer Q. 2.21, Page 2–28J, Unit-2.

d. Calculate the output voltage for the circuit of Fig. 1 with inputs of V_1 = 40 mV rms and V_2 = 20 mV rms.

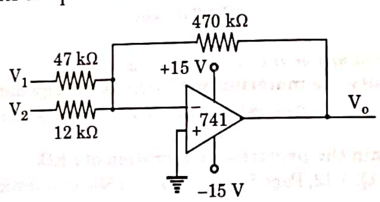

Fig. 1.

Ans. Refer Q. 3.5, Page 3–7J, Unit-3.

e. Given that I_{CQ} = 2 mA and V_{CEQ} = 10 V, determine R_1 and R_C for the network of Fig. 2.

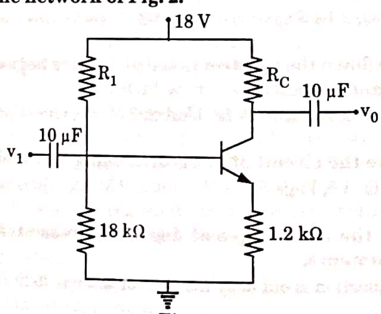

Fig. 2.

Ans. Refer Q. 2.13, Page 2–16J, Unit-2.

f. Draw and explain the block diagram of ramp type digital voltmeter. Also draw related voltage to time conversion waveforms.

Ans. This question is out of syllabus from session 2020-21.

g. Derive the expression for AM modulated waveform. Also derive the expression for modulation index.

Ans. Refer Q. 5.8, Page 5–11J, Unit-5.

h. Describe the operation of CRT with neat block diagram. How unknown frequency is measured using CRO ?

Ans. This question is out of syllabus from session 2020-21.

SECTION-C

3. Attempt any **two** of the following questions : (10.5 × 2 = 21)

a. Explain principle of operation and construction of tunnel diode. Draw its *V-I* characteristic.

Ans. Refer Q. 1.32, Page 1–42J, Unit-1.

b. Design a clamper to perform the function indicated in Fig. 3.

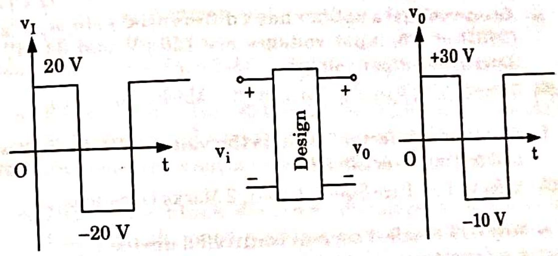

Fig. 3.

Ans. Refer Q. 1.18, Page 1–27J, Unit-1.

4. a. Draw and explain the *n*-channel JFET and draw its transfer characteristics.

Ans. Refer Q. 2.15, Page 2–17J, Unit-2.

b. Draw and explain the differential amplifier. Define CMRR and slew rate in Op-Amp.

Ans. Refer Q. 3.13, Page 3–15J, Unit-3.

5. a. Draw the CE *n-p-n* BJT characteristics. Also explain the self bias configuration in DC bias configuration.

Ans. Refer Q. 2.19, Page 2–24J, Unit-2.

b. Discuss the need of modulation in the communication engineering. Which types of modulations are used in television ?

Ans. Refer Q. 5.6, Page 5–9J, Unit-5.

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B.Tech.

(SEM. I) ODD SEMESTER THEORY EXAMINATION, 2017-18

BASIC ELECTRONICS

Time : 3 Hours **Max. Marks : 70**

Note : 1. Attempt all sections. If require any missing data; then choose suitably.

2. Any special paper specific instruction.

SECTION-A

1. Attempt all questions in brief. (2 × 7 = 14)

a. **An operational amplifier has a differential gain of 10^3 and a CMRR of 100, input voltages are 120 μV and 80 μV, and determine output voltage.**

Ans. Refer Q. 3.12, Page SQ–13J, Unit-3, 2 Marks Questions.

b. **What is ripple factor ? What is the value of RF for half wave and full wave rectifier ?**

Ans. Refer Q. 1.12, Page SQ–3J, Unit-1, 2 Marks Questions.

c. **Why BJT is called current controlled device ?**

Ans. Refer Q. 2.2, Page SQ–6J, Unit-2, 2 Marks Questions.

d. **State the advantage of digital instruments over analog instruments.**

Ans. This question is out of syllabus from session 2020-21.

e. **List of ideal characteristics of Op-Amp.**

Ans. Refer Q. 3.2, Page SQ–10J, Unit-3, 2 Marks Questions.

f. **What is modulation index ? Draw the amplitude spectrum of AM wave.**

Ans. Refer Q. 5.6, Page SQ–19J, Unit-5, 2 Marks Questions.

g. **What is trans-conductance in FET ? What is the relationship between g_m and g_{mo} ?**

Ans. Refer Q. 2.13, Page SQ–9J, Unit-2, 2 Marks Questions.

Section-B

2. Attempt any three of the following : (7 × 3 = 21)

a. **Explain the following with clear diagram :**

i. **Full wave voltage doubler**

ii. **Bridge rectifier.**

Ans.

i. Refer Q. 1.28, Page 1–36J, Unit-1.

ii. Refer Q. 1.10, Page 1–12J, Unit-1.

b. **Draw the common emitter circuit and sketch the input and output characteristics. Also explain active region, cut-off region and saturation region by indicating them on the characteristics curve.**

Ans. Refer Q. 2.7, Page 2–9J, Unit-2.

c. **Explain how op-amp can be used as**

i. **Integrator**

ii. **Inverting summer and**

iii. **Voltage follower.**

Ans. Refer Q. 3.7, Page 3–8J, Unit-3.

d. **Explain with block diagram how DMM can measure AC and DC signals and various other electrical parameters ?**

Ans. This question is out of syllabus from session 2020-21.

e. **Draw the block diagram of communication system. Calculate the percentage power saving when one side band and carrier is suppressed in an AM signal with modulation index equal to 1.**

Ans. Refer Q. 5.12, Page 5–17J, Unit-5.

SECTION-C

3. Attempt any one part of the following : (7 × 1 = 7)

1. a. **Determine the range of V_i for the Fig. 1 that will maintain the zener diode in "ON" state.**

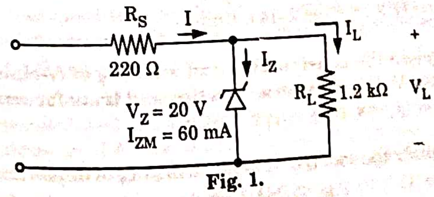

Fig. 1.

Ans. Refer Q. 1.25, Page 1–33J, Unit-1.

b. **Determine v_O for the circuit shown in Fig. 2.**

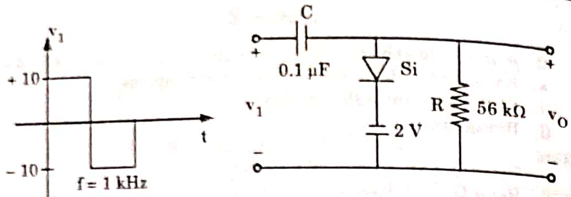

Fig. 2.

Ans. Refer Q. 1.19, Page 1–27J, Unit-1.

2. **Explain the following :**
a. **Tunnel diode**
b. **Transition capacitance and diffusion capacitance.**

Ans.
i. Refer Q. 1.32, Page 1–42J, Unit-1.
ii. This question is out of syllabus from session 2020-21.

4. Attempt any **one** part of the following : **(7 × 1 = 7)**
1. **For the network of Fig. 3**
a. **Determine R_B and R_E** b. **Find V_B, V_{CE}, and V_{BC}**

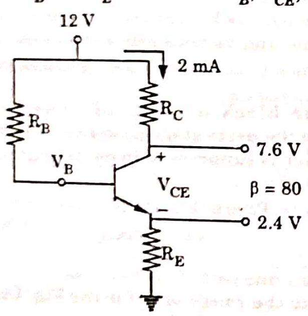

Fig. 3.

Ans. Refer Q. 2.11, Page 2–14J, Unit-2.

2. a. **Explain the construction and working of N-channel JFET. Draw the drain characteristics and transfer curve.**

Ans. Refer Q. 2.15, Page 2–17J, Unit-2.

b. **Explain the construction and working of depletion MOSFET.**

Ans. Refer Q. 2.20, Page 2–26J, Unit-2.

5. Attempt any **one** part of the following : **(7 × 1 = 7)**
1. a. **Calculate the output voltage V_0 of the circuit.**

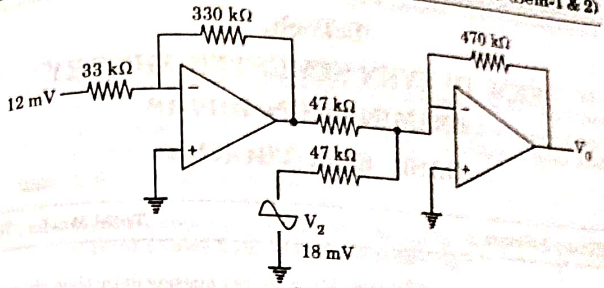

Fig. 4.

Ans. Refer Q. 3.11, Page 3–12J, Unit-3.

b. **Explain the following characteristics of an Op-Amp :**
i. **CMRR** ii. **Slew rate**

Ans. Refer Q. 3.13, Page 3–15J, Unit-3.

2. **Derive an expression for voltage gain of inverting and non-inverting ideal operational amplifier configurations.**

Ans. Refer Q. 3.3, Page 3–4J, Unit-3.

6. Attempt any **one** part of the following : **(7 × 1 = 7)**
1. **Draw and explain the block diagram of a ramp-type digital voltmeter (DVM).**

Ans. This question is out of syllabus from session 2020-21.

2. a. **Draw the general block diagram of CRO and explain each block.**

Ans. This question is out of syllabus from session 2020-21.

b. **A Lissajous pattern on an oscilloscope is stationary. It has 5 vertical tangent values and 6 horizontal tangent values. The frequency of horizontal input is 1800 Hz. Determine the frequency of vertical input.**

Ans. This question is out of syllabus from session 2020-21.

7. Attempt any **one** part of the following : **(7 × 1 = 7)**
1. **Define amplitude modulation. Derive the expression for AM modulated waveform. Define modulation index of A.M.**

Ans. Refer Q. 5.8, Page 5–11J, Unit-5.

2. **A certain AM transmitter radiates 9 kW with the carrier unmodulated and 10.125 kW when the carrier is modulated. Calculate the modulation index. If another sine wave is simultaneously transmitted with the modulation index 0.4, determine the total radiated power.**

Ans. Refer Q. 5.11, Page 5–16J, Unit-5.

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B.Tech.

(SEM. II) EVEN SEMESTER THEORY EXAMINATION, 2017-18

BASIC ELECTRONICS

Time : 3 Hours **Total Marks : 70**

Note : 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION-A

1. Attempt all question in brief : **(2 × 7 = 14)**

a. **Derive the relationship between α and β.**

Ans. Refer Q. 2.3, Page SQ–6J, Unit-2, 2 Marks Questions.

b. **The reverse saturation current of a Si *p-n* junction diode is 10 μA at 300 K. Determine the forward bias voltage to be applied to obtain diode current of 100 mA.**

Ans. Refer Q. 1.16, Page SQ–5J, Unit-1, 2 Marks Questions.

c. **A Lissajous pattern on an oscilloscope is stationary and has 4 horizontal and 3 vertical tangencies. The horizontal frequency is 50 Hz, find vertical frequency.**

Ans. This question is out of syllabus from session 2020-21.

d. **Explain the principle of operation of LED.**

Ans. Refer Q. 1.13, Page SQ–4J, Unit-1, 2 Marks Questions.

e. **Describe how FET can be used as voltage variable resistor.**

Ans. Refer Q. 2.10, Page SQ–8J, Unit-2, 2 Marks Questions.

f. **Sketch the circuit of Op-Amp as an integrator and differentiator.**

Ans. Refer Q. 3.5, Page SQ–12J, Unit-3, 2 Marks Questions.

g. **The unmodulated rms current of an AM wave is 8.93 A and it increase to 11.25 A with modulation. Determine the modulation index.**

Ans. Refer Q. 5.14, Page SQ–21J, Unit-5, 2 Marks Questions.

SECTION-B

2. Attempt any **three** of the following : **(7 × 5 = 35)**

a. **Explain the operation of full wave bridge rectifier with the help of a circuit diagram. Also sketch the input and output waveforms. Define its PIV. Also derive its ripple factor and rectification efficiency.**

Ans. Refer Q. 1.11, Page 1–15J, Unit-1.

b. **Define clipper circuit. Sketch the output waveform for the circuit shown below for given input (Fig. 1).**

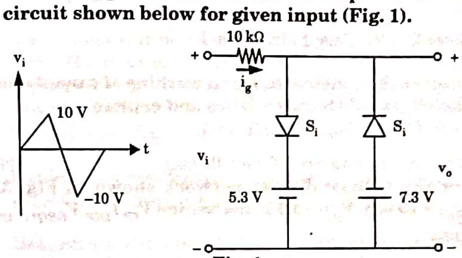

Fig. 1.

Ans. Refer Q. 1.20, Page 1–28J, Unit-1.

c. **Draw the basic structure of CB BJT and explain its principle of operation with in neat diagram along with its input and output characteristics.**

Ans. Refer Q. 2.6, Page 2–7J, Unit-2.

d. **Explain CRO with the help of diagram. How can we measure phase and frequency using CRO ?**

Ans. This question is out of syllabus from session 2020-21.

e. **Define Op-Amp with the help of block diagram. Also draw its equivalent circuit. List the ideal characteristics of Op-Amp.**

Ans. Refer Q. 3.2, Page 3–3J, Unit-3.

SECTION-C

3. Attempt any **one** of the following : **(7 × 1 = 7)**

a. i. **Find the range of R_L and I_L that will maintain a constant output of 10 V (Fig. 2).**

ii. **Also determine the maximum wattage rating of the zener diode for given circuit.**

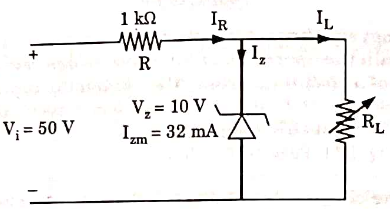

Fig. 2.

Ans. Refer Q. 1.24, Page 1–32J, Unit-1.

b. Discuss the construction and working of tunnel diode. Also sketch its I-V characteristics and explain.

Ans. Refer Q. 1.32, Page 1–42J, Unit-1.

4. Attempt any one part of the following : **(7 × 1 = 7)**

a. For the voltage divider network shown in Fig. 3. Given $I_{DSS} = 10$ mA, $V_p = -3.5$ V, determine V_G, I_{DQ}, V_{GSQ}, V_D, V_S and V_{DSQ}.

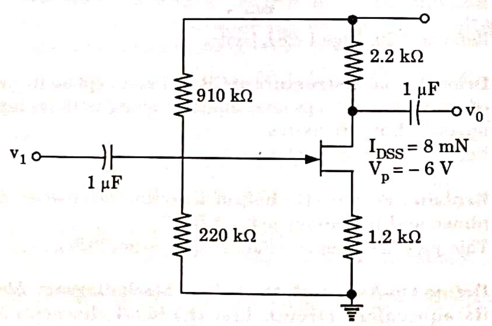

Fig. 3.

Ans. Refer Q. 2.27, Page 2–37J, Unit-2.

b. Determine the output waveform for the given network as shown in Fig. 4. Determine the output DC level and compute PIV for each diode.

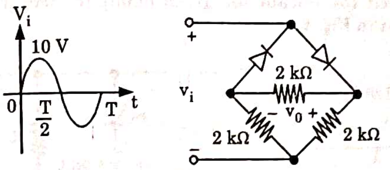

Fig. 4.

Ans. Refer Q. 1.14, Page 1–20J, Unit-1.

5. Attempt any one part of the following : **(7 × 1 = 7)**

a. Draw the circuit of *n*-channel depletion type MOSFET and explain its operation. Also draw its drain and transfer characteristics.

Ans. Refer Q. 2.20, Page 2–26J, Unit-2.

b. i. Explain the operation of Op-Amp as integrator.

Ans. Refer Q. 3.7, Page 3–9J, Unit-3.

ii. Determine the output voltage for given op-amp circuit as shown in Fig. 5.

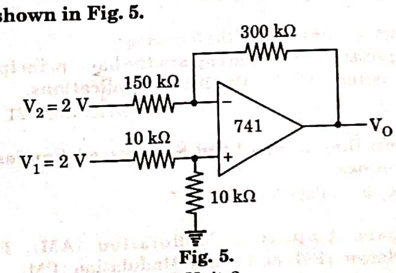

Fig. 5.

Ans. Refer Q. 3.8, Page 3–10J, Unit-3.

6. Attempt any one part of the following : **(7 × 1 = 7)**

a. i. Define Amplitude Modulation. Derive an expression for amplitude modulated wave.

Ans. Refer Q. 5.8, Page 5–11J, Unit-5.

ii. A sinusoidal carrier of 1 MHz and amplitude 100 V is amplitude modulated by a sinusoidal modulating signal of frequency 5 kHz providing 50 % modulation. Calculate the frequency and amplitude of USB and LSB.

Ans. Refer Q. 5.13, Page 5–17J, Unit-5.

b. i. Sketch the output for given clamper circuit with shown input in Fig. 6.

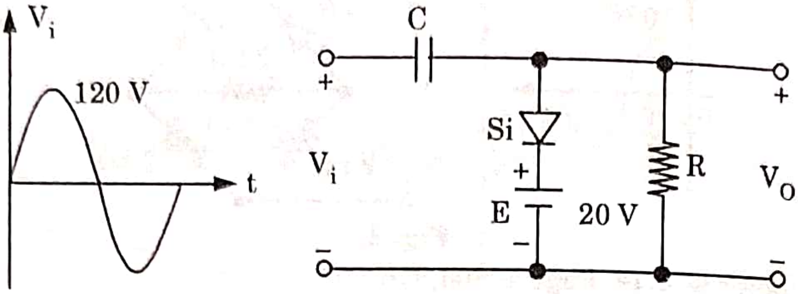

Fig. 6.

Ans. Refer Q. 1.17, Page 1–26J, Unit-1.

ii. Sketch V_O for given circuit configuration (Fig. 7).

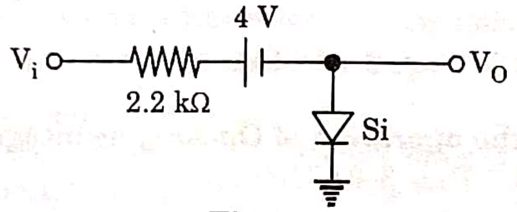

Fig. 7.

Ans. Refer Q. 1.8, Page 1–11J, Unit-1.

7. Attempt any **one** part of the following : **(7 × 1 = 7)**

a. **Using suitable diagram explain the basic principle of digital multimeter (DMM). Also list its applications.**

Ans. This question is out of syllabus from session 2020-21.

b. i. Explain Double Sideband Suppressed Carrier (DSB-SC) Techniques.

Ans. Refer Q. 5.10, Page 5–14J, Unit-5.

ii. Compare Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM).

Ans. Refer Q. 5.16, Page 5–18J, Unit-5.

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