## Assignment - 3

- 1) Inflement the following gates using 2: 1 multipleness
  - is NOT
  - ii) AND
  - iii) OR
  - III) NAND
  - in) HOR
  - V) EXOR
  - vi) EX-NOR
- 2) Implement Half Adder & Full Adder using MUX
- 3) 9 mplement Half subtractor & Full subtractor using MUX
- 4) Implement the following function with 8:1 MUX F(A,B,C,D) = TTM(1,3,5,6,11,12) + d(7,9)
- 5) gorphement X = AB+ ABC+ AC using 4:11 MUX
- 6) Implement the following function by using 4 to 1 mux and fue other gates as possible

 $f(\omega_1,\omega_2,\omega_3,\omega_4) = \overline{\omega_1}\overline{\omega_2}\overline{\omega_3}\overline{\omega_4} + \omega_1\omega_2 + \omega_1\omega_3 + \omega_1\omega_4 + \omega_2\omega_4$ 

Assume that only uncomplemented inputs w, w2, w3, w4 ore avoilable

- 7) convert the following flip flop
  - i) SR to T
  - ii) JK to SR
  - iii) JK to D
  - IV) D to T
  - V) T to SR
  - vi) T to JK
  - vii) T to D

- 8) 9 mplement 4:16 decoder using 3:8 decoder
- 9) Implement the following functions using 4:16 decoder
  - i) F, (A,B,C,D) = Em (1,2,4,7,8,11,12,13)
  - ii) F2 (A, B, C,D) = TM(10, 12, 13, 14)
  - iii) F3 (A,B,C,D) = Zm (1,5,8,10)
- 3 mplement the following functions using suitable demux & logic gates (0)

Y,=f,(A,B,C) = Em (0,1,3,5,6)

Y2= +2(A,B,C) = Zm(0,1,2,4,6)

43 = +3 (A,B, W) = Im (1,2,3,6) Draw logic diagrams

(1) Somplement the following multiple '0/8 function using f. (AB, () = \(\int(0,1,3,7) + d(2,5) suitable Deniex.

f2 (A,B,C) = Sm(1,5,7)

f3 (A,B,C) = Em(0,2,4,6)

(2) 9 mplement 1:16 demux using 1:8 demux