ModelSim Tutorial#1

Modelsim is an easy-to-use yet verstail VHDL, Verilog, SystemC simulator by Mentor Graphics. It supports behavioral, register transfer level, and gate-level modeling. ModelSim supports all platforms.

This tutorial creates an 'And gate' with VHDL and tests it. The VHDL file is already given to you named 'and_gate'.

N.B.: The following steps are only one way of many possible ways to make a hardware design, feel free to use other steps that are easier to you.

1 Download

You can download a free edition from one of the following links

- `http://fpgasoftware.intel.com/16.0/?product=modelsim_ae#tabs-2` install starter edition.
- `https://www.mentor.com/company/higher_ed/modelsim-student-edition`

2 Create Project

1. From Menu, File → New → project.
2. Write a Name for your Project, and remember the location you saved it in. Fig.1
3. The Library is where all the compiled designs are saved, its default name is work. Fig.1
4. Make Sure Your project Tab is opened. if not, open it from Menu, View → Project. Fig.2

3 Add a new design file to the Project

1. In Project Tab Fig.2, right click and choose Add to project → New file. (or existing file if you already have one).
2. Choose File type as VHDL.
3. give the file a name "or_gate" and press ok.
4. double click on the file name in the project tab to open it.

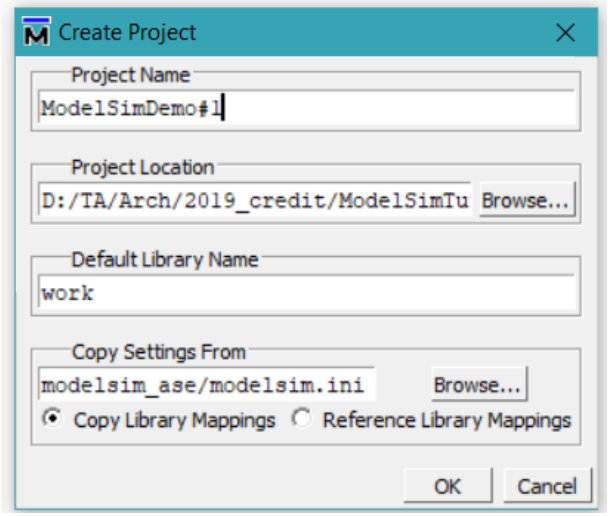

Figure 1: Create Project

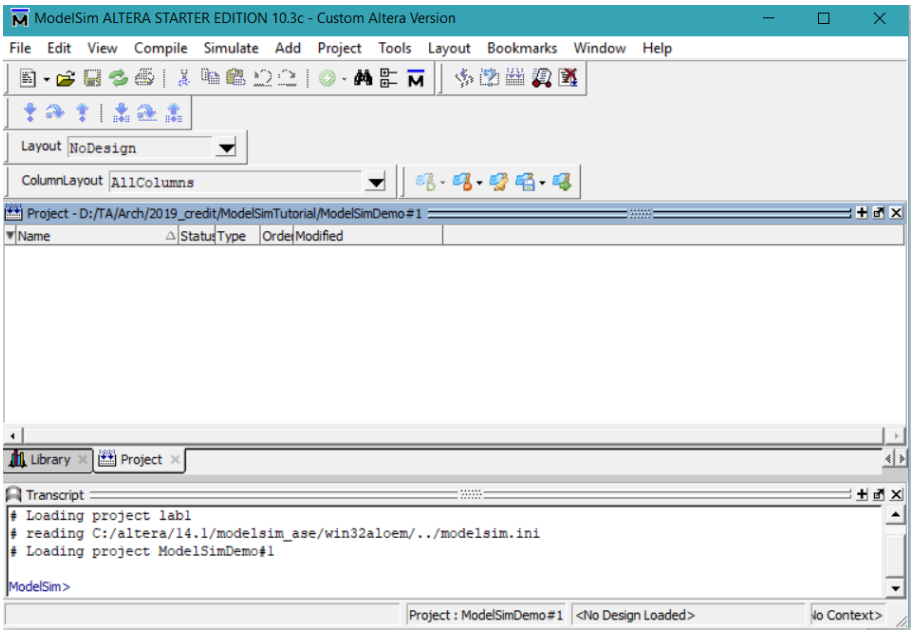

Figure 2: Create Project

4 Add an already made design file to the Project

1. In Project Tab Fig.2, right click and choose Add to project → Existing file.
2. Browse and choose “and_gate.vhd“.
3. press ok.
4. double click on the file name in the project tab to open it.

5 Compile

1. **Make Sure that the file is saved Ctrl+S**.
2. In Project Tab Fig.3, right click on the file named ‘and_gate‘ and choose compile → compile selected.
3. Alternatively you can choose it from the compile menu Fig.3.
4. Another Alternative is from the toolbar Fig.3.
5. Check the transcript to make sure no errors. (there should be one error Fig.5).
6. Double click on the error line in the transcript will open another window Fig.6. Notice the red line mentioning the file containing the error, the line number between braces and the description of the error.
7. Double click on the file name in the project tab to open it Fig.2.
8. Read the error carefully it says expected ”;” near end in line (16), that means that the previous line is missing a semicolon, check line 15 Fig.6.
9. Add a semicolon to line 15 then save the file.
10. Compile and make sure it has no further errors.

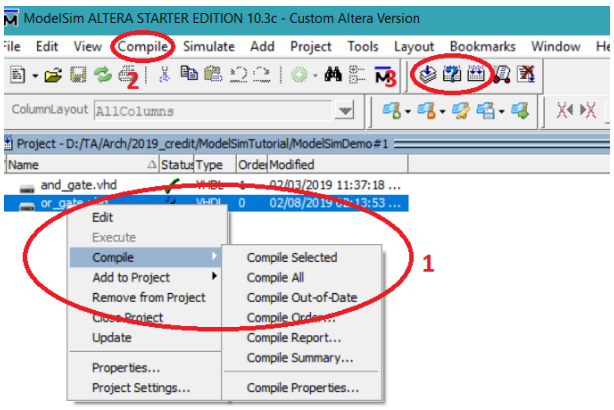

Figure 3: Compile file

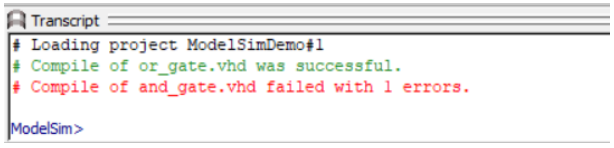

Figure 4: Transcript

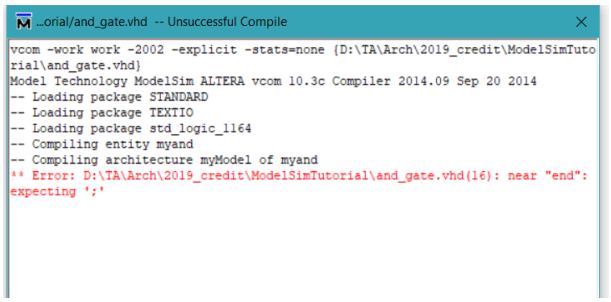

Figure 5: Check error Description

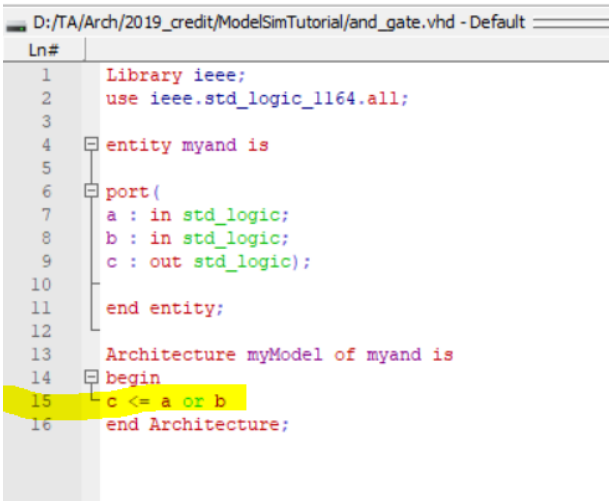

Figure 6: Edit File

6 Simulate and Save Results

1. From Menu, Simulate → Start Simulation.
2. A pop-up window will appear, expand your library ‘work‘.
3. Choose myand and press ok. (Notice that although the file is named and_gate, the design is not necessary named the same).
4. **Watch what happened in your Transcript ‘vsim -gui work.myand‘
5. A New tab will open called Objects Fig.7, if it didn’t open it from view menu.
6. Objects tab has all the inputs and outputs to your circuit. Select All of them and right click add to wave.
7. In the wave Fig.8, right click on input ‘a‘ then choose force and write value 1 then ok.
8. In the wave Fig.8, right click on input ‘b‘ then choose force and write value 1 then ok.
9. **Watch what happened in your Transcript ‘force -freeze sim:/myand/b 1 0‘
10. Don’t force anything on c, it is your output.
11. Hit the run button in the ToolBar Fig.9.
12. **Watch what happened in your Transcript ‘run‘.

13. Repeat the last two steps to try all possible values (1,1; 1,0 ; 0,1 ; 0,0).

14. Watch the wave form Fig.8, and notice that the output ‘c‘ have value 1 when a is 1 and b is 0, that means that we have an error in design.

15. Check the Design file, fix the error, Save, Compile then repeat the simulation.

16. **You can save the commands in the transcript into an external file, then copy them back to transcript to repeat the simulation. This file is called a do file

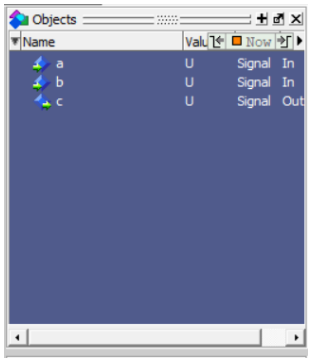

Figure 7: Object window

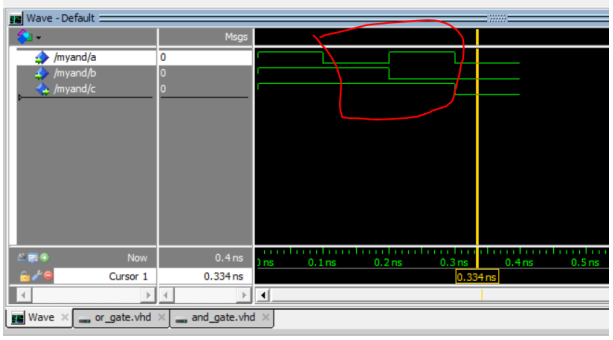

Figure 8: Wave Form

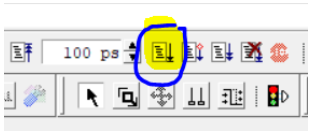

Figure 9: Run button

References

[1] Official modelsim documentation. link.