



Figure 7.61 Pipelined processor with full hazard handling

Forward to solve data hazards when possible³:

```

if ((Rs1E == RdM) & RegWriteM) & (Rs1E != 0) then
    ForwardAE = 10
else if ((Rs1E == RdW) & RegWriteW) & (Rs1E != 0) then
    ForwardAE = 01
else
    ForwardAE = 00

```

Stall when a load hazard occurs:

```

lwStall = ResultSrcE0 & ((Rs1D == RdE) | (Rs2D == RdE))
StallF = lwStall
StallD = lwStall

```

Flush when a branch is taken or a load introduces a bubble:

```

FlushD = PCSrcE
FlushE = lwStall | PCSrcE

```

³ Recall that the forwarding logic for *SrcBE* (*ForwardBE*) is identical except that it checks *Rs2E* instead of *Rs1E*.