Akram_9_29_2021_Lab_4A_4B

Wednesday, September 29, 2021

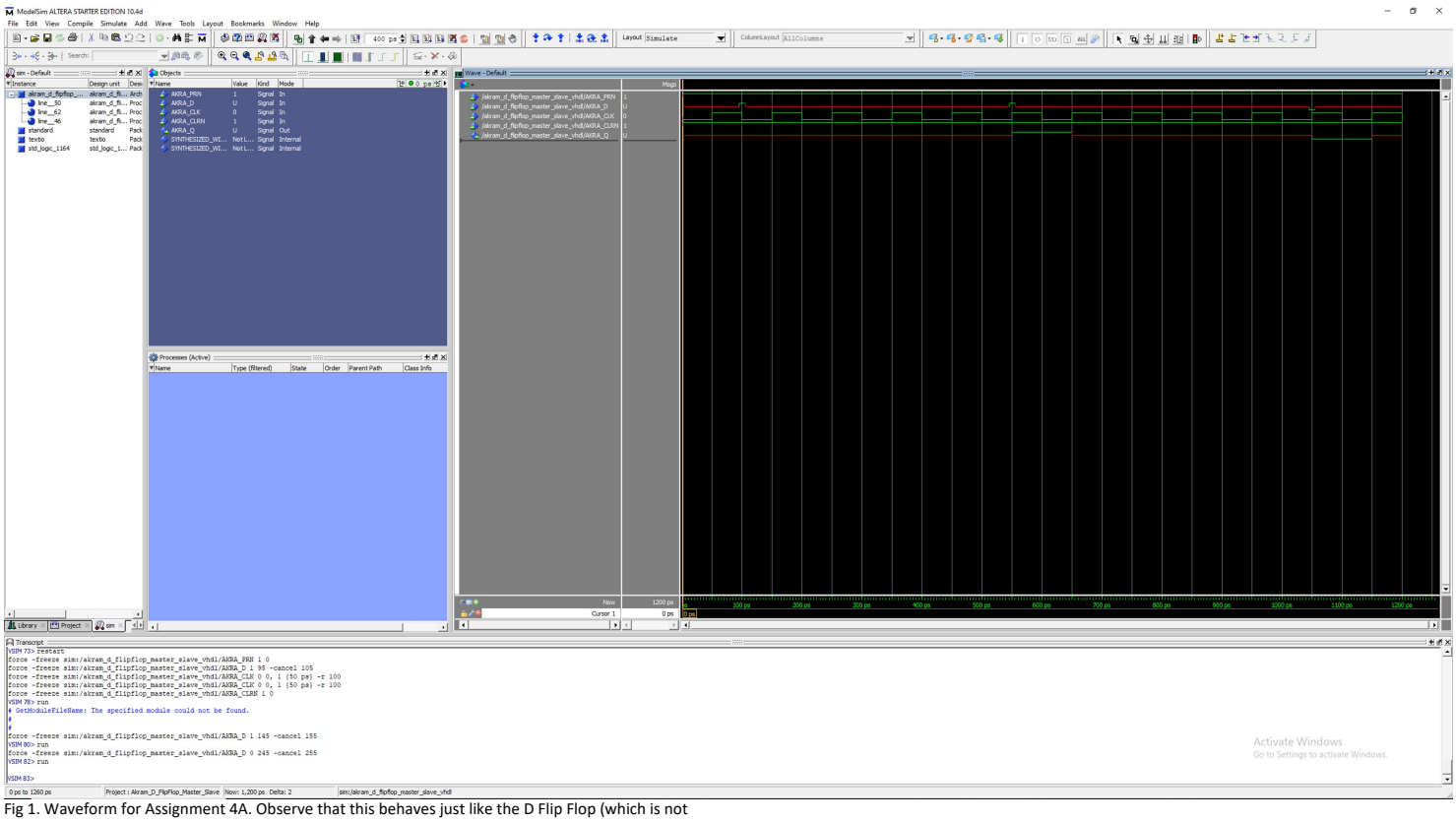

Fig 1. Waveform for Assignment 4A. Observe that this behaves just like the D Flip Flop (which is not surprising), input Q changes according to a POSITIVE-EDGE trigger and the value of D is reflected as the CLK rises from 0 to 1.

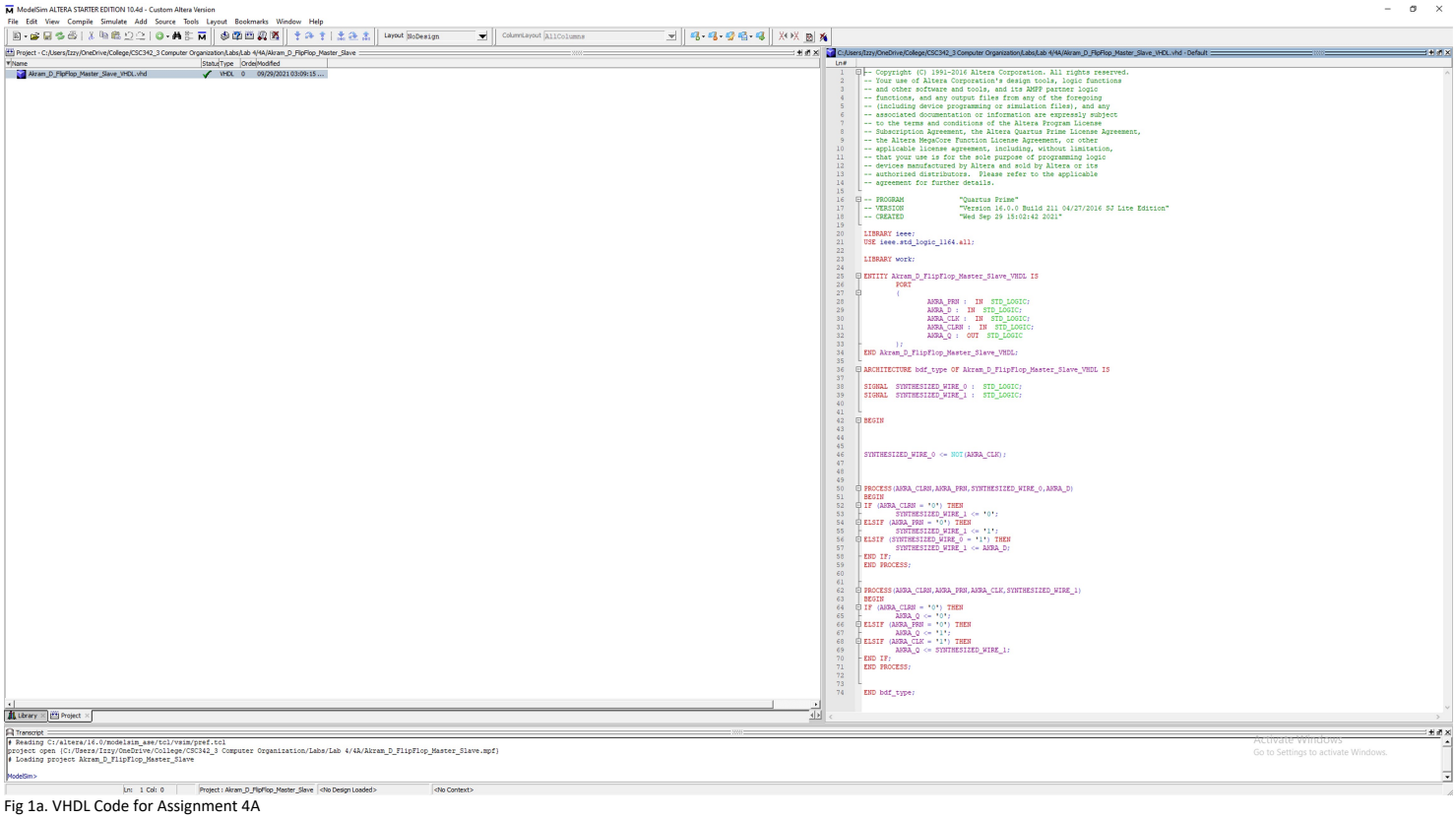

Fig 1a. VHDL Code for Assignment 4A

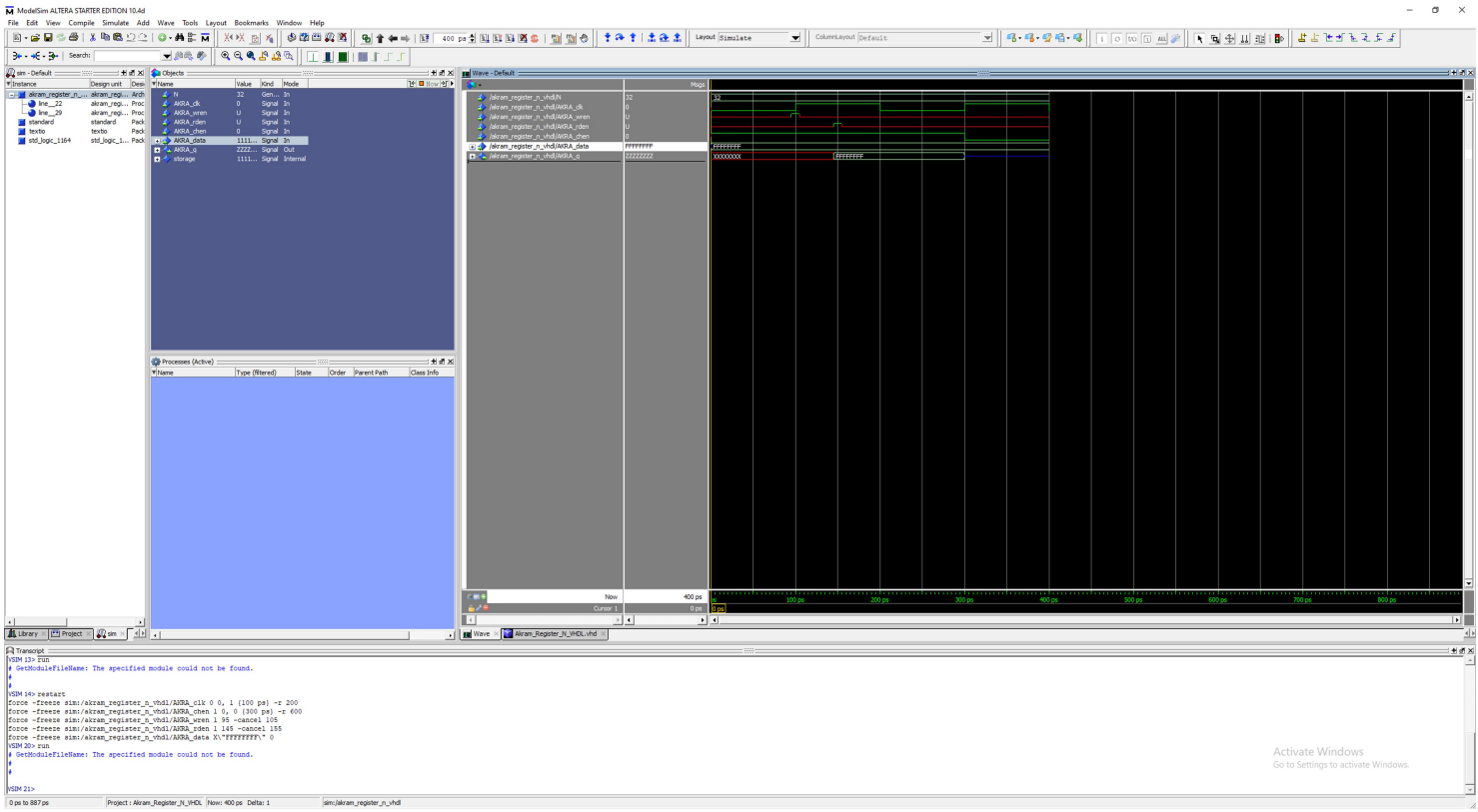

Fig 2. Waveform for Assignment 4B.
At 100 ps: wren enabled at rising edge of CLK (input data "FFFFFFFF" is stored behind the scenes),
at 150 ps: rden is enabled (now we can see that data output),
at 300 ps: chen is disabled (output is undefined).

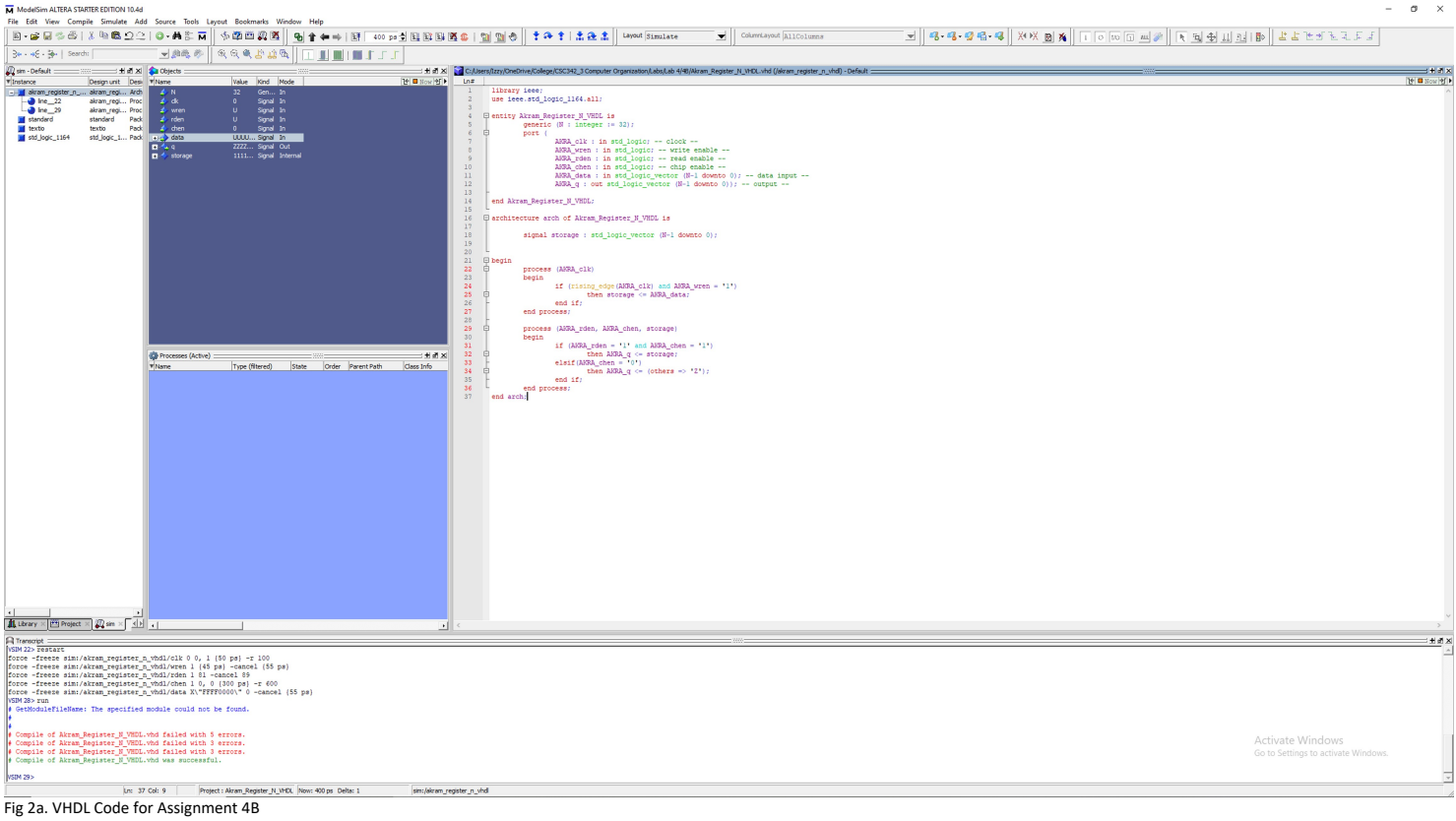

Fig 2a. VHDL Code for Assignment 4B