

Ismail Akram
CSC343 FALL2021

Wednesday, September 1, 2021 6:00 PM

CSC 343 FALL 2021

Laboratory Exercise Tutorial:

Design Entry Specified:

Schematic Diagram of digital circuits

Hardware Description Language (VHDL)

VHDL with LPM(Library Parameterized Modules)

File > Create / Update > Create HDL Design File from Current File...

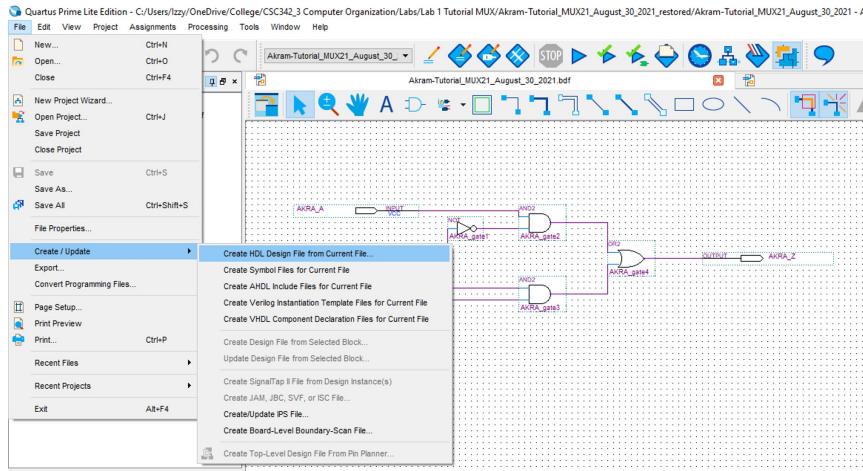


Fig 1. Creating VHDL of block diagram (2:1 MUX)

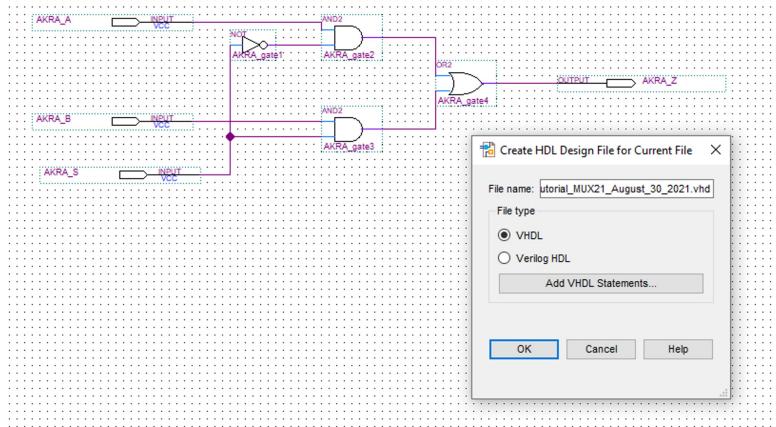


Fig 2. Creating VHDL file

File > Open > VHDL File

```
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15
16 -- PROGRAM      "Quartus Prime"
17 -- VERSION     "Version 16.0.0 Build 211 04/27/2016 SJ Lite Edition"
18 -- CREATED    "Wed Sep 01 18:04:17 2021"
19
20 LIBRARY ieee;
21 USE ieee.std_logic_1164.all;
22
23 LIBRARY work;
24
25 ENTITY Akram_Tutorial_MUX21_August_30_2021 IS
26   PORT
27   (
28     AKRA_A : IN STD_LOGIC;
29     AKRA_B : IN STD_LOGIC;
30     AKRA_S : IN STD_LOGIC;
31     AKRA_Z : OUT STD_LOGIC
32   );
33 END Akram_Tutorial_MUX21_August_30_2021;
34
35 ARCHITECTURE bdf_type OF Akram_Tutorial_MUX21_August_30_2021 IS
36
37 SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;
38 SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;
39 SIGNAL SYNTHESIZED_WIRE_2 : STD_LOGIC;
40
41 BEGIN
42
43 |
44
45 SYNTHESIZED_WIRE_0 <= NOT(AKRA_S);
46
47
48 SYNTHESIZED_WIRE_2 <= AKRA_A AND SYNTHESIZED_WIRE_0;
49
50
51 SYNTHESIZED_WIRE_1 <= AKRA_B AND AKRA_S;
52
53
54 AKRA_Z <= SYNTHESIZED_WIRE_1 OR SYNTHESIZED_WIRE_2;
55
56
57
58 END bdf_type;
```

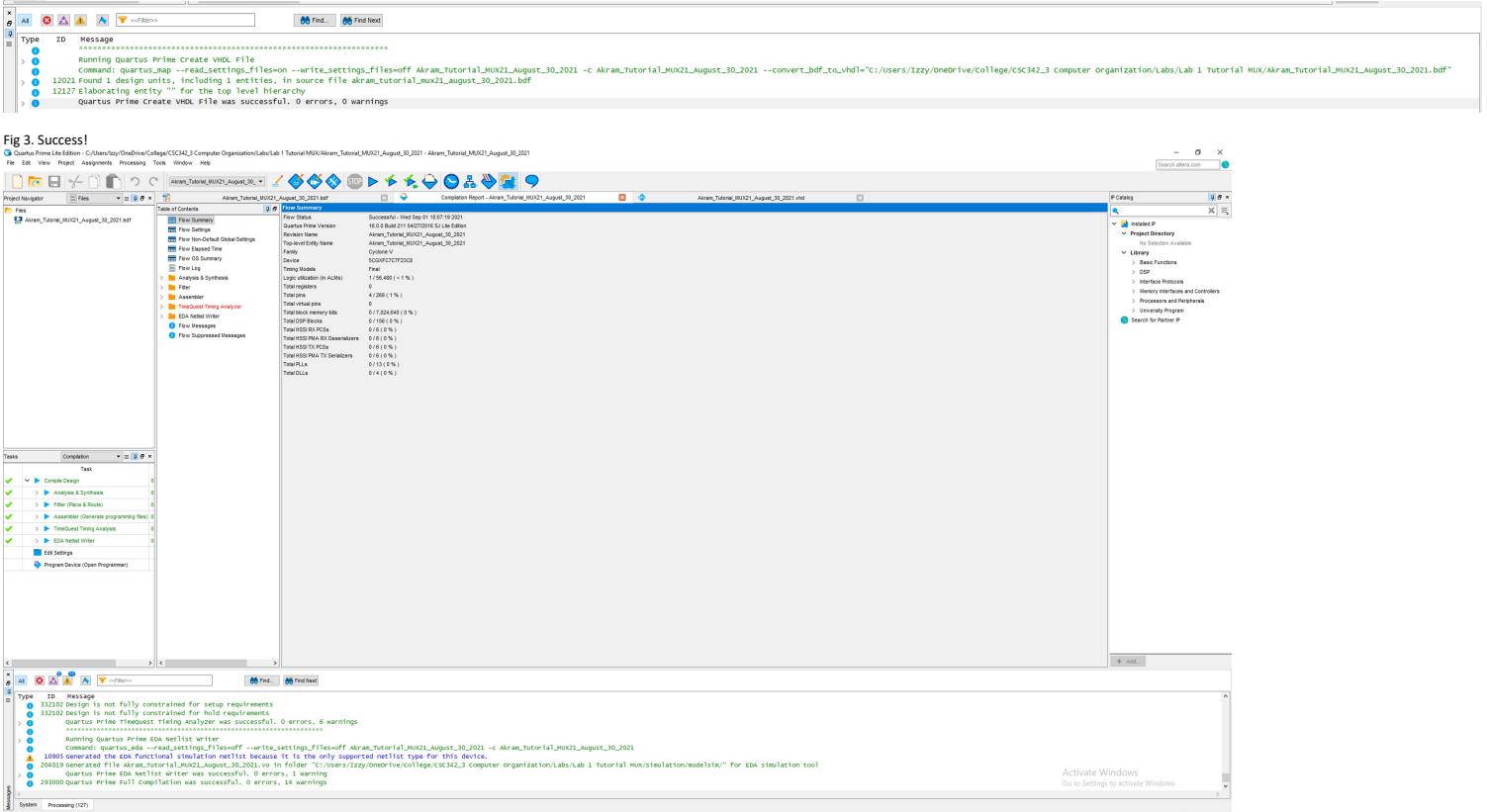


Fig 4. Compilation success

Quartus Prime Lite Edition - C:/Users/Izzy/OneDrive/College/CSC342_

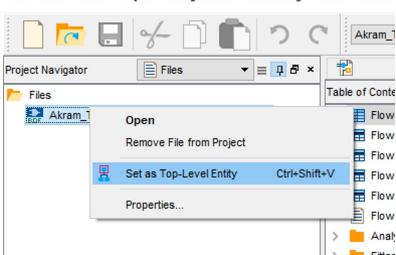


Fig 5. Setting file as top-level entry

Task 2. LPM

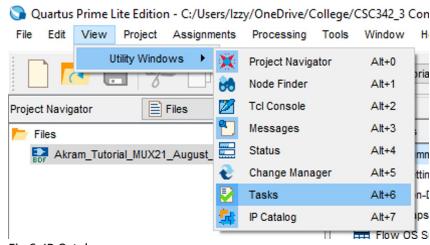


Fig 6. IP Catalog

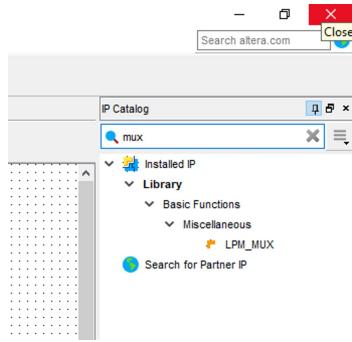


Fig 7. Searching for MUX

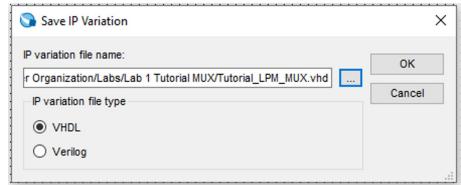
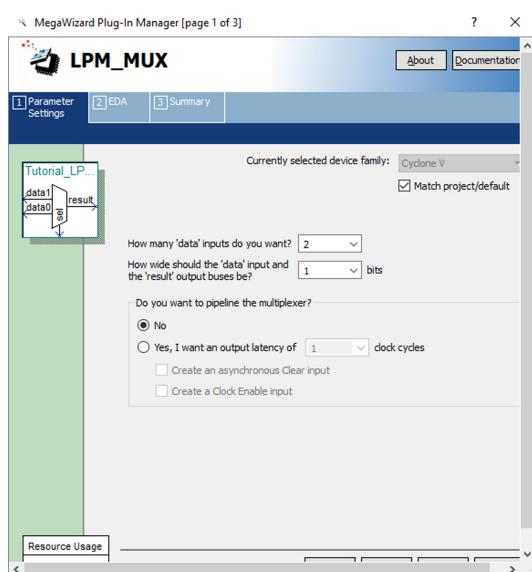


Fig 8. Saving file as Tutorial_LPM_MUX.vhd



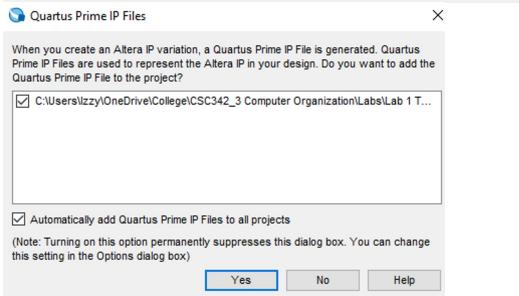
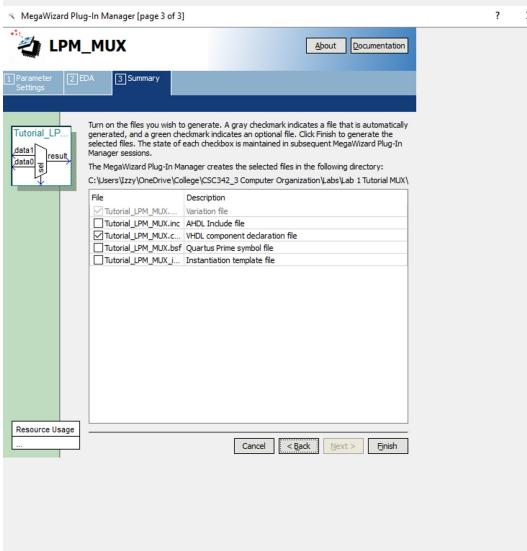
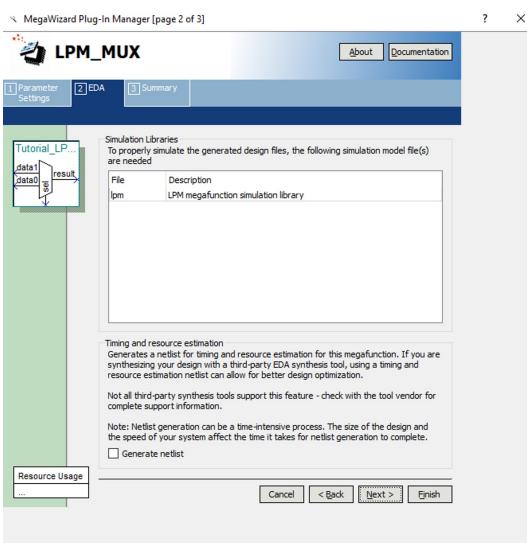


Fig 9. Creating LPM_MUX

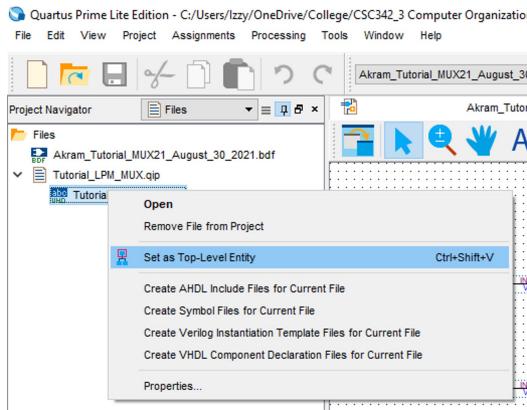


Fig 10. Setting the new MUX file as top-level entity

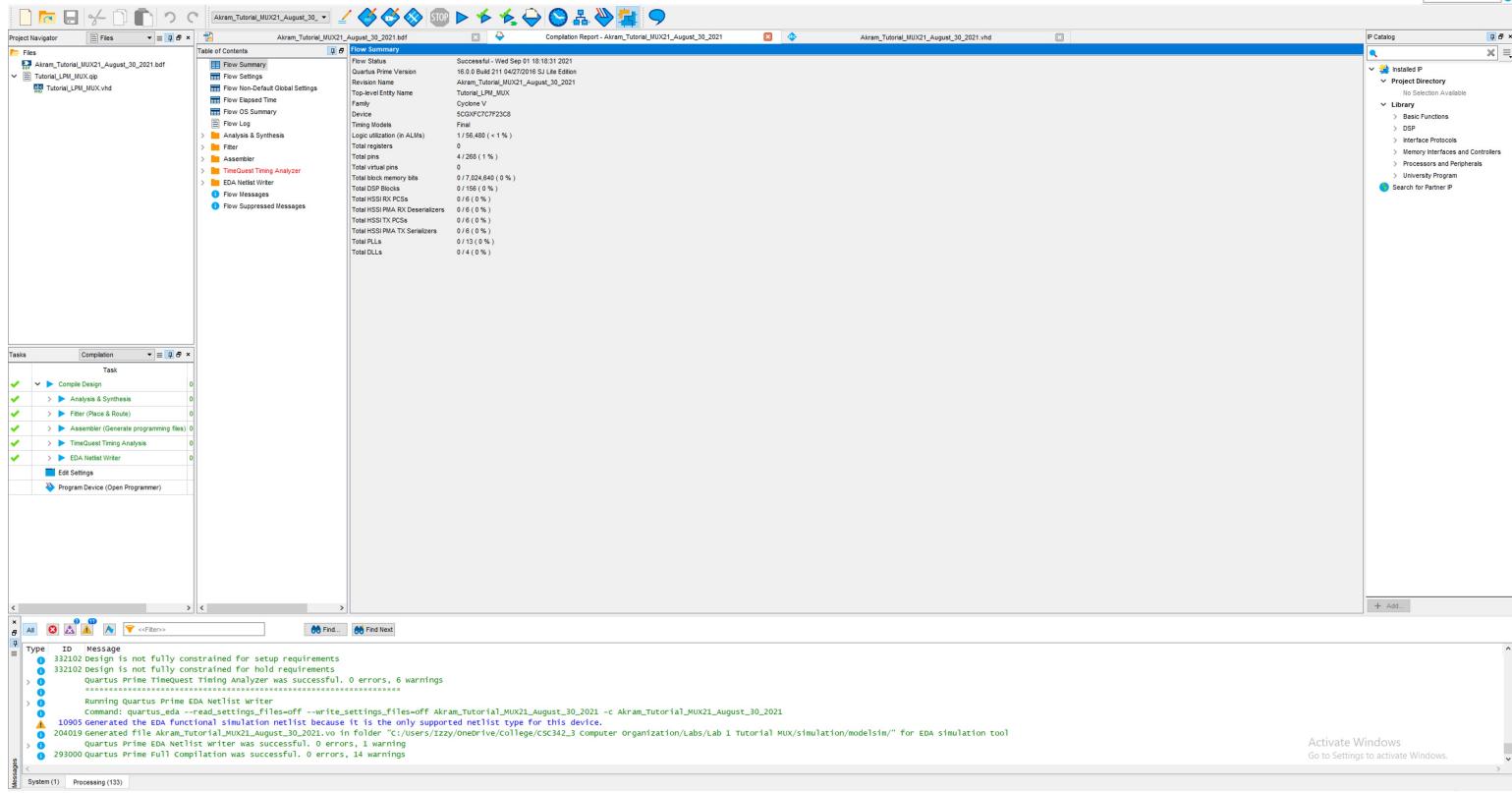


Fig 10. Compilation successful and transcript included