CSC 343, Fall 2021

Very SIMPLE Add-Sub unit with Register file (3-ported RAM)

Instructor: Professor Izidor Gertner

Screenshots with brief explanations due: OCTOBER 13, 2021, BY 6:15 PM

Report, Video, QAR file_ with README : October 17 TH, 2021, by 10:00 PMN

GRADING

I will grade based on the following:

Please SELF EVALUATE your work based on the following grading RUBRIC and submit to me in a separate file named mylast_name_my_evaluation_ grade_add_sub

A. 40 points

Shown in the waveforms windows

- Content of Register named Instruction Register -IR specify two operand registers, destination register where to store the result, and the operation code: add or sub.

The fields should be as following:

- Instruction Register Opcode Bits [26:31] = 000000 encode addition operation
- Instruction Register Opcode Bits [26:31] = 000001 encode subtraction operation

- Instruction Register Bits [21:26] = destination register index ranging from {00000} to {11111}
- Instruction Register Bits [16:20] = source register index ranging from {00000} to {11111}
- Instruction Register Bits [11:15] = source register index ranging from {00000} to {11111}
- The remaining bits in IR are set to zero.
- Show IN WAVEFORM WINDOW the corresponding registers in Register File

Show the above for three different sets of numbers.

B. 40 points

For registers RS,RT,RD 5 bit addresses have to be stored in IR register fields, and applied to register ports RA,RB,RW and shown in waveform window.

Demonstrate in waveform window addition subtraction operation from first writing event to the next writing event. Repeat the above for three different set of numbers.

C. 20 points for 2 min video presentation
D. QAR file named last_name lab title + README file that explains HOW TO VERIFY YOUR DESIGN.

NOTE: PLEASE BE HONEST. IF YOUR GRADE IS MUCH HIGHER THAN MY GRADE , I WILL REDUCE THE GRADE.