

Akram_9_29_2021_Lab_4A_4B

Wednesday, September 29, 2021

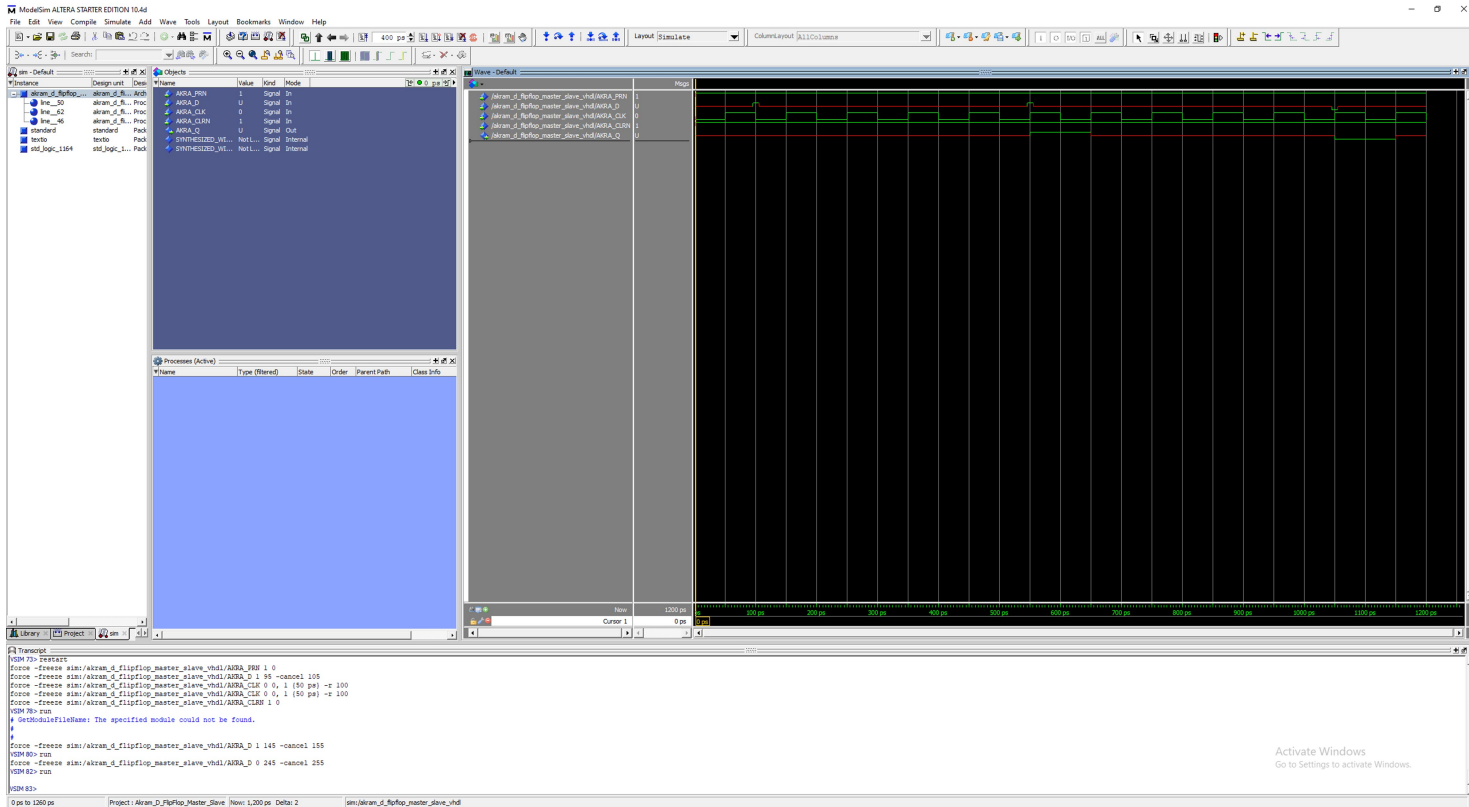


Fig 1. Waveform for Assignment 4A. Observe that this behaves just like the D Flip Flop (which is not surprising), input Q changes according to a POSITIVE-EDGE trigger and the value of D is reflected as the CLK rises from 0 to 1.

The screenshot displays the Altera Quartus Prime IDE interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, Help. Below the menu is a toolbar with various icons for project management and simulation.

The main workspace shows the source code for the file `Alram_D_FlipFlop_Master_Slave_VHDL.vhd`. The code is written in VHDL and implements a master-slave flip-flop circuit. Key components include:

- Entity Declaration:** `entity Alram_D_FlipFlop_Master_Slave_VHDL is`
- Ports:**
 - `AURA_PSR : IN STD_LOGIC;` (Asynchronous Reset)
 - `AURA_D : IN STD_LOGIC;` (Data Input)
 - `AURA_CLK : IN STD_LOGIC;` (Clock Input)
 - `AURA_CLR : IN STD_LOGIC;` (Clear Input)
 - `AURA_Q : OUT STD_LOGIC;` (Output)
- Architecture:** `architecture bdf_type of Alram_D_FlipFlop_Master_Slave_VHDL is`
- Signals:**
 - `SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;`
 - `SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;`
- Logic Implementation:**
 - Reset Logic:** A process triggered by `AURA_PSR` sets `SYNTHESIZED_WIRE_0` to '0' if the reset is active ('1').
 - Data Path Logic:** A process triggered by `AURA_CLK` updates `SYNTHESIZED_WIRE_1` based on the value of `AURA_D` when the clock edge is detected.
 - Output Assignment:** The output `AURA_Q` is assigned the value of `SYNTHESIZED_WIRE_1`.

The bottom status bar indicates the current design state: "Ln: 1 Col: 0 Project: Alram_D_FlipFlop_Master_Slave <No Design Loaded>"

Fig 1a. VHDL Code for Assignment 4A

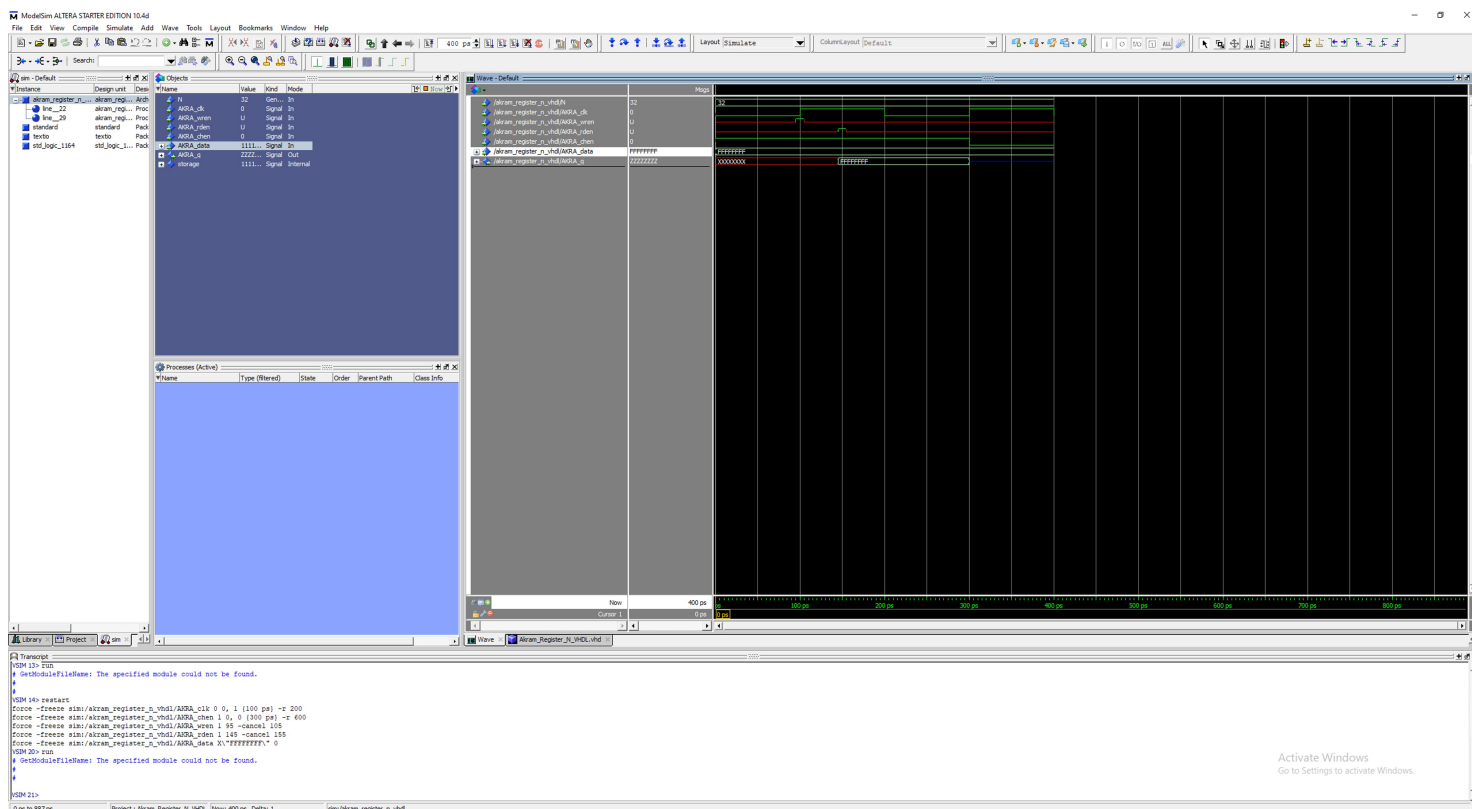


Fig 2. Waveform for Assignment 4B.

At 100 ps: wren is enabled at rising edge of CLK (input data "FFFFFFF" is stored behind the scenes),
at 150 ps: rden is enabled (now we can see that data output),
at 300 ps: chen is disabled (output is undefined).

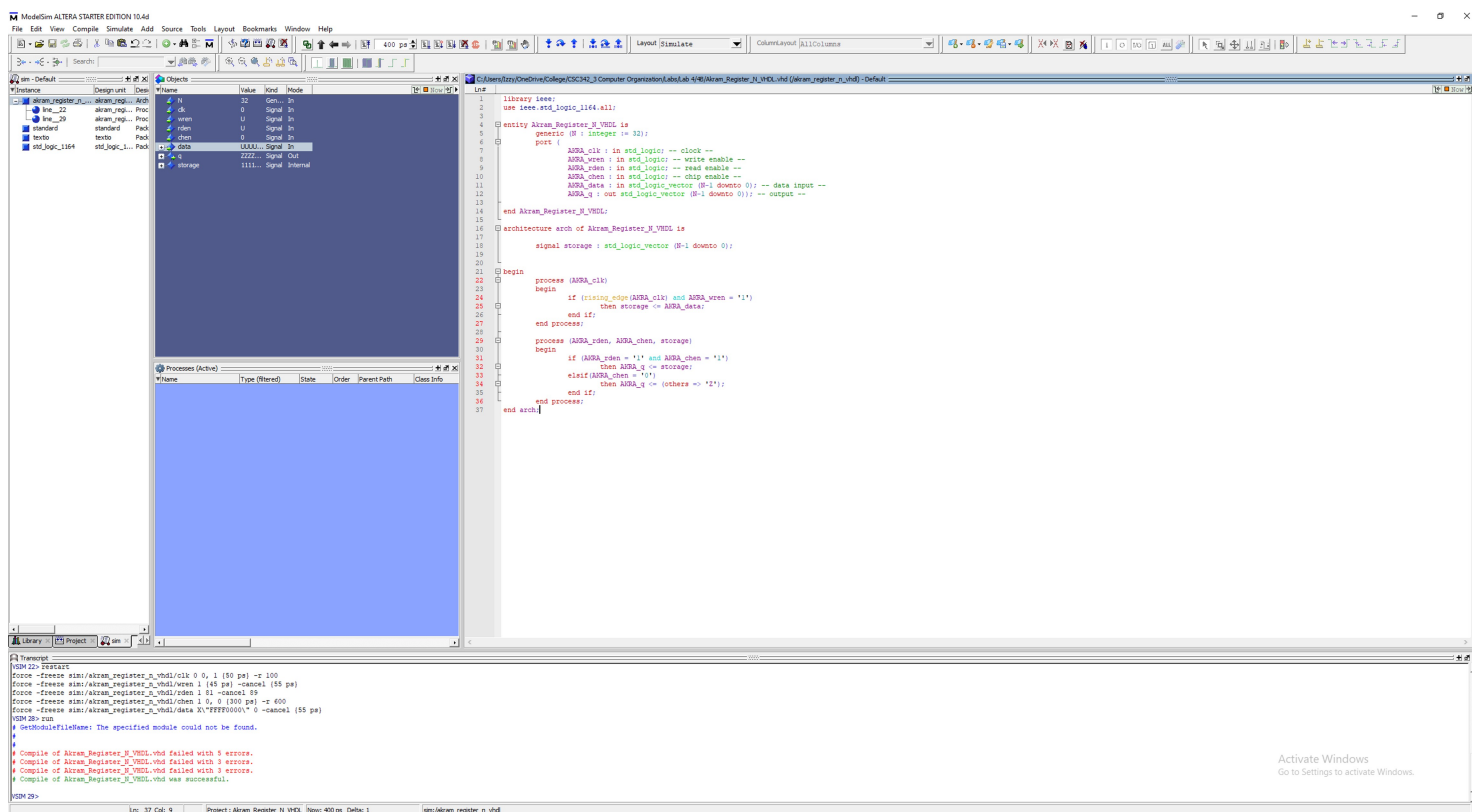


Fig 2a. VHDL Code for Assignment 4B