

Akram 10 6 2021 Memory Blocks

Wednesday, October 6, 2021 2:31 PM

1-port RAM

Quartus Prime Lite Edition - C:\Users\itz\OneDrive\College\CS343_Computer Organization\Labs\Lab 4\Memory_Blocks\Akram_10_3_2021_Lab4_Memory_Blocks - Akram_10_3_2021_Lab4_Memory_Blocks

File Edit View Project Assignment Processing Tools Window Help

Altera Quartus II

Project Navigator Files ram32x4.vhd ram32x4.hd

File ram32x4.vhd

LIBRARY ieee;
USE ieee.std_logic_1164.all;
LIBRARY altera_mf;
USE altera_mf.altera_mf_components.all;
ENTITY ram32x4 IS
PORT
(
address : IN STD_LOGIC_VECTOR(4 DOWNTO 0);
clock : IN STD_LOGIC := '1';
data : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
wein : IN STD_LOGIC;
q : OUT STD_LOGIC_VECTOR(3 DOWNTO 0)
)
END ram32x4;

ARCHITECTURE SYN OF ram32x4 IS
SIGNAL sub_wire0 : STDLOGIC_VECTOR(3 DOWNTO 0);

BEGIN
q <= sub_wire0(3 DOWNTO 0);
altsyncram_component : altsyncram
GENERIC MAP (
clock_enable_input_a => "BYPASS",
intended_device_family => "Cyclone V",
internal_address_width => "10",
input_data_width_a => "4",
numwords_a => "32",
output_data_width_a => "4",
open_drain_mode_a => "NONE",
power_up_initial_value_a => "UNREGISTERED",
read_during_write_mode_port_a => "FALSE",
read_others_during_write => "FALSE",
widthad_a => "5",
widthdata_a => "1"
)
PORT MAP (
address_a => address,
clock => clock,
data_a => data,
wein => wein,
q_a => sub_wire0
)
END SYN;

-- CNX file retrieval info
-- Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
-- Retrieval info: PRIVATE: AclAddr NUMERIC "0"
-- Retrieval info: PRIVATE: AclByte NUMERIC "0"

Task Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- TimeQuest Timing Analysis
- EDA Netlist Writer

Ed Settings

Program Device (Open Programmer)

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IP Catalog

Installed IP

Project Directory

Library

- Basic Functions
- DSP
- Interface Protocols
- Memory Interfaces and Controllers
- Processors and Peripherals

Search for Pentester IP

Fig 1. VHDL code generated of ram32x4.vhd

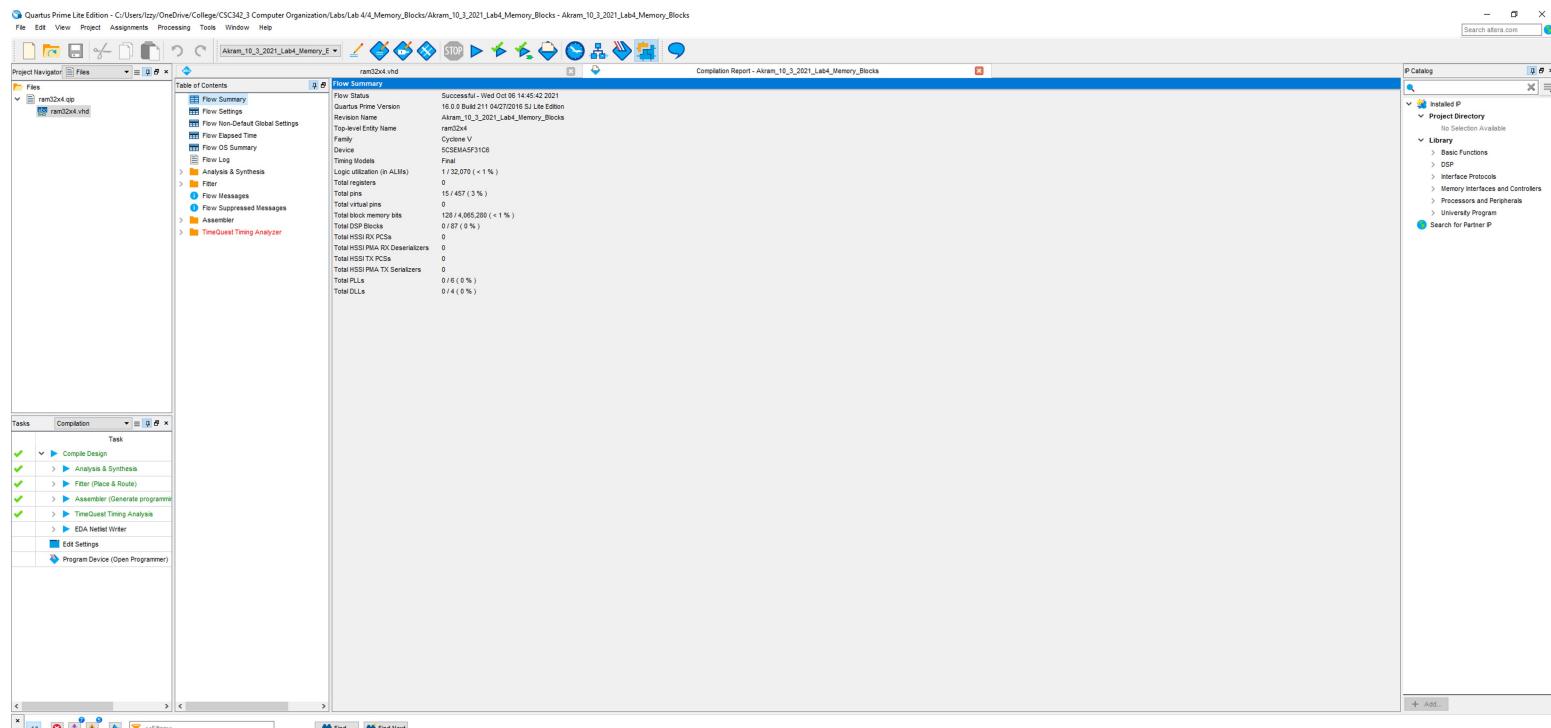


Fig 2. Consultation report showing a 429 kbit

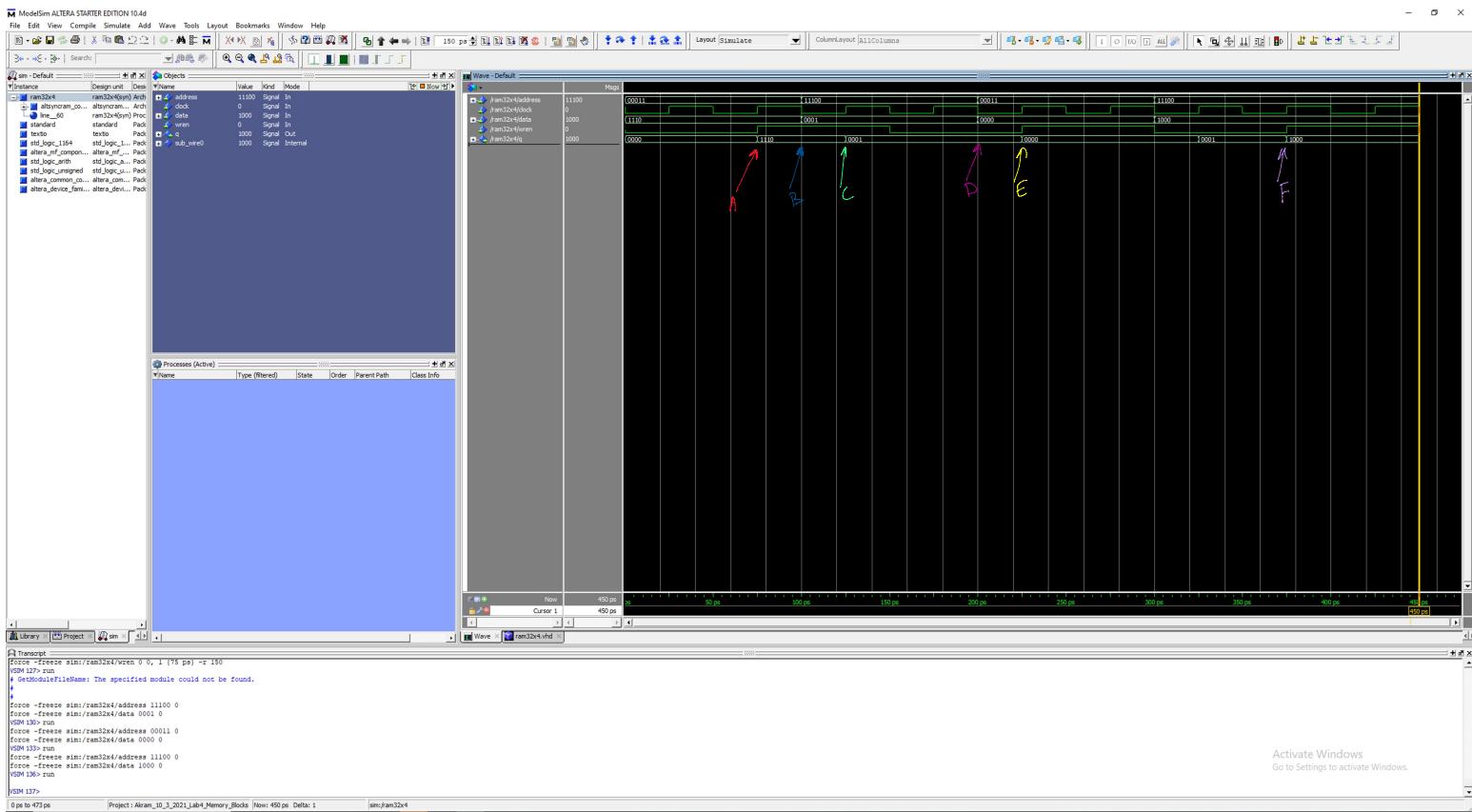


Fig 3. Waveform Simulation for ram32x4.vhd.

At **Red Arrow A**: rising edge (CLK and wren are 1) data input "1110" at is displayed at address 00011,
 At **Blue Arrow B**: address changed to 11100 and data input "0001",
 At **Green Arrow C**: output of address 11100 is displayed as "0001",
 At **Pink Arrow D**: address changed back to 00011 and data input "0000" is inputted,
 At **Yellow Arrow E**: rising edge (CLK and wren are 1) data input "0000" at is displayed at address 00011
 At **Purple Arrow F**: data output "1000" is outputted in address 11100.

2-port RAM

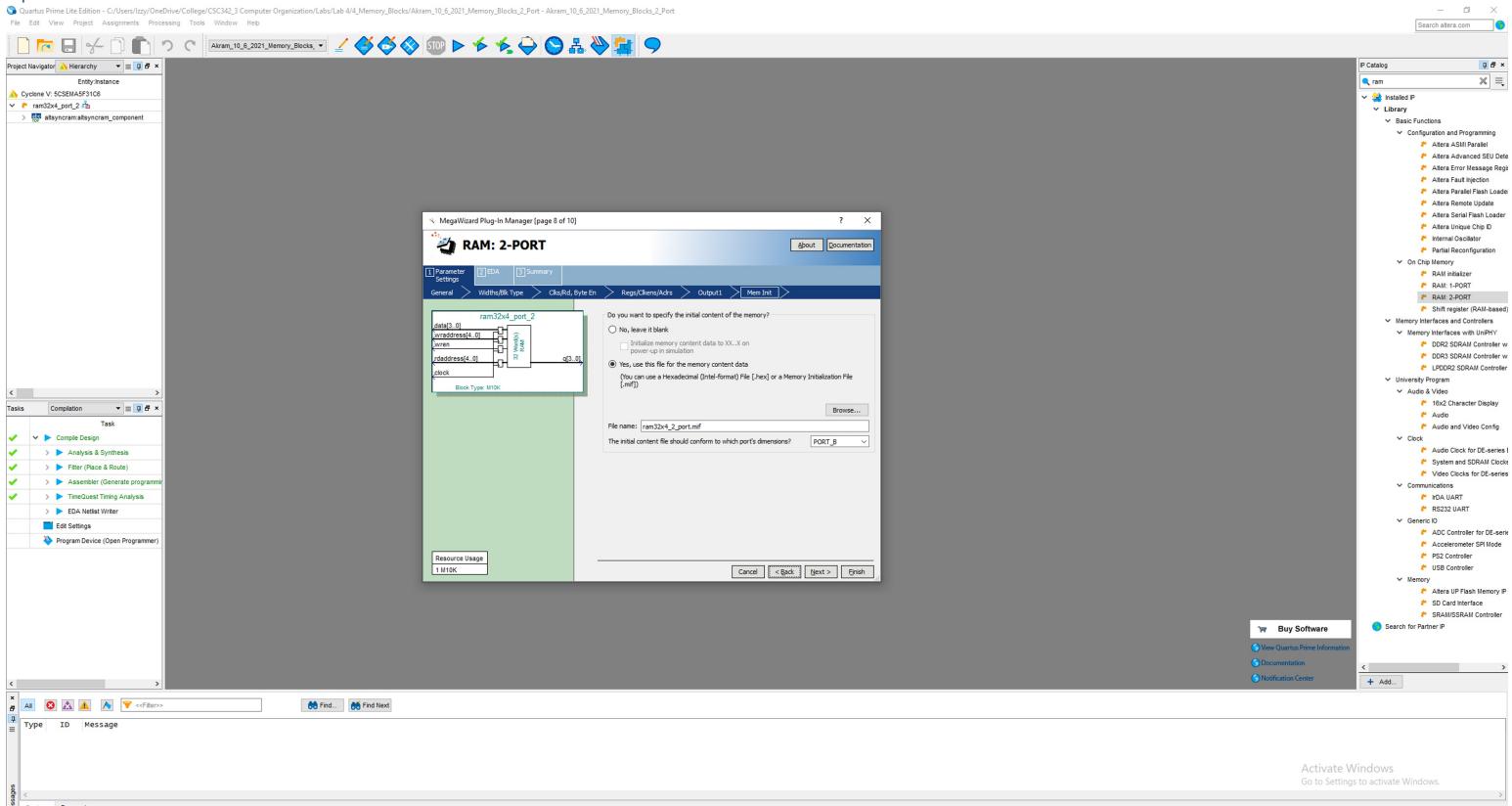


Fig 4. IP Catalogue > "RAM" > 2-Port, including .mif file

Quartus Prime Lite Edition - C:/Users/izzy/OneDrive/College/CSC342_3 Computer Organization/Labs/Lab 4/4_Memory_Blocks/Akram_10_8_2021_Memory_Blocks_2_Port - Akram_10_8_2021_Memory_Blocks_2_Port

File Edit View Project Assignments Processing Tools Window Help

Akram_10_8_2021_Memory_Blocks ram32x4_port_2.vhd

Project Navigator Files ram32x4_port_2.vhd

```

25 --(including device programming or simulation files), and any
26 --associated documentation or information are expressly subject
27 --to the terms and conditions contained in the License Agreement,
28 --Subscription Agreement, the Altera Quartus Prime License Agreement,
29 --and/or applicable license agreement, including, without limitation,
30 --your use of Altera components, devices, software, documentation, and
31 --devices manufactured by Altera Corporation and its subsidiaries.
32 --altera.com
33 --authorized distributors. Please refer to the applicable
34 --agreement for further details.
35
36
37 LIBRARY ieee;
38 USE ieee.std_logic_1164.all;
39 USE ieee.alteraw.all;
40 USE altera_mf.altera_mf_components.all;
41
42 ENTITY ram32x4_port_2 IS
43 PORT
44 (
45   clock : IN STD_LOGIC := "1";
46   address_a : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
47   rdaddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
48   wraddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
49   write_en : IN STD_LOGIC_VECTOR (0 DOWNTO 0);
50   q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
51 );
52 END ram32x4_port_2;
53
54
55 ARCHITECTURE SYN OF ram32x4_port_2 IS
56 BEGIN
57   sub_wire0 : STD_LOGIC_VECTOR (3 DOWNTO 0);
58
59   BEG
60     q <= sub_wire0(C DOWNTO 0);
61
62     altsyncram_component : altSyncram
63     GENERIC MAP
64       (
65         init_file_b => "NONE",
66         address_req_b => "CLOCK0",
67         address_a => "BYPASS",
68         clock_enable_input_a => "BYPASS",
69         clock_enable_output_b => "BYPASS",
70         data_a => "UNINITIALIZED",
71         intended_device_family => "Cyclone V",
72         latency_a => "1",
73         numwords_a => "32",
74         operation_mode => "DUAL_PORT",
75         output_a => "DATA",
76         outputdata_req_b => "UNREGISTERED",
77         power_up_uninitialized => "FALSE",
78         ram_size => "128",
79         read_during_write_mode_mixed_ports => "DONT_CARE",
80         write_a => "DATA",
81         widthad_b => "5",
82         widthad_a => "4",
83         widthb => "4",
84         widtha => "1"
85       );
86
87     PORT MAP
88       (
89         address_a => wraddress,
90         address_b => rdaddress,
91         clock_a => clock,
92         data_a => data,
93         write_en_a => write_en,
94         q_b => sub_wire0
95       );
96
97   END SYN;
98
99   END;
100

```

Tasks Compilation

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Messages

Type ID Message

Activate Windows
Go to Settings to activate Windows.

Fig 5. VHDL code for ram32x4_port_2.vhd

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File Edit View Project Assignments Processing Tools Window Help

Akram_10_8_2021_Memory_Blocks ram32x4_port_2.vhd

Project Navigator Files ram32x4_port_2.vhd

Compilation Report - Akram_10_8_2021_Memory_Blocks_2_Port

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Run Messages
- Run Suppressed Messages
- Assembler
- TimeQuest Timing Analyzer

Flow Status: Successful - Wed Oct 06 16:17:30 2021

Quartus Prime Version: 16.0 Build 211 34272016 SJ Lite Edition

Revision Name: Akram_10_8_2021_Memory_Blocks_2_Port

Top-level Entity Name: ram32x4_port_2

Family: Cyclone V

Device: 5CSEMAF310C

Timing Models: Final

Logic utilization (in ALMs): 1 / 32,070 (< 1 %)

Total registers: 0

Total flip-flops: 20 / 457 (4 %)

Total virtual pins: 20

Total block memory bits: 128 / 4,065,200 (< 1 %)

Total DSP Blocks: 0 / 87 (0 %)

Total HSPC PCAs: 0

Total HSSP RX Deserializers: 0

Total HSSP TX PCAs: 0

Total HSSP TX Serializers: 0

Total PLLs: 0 / 0 (0 %)

Total DLLs: 0 / 4 (0 %)

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Messages

Type ID Message

- 332146 Worst-case minimum pulse width slack is -2.174
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
- 293300 Quartus Prime Full compilation was successful. 0 errors, 12 warnings

Activate Windows
Go to Settings to activate Windows.

Fig 6. Compilation successful

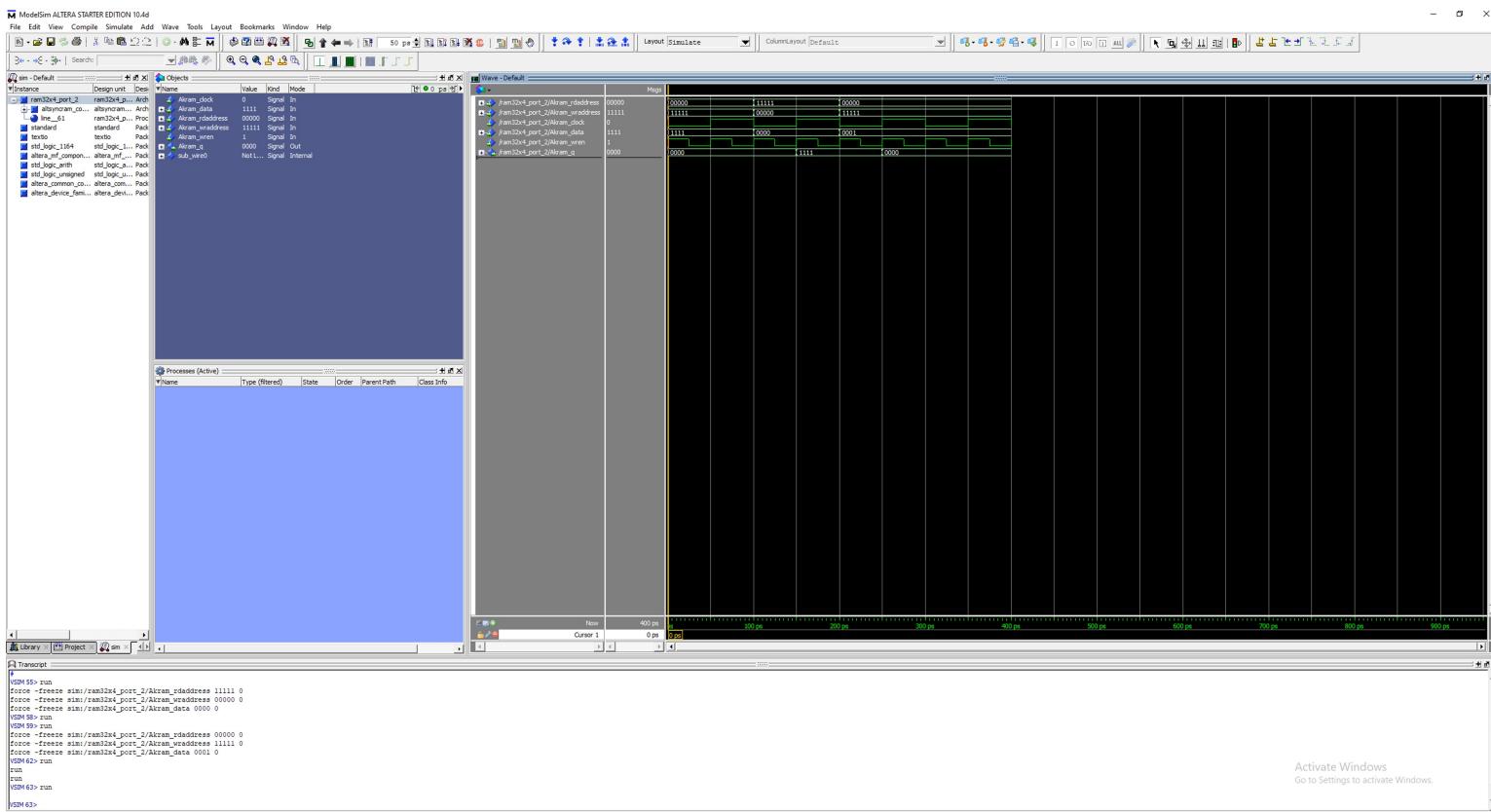


Fig 7. Waveform simulation for ram32x4_2_port
At 0 ps: read address is "00000", write address is "1111", data input "1111"
At 50 ps: wren and CLK synch rising edges, storing data input "1111"
At 100 ps: read address is "1111", write address is "00000"
At 200 ps: read address changed to "00000", write address to "1111" and output of address "00000" is displayed as "0000"
At 250 ps: wren and CLK synch rising edges, storing data input "1111" to address "1111" and output of address "00000" is displayed as "0000"

3-port

I understand the idea is to connect 2 dual-ports but I don't know how to do it, I ran out of time.