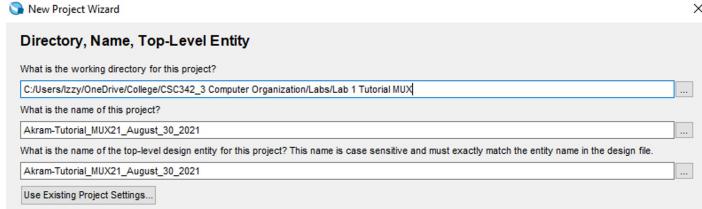


Akram-Tutorial_MUX21_August_30_2021

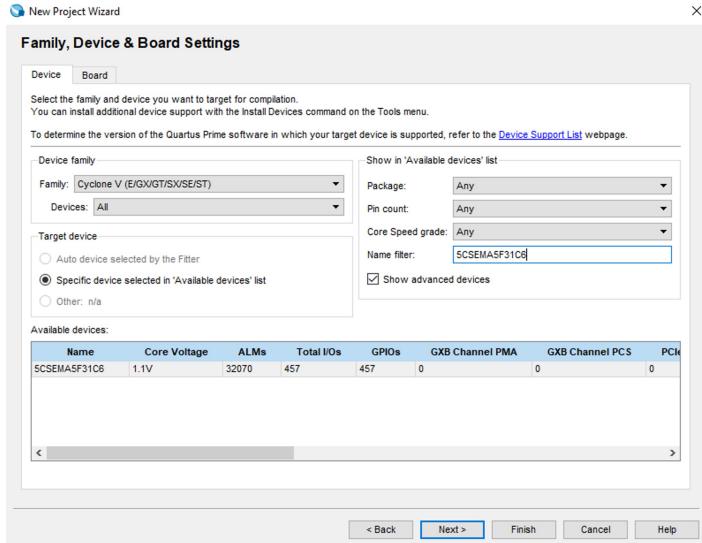
Monday, August 30, 2021 4:11 PM



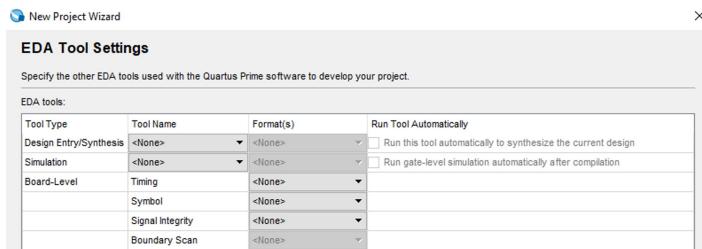
Starting a New Project in Quartus.

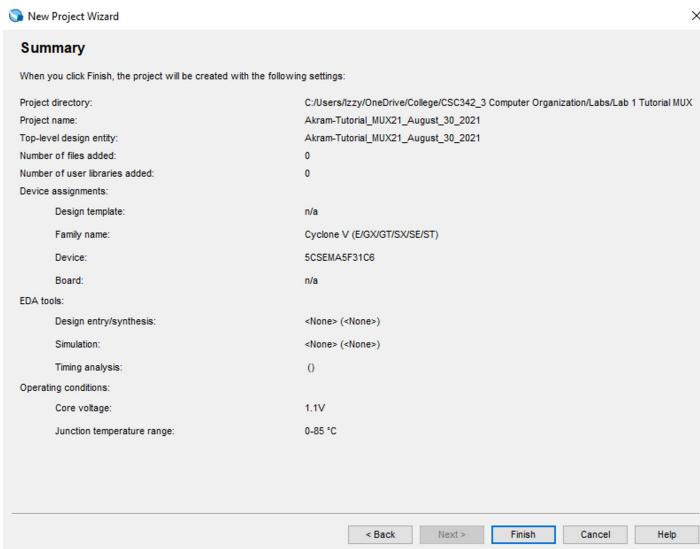


File name as Akram-Tutorial_MUX21_August_30_2021. As instructed.



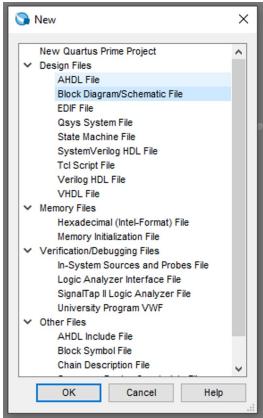
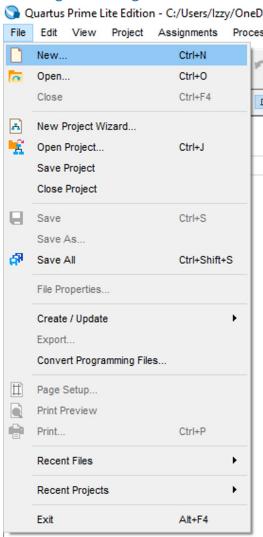
Using specified settings





Project summary

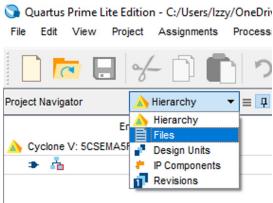
Creating block diagram

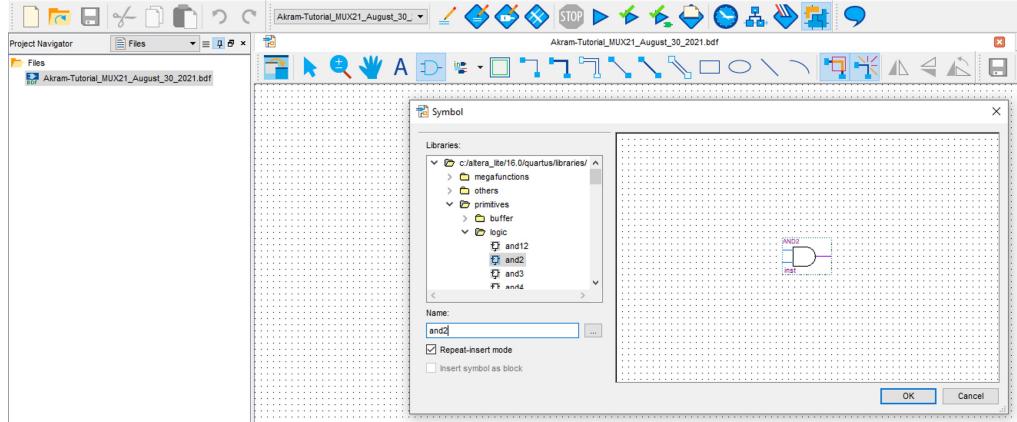
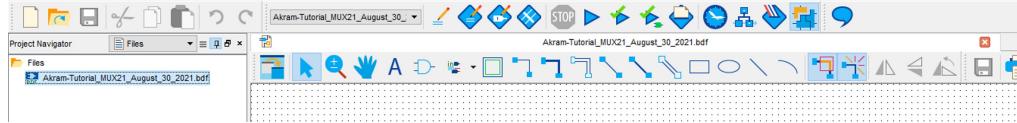
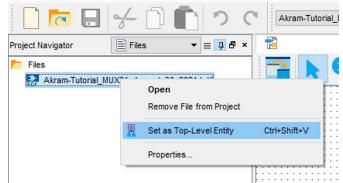


File > Save As

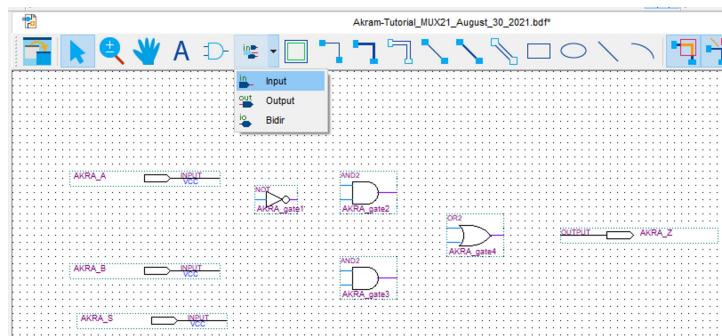
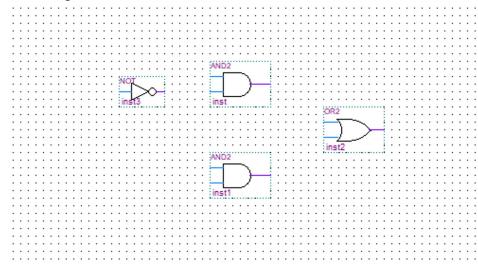
Akram-Tutorial_MUX21_August_30_2021

Block Diagram/Schematic Files (*.bdf)

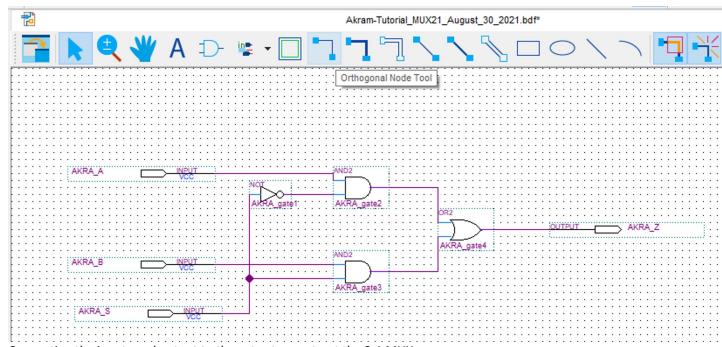


**Adding gates :**

- or2
- and2
- and2
- not gate



Adding inputs and output to gates and renamed them appropriately.

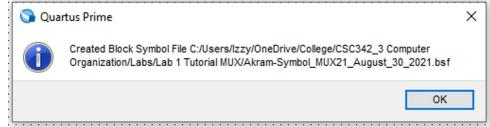


Connecting the inputs and output to the gates to construct the 2:1 MUX

File > Save

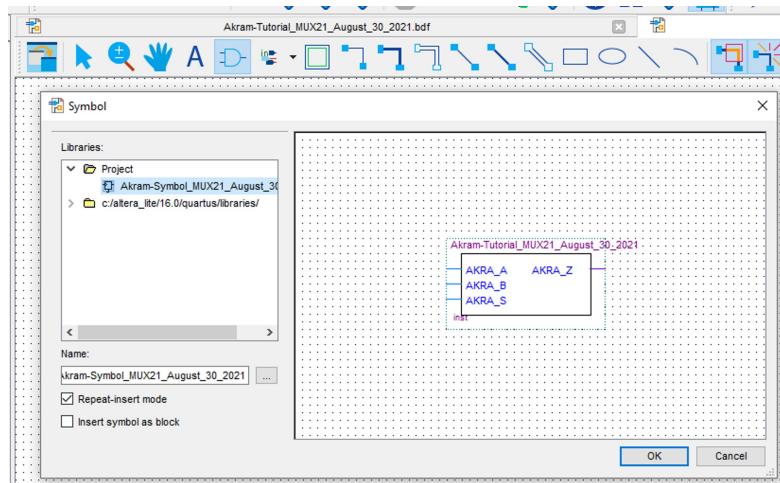
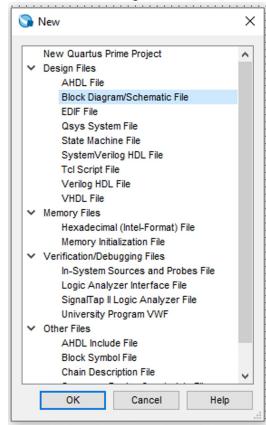
Symbol Creation

File > Create/Update > Create Symbol Files for current file

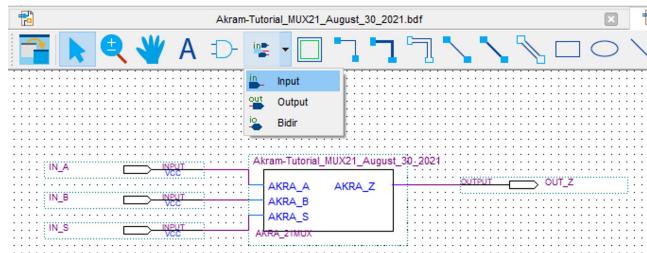


Created block symbol of 2:1 MUX

File > New > Block/diagram Schematic File



Imported MUX to new block diagram file



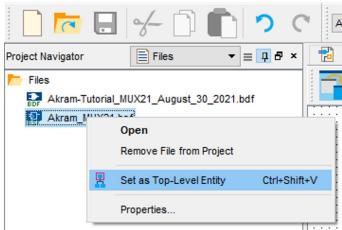
Adding inputs and output, and connecting them to the 21MUX Symbol and renaming appropriately.

File name: Akram_MUX21.bdf
Save as type: Block Diagram/Schematic Files (*.bdf)

Saving block diagram so I can compile.

Quartus Prime Lite Edition - C:/Users/Izzy/OneDrive/College/CS

File Edit View Project Assignments Processing Tools \



Setting Symbol as top-level

Quartus Prime Lite Edition - C:/Users/Izzy/OneDrive/College/CSC424_3 Computer Organization/Labs/Lab 1 Tutorial MUX/Akram-Tutorial_MUX21_August_30_2021 - Akram-Tutorial_MUX21_August_30_2021

Flow Status: Successful - Wed Sep 01 11:51:56 2021
Quartus Prime Version: 16.0 Build 211 04/07/2016 SJ Lite Edition
Revision Name: Akram-Tutorial_MUX21_August_30_2021
Top-Level Entity Name: Akram_MUX21
Flow Log:
Device: 5CSEMAFSF1C8
Timing Models: Final
Logic utilization (in ALMs): 1 / 32,870 (< 1 %)
Total ALMs: 0
Total pins: 4 / 457 (< 1 %)
Total virtual pins: 0
Total block memory cells: 0 / 4,065,280 (0 %)
Total block ROM cells: 0 / 87 (0 %)
Total IHSI RX PCNs: 0
Total IHSI PNA RX Deserializers: 0
Total IHSI TX PCNs: 0
Total IHSI PNA TX Serializers: 0
Total DFFs: 0 / 6 (0 %)
Total DLLs: 0 / 4 (0 %)

Tasks

Task	Compilation
Compile Design	0
Analysis & Synthesis	0
Filter (Place & Route)	0
Assembler (Generate programming files)	0
TimeQuest Timing Analysis	0
EDA Netlist Writer	0
Fitter Settings	0
Program Device (Open Programmer)	0

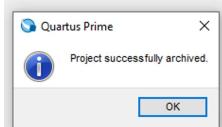
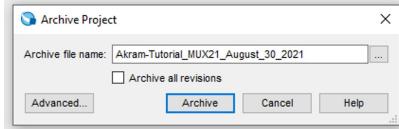
Type ID Message

- 332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
- 332140 No Setup paths to report
- 332140 No Hold paths to report
- 332140 No Recovery paths to report
- 332140 No Removal paths to report
- 332140 No Minimal Paths to report
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- 2930000 Quartus Prime Timequest Timing Analyzer was successful. 0 errors, 6 warnings
- 2930000 Quartus Prime Full compilation was successful. 0 errors, 13 warnings

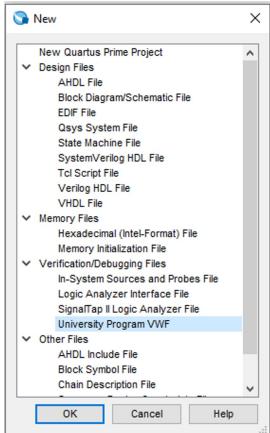
Compiled successfully

File > Save Project

Project > Archive Project



Simulation

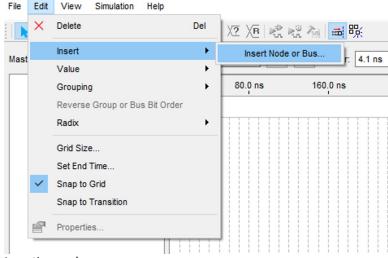


Creating new simulation file

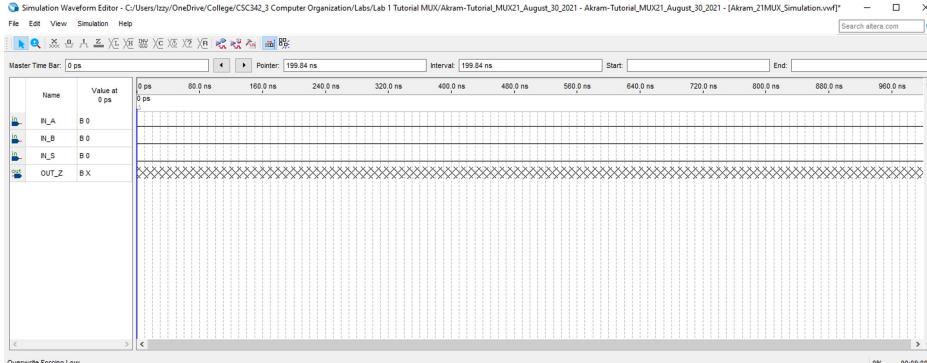
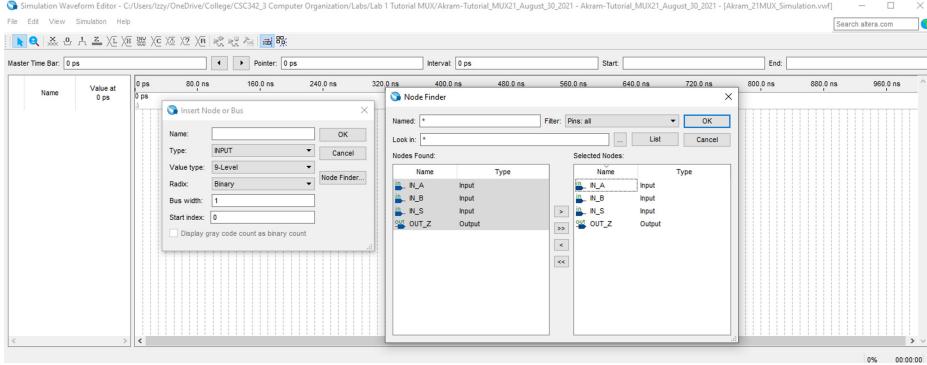
File name: **Akram_21MUX_Simulation**
Save as type: University Program VWF (*.vwf)

Saving

Simulation Waveform Editor - C:/Users/izzy/OneDrive/College/CSC342_3 Computer Organization/Labs/Lab 1 Tutorial MUX/Akram-Tutorial_MUX21_August_30_2021 - Akram-Tutorial_MUX21_August_30_2021 - [Akram_21MUX_Simulation.vwf]

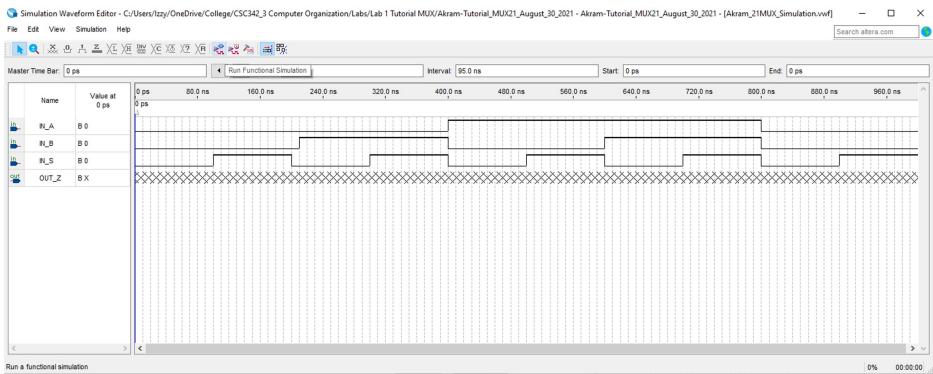


Inserting nodes

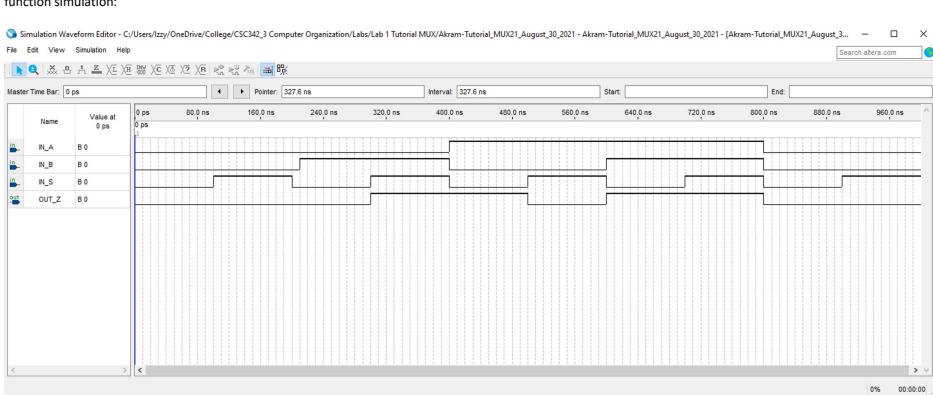


Overwrite Forcing Low

Newly created simulation with inputs and outputs



Run a functional simulation
Edited input. Using overwrite clock and overwrite invert. So we can test multiple inputs. Now running function simulation:

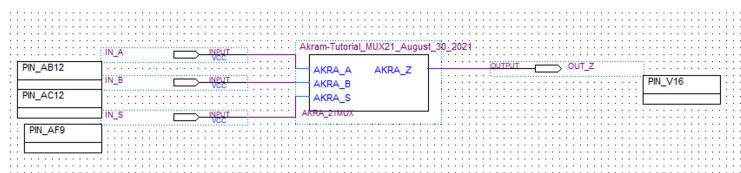
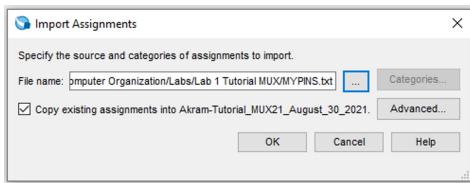
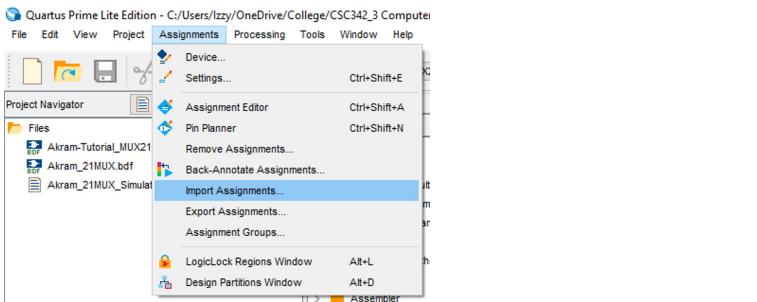


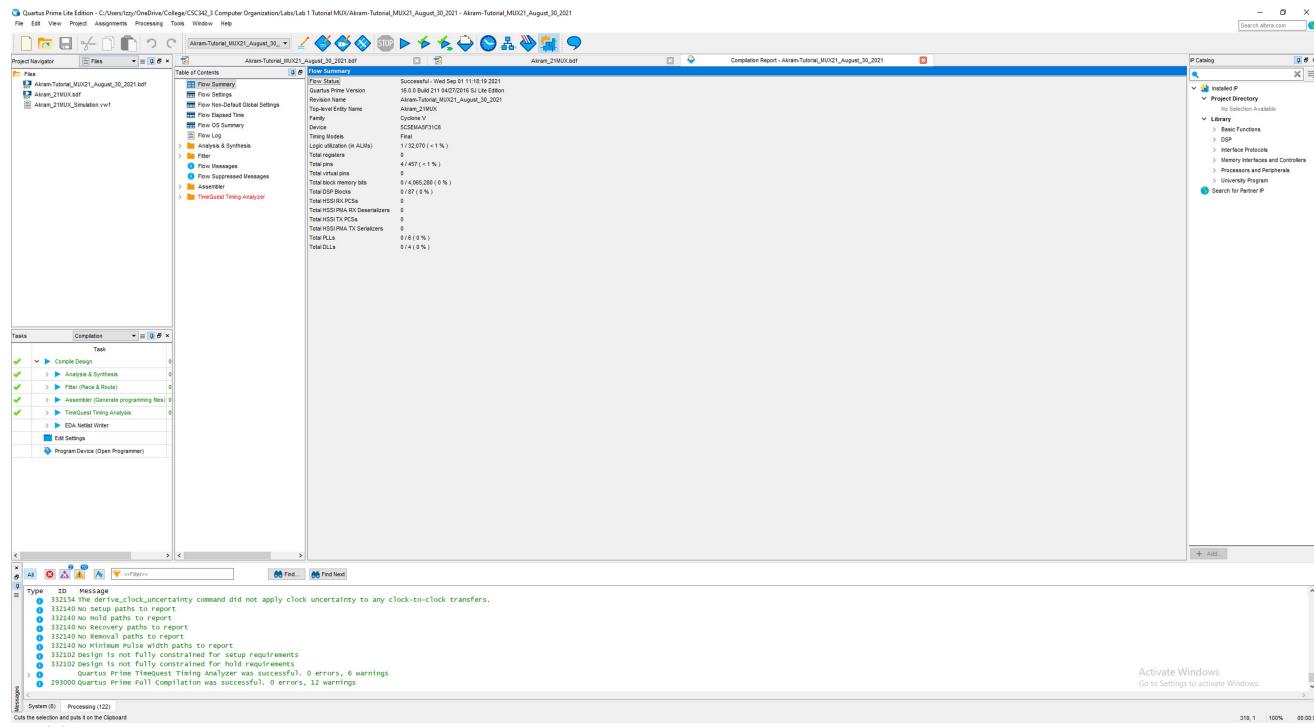
Generated simulation using "Run Functional Simulation".

PIN Assignments

*Untitled - Notepad
File Edit Format View Help
To, Location
IN_A, PIN_AB12
IN_B, PIN_AC12
IN_S, PIN_AF9
OUT_Z, PIN_V16

Creating .txt file for PIN assignment





```
1 -- Copyright (C) 1991-2016 Altera Corporation. All rights reserved.
2 -- Your use of Altera Corporation's design tools, logic functions
3 -- and other software and tools, and its AMPP partner logic
4 -- functions, and any output files from any of the foregoing
5 -- (including device programming or simulation files), and any
6 -- associated documentation or information are expressly subject
7 -- to the terms and conditions of the Altera Program License
8 -- Subscription Agreement, the Altera Quartus Prime License Agreement,
9 -- the Altera MegaCore Function License Agreement, or other
10 -- applicable license agreement, including, without limitation,
11 -- that your use is for the sole purpose of programming logic
12 -- devices manufactured by Altera and sold by Altera or its
13 -- authorized distributors. Please refer to the applicable
14 -- agreement for further details.
15
16 -- PROGRAM    "Quartus Prime"
17 -- VERSION   "Version 16.0.0 Build 211 04/27/2016 SJ Lite Edition"
18 -- CREATED   "wed Sep 01 11:24:33 2021"
19
20 LIBRARY ieee;
21 USE ieee.std_logic_1164.all;
22
23 LIBRARY work;
24
25 ENTITY Akram_21MUX IS
26 PORT
27 (
28     IN_A : IN STD_LOGIC;
29     IN_B : IN STD_LOGIC;
30     IN_S : IN STD_LOGIC;
31     OUT_Z : OUT STD_LOGIC;
32 );
33 END Akram_21MUX;
34
35 ARCHITECTURE bdf_type OF Akram_21MUX IS
36
37 COMPONENT akram-tutorial_mux21_august_30_2021
38 PORT(AKRA_A : IN STD_LOGIC;
39       AKRA_B : IN STD_LOGIC;
40       AKRA_S : IN STD_LOGIC;
41       AKRA_Z : OUT STD_LOGIC);
42 );
43 END COMPONENT;
44
45
46 BEGIN
47
48 b2v_AKRA_21MUX : akram-tutorial_mux21_august_30_2021
49 PORT MAP(AKRA_A => IN_A,
50           AKRA_B => IN_B,
51           AKRA_S => IN_S,
52           AKRA_Z => OUT_Z);
53
54
55
56
57
58 END bdf_type;
```

VHDL generated.