

Laboratory Exercise: Schematic Capture digital circuits

Instructor: Professor Izidor Gertner

Tutorial – Digital Circuit Block Diagram Design Method with Quartus

PART 1. Quartus block diagram design and compilation

PART 2. Circuit Simulation

PART 3. PIN Assignments

TASKS TO PERFORM :

TASK 1 IMPLEMENT PART 1, PART 2, PART 3 AS DESCRIBED IN TUTORIAL.

TASK 2 REPEAT TASK 1 FOR 2:1 MULTIPLEXER.

Task 3 Create VHDL code from the schematic diagram you have designed (hint: use submenu item save as VHDL). Examine the VHDL code you have created.

SUBMIT SCREENSHOTS ONLY WITH EXPLANATIONS, NO REPORT.

File name you submit should be in the following format

LAST_NAME_LAB_TITLE

Objective

Using the schematic capture (block diagram method), this tutorial will explain the basic tools for circuit design in Quartus.

In this tutorial you will learn how to:

- Create and set up a new project
- Create a block diagram file
- Design a basic digital circuit using block diagrams
- Include input and output pins in your design
- Create a symbol out of your designed circuit
- Compile your project
- Simulate your project to verify correct behavior
- Create PIN assignments •

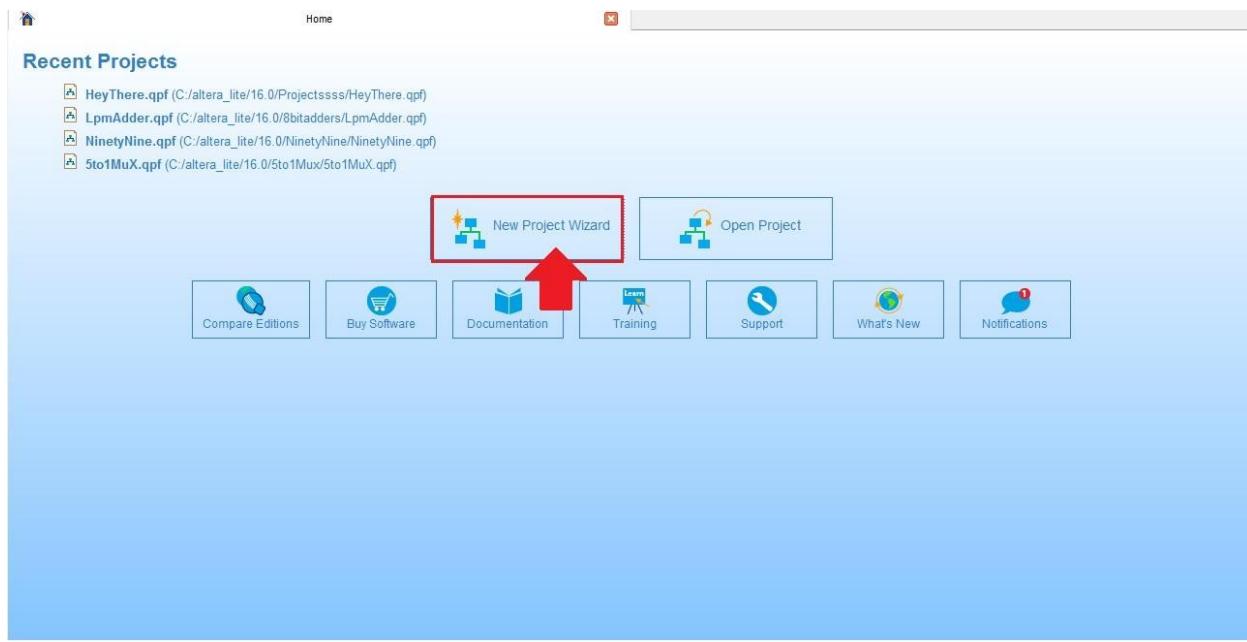
Note: In order to follow along this tutorial, we assume that you have already downloaded and installed Quartus Prime Lite and its necessary components for testing in the DE1-SOC board. If you have not done so, please refer to our tutorial Quartus Download and Setup.

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Please note the screenshots depend on the version of Quartus you use. Please modify where needed.

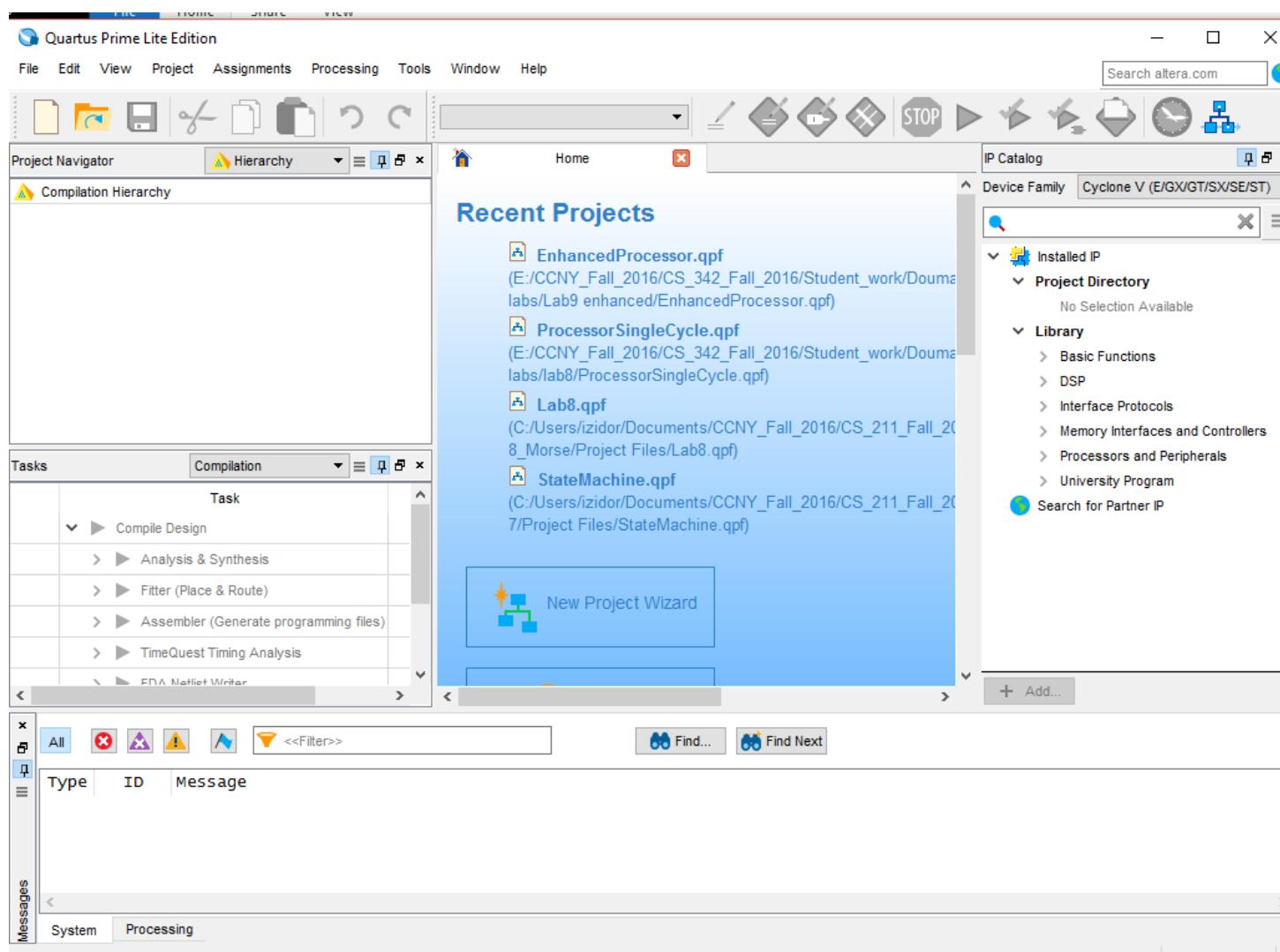
PART 1. Quartus block diagram design and compilation

Start the Quartus software from your program files. Quartus creates a shortcut in your Desktop during installation). The Quartus program starts up with the following screen with the options to create a new project or open an existing project. Click **New Project Wizard**



OR

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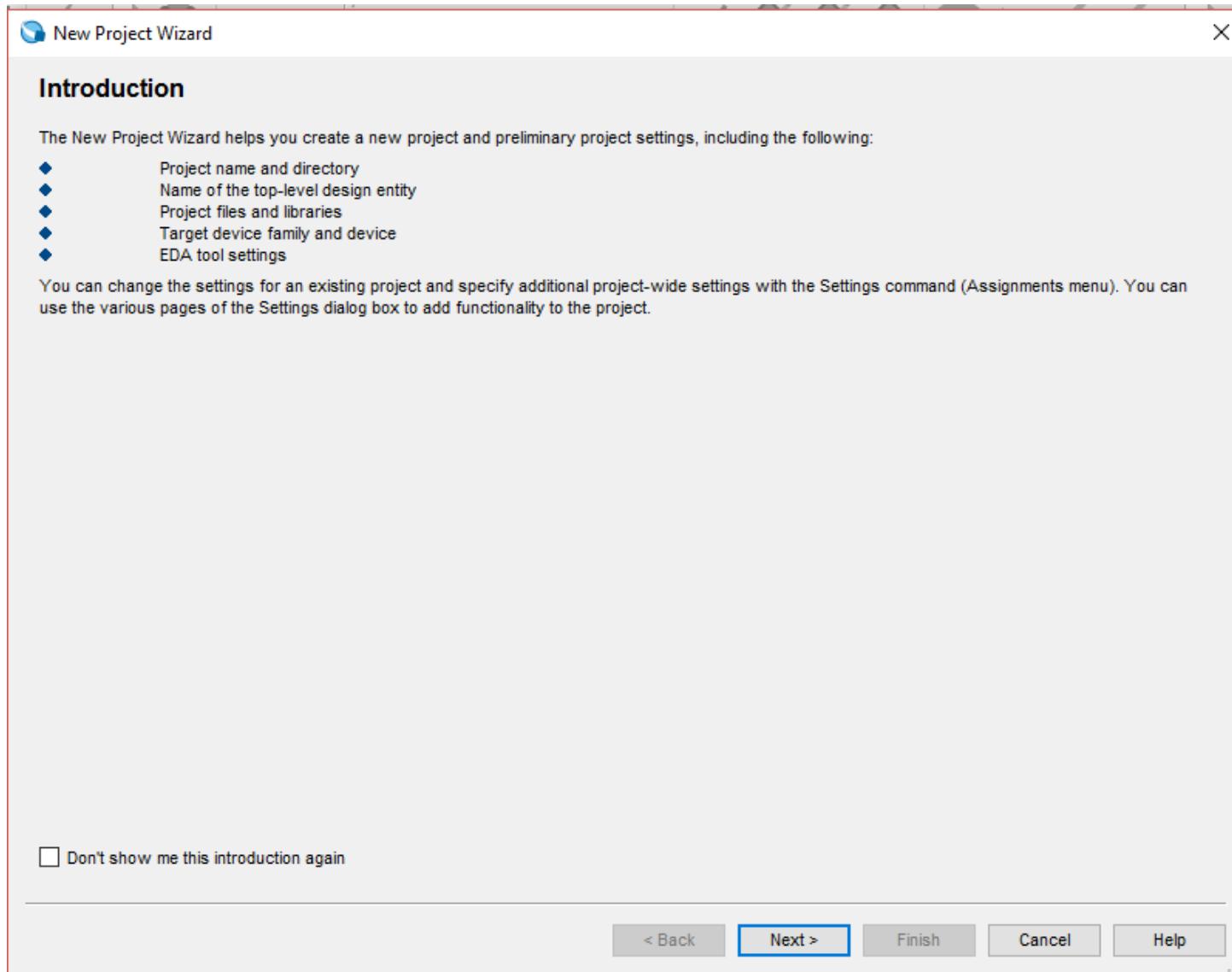
Click New Project Wizard

To get

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Click NEXT

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Click and create a directory

PATH/My_LastName_CS343_SP17

In this directory Create a subdirectory
path/Cs343_Lab_#number_TITLE_LastName_SP17
This naming format is REQUIRED!

NOTE: PROJECTS THAT USE DIFFERENT NAMING FORMAT WILL NOT BE GRADED!



Directory, Name, Top-Level Entity

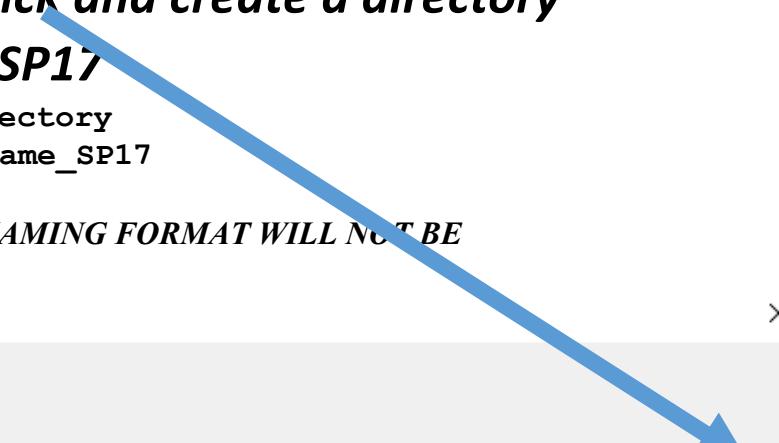
What is the working directory for this project?
C:\altera_lite\16.0

What is the name of this project?
BasicTutorial

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
BasicTutorial

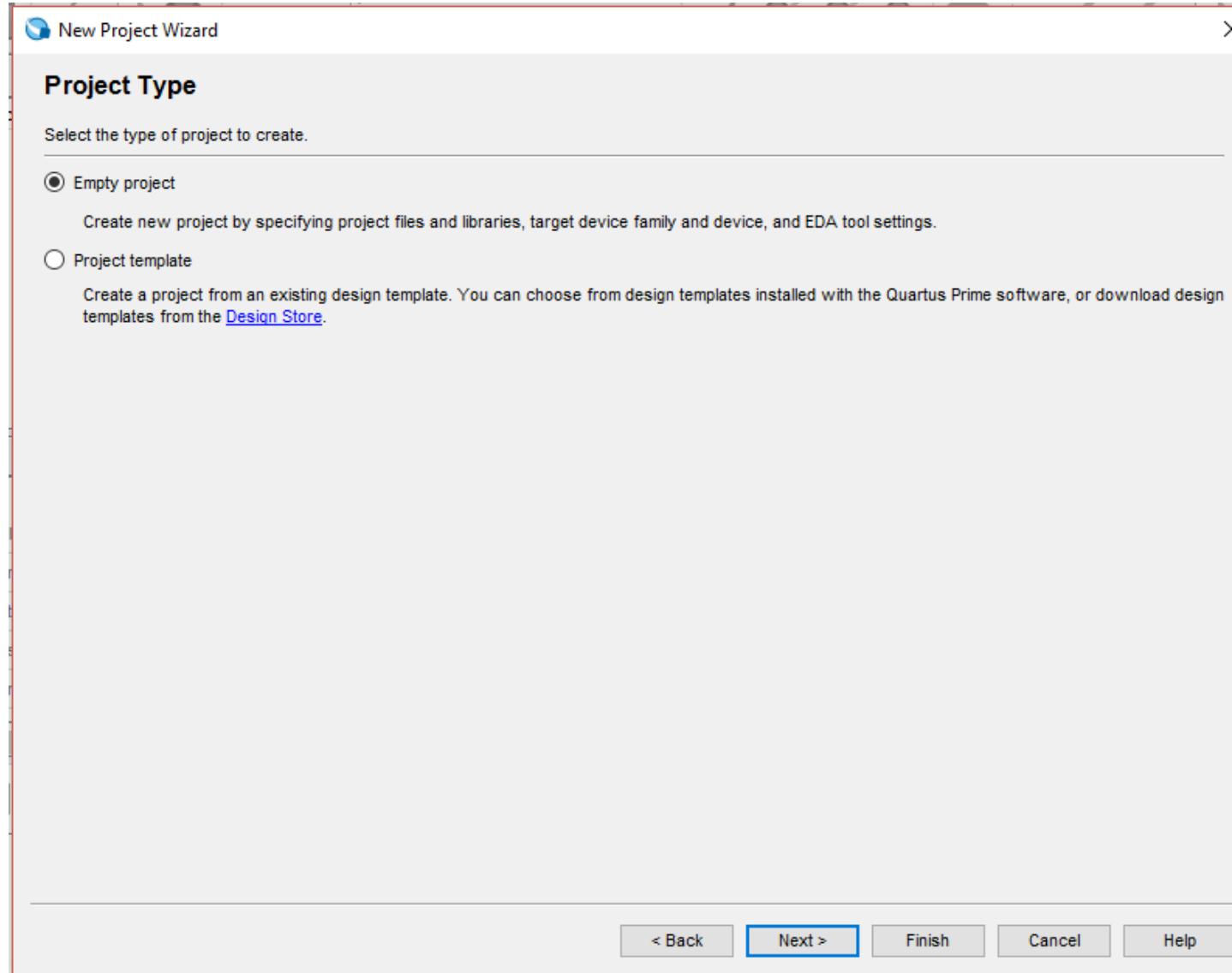
Use Existing Project Settings...

< Back Next > Finish Cancel Help



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Click NEXT and select Empty Project



Then Click NEXT

Skip the NEXT screen on adding files and proceed to the screen on setting family and device settings.

- In the Device Family dropdown menu:

Cyclone V (E/GX/GT/SX/SE/ST) 5CSEMA5F31C6

- In the Available Devices box:

(It is also easy to look for the Device by typing 5CSEMA5F31C6 on the Name Filter box.)

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New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)
Devices: All

Target device

Auto device selected by the Filter
 Specific device selected in 'Available devices' list
 Other: n/a

Show in 'Available devices' list

Package: Any
Pin count: Any
Core Speed grade: Any
Name filter:

Show advanced devices

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	F
5CSEMA4U23I7	1.1V	15880	314	314	0	0	0
5CSEMA5F31A7	1.1V	32070	457	457	0	0	0
5CSEMA5F31C6	1.1V	32070	457	457	0	0	0
5CSEMA5F31C7	1.1V	32070	457	457	0	0	0
5CSEMA5F31C8	1.1V	32070	457	457	0	0	0
...

< Back Next > Finish Cancel Help

Click NEXT
In the EDA TOOL SETTINGS

SIMULATION select to NONE
As shown below:

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New Project Wizard

EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back **Next >** Finish Cancel Help

Click next you should get SUMMARY Window

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New Project Wizard X

Summary

When you click Finish, the project will be created with the following settings:

Project directory: C:/Users/izidor/Documents/CCNY_SPRING_2017/CS211_spring2017/MyLAST_Name_cs211/Lab_1_MasterPR_LastName

Project name: BasicTutorial

Top-level design entity: BasicTutorial

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Design template:	n/a
Family name:	Cyclone V (E/GX/GT/SX/SE/ST)
Device:	5CSEMA5F31C6
Board:	n/a

EDA tools:

Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	()

Operating conditions:

Core voltage:	1.1V
Junction temperature range:	0-85 °C

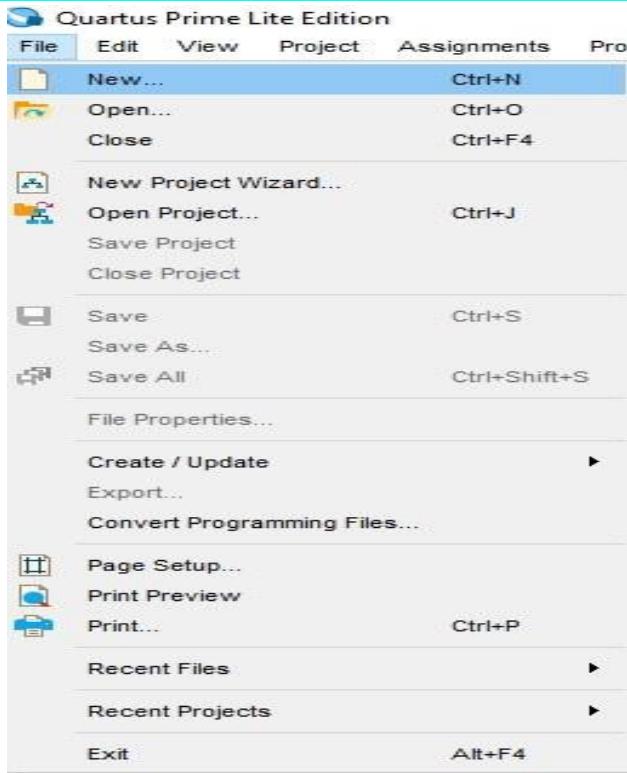
[< Back](#) [Next >](#) Finish [Cancel](#) [Help](#)

Click **FINISH**.

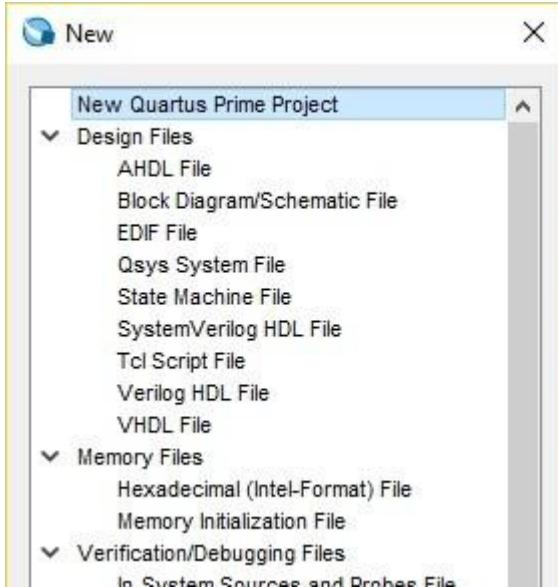
Now please go the section creating your design.

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Alternatively, you can create a new project by going to File > New...

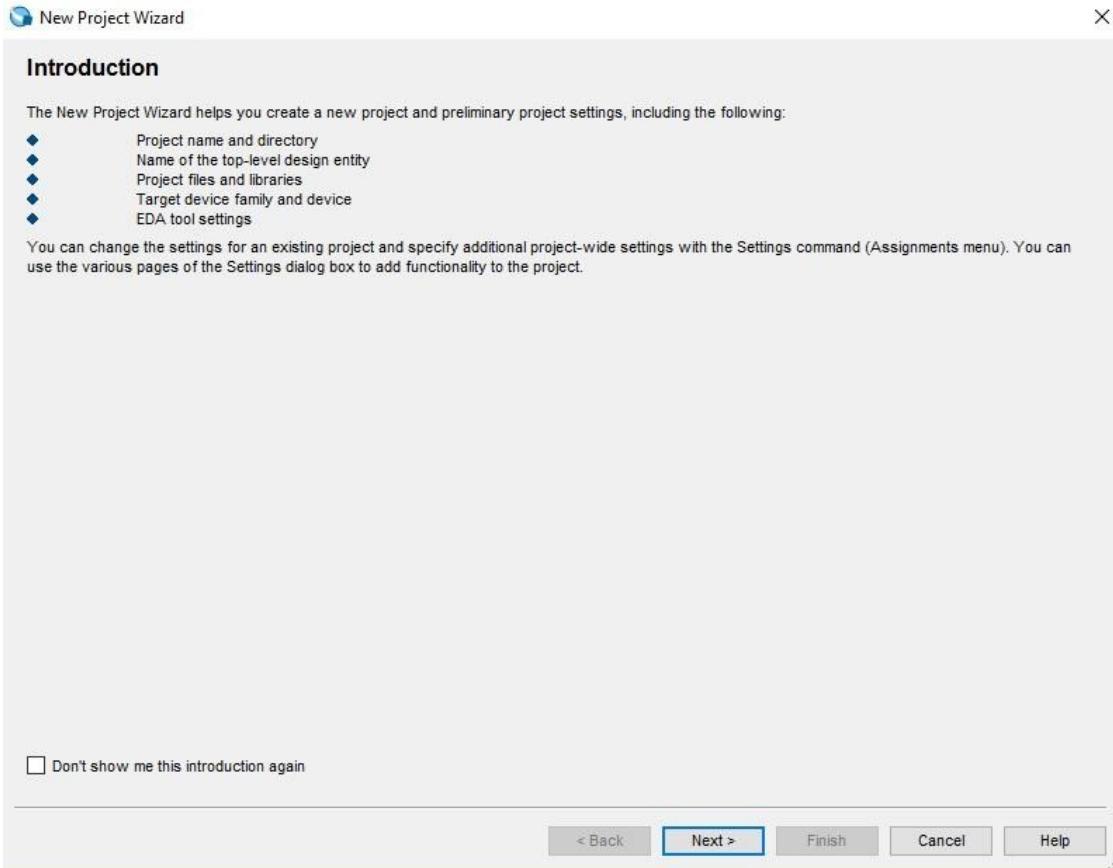


The following window appears, select **New Quartus Prime Project**



Once you create a project, the following screen for project wizard appears. Click Next

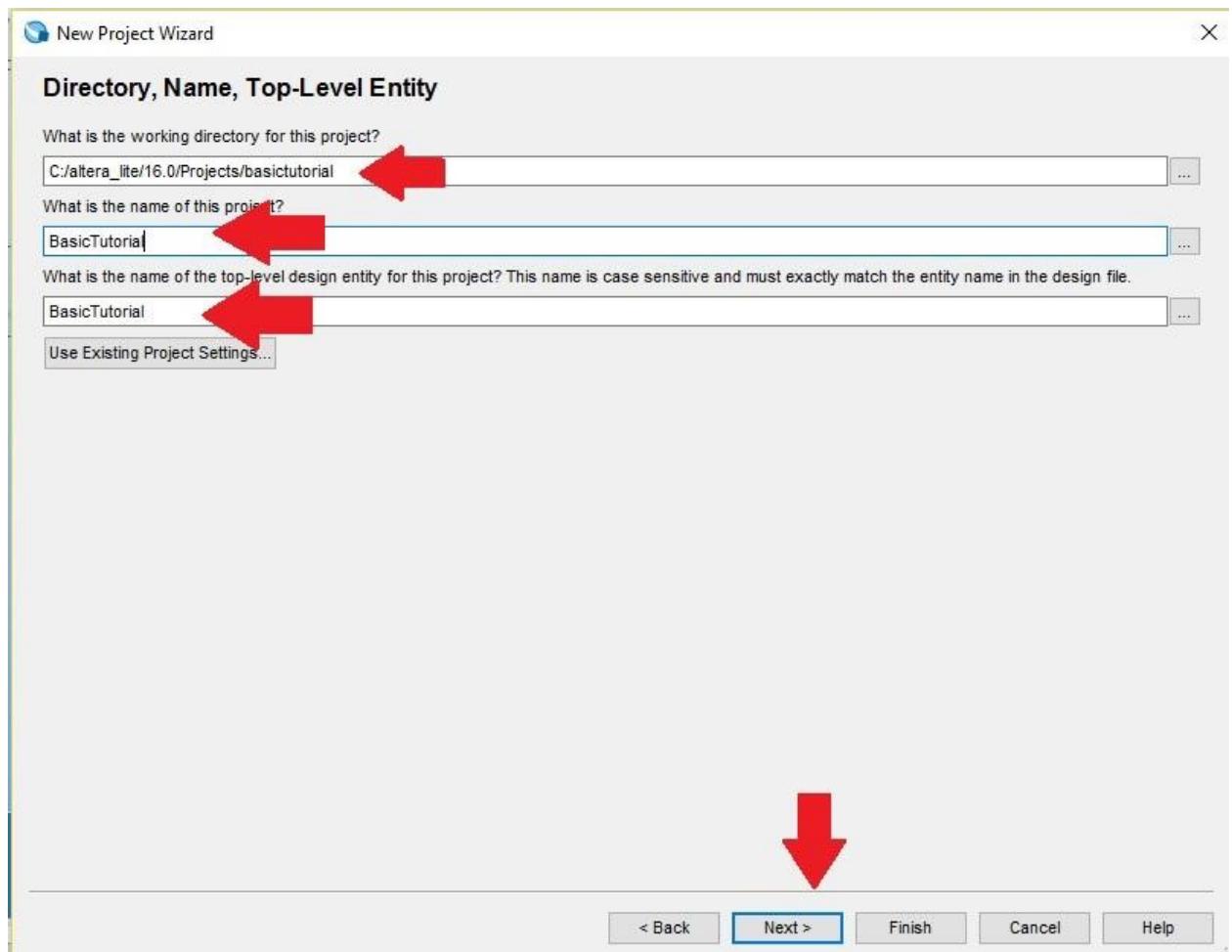
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The screen for setting up your project location and name appears. The working directory in the picture below was chosen by preference. The default location would have been in the installation directory. Each version upgrades of Quartus creates a separate installation folder. Hence, it is advisable to have a separate folder for Quartus projects. This choice is left to the user. Enter the project name, in our case we decided to call it BasicTutorial (you can call it any name you prefer). You do not need to fill up the field for the top-level design entity for this tutorial because we are going to create a single circuit for demonstration purposes. Therefore, Quartus will take the project name as the top-level design for your project.

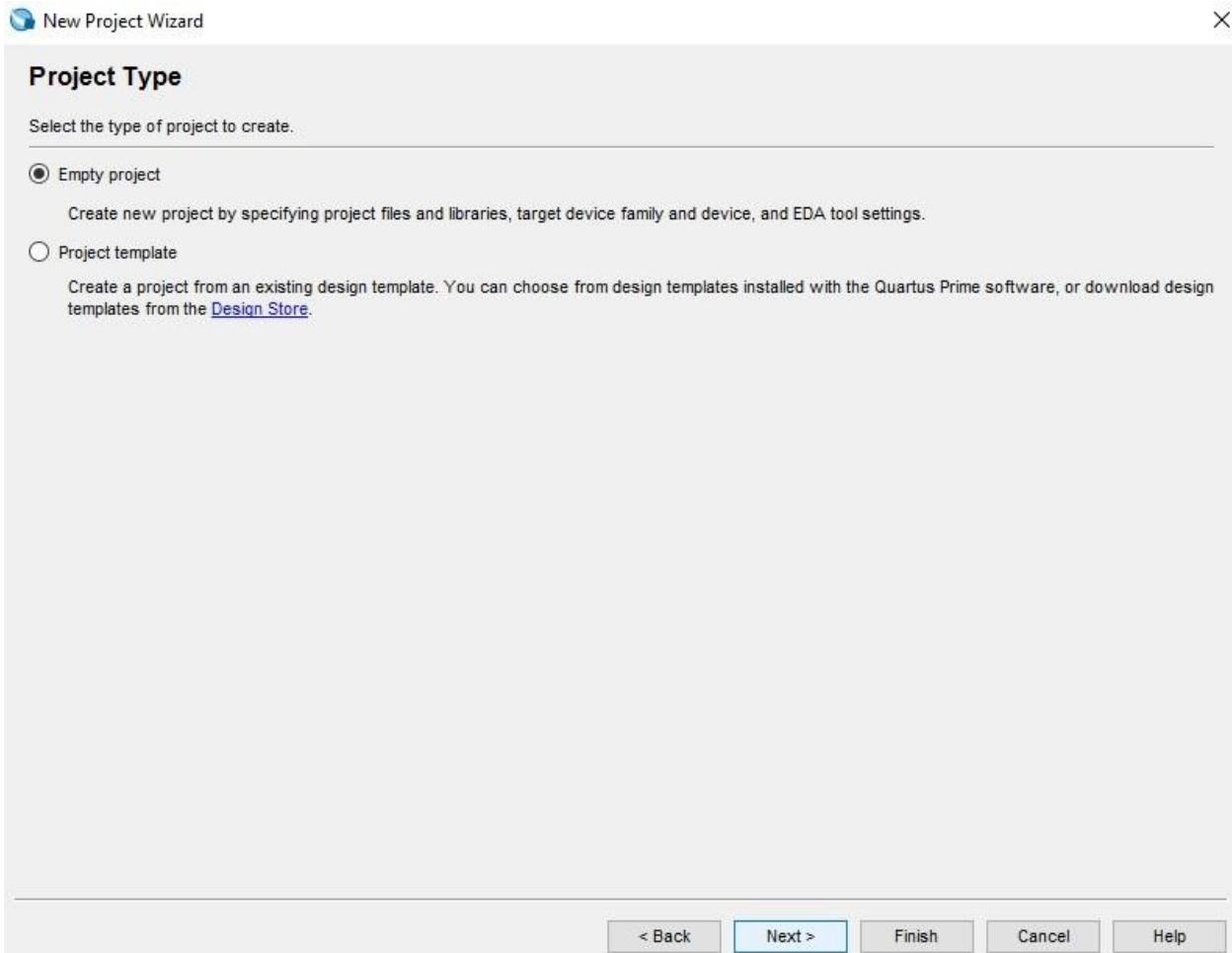
Once you fill up the required info indicated by the arrows below, hit Next. If Quartus asks you if you want to create a new folder if the location does not exist, click Yes.

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Select **Empty Project** then Next again.

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Skip the next screen on adding files and proceed to the screen on setting family and device settings.

Altera has a long list of FPGA chips including Flex10k, Max7000, Stratix, Cyclone (I, II, III, IV,V). In our labs we will use the DE1-SOC board which comes with the Cyclone V chip on it. For this tutorial and all subsequent assignments in this series, please choose the following:

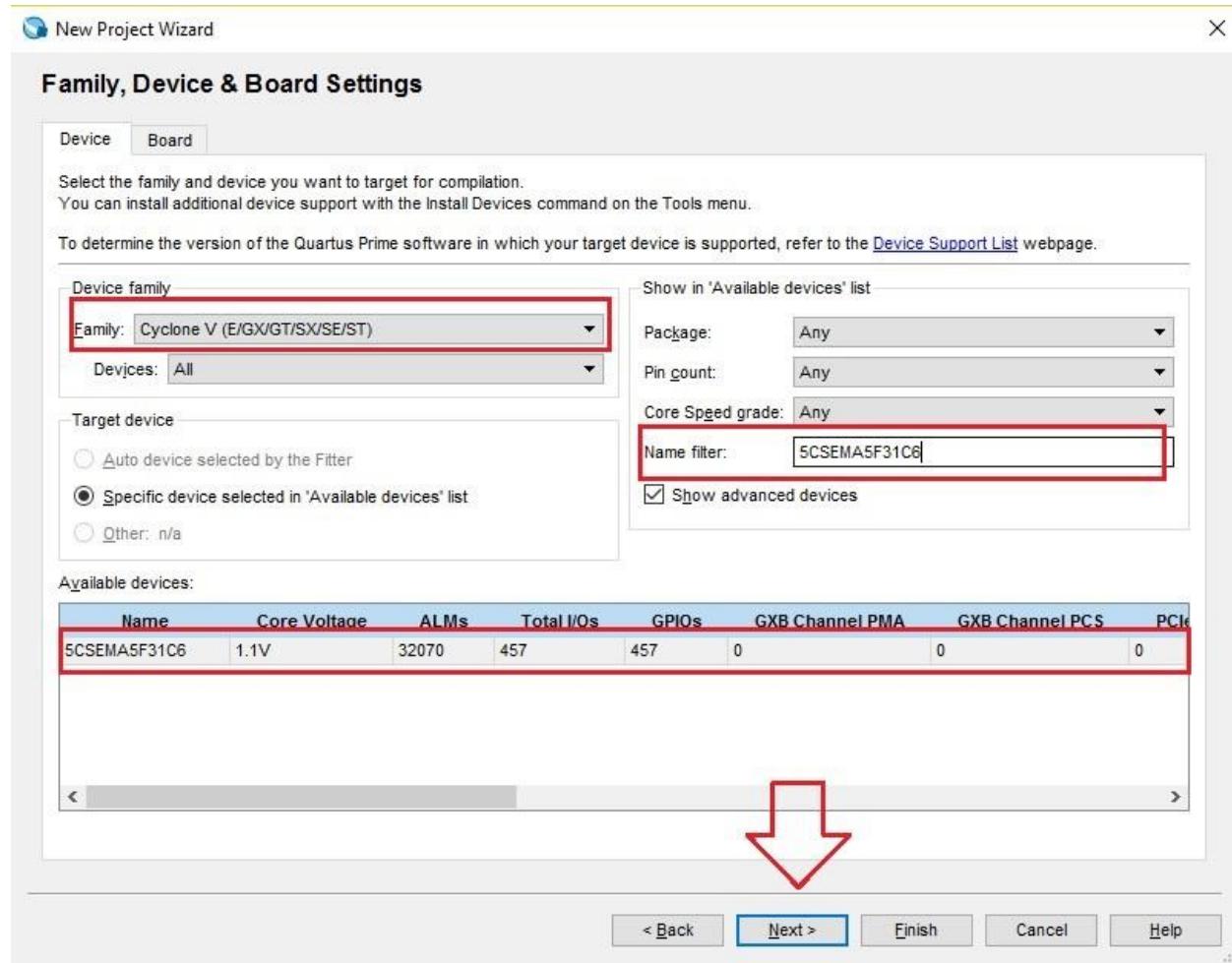
- In the Device Family dropdown menu:

Cyclone V (E/GX/GT/SX/SE/ST) 5CSEMA5F31C6

- In the Available Devices box:

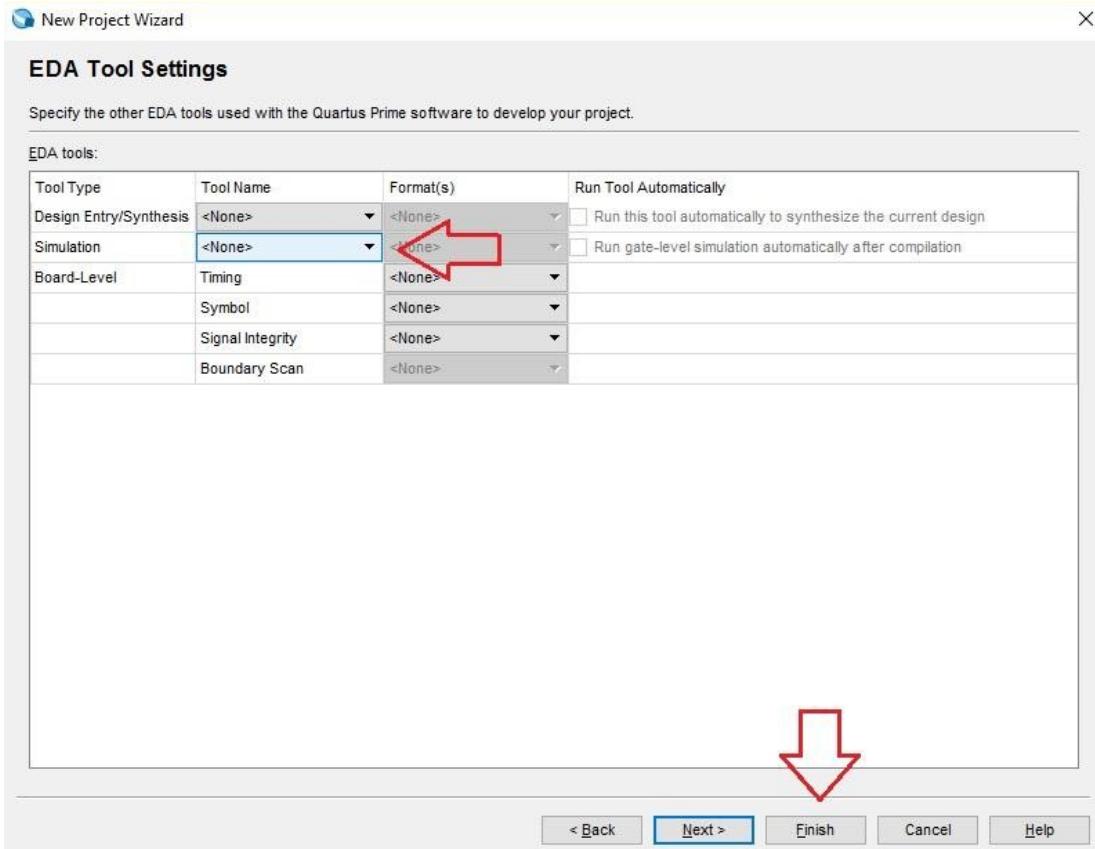
(It is also easy to look for the Device by typing 5CSEMA5F31C6 on the Name Filter box.)

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After you are done selected your options for the device, click Next. You are presented with a screen for EDA Tools Settings. We do not need these tools for our tutorials. Make sure that the options in your screen look similar to the picture below. If you have Model-Sim Altera in your Simulation field, change it to **None**. Now we are done setting up our project. Click **Finish**.

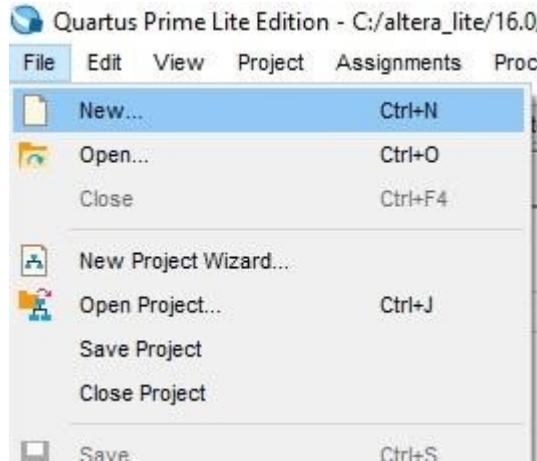
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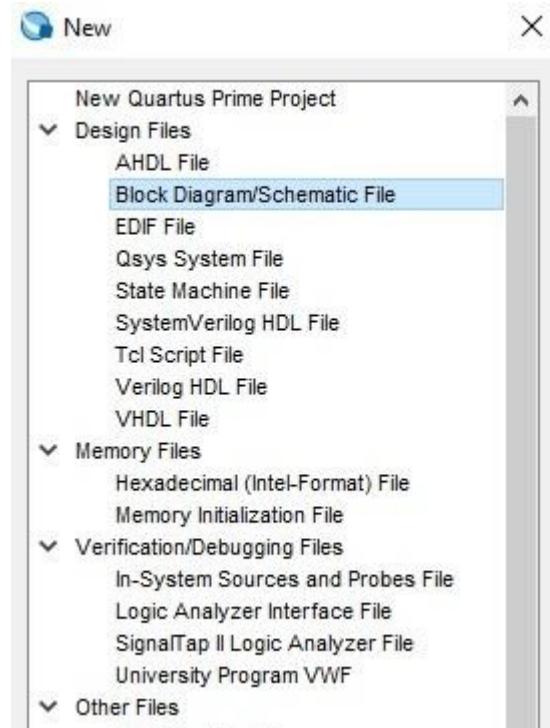
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Creating Your New Design

We are ready to start designing our digital circuit. Click **File > New...**



The following window appears, select **Block Diagram/Schematic File** option to proceed with the design.

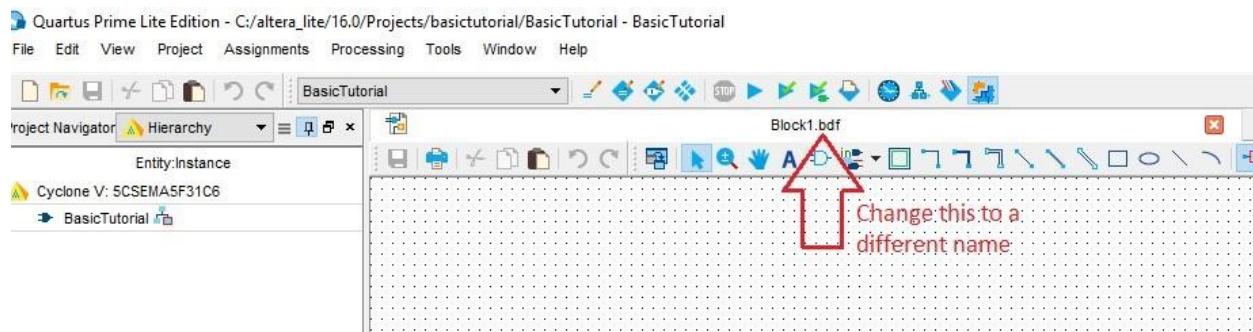


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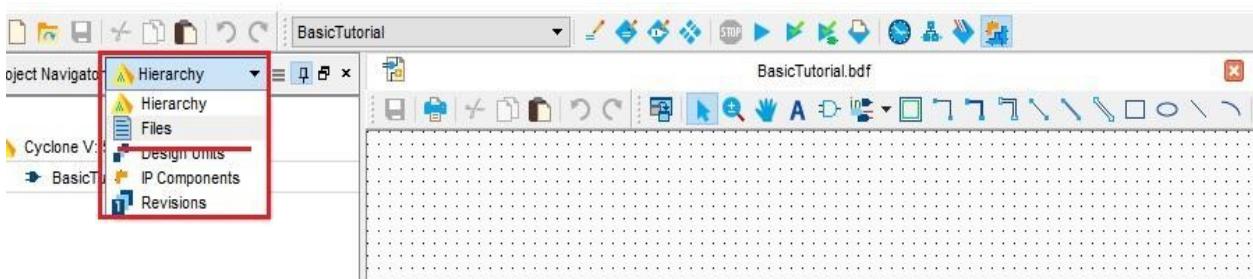
Note: There are several file types listed in the above screen:

- Block Diagram/ Schematic file entry is chosen for graphical entry of the schematic and is the preferred form of logic diagram entry.
- Verilog and VHDL file is also supported to input the circuit description in those languages. We also have a file for Memory initialization file. This file is used to store a certain pattern of hexadecimal digits. This will be useful in later labs in this course.
- The other file of interest is the Vector Waveform File. This file is used to setup the testing waveforms for input and to observe the output after the simulation. We will show you how to create a vector waveform file later in this tutorial.

You have now a block diagram file. The default name will be Block#.bdf, where # represents some default number chosen by Quartus. Before proceeding change the name of the file to a name of your choice. If you keep this name it will be hard to remember what the file does. Change it to a more meaningful name by going to **File > Save As...**



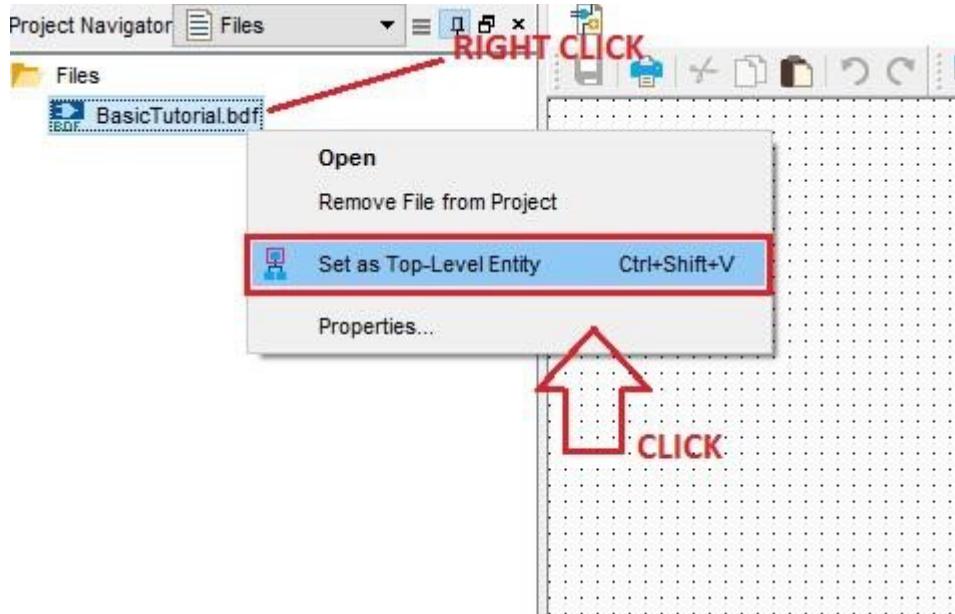
In our case we renamed the file to BasicTutorial.bdf. Now you need to set this file as your top level entity in your Project to be able to compile.



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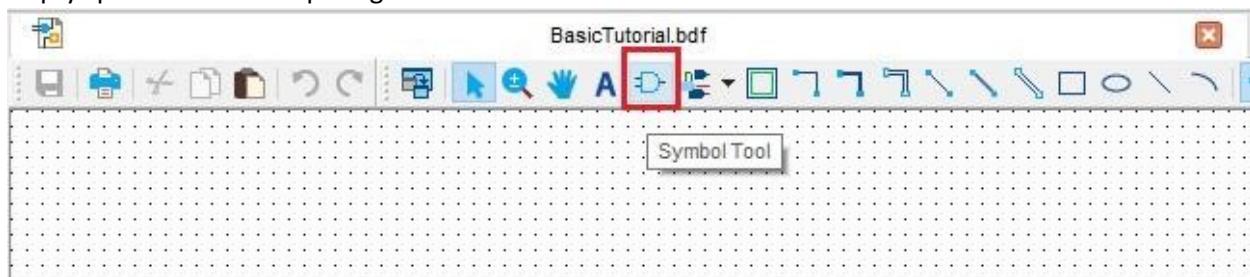
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Click on **Hierarchy**, a drop menu will appear as shown in the picture above. Select **Files**. Then right-click the name of the file **BasicTutorial.bdf** and select **Set as Top-Level Entity**.



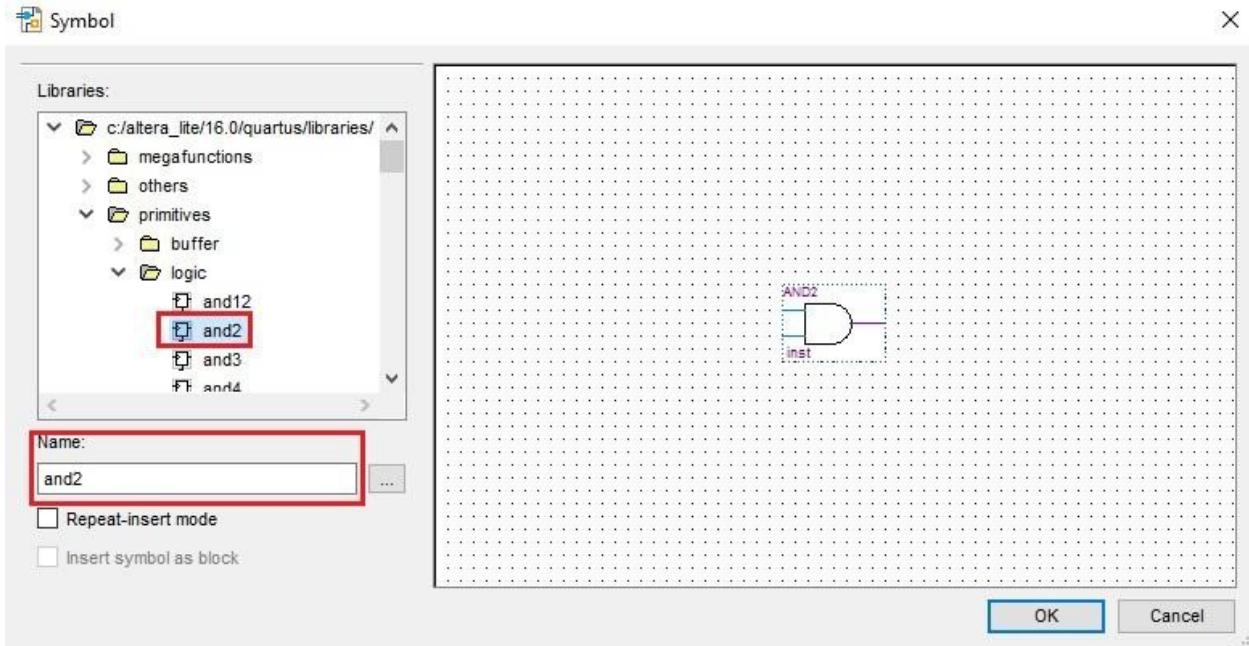
We are now ready to design a circuit using the block-diagram method.

To enter a symbol click the **Symbol Tool** as shown below. Alternatively, you can also double-click on an empty space in the workspace grid.



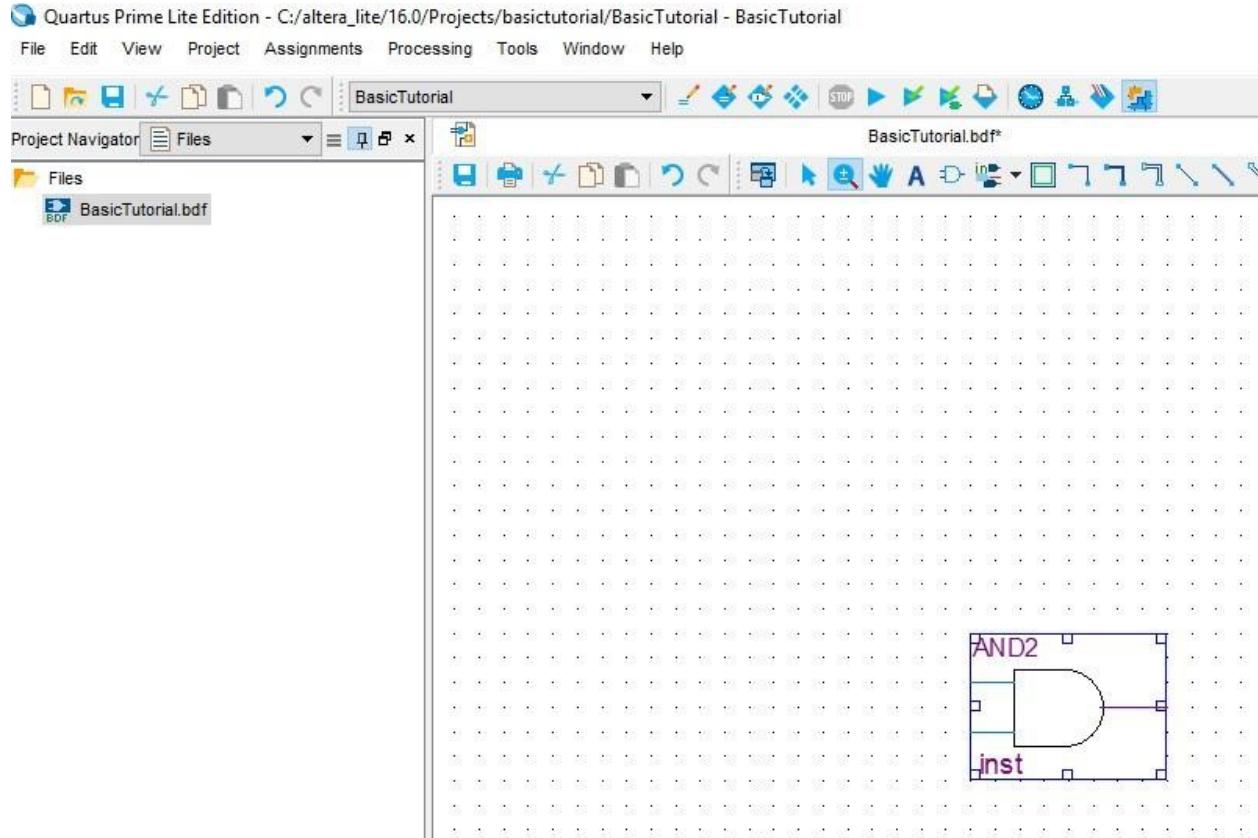
Now navigate through the file system as shown in the picture and choose the **and2** symbol. You do this by going to **Primitives > Logic > and2**. Then hit **OK**.

The name **and2** means that you have a AND gate with 2 inputs, for instance a **nor8** is a NOR gate with 8 inputs. Alternatively, you can find the gate by searching in the Name bar, also shown in the picture below.

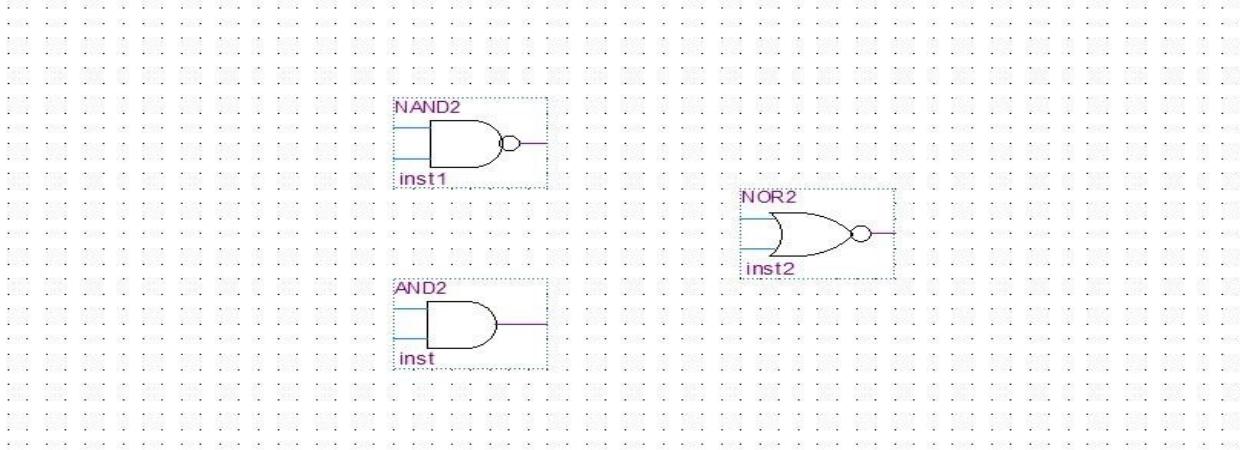
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When you get familiar with the names of the gates you can just type their names in the search box called "Name".

You are now ready to place your symbol in your working space. Click once anywhere in the grid to place it as shown in the picture below.

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Observe that your mouse has turned into a dim image of the symbol you are currently entering. If you want your mouse to be free from creating any further symbols, press **Esc** on your keyboard. Now insert a symbol for NAND and NOR by following the same method. The name of the symbols in this case will be **nand2** and **nor2** respectively. If you wish to delete any incorrect entry, select the symbol and press **Delete** on your keyboard. You should have a setup like this:

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For each symbol CHANGE INSTANT NAME by PROPERTIES->GENERAL in the instance name field type your Name> The format of instance name is

First 4 Letters of your last name_gate1

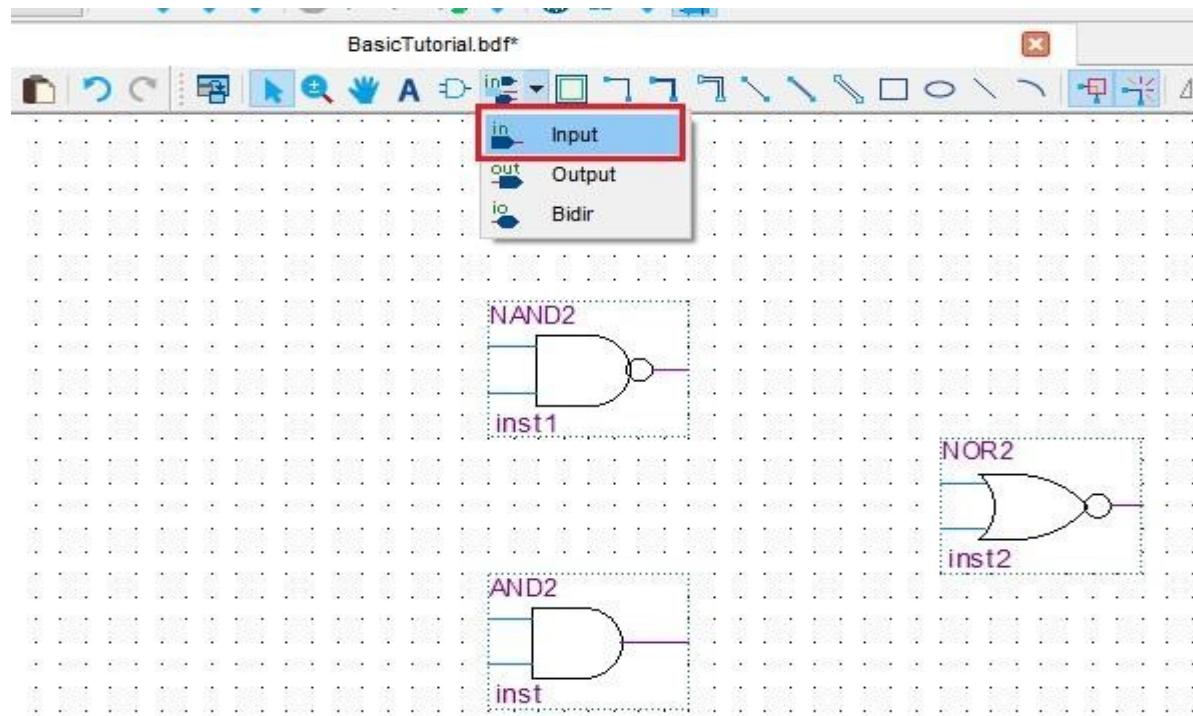
e.g. **FISK_gate1**.

Try to change font color.

After you changed names for all instances save the file.

Adding input and output PINs

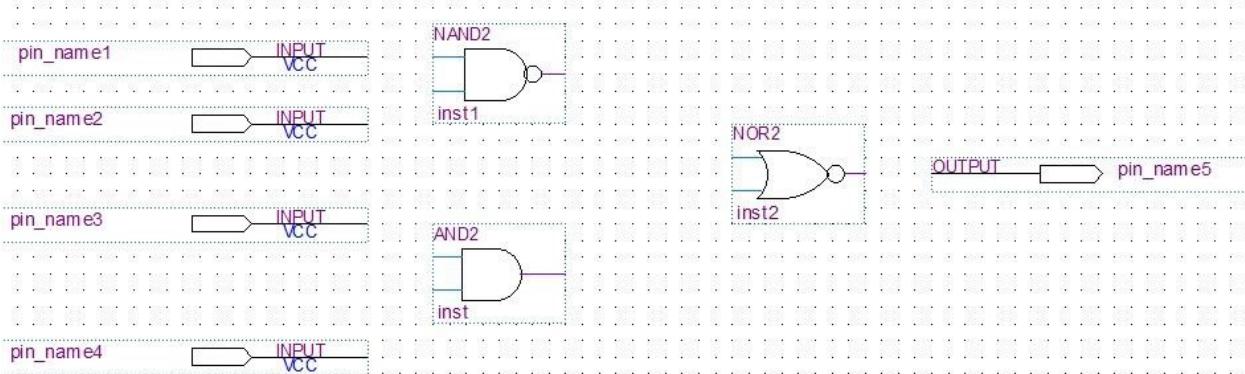
Now it is time to add input and output pins. Click on the **Pin Tool** down arrow and choose **Input**.



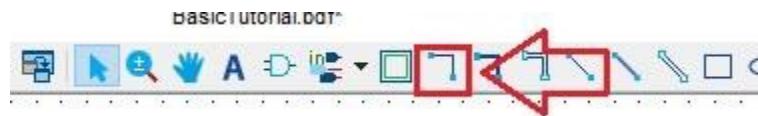
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Enter 4 input pins by clicking on the workspace four times. After you are done click the Pin Tool down arrow again and this time choose **Output**. Now click once in the workspace to enter 1 output pin. After you are done, hit **Esc** in your keyboard.

You should have something like this now:



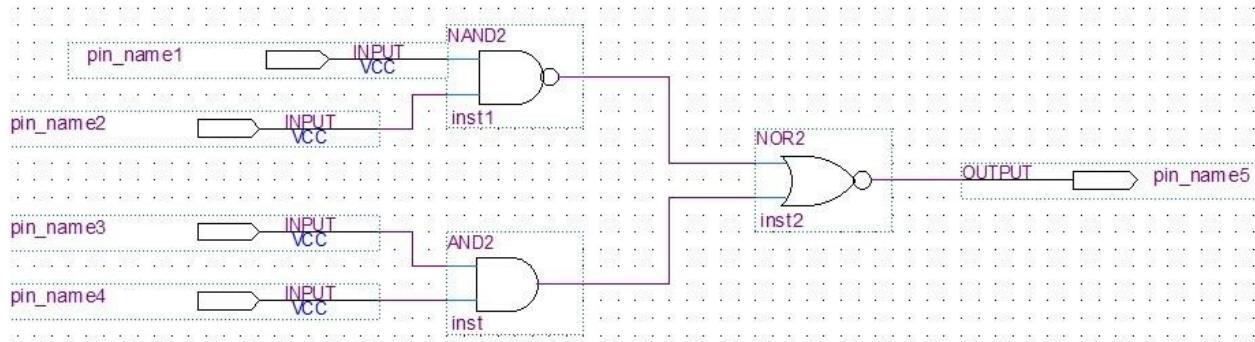
Now connect the pins and the gates by clicking the **Orthogonal Node Tool** (see figure below).



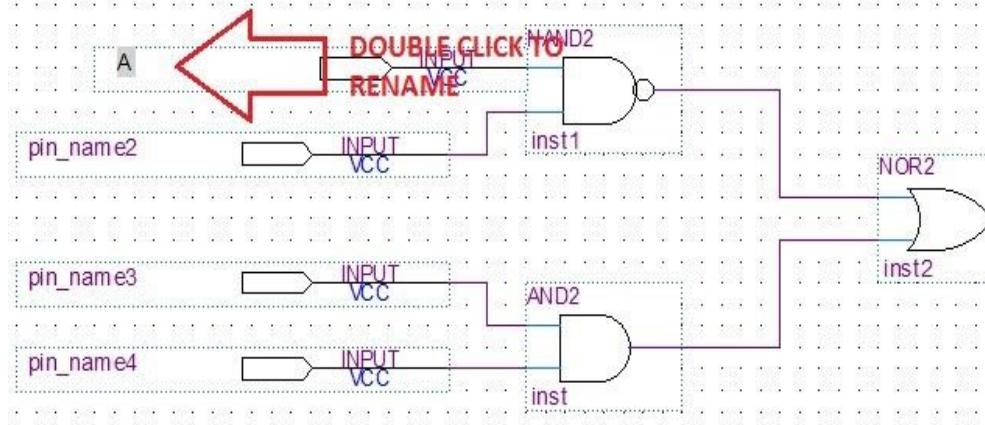
With this tool selected, connect the ends of the gates and input/output pins as shown below. You can click and drag from one end of a gate to the next symbol or pin and Quartus will snap them automatically. You can also move the symbols and pins by clicking and dragging them with your mouse to have a better visual arrangement. **Make sure that there are no breaks in the wires and no disconnected pins or gates, otherwise your design will not compile!**

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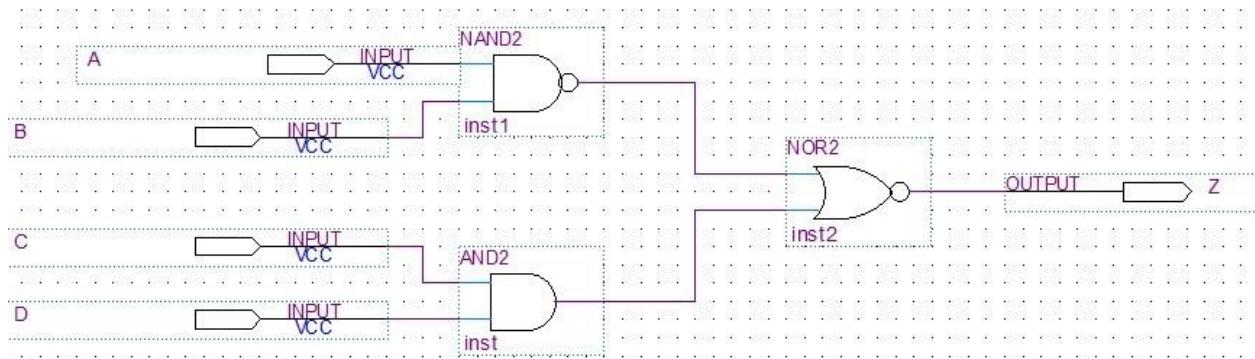
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Now double click on **pin_name1** and rename it to **A**. The FORMAT OF name is **FIRST 4 Letters of LastName and symbol name** e.g A, B, etc. You can also use PROPERTIES menu item to do this.



Proceed to rename all your input and output pins by the same method to give them more meaningful names that are easier to refer to. This should be the final appearance of your design.

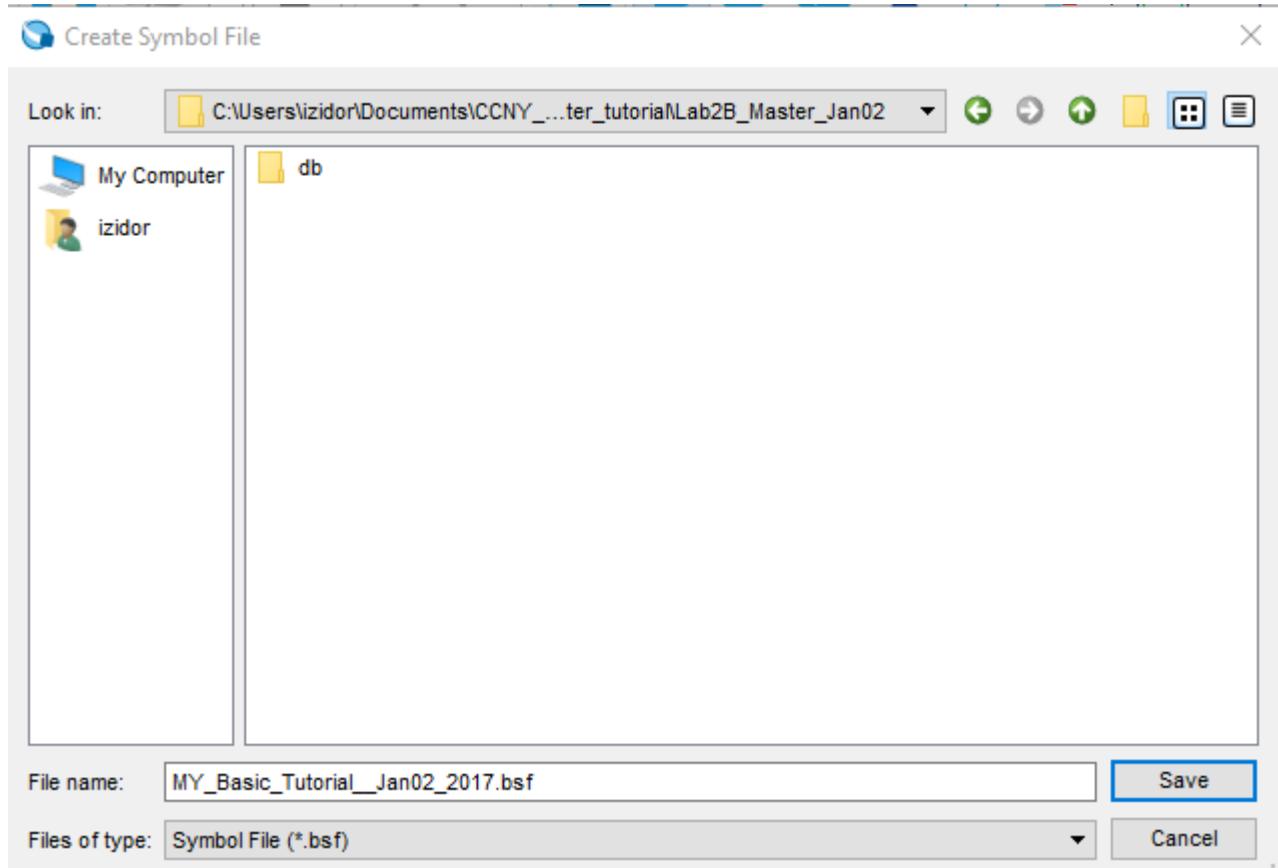


Save your design by clicking **File > Save**.

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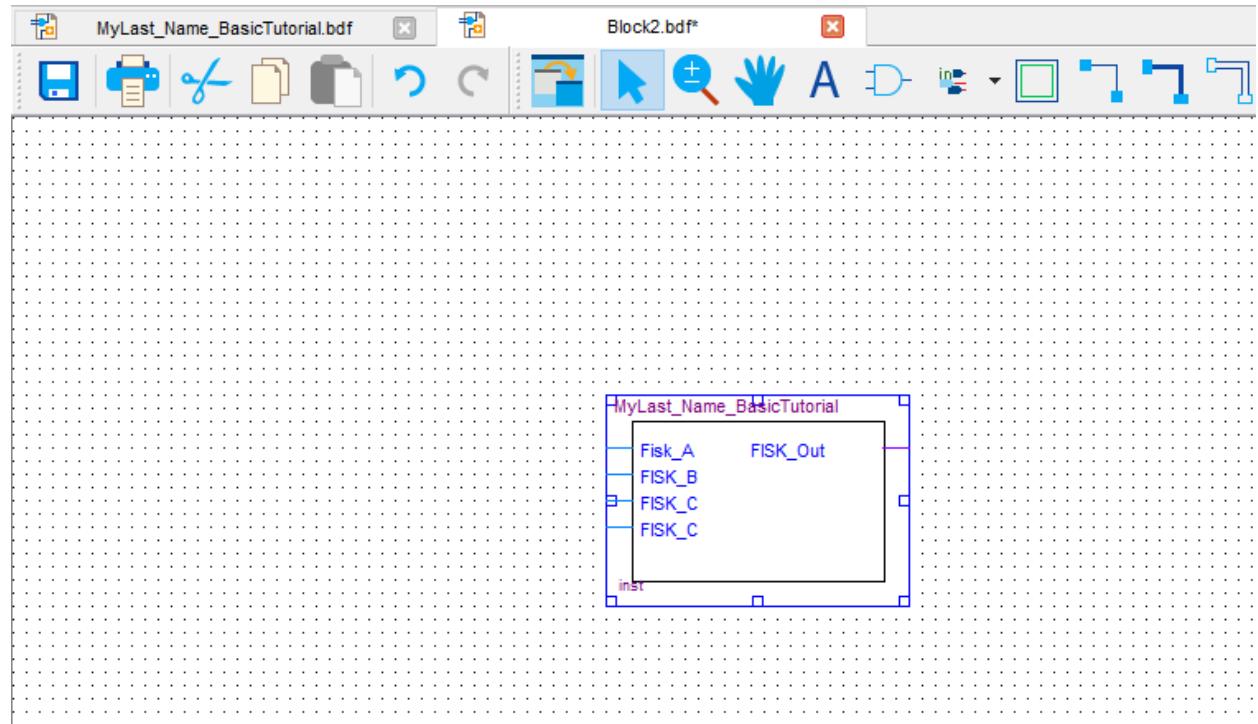
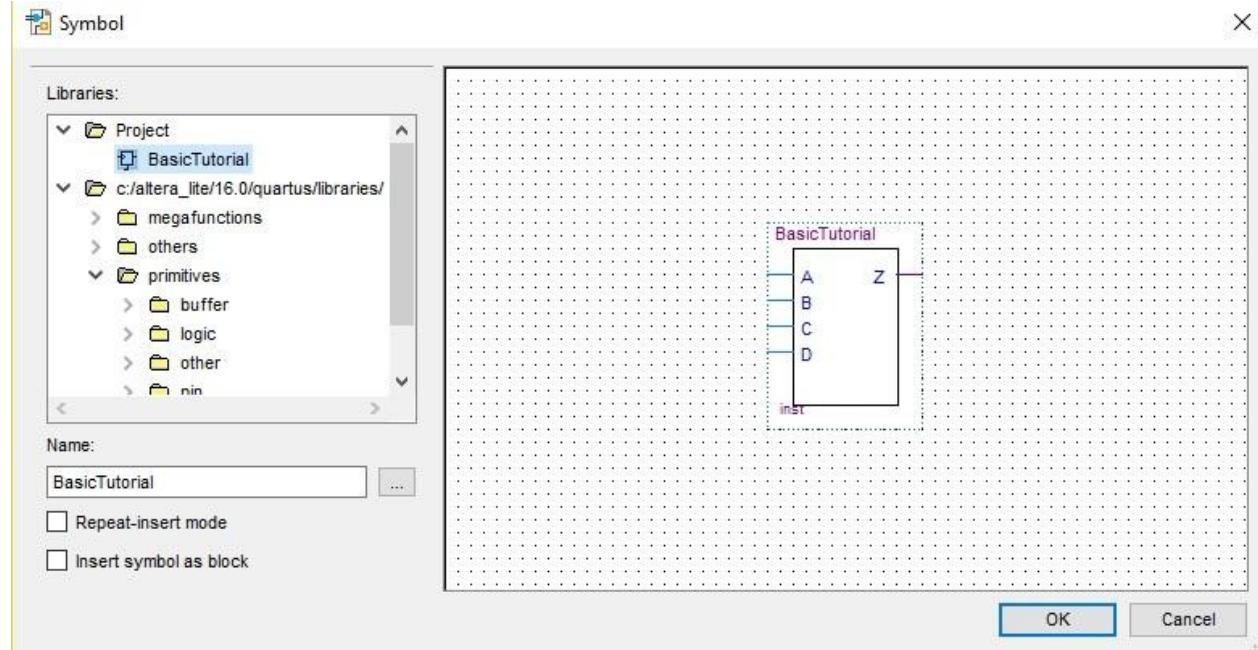
Symbol Creation

Now we are ready to turn this design into a symbol. Choose **File > Create/Update > Create Symbol Files for current file**. Quartus will ask you to give a name to this symbol. In our case, we named it as **BasicTutorial.bsf**. Quartus will notify you after the symbol is created, hit **OK**.



Now we can use this symbol that we just created in a new Quartus design file. To do this, go to **File > New > Block/diagram Schematic File**, as shown before in this tutorial. Hit **OK**.

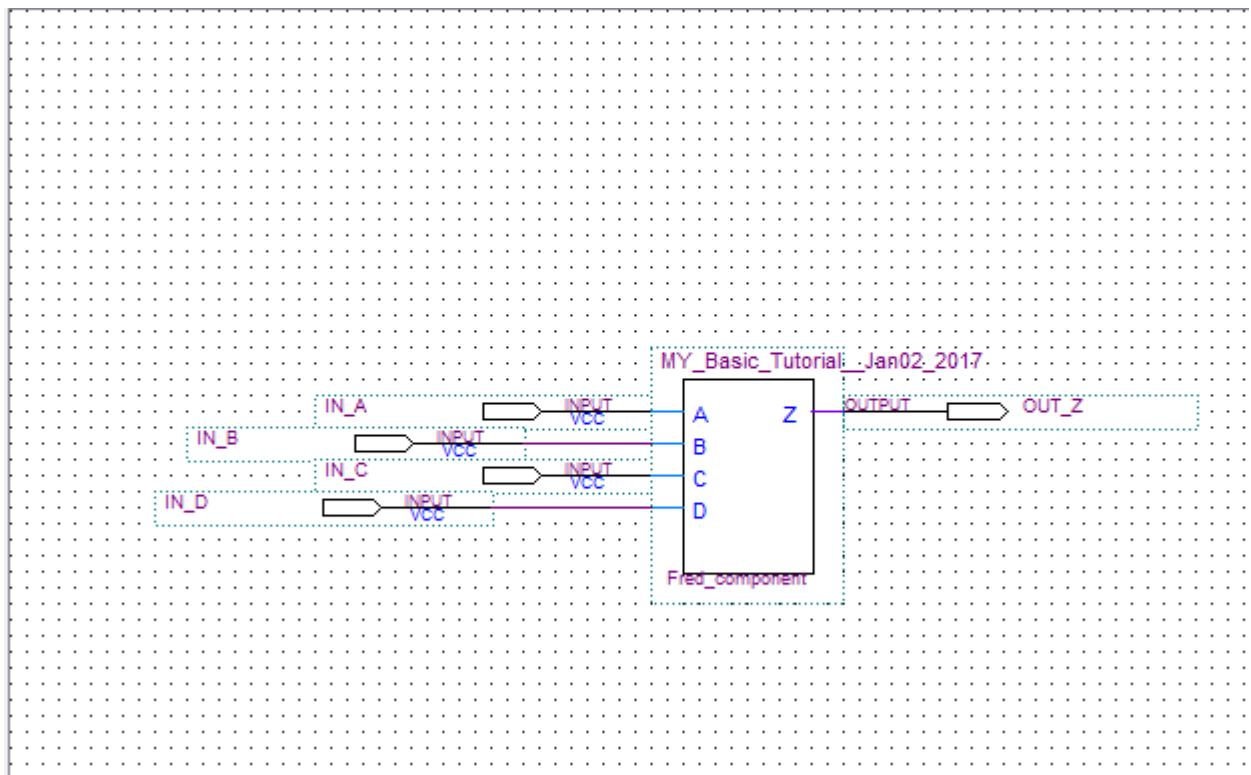
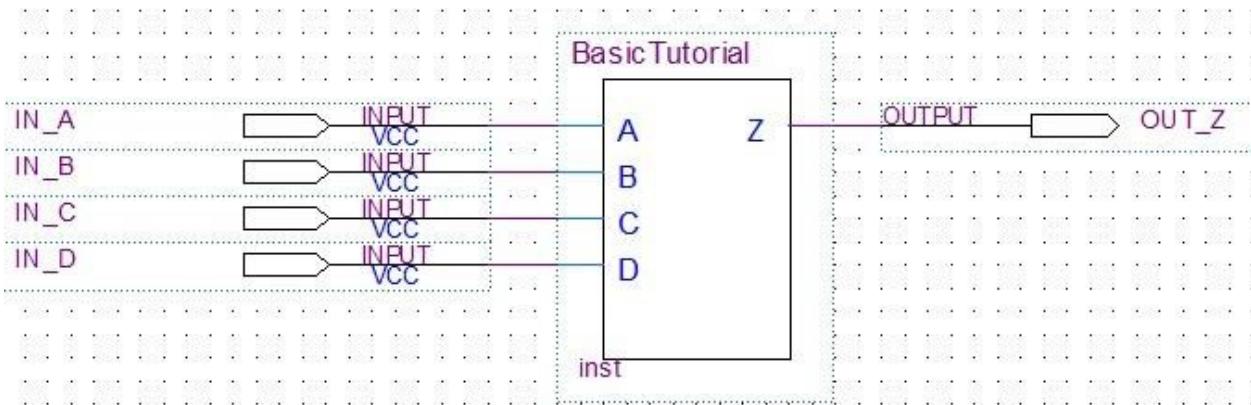
Click on the **Symbol Tool** button to bring up the symbol screen. You should see the symbol just created under the **Project** folder in the Libraries pane on the left. Refer to the picture below.

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Insert the symbol in the workspace. Following the method shown above for input/output insertion and renaming, configure the pins for the symbol as shown in the image below (The input and output pin names are up to you).

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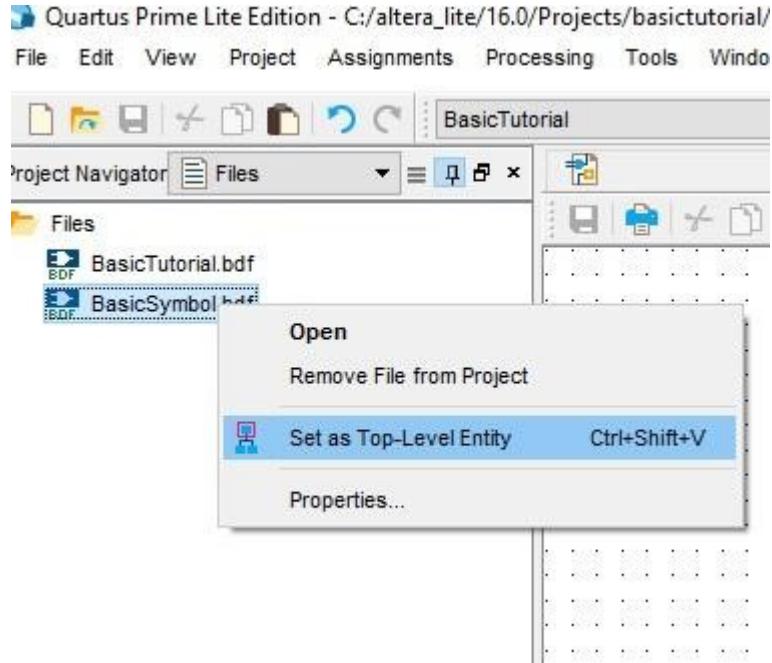


After making our changes, save this new file with a more meaningful name than the default name. We decided to name ours BasicSymbol.bdf, you can name it any way you want.

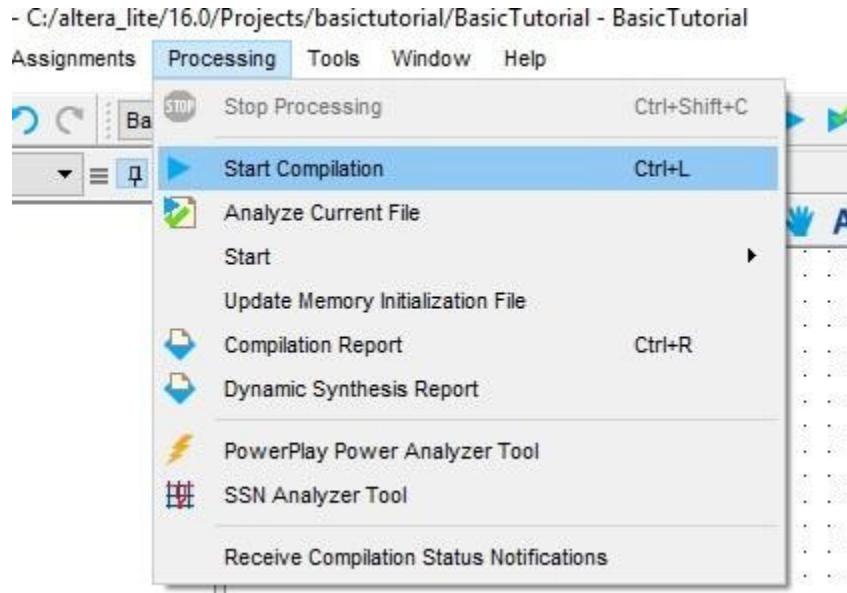
Set this newly created file as top-level entity by the method shown previously: right-clicking on the file name in the File tab and choosing Set as Top-Level Entity. You can also look at the following picture:

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To compile the project, click on **Processing > Start Compilation**. You can also compile by hitting the **Start Compilation** button in the menu bar. This would carry out a series of steps from Analysis and Synthesis, Fitter (Place & Route), Assembler and Timing Analysis.



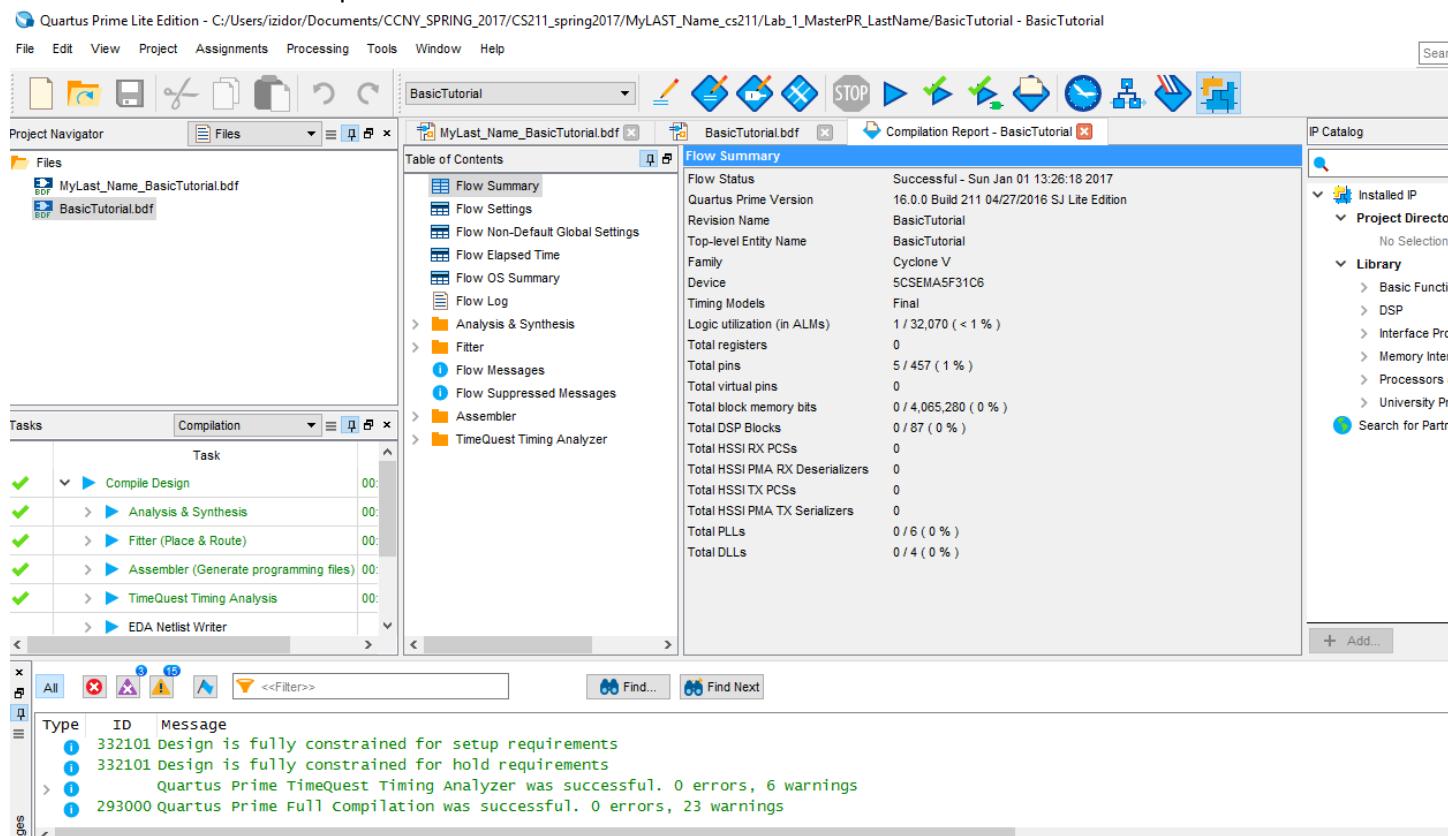
The window below shows the compilation messages. If there are any messages in red, they need to be fixed. **If you have a compilation error, it is most likely of an error in your design diagram due to a misconnected gate, symbol, input/output pin or broken wire.**

The time it takes Quartus to compile your design depends on the speed and configuration of your computer.

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Type	ID	Message
1	332096	The command derive_clocks did not find any clocks to derive. No clocks were created or changed.
1	332068	No clocks defined in design.
1	332154	The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
1	332140	No Setup paths to report
1	332140	No Hold paths to report
1	332140	No Recovery paths to report
1	332140	No Removal paths to report
1	332140	No Minimum Pulse Width paths to report
1	332102	Design is not fully constrained for setup requirements
1	332102	Design is not fully constrained for hold requirements
> 1		Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
> 1	293000	Quartus Prime Full Compilation was successful. 0 errors, 13 warnings

This is result of correct compilation:



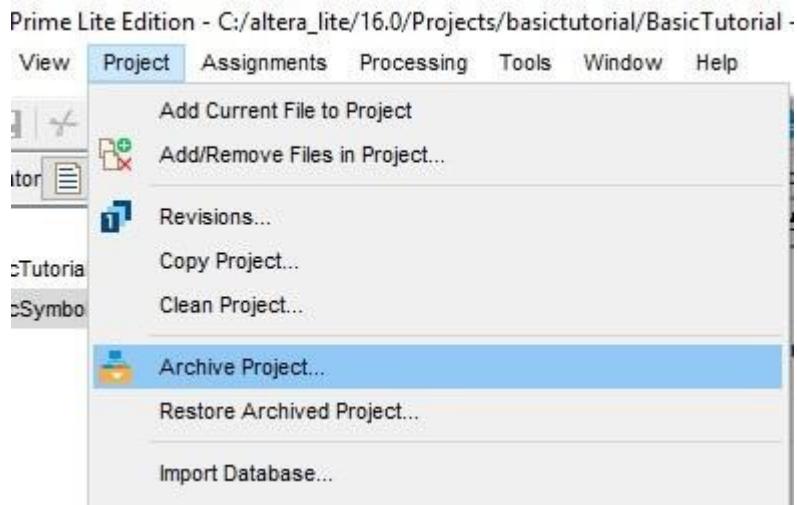
Once you compile, you need to carry out a simulation. Please refer to the Simulation instructions in part 2 of this tutorial.

Save your project (**File > Save Project**).

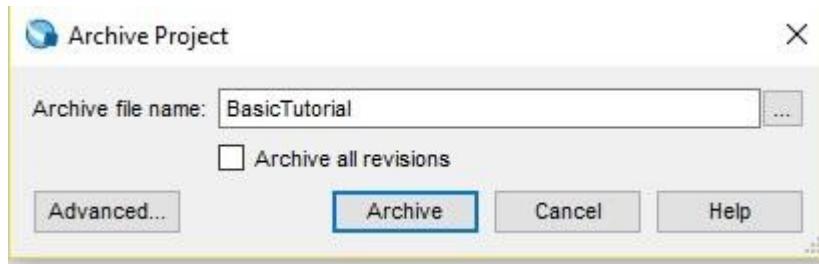
Quartus provides a means to archive the files into a small Quartus archival which is convenient for transfer to a flash drive or uploading to your email. You can restore the files from this archival on a different machine or simply keep these archives as a backup for your designs. To do this, first check whether all the required files are present in the project (**Project > Add/Remove files in Project**).

To archive, click **Project > Archive Project**.

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This results in the following popup window:

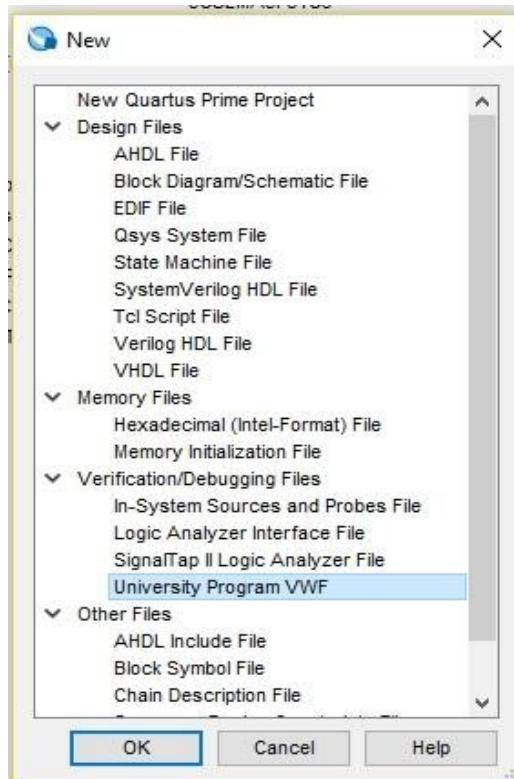


Enter a name for your Archive file and hit **Archive**.

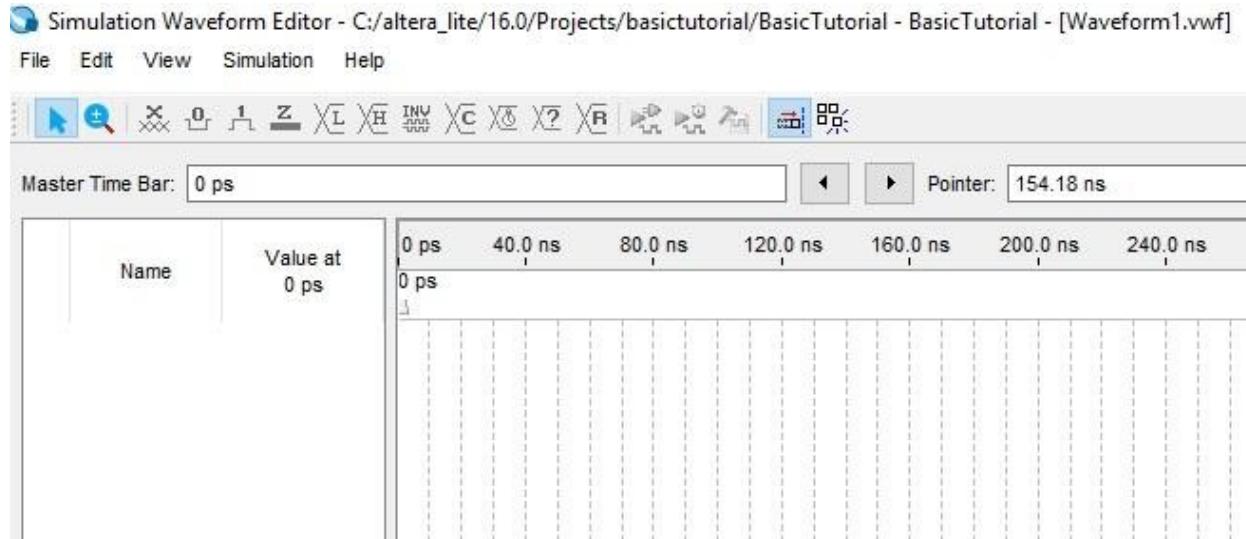
All the relevant files for the project will be automatically included and archived. You can locate the archived file as your project name.qar (Quartus II Archive File) in the directory where the project was initially created. To restore, open Quartus and click **Project > Restore Archived file**. Browse to locate the .qar file and then set a restore directory.

PART 2. Circuit simulation

Once you have your compiled your file with your circuit design, it is time to simulate it.
Go to **File > New... > University Program VWF** and then hit **OK**. (VWF stands for Vector Waveform File)

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You should now get the following screen. It consists of two main panes, the left pane is where you specify your inputs and outputs of your circuit, and the right pane is the waveform editor.



Go to File > Save as... and save this new file as basictutorial_simulation.vwf

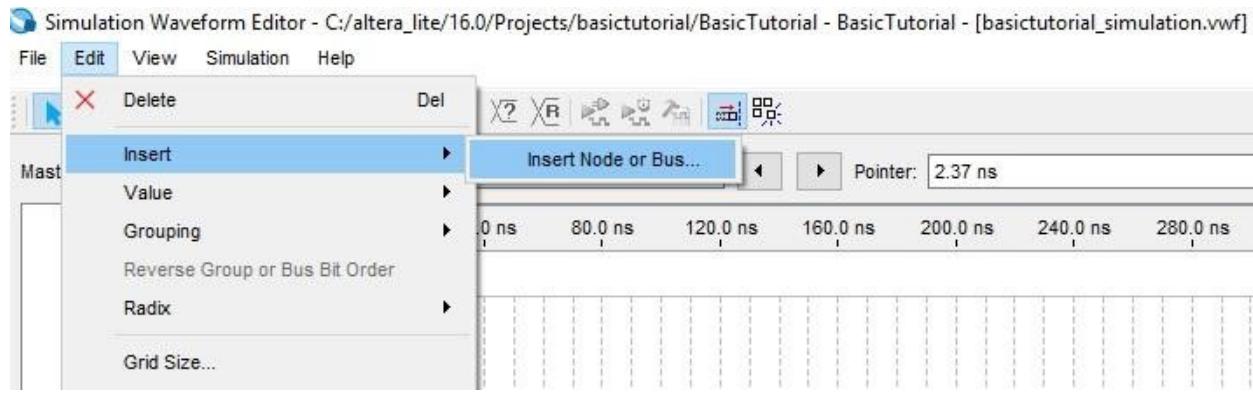
If you are following this tutorial directly from the previous part, your top-level design should be the file that contains the symbol with four inputs (IN_A, IN_B, IN_C, IN_D) and one output (OUT_Z). Otherwise,

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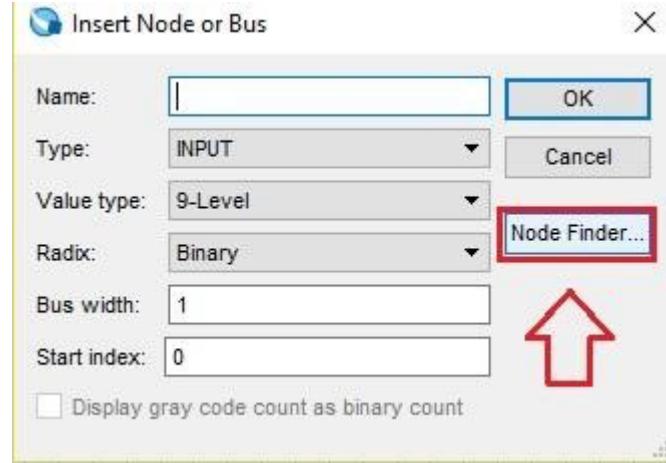
you should first open the project that contains the file you need to simulate, and then set the file to be simulated as top-level and compile following the instructions described in part 2 of this tutorial.

Before editing the waveform, we need to locate the desired signals that are implemented in the circuit. Quartus refers to the signals as “nodes”, and so they can be input nodes or output nodes.

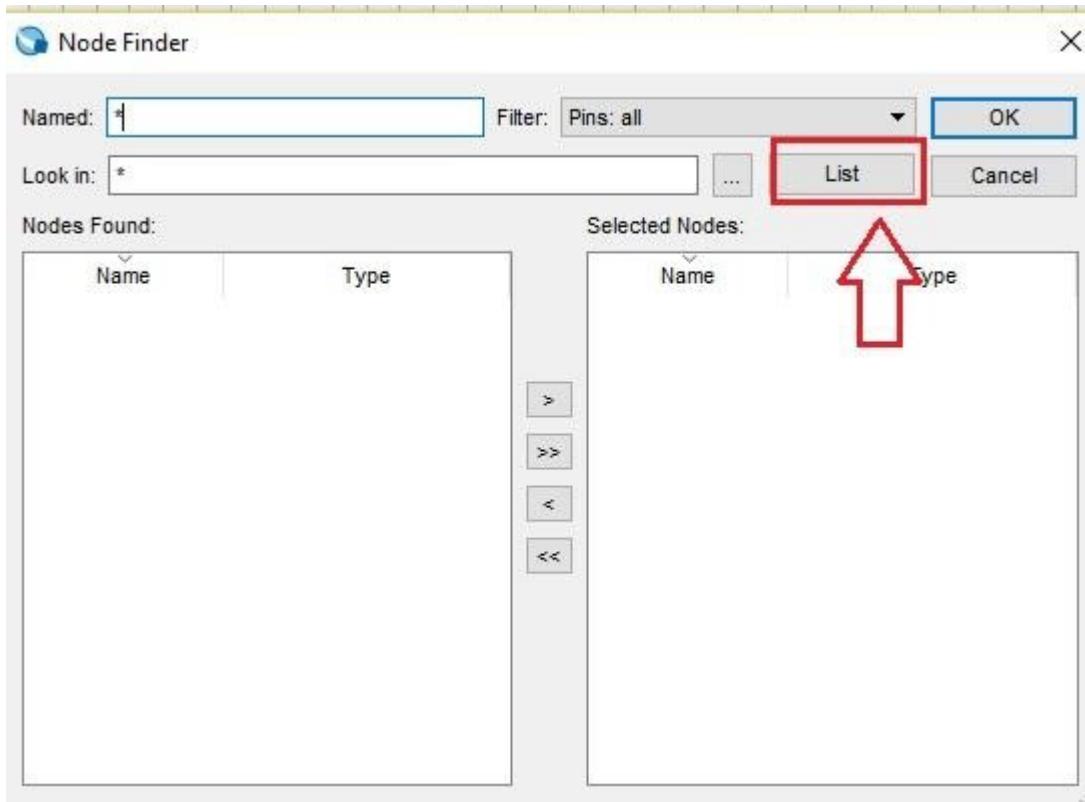
To include the nodes in the waveform editor go to **Edit > Insert > Insert Node or Bus**. (Alternatively, you can also right click the empty pane on the left and select Insert Node or Bus).



Click the **Node Finder** button.

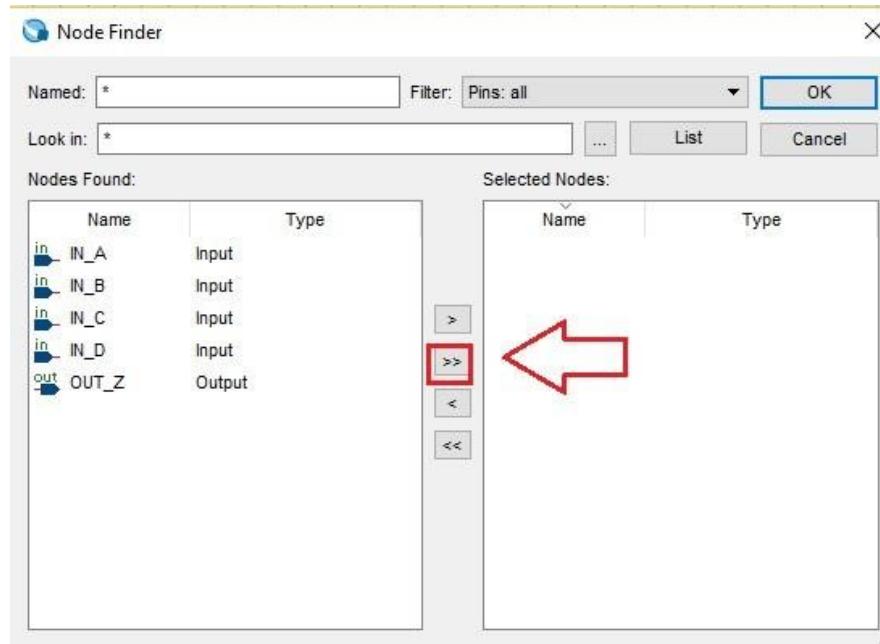


The Node Finder window appears. In our circuit, we are interested only in the nodes that appear on the pins (external connections in the circuit board). Therefore, in the Filter dropdown menu choose **Pins: all**, and then click the **List** button.

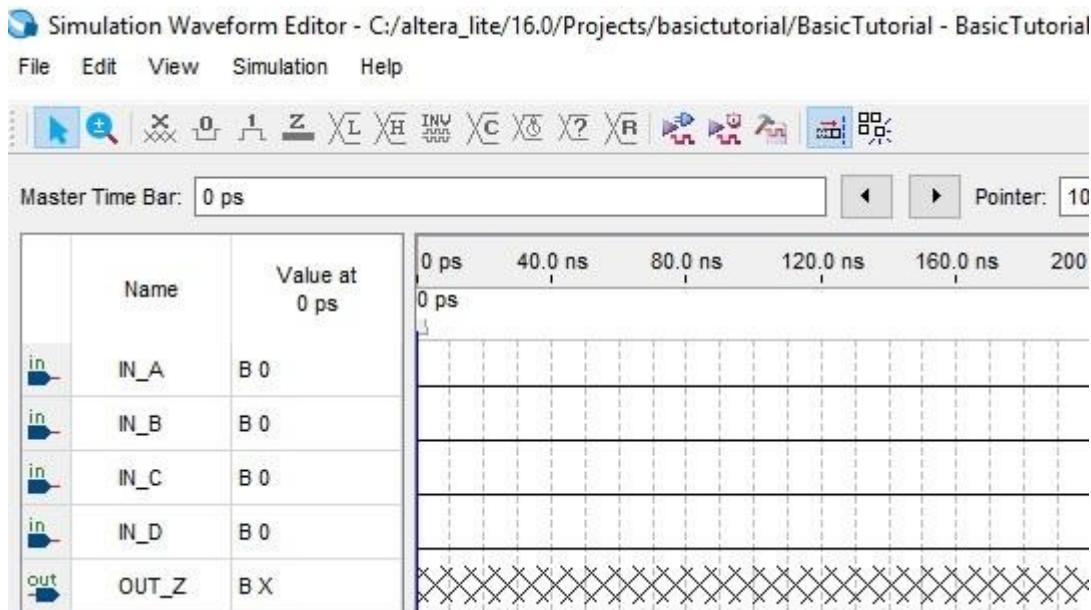
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This will list all the pins in the Nodes Found field on the left of the Node Finder window. Select all the pins and click the > button. Alternatively, you can also hit the >> button without having to select all the pins first, this will select all the pins and put them in the Selected Nodes field on the right. After you are done, hit OK to exit this popup window, and then OK again to go back to the main simulation window.

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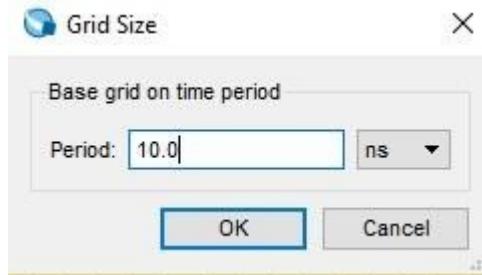


You should now have your right pane populated a waveform as shown in the picture. All input signals are at logic level 0 and the output OUT_Z is shown as undefined (depicted in crosshatch pattern).



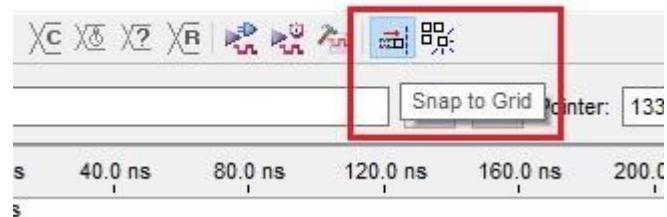
Now we need to draw the input waveforms on the right pane. Before we start drawing waveforms, we need to adjust our grid. Go to **Edit > Grid Size** and give it an input value of 10 ns.

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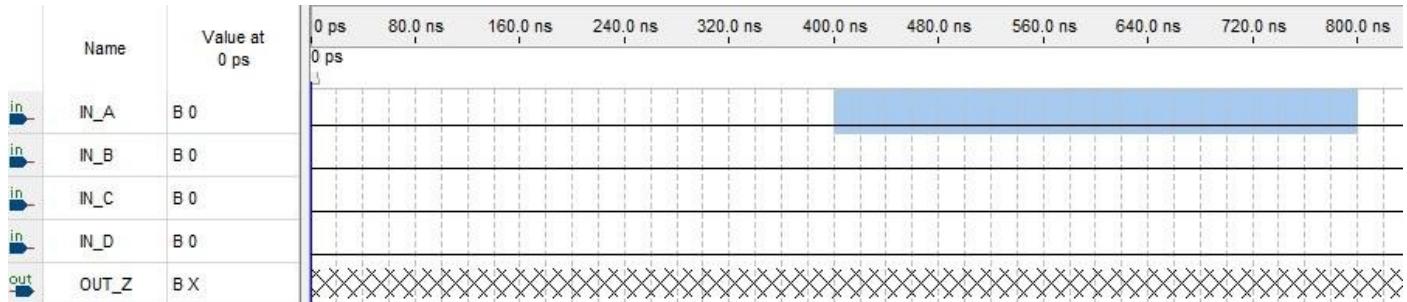
To make it easier to draw your waveform, make sure you have the **Snap to grid** option activated.

a_lite/16.0/Projects/basictutorial/BasicTutorial - BasicTutorial

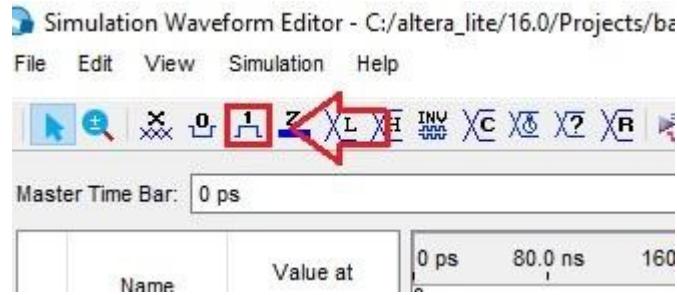


We are ready to start drawing waveforms now. This can be done in different ways. The most common way is to highlight a specific time range and specify the value of the signal. For instance, click the mouse on the IN_A waveform row in a cell near the 400ns and drag the mouse to the 800ns point.

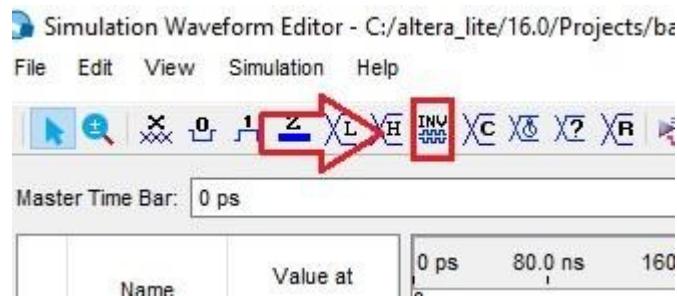
This will select the interval and it will be highlighted in blue, as shown below.



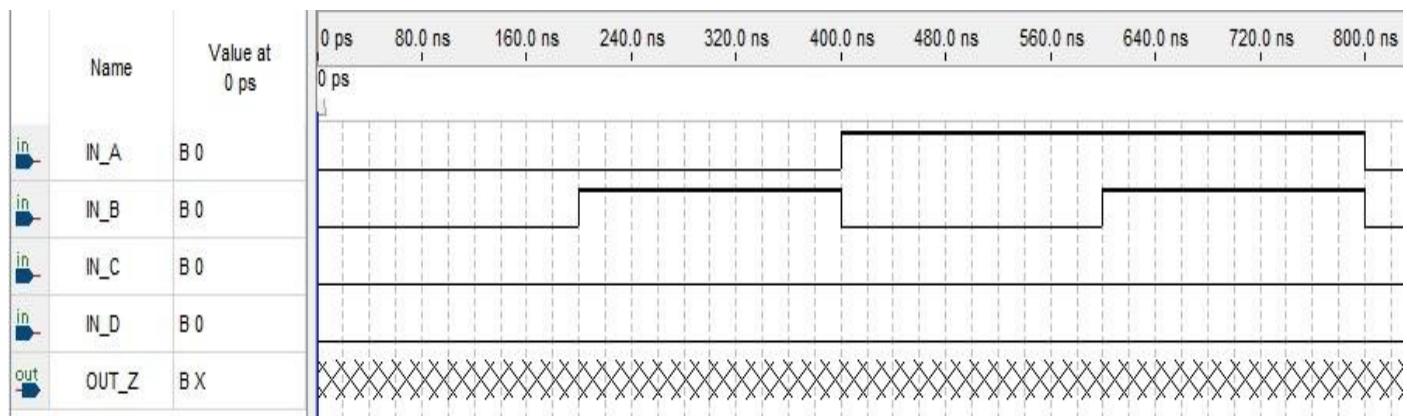
Now it is time to give this input a value, click on the **Forcing High (1)** icon to give this interval a value of 1.

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Another way to do this is using the **Invert** icon. If the value of a waveform a selected interval is 0 it will turn it into 1 and vice versa. Select the interval on IN_B from 200 to 400ns and click the **Invert** icon. Now, select the interval on IN_B from 600 to 800 and click the **Invert** icon once again.

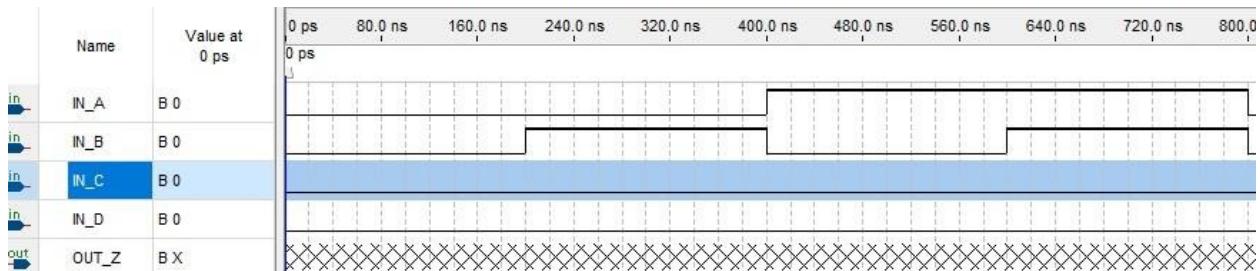


Your waveform should look like this so far:

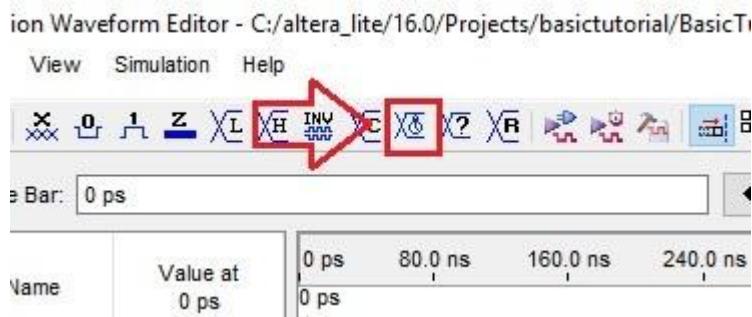


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For IN_C we will use a different approach. This signal will alternate between the logic values 0 and 1 at each 100 ns interval. This is usually the pattern of a clock that is used in many logic circuits. If your input has a defined constant pattern such of a clock, instead of editing individual intervals you can edit the whole input at once. Click on the IN_C input from the left pane; it will select the whole row:



Now click the Overwrite Clock button



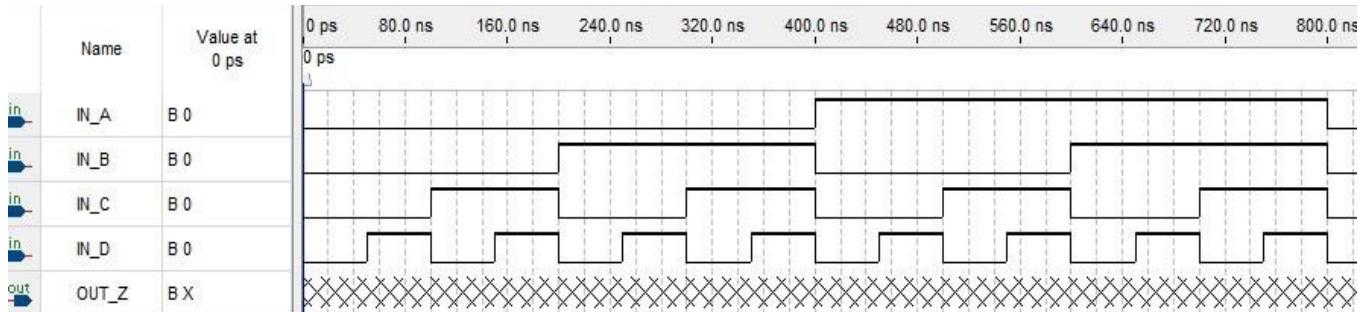
A screen will pop up. Give it the following values:

Period: 200 ns

Duty cycle %: 50

This basically means that we will take the waveform at every 200 ns and within that timeframe it will have a logic value of 0 for half of it (or 50%) and for the other half it will have the opposite value of 1. Do the same for IN_D: Click on IN_D to select the whole row, click on the Clock button but this time give the period a value of 100 ns.

In the end, you should have a waveform like this:

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This configuration basically covers all possible combinations of input values (0 and 1) that could happen among all inputs from A to D.

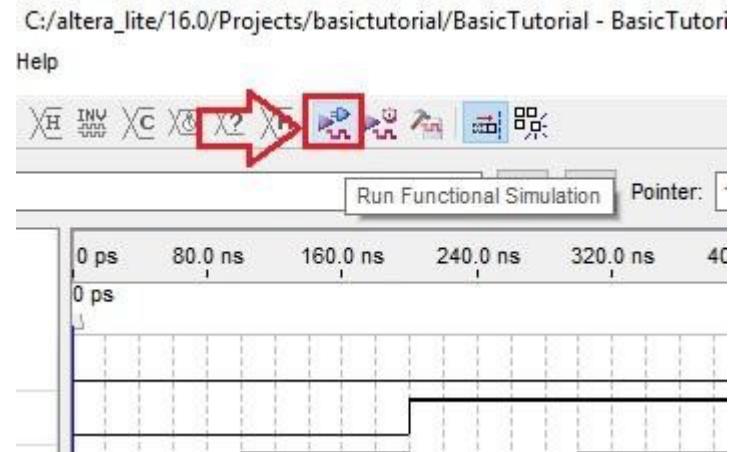
There are two types of simulation available: [Functional Simulation](#) and [Timing Simulation](#). We will explain both now.

Functional Simulation simply tests the logic "functional" operation of the circuit. There is no consideration for delay through the internal logic or the routing delay paths associated with where the placer and the router interconnect things. It simply allows you to see that what you think you are coding provides the results you are intending.

With **Timing Simulation**, the delay associated with the logic elements and the interconnected routing are taken into consideration (based on the speed grade of the chip selected); therefore, the results you obtain in your waveform will differ from what your logic tables tell you.

In this course, we will be doing functional simulations.

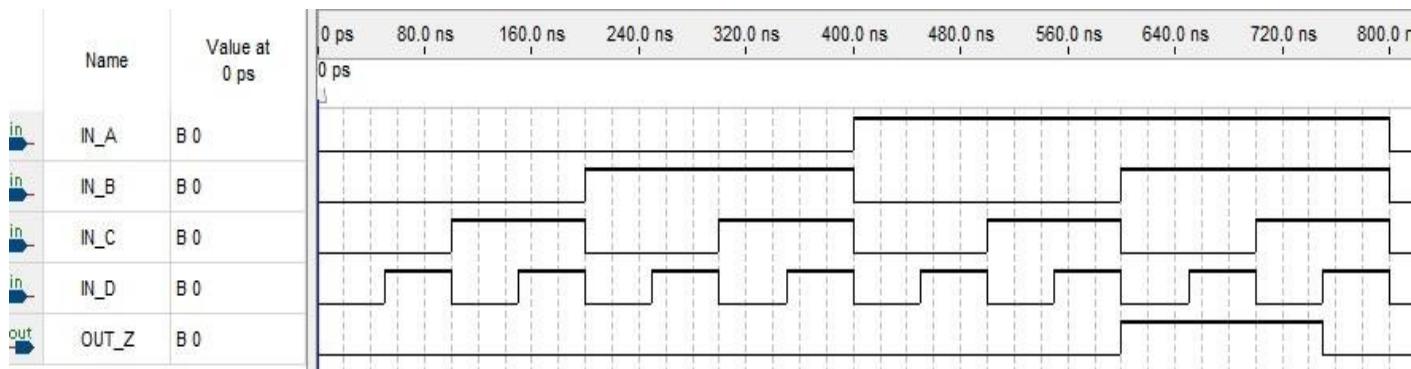
To do a functional simulation, go to **Simulation > Run Functional Simulation**, or click the **Run Functional Simulation** icon.



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A pop-up window will show the progress of the simulation then automatically close when it is done. If it finds any errors, it will show a notification. A second Simulation Waveform window will open afterwards depicting the result of the simulation, as shown below



The output waveform is **read-only**, so any changes in simulation have to be done by modifying the basictutorial_simulation.vwf file and repeating the simulations process. Here you can check the correctness of our designs by checking the values of the inputs and the corresponding output value generated at the specific intervals. For this circuit, the output will be asserted or high in three different scenarios: when A and B are 1; when A, B and C are 1; or when A, B and D are 1; other configurations of inputs yield to 0 output.

PART 3. PIN assignments

After you are done simulating, you should be ready to load your circuit design onto the DE1-SOC board., if available. This semester we are not using DE1-soc board. Generally, you should write a text file with the names of your inputs and the names of the pins in the board you want them to be mapped to.

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PIN ASSIGNMENTS

You can view the pin assignments in the User Manual for the DE1-SOC board which can be download with this link. If the link does not work, make an internet search for DE1-SOC User Manual.

<http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=167&No=836&PartNo=4>

Once you have the manual, check from page 22 up to page 27. You will find the assignments for the clock, inputs and outputs.

You can make a text file that contains your pin assignments and save it with any name you want.

```
To , Location my_pin_name, PIN_AB12  
my_bus[0], PIN_AC12  
my_bus[1], PIN_AF9
```

The figure above shows how you would write your pin assignments file. You start the file with “To, Location.” On each line, you put the name of the pin you want to assign to the left, and the pin code of the DE1-SOC Board to the right, separated by a comma.

If the pin you want to assign is a bus or vector, you can assign each bit of the bus by writing the name of the bus with the bit you want to assign in square brackets.

Usually, when you assign an input pin, it will be assigned to the switch or pushbutton. An output pin would usually be assigned to an LED or the seven-segment displays.

Following the example from part 2 of this tutorial, the pin assignment text file for our designed circuit may look like this:

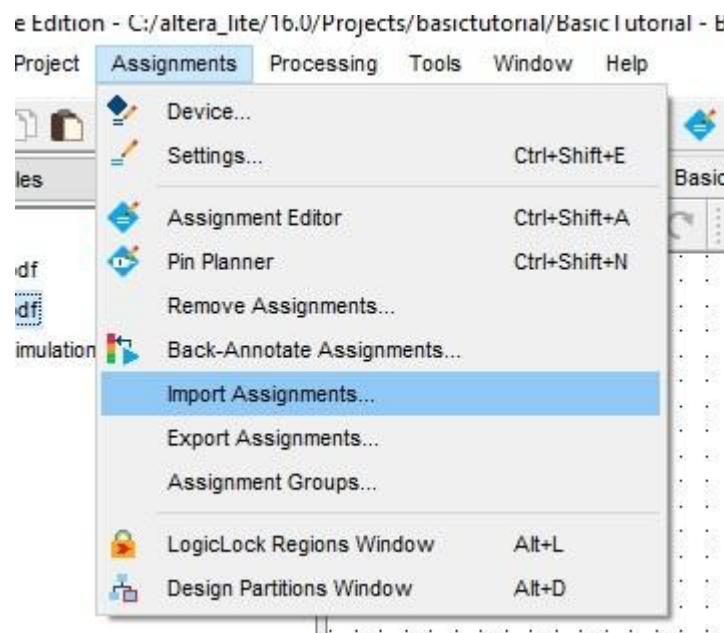
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To, Location

IN_A, PIN_AB12
IN_B, PIN_AC12
IN_C, PIN_AF9
IN_D, PIN_AF10
OUT_Z, PIN_V16

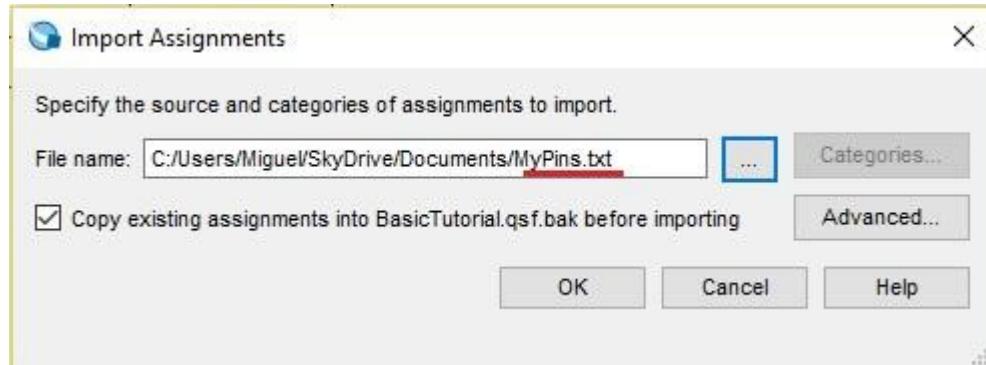
Here, PIN_AB12 to PIN_AF10 refer to the rightmost switches in the DE1-SOC board. The output is mapped to the rightmost RED LED light (PIN_V16).

To use the pin assignments text file that you wrote, you need to import it to your project.
In Quartus go to: **Assignments >> Import Assignments...**

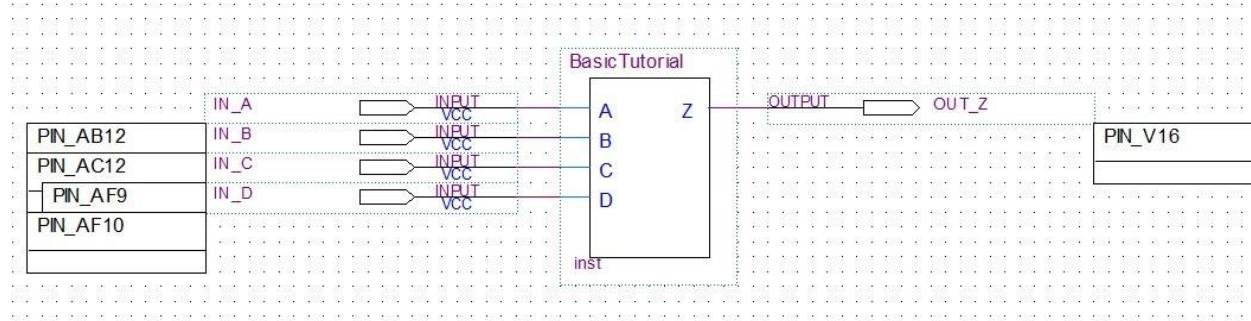


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After opening the dialogue for importing assignments, set the file location for your pin assignments text file and press **OK**.



Your pins should now show on your block diagram file if you compile.



Compile again.

You can now load your circuit onto the DE1-SOC Board

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