

Printout

Task 1

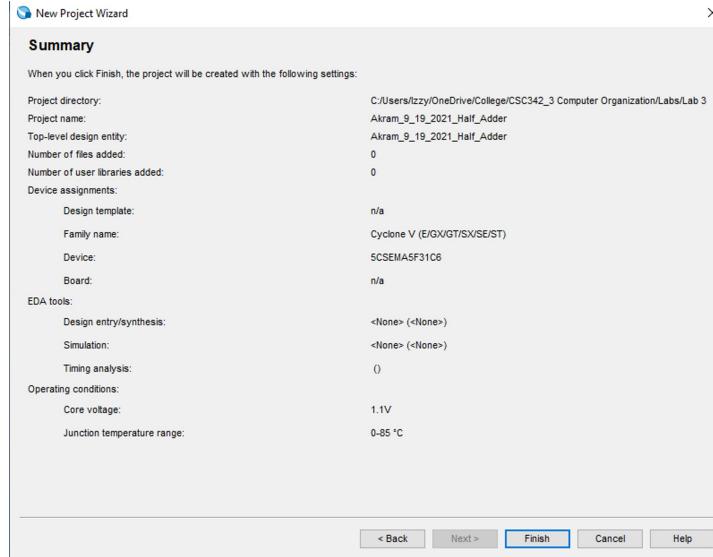


Fig 1. Creating new project for half adder (all projects will be in the same directory)

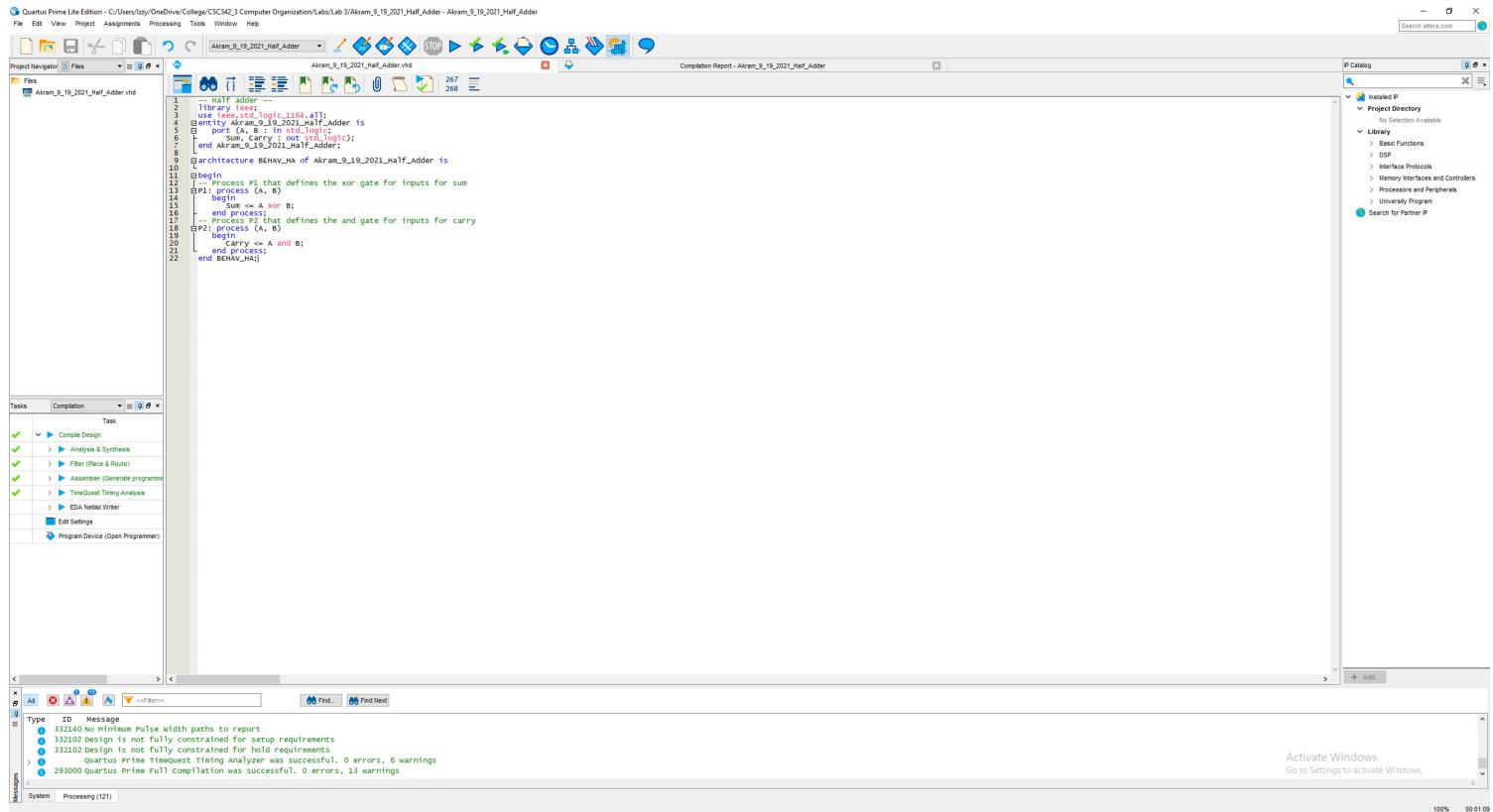


Fig 2. File > New > VHDL File > Input Code > Save > Set "Akram_9_19_2021_Half_adder" as Top-Level Entity > Compile

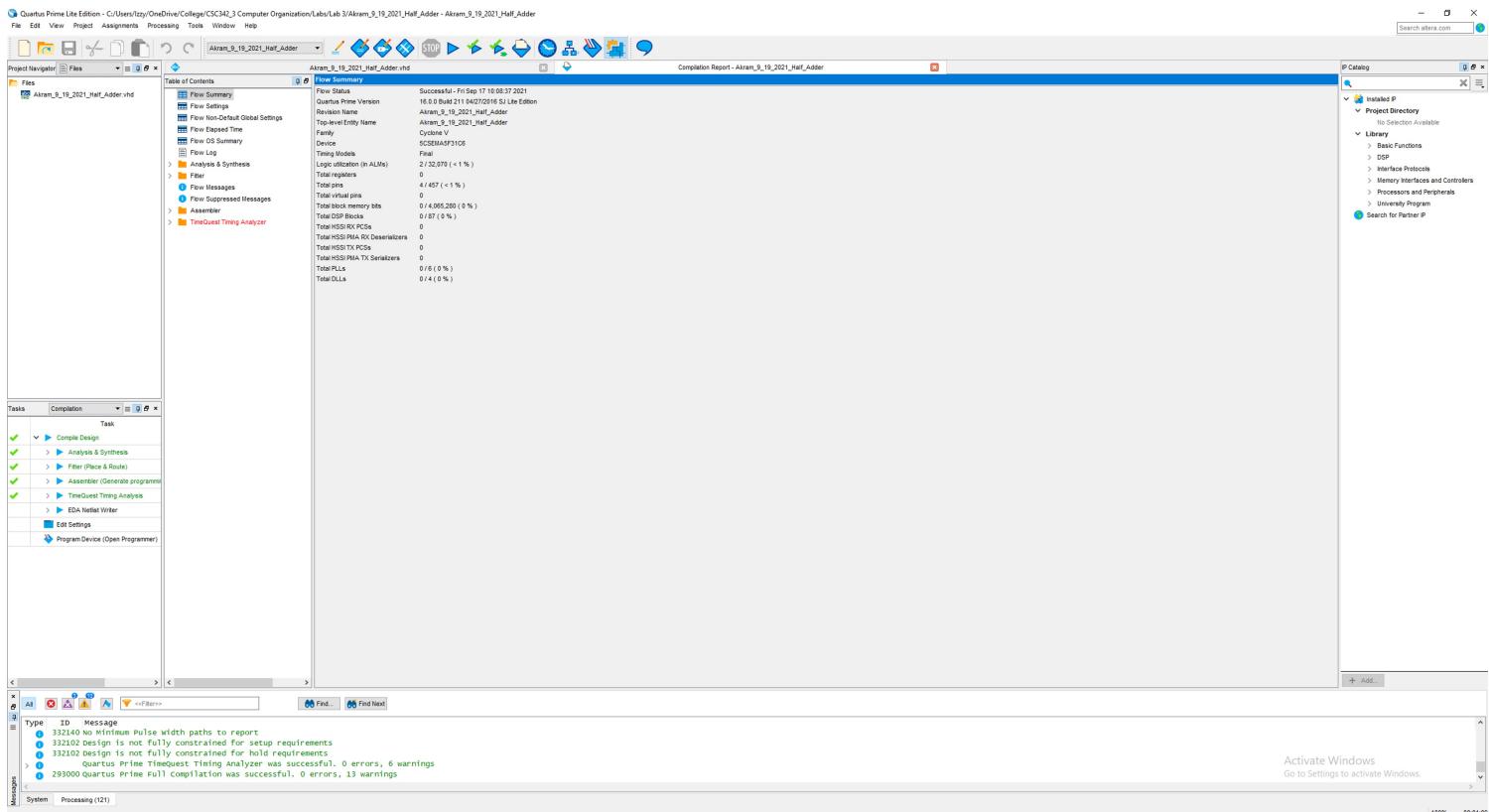


Fig 3. Compiled successfully

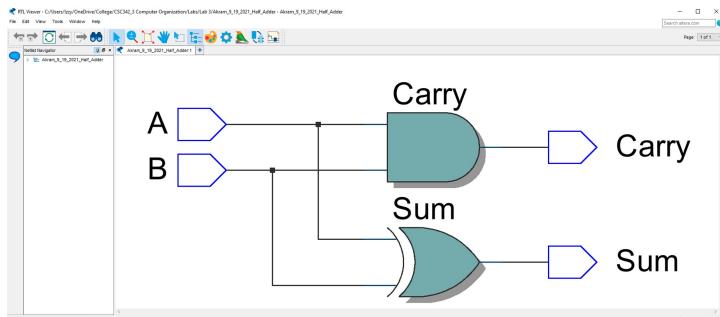


Fig 4. Tools > Netlist Viewers > RTL Viewer ... for verification

Task 2

New Project Wizard

Summary

When you click Finish, the project will be created with the following settings:

Project directory:	C:\Users\Izzy\OneDrive\College\CSC342_3 Computer Organization\Labs\Lab 3
Project name:	Akram_9_19_2021_1_Bit_Full_Adder
Top-level design entity:	Akram_9_19_2021_1_Bit_Full_Adder
Number of files added:	0
Number of user libraries added:	0
Device assignments:	n/a
Design template:	n/a
Family name:	Cyclone V (E/GX/GT/SX/SE/ST)
Device:	5CSEMA5F31C8
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	0
Operating conditions:	
Core voltage:	1.1V
Junction temperature range:	0-85 °C

< Back Next > Finish Cancel Help

Fig 5. Creating new project for full adder within the same directory as the previous half adder (we will be using that as a component).

Quartus Prime Lite Edition - C:\Users\itzv\OneDrive\College\CSC342_3 Computer Organization\Labs\Lab 3\Akram_9_19_2021_1_Bit_Full_Adder - Akram_9_19_2021_1_Bit_Full_Adder

File Edit View Project Assignments Processing Tools Windows Help

Akram_9_19_2021_1_Bit_Full_Adder - Akram_9_19_2021_1_Bit_Full_Adder.vhd

Compilation Report - Akram_9_19_2021_1_Bit_Full_Adder

Project Navigator Files

```

1  --> FULL adder --
2  library IEEE;
3  use IEEE.STD.TEXTIO.TEXTIO.all;
4  entity Akram_9_19_2021_1_Bit_Full_Adder is
5    port (A, B, Cin : in STD.TEXTIO.TEXTIO.all;
6          Sum, Carry : out STD.TEXTIO.TEXTIO.all);
7  end entity;
8
9  architecture BEHAV_FA of Akram_9_19_2021_1_Bit_Full_Adder is
10
11    signal S1, C1, C2 : STD.TEXTIO.TEXTIO.all;
12    component Akram_9_19_2021_Half_Adder
13    port (A, B, Cin : in STD.TEXTIO.TEXTIO.all;
14          Sum, Carry : out STD.TEXTIO.TEXTIO.all);
15    end component;
16
17    begin
18      HAD: Akram_9_19_2021_Half_Adder
19        port map (A, B, Cin, S1, Sum, C2);
20      HAD: Akram_9_19_2021_Half_Adder
21        port map (Cin, S1, Sum, C2);
22    end BEHAV_FA;

```

IP Catalog

Tasks Compilation

Task

- ✓ Complete Design
- ✓ Analysis & Synthesis
- ✓ Filter (Place & Route)
- ✓ Assembler (Generate programs)
- ✓ TimeQuest Timing Analysis
- ✓ EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Messages

All Find... Find Next

Type ID Message

- 332140 No Minimum Pulse width paths to report
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timequest Timing Analyzer was successful. 0 errors, 6 warnings
- 293000 quartus prime full compilation was successful. 0 errors, 14 warnings

Activate Windows
Go to Settings to activate Windows.

Fig 6. File > New > VHDL File > Input Code (using the half adder as a component) > Set as Top-level entity > Compile

Quartus Prime Lite Edition - C:\Users\itzv\OneDrive\College\CSC342_3 Computer Organization\Labs\Lab 3\Akram_9_19_2021_1_Bit_Full_Adder - Akram_9_19_2021_1_Bit_Full_Adder

File Edit View Project Assignments Processing Tools Windows Help

Akram_9_19_2021_1_Bit_Full_Adder - Akram_9_19_2021_1_Bit_Full_Adder.vhd

Compilation Report - Akram_9_19_2021_1_Bit_Full_Adder

Project Navigator Files

Table of Contents

Flow Status

Successful / Fri Sep 17 10:14:23 2021

Flow Version

Quartus Prime Version 16.0 Build 211 04/27/2016 SJ Lite Edition

Revision Name

Akram_9_19_2021_1_Bit_Full_Adder

Top-level Entity Name

Akram_9_19_2021_1_Bit_Full_Adder

Cyclone V

Device

5CSEMA5F10C

Timing Model

Final

Logo location (In ALMs)

2732370 (+ 1 %)

Total registers

0

Total pins

5 / 457 (1 %)

Total virtual pins

0

Total memory bits

0 / 4005200 (0 %)

Total DSP Blocks

0 / 87 (0 %)

Total HSD RX PCMs

0

Total HSD PMA RX Deserializers

0

Total HSD PMA TX Serializers

0

Total HSD PMA TX Deserializers

0

Total PLLs

0 / 6 (0 %)

Total DLLs

0 / 4 (0 %)

IP Catalog

Tasks Compilation

Task

- ✓ Complete Design
- ✓ Analysis & Synthesis
- ✓ Filter (Place & Route)
- ✓ Assembler (Generate programs)
- ✓ TimeQuest Timing Analysis
- ✓ EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Messages

All Find... Find Next

Type ID Message

- 332140 No Minimum Pulse width paths to report
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timequest Timing Analyzer was successful. 0 errors, 6 warnings
- 293000 quartus prime full compilation was successful. 0 errors, 14 warnings

Activate Windows
Go to Settings to activate Windows.

Fig 7. Compilation successful

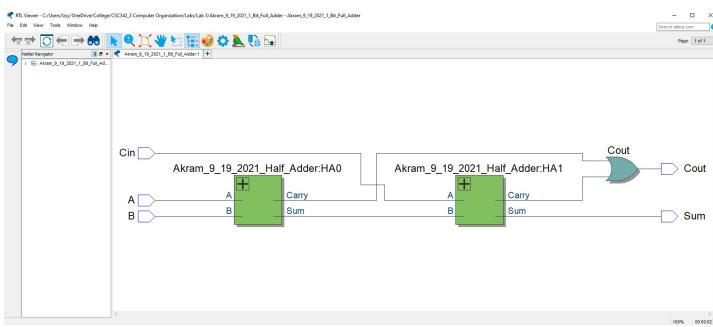


Fig 8. Tools > Netlist Viewers > RTL Viewer ... for verification

Task 3

New Project Wizard

Summary

When you click Finish, the project will be created with the following settings:

Project directory:	C:\Users\lizzy\OneDrive\College\CSC342_3 Computer Organization\Lab\Lab 3\Akram_9_19_2021_4_Bit_Adder
Project name:	Akram_9_19_2021_4_Bit_Adder
Top-level design entity:	Akram_9_19_2021_4_Bit_Adder
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone V (E/GX/GT/SX/SE/ST)
Device:	SCSEMA5F31C8
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> <None>
Simulation:	<None> <None>
Timing analysis:	(0)
Operating conditions:	
Core voltage:	1.1V
Junction temperature range:	0-85 °C

< Back Next > **Finish** Cancel Help

Fig 9. Creating a new project for 4-bit adder within the same directory as the other projects

```

library IEEE;
use IEEE.STD.TEXT.all;
entity Akram_9_19_2021_4_Bit_Adder is
    port (A, B : in STD.TEXT_VECTOR(3 downto 0);
          Cin : in STD.TEXT_VECTOR(0 downto 0);
          Sum : out STD.TEXT_VECTOR(3 downto 0);
          Cout : out STD.TEXT_VECTOR(0 downto 0));
end Akram_9_19_2021_4_Bit_Adder;

architecture BEHAV_IIBA of Akram_9_19_2021_4_Bit_Adder is
    signal C : STD.TEXT_VECTOR(4 downto 0);
    component Akram_9_19_2021_1_bit_Full_Adder
        port (A, B : in STD.TEXT_VECTOR(1 downto 0);
              Cin : in STD.TEXT_VECTOR(0 downto 0);
              Sum, Cout : out STD.TEXT_VECTOR(1 downto 0));
    end component;
begin
    F00: Akram_9_19_2021_1_bit_Full_Adder
        port map (A(3), B(3), Cin(0), Sum(3), Cout(0));
    F01: Akram_9_19_2021_1_bit_Full_Adder
        port map (A(2), B(2), Cin(1), Sum(2), Cout(1));
    F02: Akram_9_19_2021_1_bit_Full_Adder
        port map (A(1), B(1), Cin(2), Sum(1), Cout(2));
    F03: Akram_9_19_2021_1_bit_Full_Adder
        port map (A(0), B(0), Cin(3), Sum(0), Cout(3));
end BEHAV_IIBA;

```

Fig 10. File > New > VHDL File > Typing Code (using the full adder as a component) > Set as Top-level entity > Compile

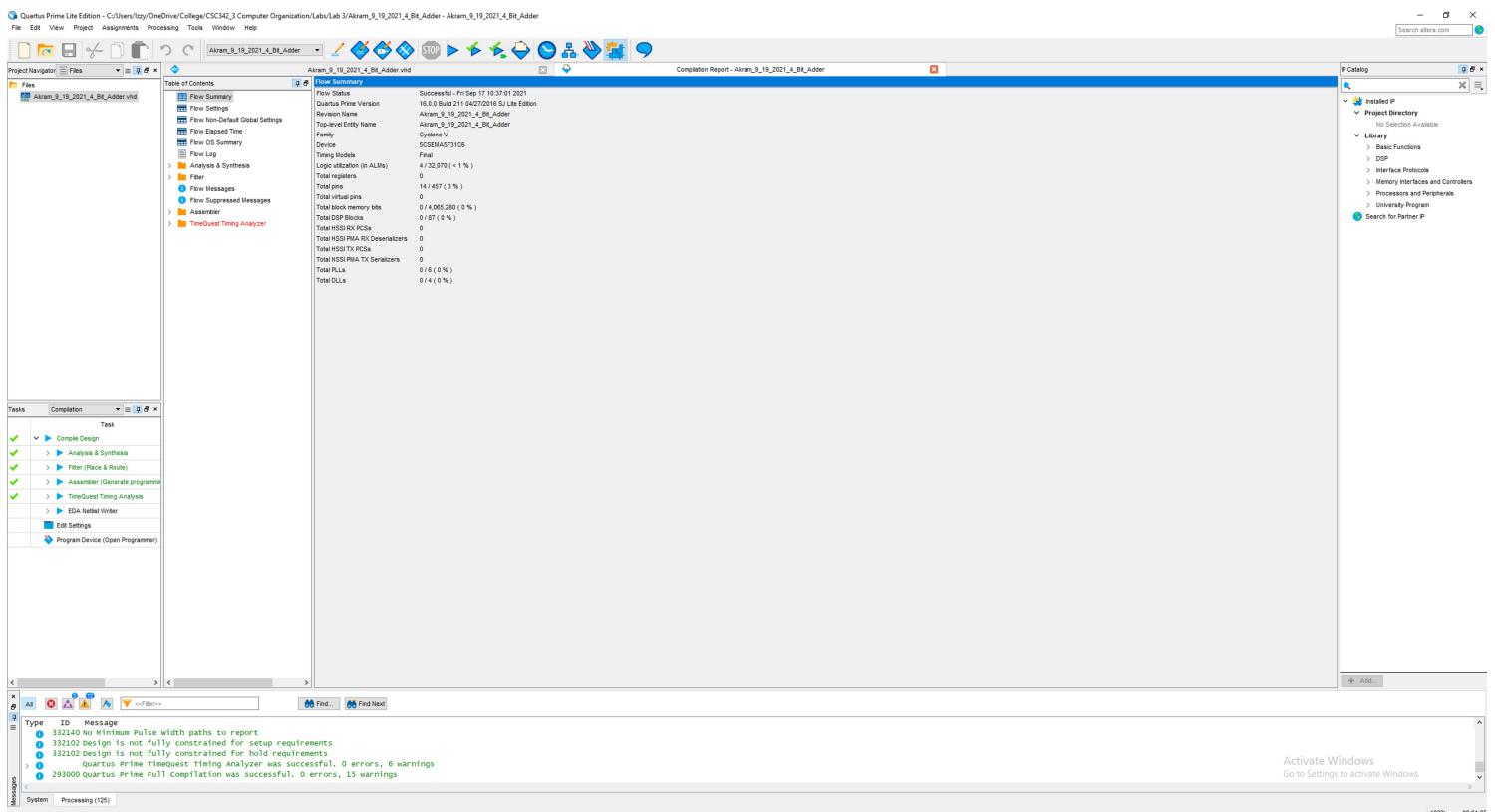


Fig 11. Compiled successfully

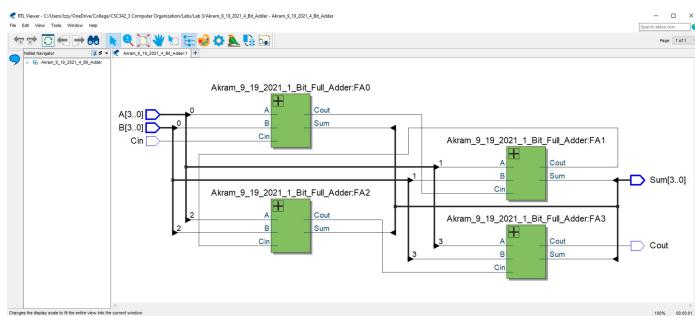


Fig 12. Tools > Netlist Viewers > RTL Viewer ... for verification

Task 4

New Project Wizard

Summary

When you click Finish, the project will be created with the following settings:

Project directory:	C:/Users/izzy/OneDrive/College/CSC342_3 Computer Organization/Labs/Lab 3
Project name:	Akram_9_19_2021_4_Bit_Add_Sub
Top-level design entity:	Akram_9_19_2021_4_Bit_Add_Sub
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone V (E/GX/GT/SX/SE/ST)
Device:	SCSEMA5F31C6
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	()
Operating conditions:	
Core voltage:	1.1V
Junction temperature range:	0-85 °C

< Back Next > **Finish** Cancel Help

Fig 13. Creating a new project for 4-bit add/sub within the same directory as the other projects

Quartus Prime Lite Edition - C:\Users\itzv\OneDrive\College\CS342_3 Computer Organization\Labs\Lab 3\Akram_9_19_2021_4_Bit_Add_Sub - Akram_9_19_2021_4_Bit_Add_Sub

File Edit View Project Assignments Processor Tools Window Help

Akram_9_19_2021_4_Bit_Add_Sub.vhd

Compilation Report - Akram_9_19_2021_4_Bit_Add_Sub

IP Catalog

```

1  library IEEE;
2  use IEEE.STD.TEXT.all;
3  use IEEE.STD.TEXT.TEXT.all;
4  use IEEE.STD.TEXT.TEXT.TEXT.all;
5  use IEEE.STD.TEXT.TEXT.TEXT.TEXT.all;
6  use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.all;
7  use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
8  use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
9  use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
10 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
11 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
12 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
13 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
14 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
15 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
16 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
17 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
18 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
19 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
20 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
21 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
22 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
23 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
24 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
25 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
26 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
27 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
28 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
29 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
30 use IEEE.STD.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.TEXT.all;
31 end BEHAV_ABAB;

```

Tasks Compilation

- Task
- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Assembler Generate program
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Messages

All Find... Find Next

Type ID Message

- 332140 No minimum pulse width paths to report
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 13 warnings

Activate Windows Go to Settings to activate Windows.

Fig 14. File > New > VHDL File > Typing Code > Set as Top-level entity > Compile

Quartus Prime Lite Edition - C:\Users\itzv\OneDrive\College\CS342_3 Computer Organization\Labs\Lab 3\Akram_9_19_2021_4_Bit_Add_Sub - Akram_9_19_2021_4_Bit_Add_Sub

File Edit View Project Assignments Processor Tools Window Help

Akram_9_19_2021_4_Bit_Add_Sub.vhd

Compilation Report - Akram_9_19_2021_4_Bit_Add_Sub

IP Catalog

Table of Contents

Flow Summary

Flow State	Success
Output Prime Version	16.0 Build 211 04/27/2016 SJ Lite Edition
Revision Name	Akram_9_19_2021_4_Bit_Add_Sub
Top-level Entity Name	Akram_9_19_2021_4_Bit_Add_Sub
Flow OS Summary	
Flow Log	
Analysis & Synthesis	
Filter	
Suppressed Messages	
Total Messages	0
Total Suppressed Messages	0
Assembler	
TimeQuest Timing Analyzer	

Flow Summary

Flow State	Success
Output Prime Version	16.0 Build 211 04/27/2016 SJ Lite Edition
Revision Name	Akram_9_19_2021_4_Bit_Add_Sub
Top-level Entity Name	Akram_9_19_2021_4_Bit_Add_Sub
Flow OS Summary	
Flow Log	
Analysis & Synthesis	
Filter	
Suppressed Messages	
Total Messages	0
Total Suppressed Messages	0
Assembler	
TimeQuest Timing Analyzer	

Tasks Compilation

- Task
- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Assembler Generate program
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Messages

All Find... Find Next

Type ID Message

- 332140 No minimum pulse width paths to report
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 13 warnings

Activate Windows Go to Settings to activate Windows.

Fig 15. Compilation successful

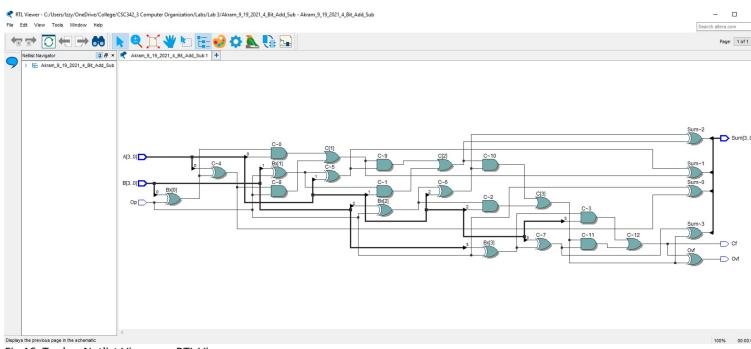


Fig 16. Tools > Nlist Viewers > RTL Viewer

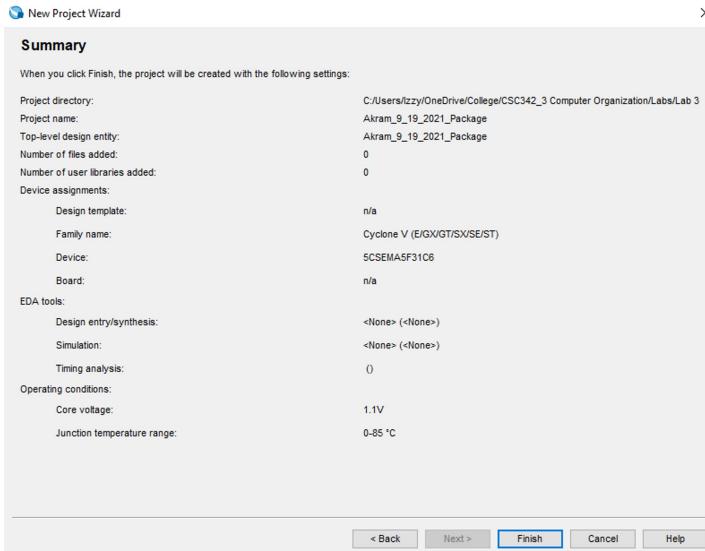


Fig 17. Creating new project for packaging

```

library IEEE;
use IEEE.STD.TEXT.all;
package Akram_9_19_2021_Package is
component Akram_9_19_2021_4_BIT_Adder
port (A, B : in std_logic_vector(3 downto 0);
      Cin : in std_logic;
      Cout : out std_logic;
      CF, OF : out std_logic; -- carry flag, overflow);
end component;

component Akram_9_19_2021_1_Bit_Plus1_Adder
port (A, B : in std_logic;
      Sum : out std_logic);
end component;

component Akram_9_19_2021_1_Bit_Plus1_Half_Adder
port (A, B : in std_logic;
      Cin : in std_logic;
      Sum : out std_logic;
      CF : out std_logic);
end component;

component Akram_9_19_2021_4_BIT_Add_sub
port (A, B : in std_logic_vector(3 downto 0);
      Cin : in std_logic;
      CF, OF, ovf : out std_logic; -- carry flag, overflow);
end component;
end Akram_9_19_2021_Package;

```

Fig 18. File > New > VHDL File > Typing Packaging Code > Save

Task 6

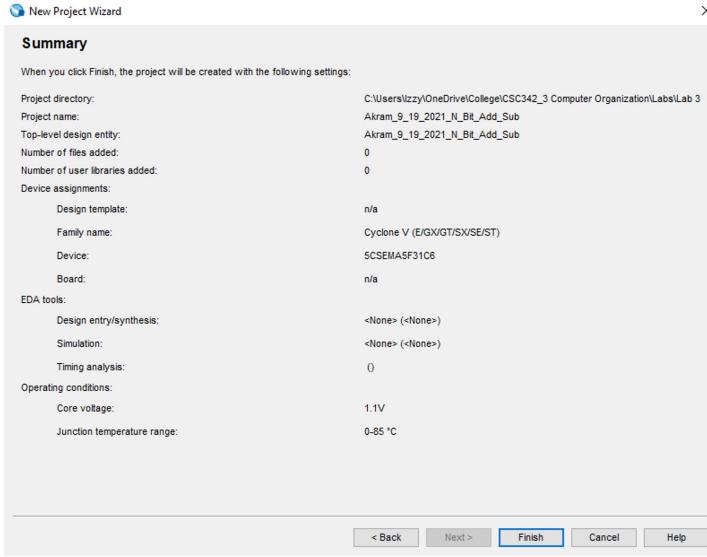


Fig 19. Creating new project for n bit add/sub

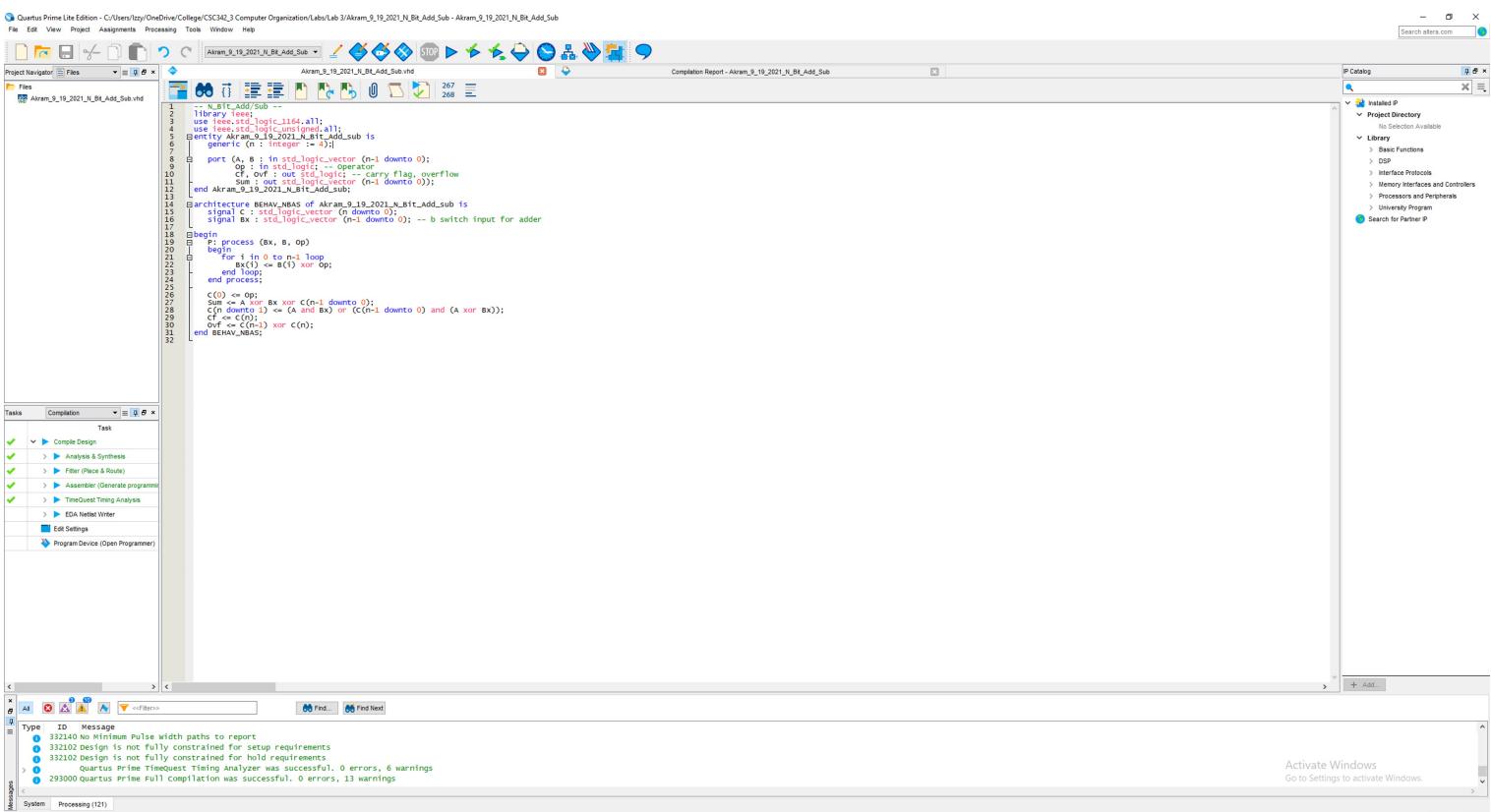


Fig 20. File > New > VHDL File > Typing Code for N-Bit sub/add (in this case, I just edited my 4-bit add/sub file) > Set as Top-level entity > Compile

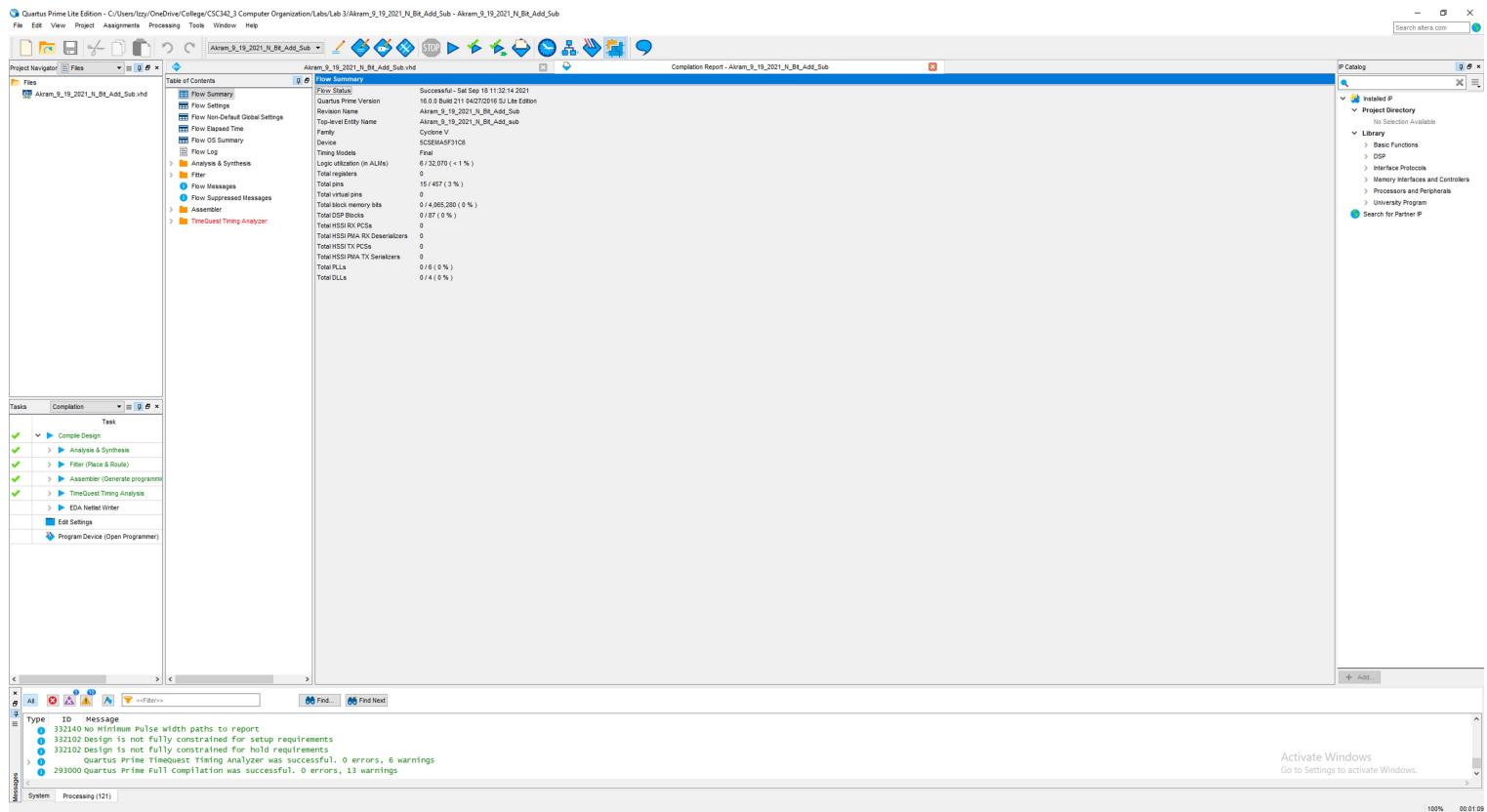


Fig 21. Compilation successful

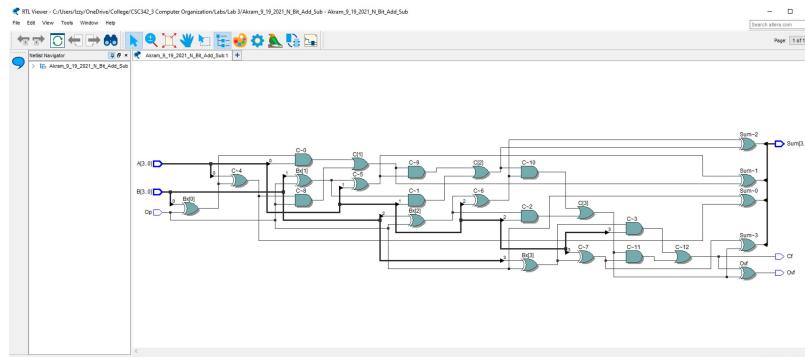


Fig 22. Tools > Netlist Viewers > RTL Viewer

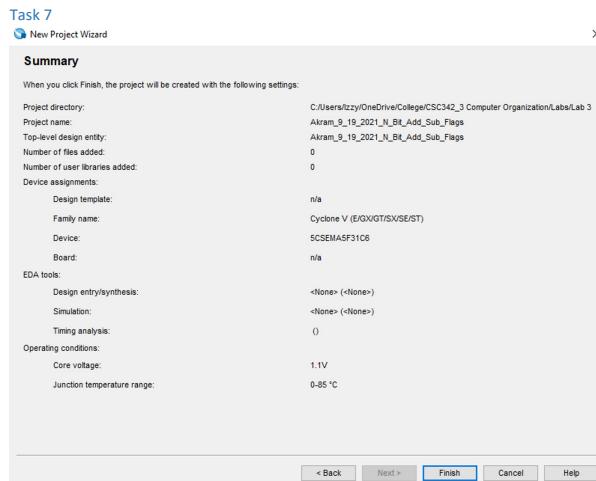


Fig. 23 Creating a new project to add flags Overflow, Negative, and Zero to N-Bit add/sub

Quartus Prime Lite Edition - C:/Users/lzzz/OneDrive/College/CSC342_3 Computer Organization/Labs/Lab 3/Akram_9_19_2021_N_Bit_Add_Sub_Flags - Akram_9_19_2021_N_Bit_Add_Sub_Flags

```

-- N_Bit_Add_Sub_Flags --
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity Akram_9_19_2021_N_Bit_Add_Sub_Flags is
generic (n : integer := 8);
port (A, B : in std_logic_vector(n-1 downto 0);
      op : out std_logic; -- operator
      ovf, Negf, Zerf : out std_logic; -- Carry Flag, overflow, Negative, Zero
      sum : out std_logic_vector(n-1 downto 0));
end Akram_9_19_2021_N_Bit_Add_Sub_Flags;

architecture BEHAVIORAL of Akram_9_19_2021_N_Bit_Add_Sub_Flags is
begin
process (A, B, op)
begin
for i in 0 to n-1 loop
    sum := A(i) < op > B(i);
    if sum >= B(i) then
        ovf := '1';
        Negf := '0';
        Zerf := '0';
    else
        ovf := '0';
        Negf := '1';
        Zerf := '0';
    end if;
end loop;
end process;
begin
op <= A(0) & B(0);
Temp_Sum <= A(0) < op > B(0);
for i in 1 to n-1 loop
    Temp_Sum := Temp_Sum < op > (A(i) & B(i));
    if Temp_Sum >= B(i) then
        ovf <= '1';
        Negf <= '0';
        Zerf <= '0';
    else
        ovf <= '0';
        Negf <= '1';
        Zerf <= '0';
    end if;
end loop;
end BEHAVIORAL;

```

Tasks Compilation > &

Message ID: Message

- 332140 No Minimum Pulse width paths to report
- 332100 Design is not fully constrained for setup requirements
- 332100 Design is not fully constrained for hold requirements
- > 293000 Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
- > 293000 quartus prime full compilation was successful. 0 errors, 13 warnings

Fig 24. File > New > VHDL File > Typing Code for flags (in this case, I just edited my N-bit add/sub file and added a library alongside a temp variable as a signal for sum) > Set as Top-level entity > Compile

Quartus Prime Lite Edition - C:/Users/lzzz/OneDrive/College/CSC342_3 Computer Organization/Labs/Lab 3/Akram_9_19_2021_N_Bit_Add_Sub_Flags - Akram_9_19_2021_N_Bit_Add_Sub_Flags

Flow Summary

Flow Summary

Flow Analysis & Synthesis

Flow Analysis & Synthesis

Flow Timed Simulation

Flow Power

Flow Global Settings

Flow Default Global Settings

Flow Hold Time

Flow OS Summary

Flow Log

Analysis & Synthesis

Analysis & Synthesis

Timing Analysis

Timing Analysis

Assembler

TimeQuest Timing Analyzer

System Processing (121)

Activate Windows
Go to Settings to activate Windows.

Type ID: Message

- 332140 No Minimum Pulse width paths to report
- 332100 Design is not fully constrained for setup requirements
- 332100 Design is not fully constrained for hold requirements
- > 293000 Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
- > 293000 quartus prime full compilation was successful. 0 errors, 13 warnings

Fig 25. Compilation successful

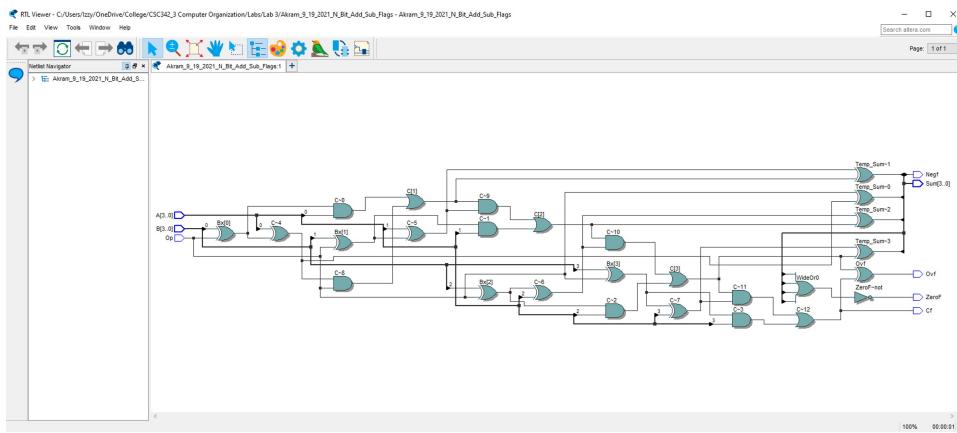


Fig 26. Tools > Netlist Viewers > RTL Viewer

Task 8

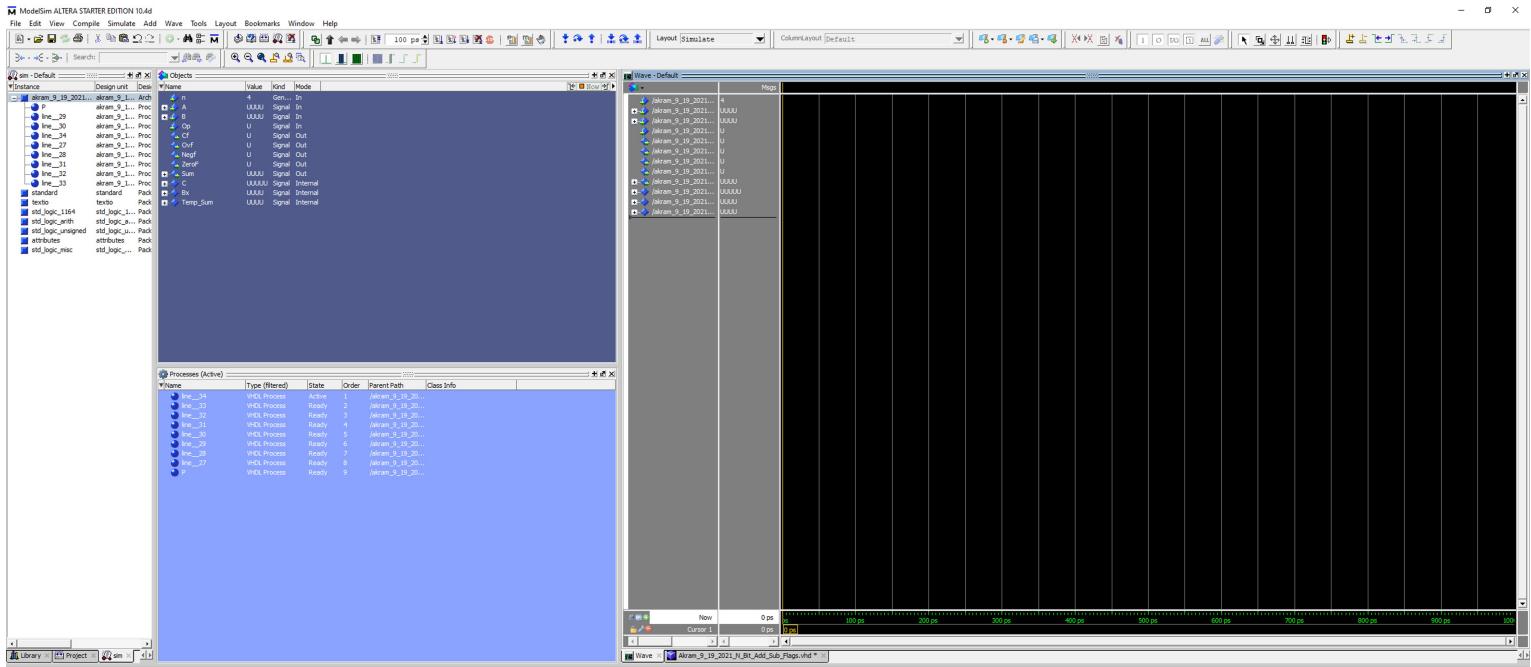
ModelSim ALTERA STARTER EDITION 10.4d - Custom Altera Version



 Akram_9_19_2021_4_Bit_Add_Sub.... ✓ VHDL 2 09/17/2021 02:55:51



Fig 27. Opened up VHDL files in ModelSim for testing simulations



```

Transcript
# Loading work_aclr9_1_0_21_n_bit_add_sub_flag behav_tbnsf
#-----#
#-----# Interpreted
#-----#
sim: [akram_9_19_2021_n_bit_add_sub_flag/n
sim: [akram_9_19_2021_n_bit_add_sub_flag/0
sim: [akram_9_19_2021_n_bit_add_sub_flag/1
sim: [akram_9_19_2021_n_bit_add_sub_flag/2
sim: [akram_9_19_2021_n_bit_add_sub_flag/3
sim: [akram_9_19_2021_n_bit_add_sub_flag/4
sim: [akram_9_19_2021_n_bit_add_sub_flag/5
sim: [akram_9_19_2021_n_bit_add_sub_flag/6
sim: [akram_9_19_2021_n_bit_add_sub_flag/7
sim: [akram_9_19_2021_n_bit_add_sub_flag/8
sim: [akram_9_19_2021_n_bit_add_sub_flag/9
sim: [akram_9_19_2021_n_bit_add_sub_flag/Op
sim: [akram_9_19_2021_n_bit_add_sub_flag/Or
sim: [akram_9_19_2021_n_bit_add_sub_flag/And
sim: [akram_9_19_2021_n_bit_add_sub_flag/Not
sim: [akram_9_19_2021_n_bit_add_sub_flag/Zero
sim: [akram_9_19_2021_n_bit_add_sub_flag/ZeroF
sim: [akram_9_19_2021_n_bit_add_sub_flag/Sum
sim: [akram_9_19_2021_n_bit_add_sub_flag/SumF
sim: [akram_9_19_2021_n_bit_add_sub_flag/Bx
sim: [akram_9_19_2021_n_bit_add_sub_flag/Tmp_Sum
sim: [akram_9_19_2021_n_bit_add_sub_flag/Tmp_SumF

PSIM-4

EndSimulation - Project: n_bit_add_sub_flag - New Spec Delta: 0
sim: [akram_9_19_2021_n_bit_add_sub_flag

```

4-bit Simulation a-f

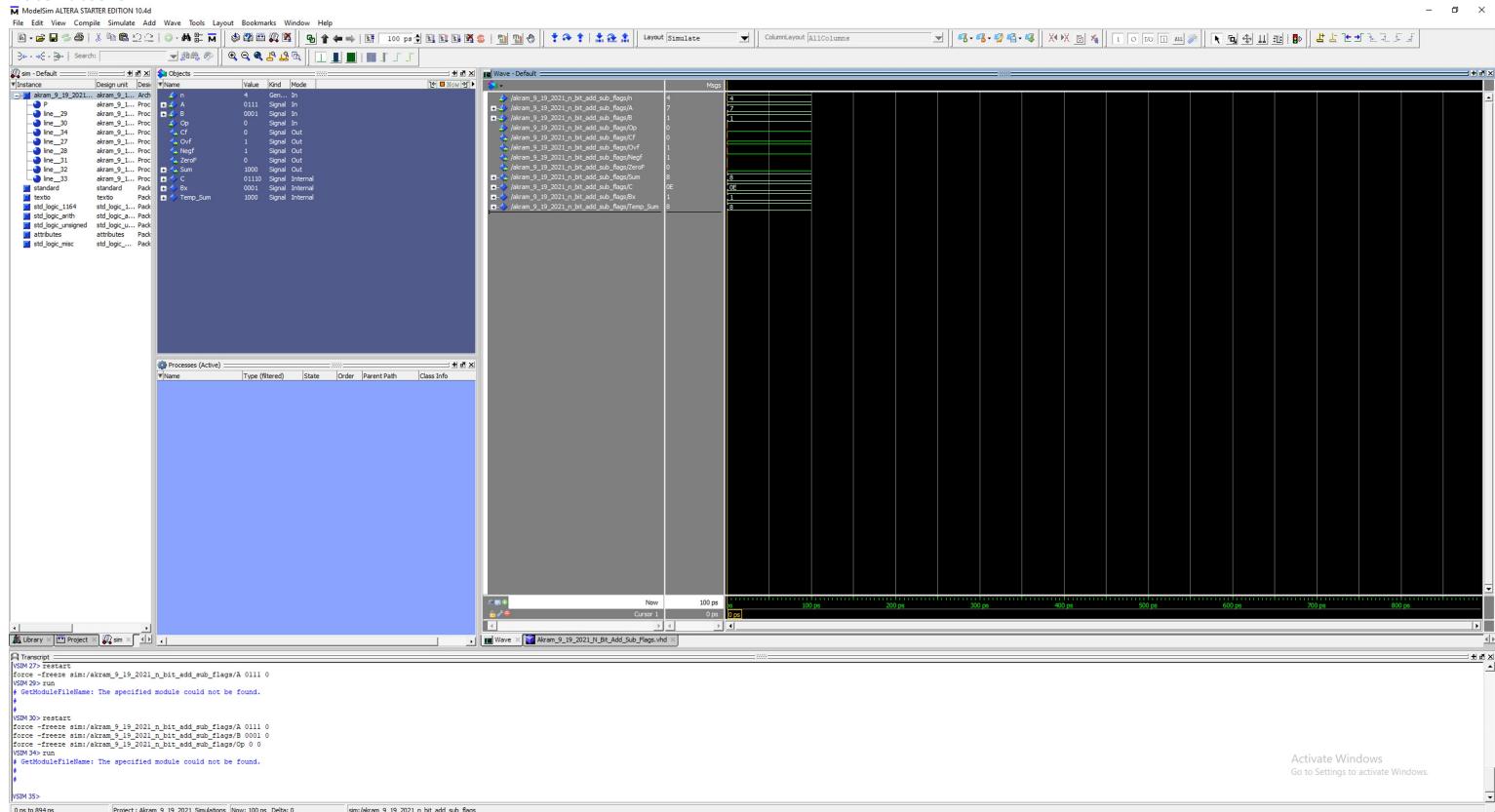


Fig 29. (Task a) A = "Most positive input" i.e. 0111, B = 0001, Op = 0 (addition), so Sum = 8.

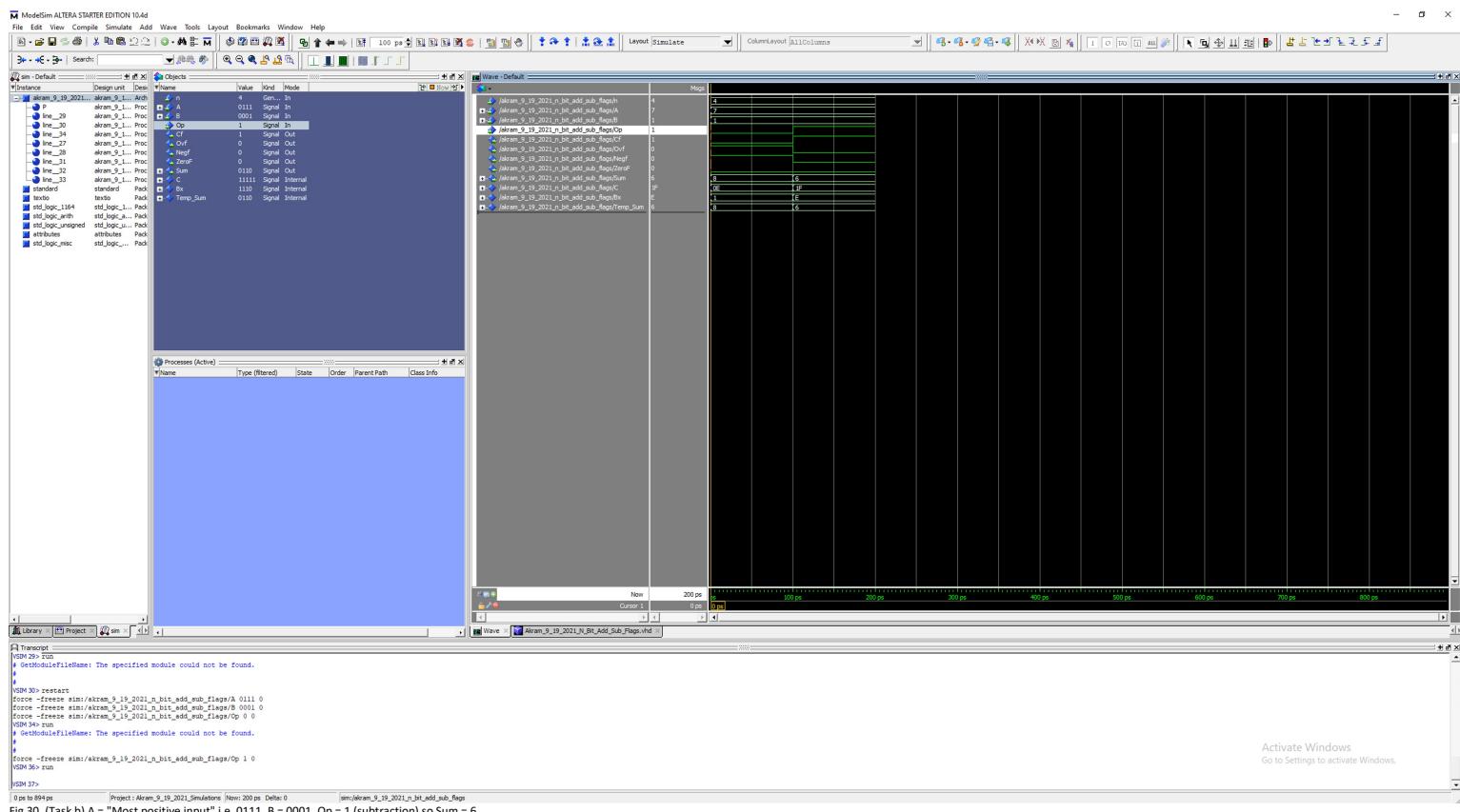


Fig 30. (Task b) A = "Most positive input" i.e. 0111, B = 0001, Op = 1 (subtraction) so Sum = 6.

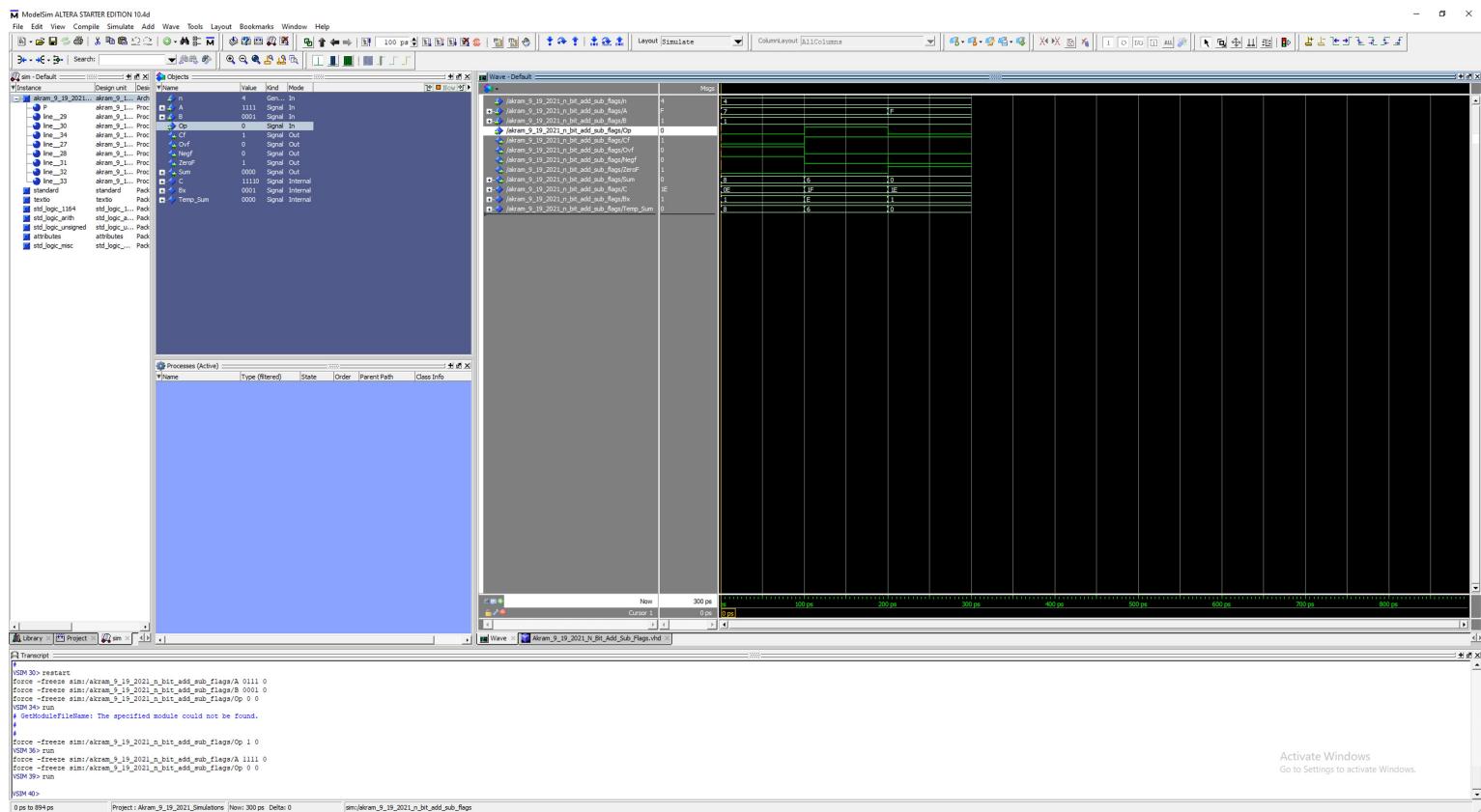


Fig 31. (Task c) = "Most negative input" i.e. 1111, B = 0001, Op = 0 (addition) so Sum = 0, Carry = 1E.

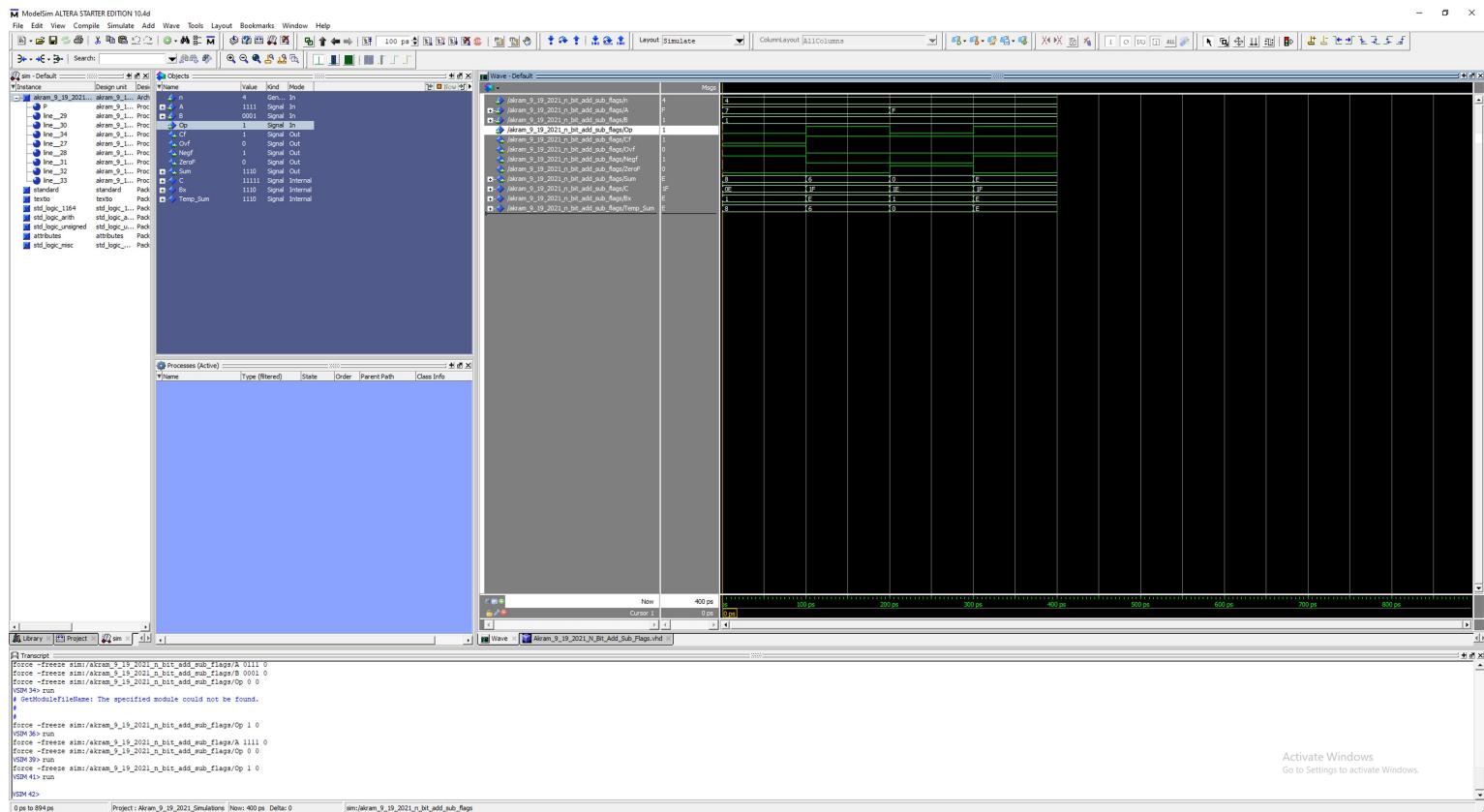


Fig 32. (Task d) A = "Most negative input" i.e. 1111, B = 0001, Op = 0 (addition) so Sum = 0, Carry = 1E.

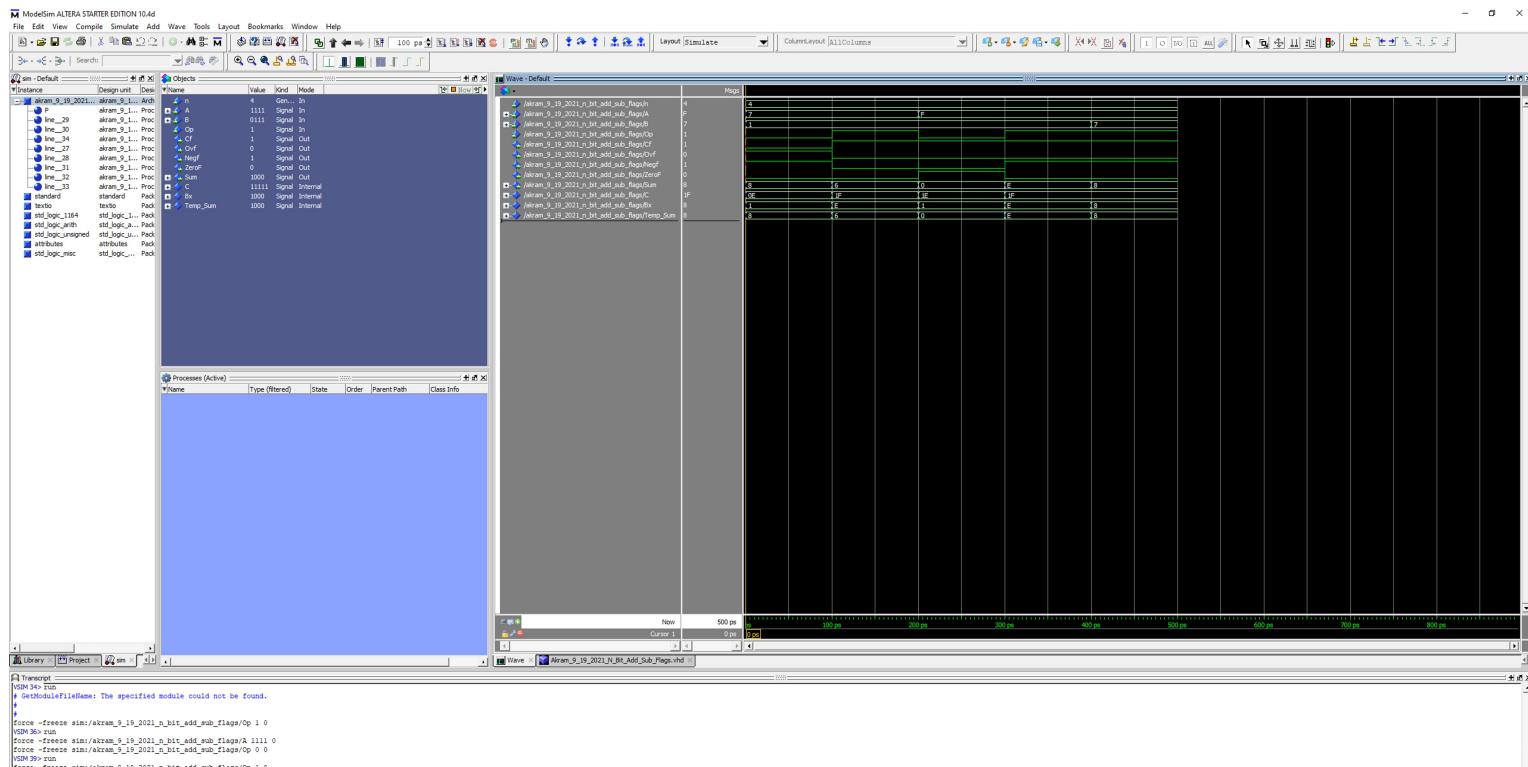


Fig 33. (Task e) A = "most positive input" i.e. 0111, B = "Most negative input" i.e. 1111, Op = 1 (Subtraction) so Sum = 8, Carry = 1F.

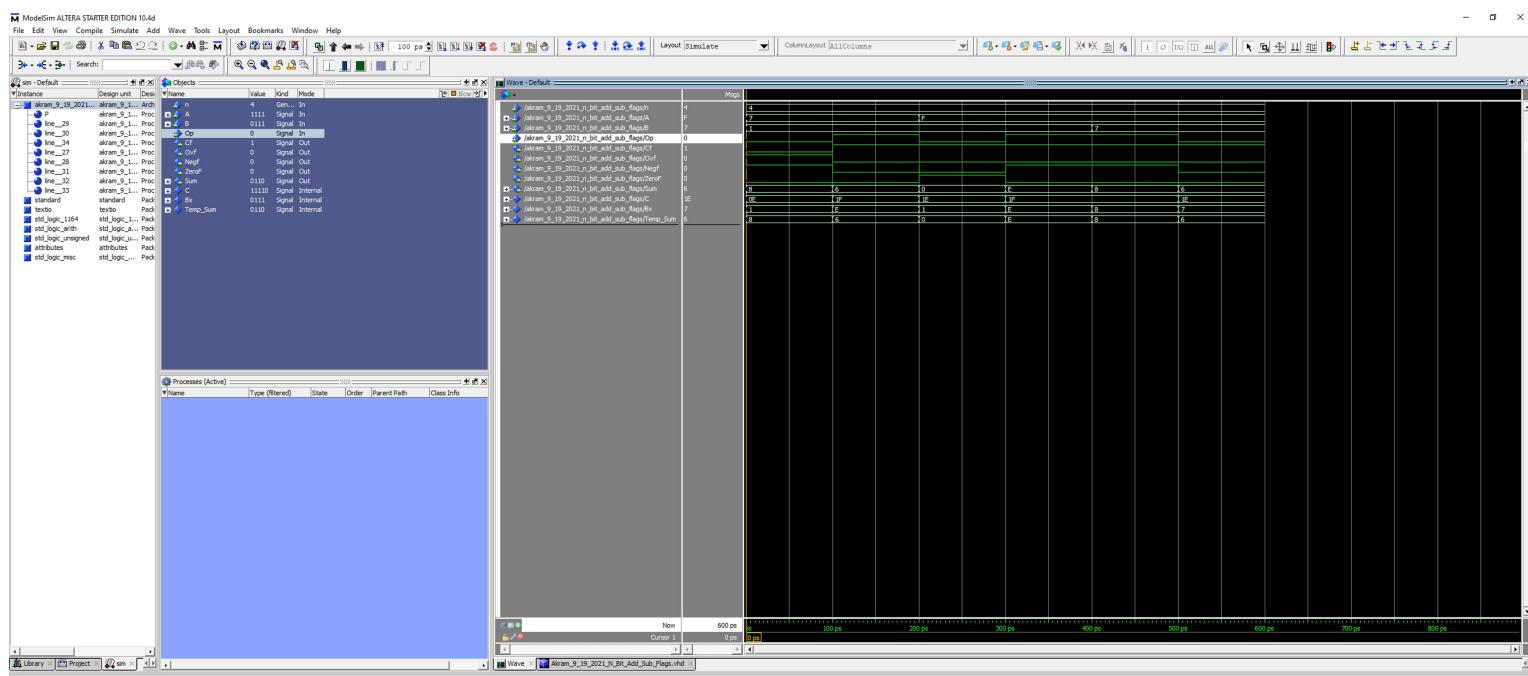


Fig 34. (Task f) A = "most positive input" i.e. 0111, B = "Most negative input" i.e. 1111, Op = 0 (Addition) so Sum = 6, Carry = 1E

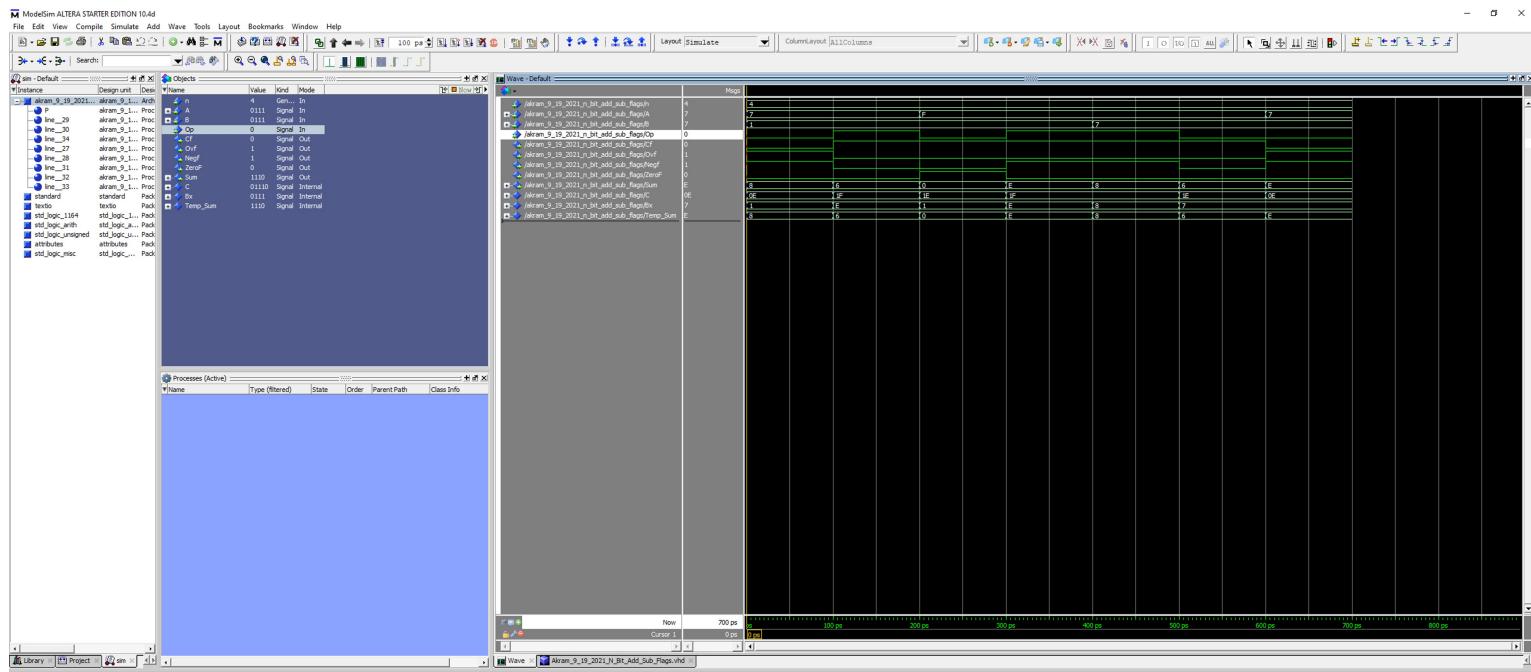
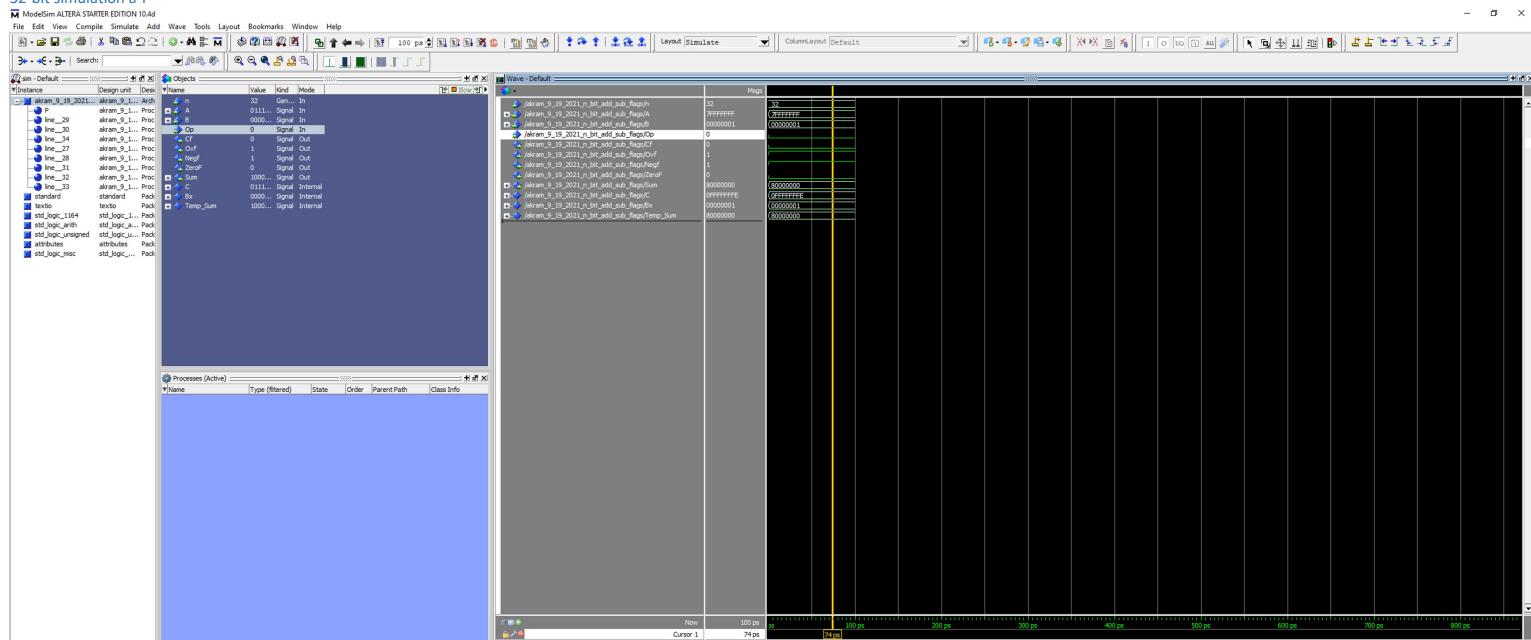
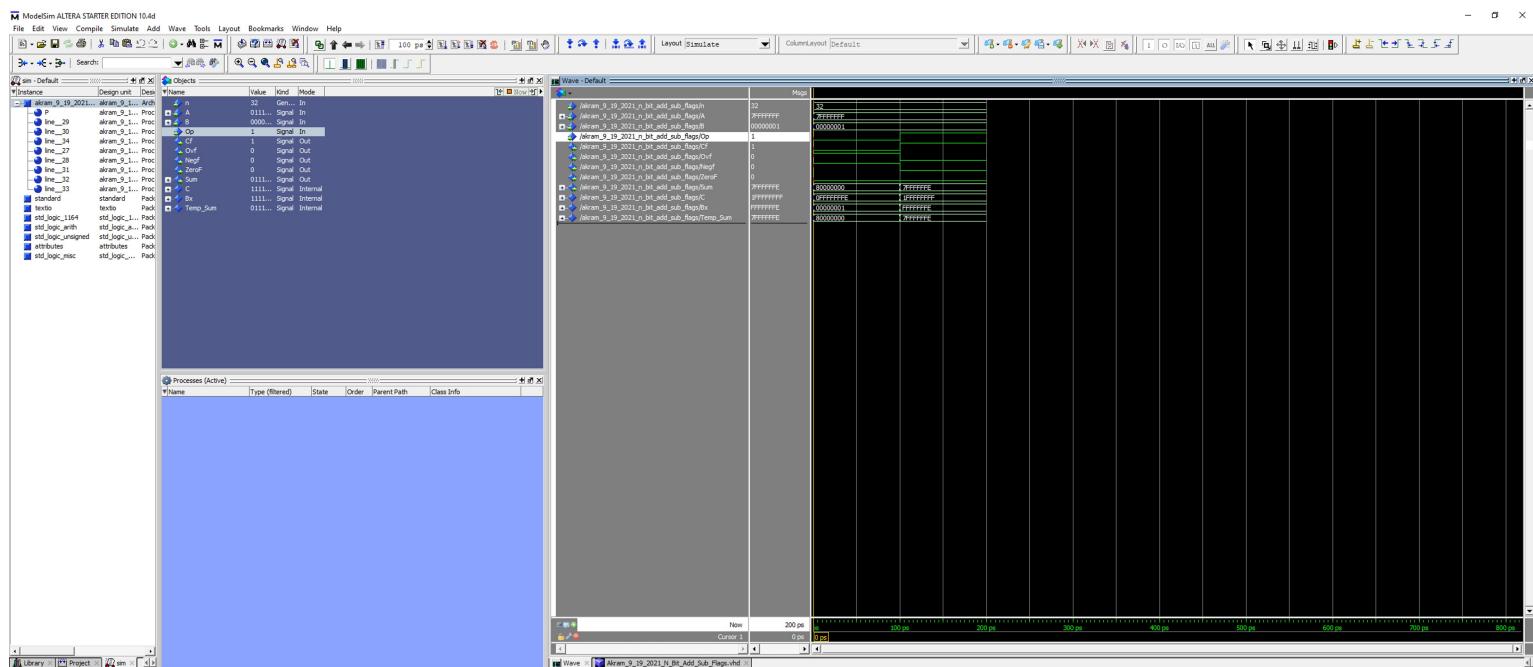


Fig 35. (Task g) A = "most positive input" i.e. 0111, B = "most negative input" i.e. 0111, Op = 1 (Subtraction) so Sum = E, Carry = 0E

32-bit simulation a-f



0 ps to 869 ps Project : Akram_9_19_2021_Simulations Now: 100 ps Deltas: 0 sim:/akram_9_19_2021_n_bit_add_sub_Regs



```

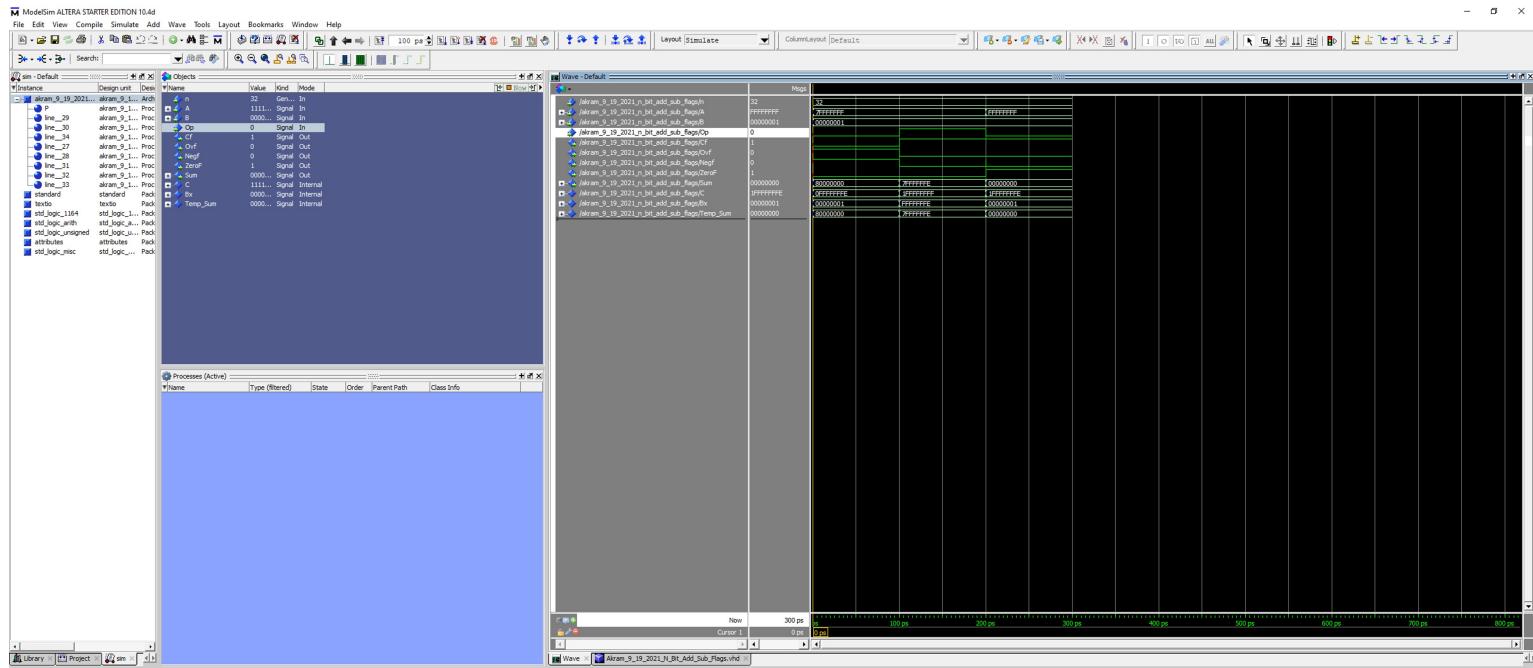
VSM> run
# Set module file name: The specified module could not be found.

force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 01111111111111111111111111111111
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 00000000000000000000000000000001
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/Op 1
VSM> restart
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 00000000000000000000000000000000
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 01111111111111111111111111111111
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/Op 0
VSM> run
# Set module file name: The specified module could not be found.

force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 0
VSM> run

```

Fig 37. (Task b) A = "Most positive input" i.e. 7FFFFFFF, B = 00000001, Op = 1 (subtraction), so Sum = 7FFFFFFE, Carry = 1FFFFFFE.



```

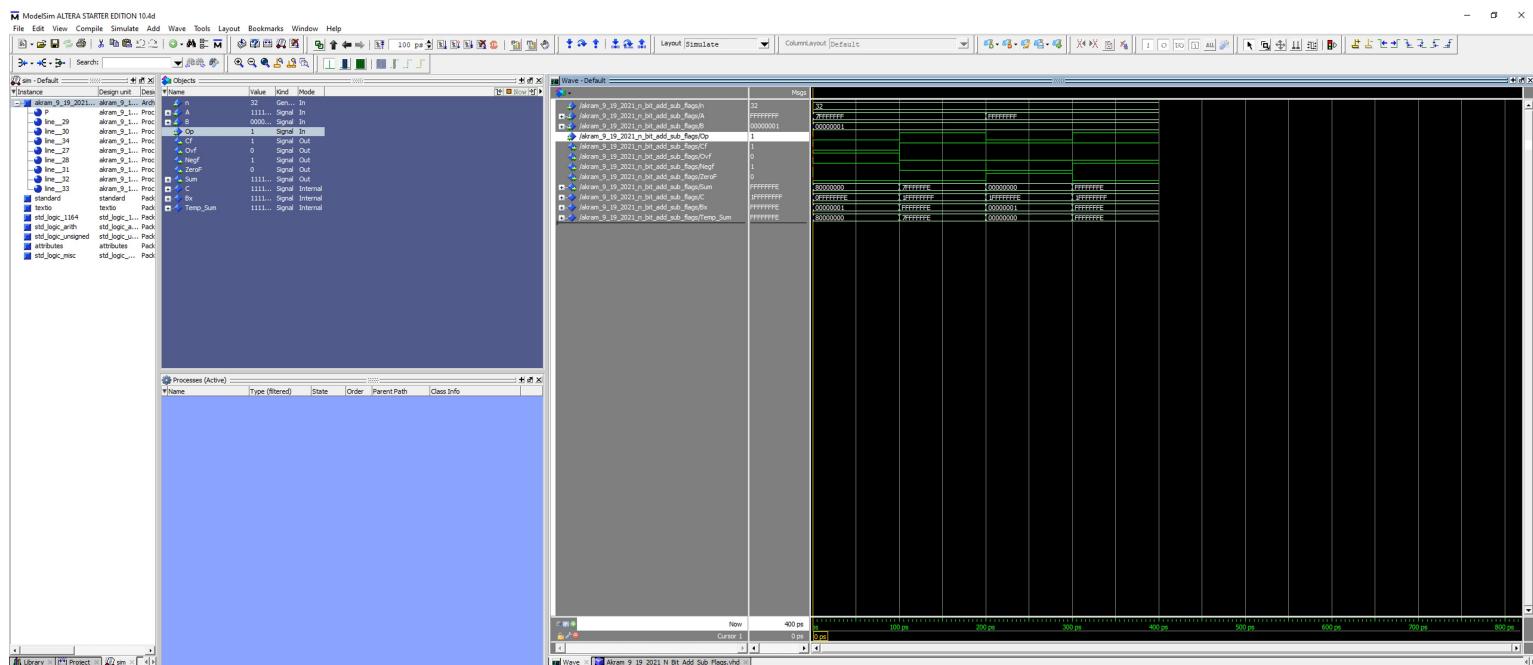
VSM> run
# Set module file name: The specified module could not be found.

force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 00000000000000000000000000000000
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 01111111111111111111111111111111
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/Op 0
VSM> run
# Set module file name: The specified module could not be found.

force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 0
VSM> run
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 11111111111111111111111111111111
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 0
VSM> run

```

Fig 38. (Task c) A = "Most negative input" i.e. FFFFFFFF, B = 00000001, Op = 0 (addition), so Sum = 00000000, Carry = 1FFFFFFE.



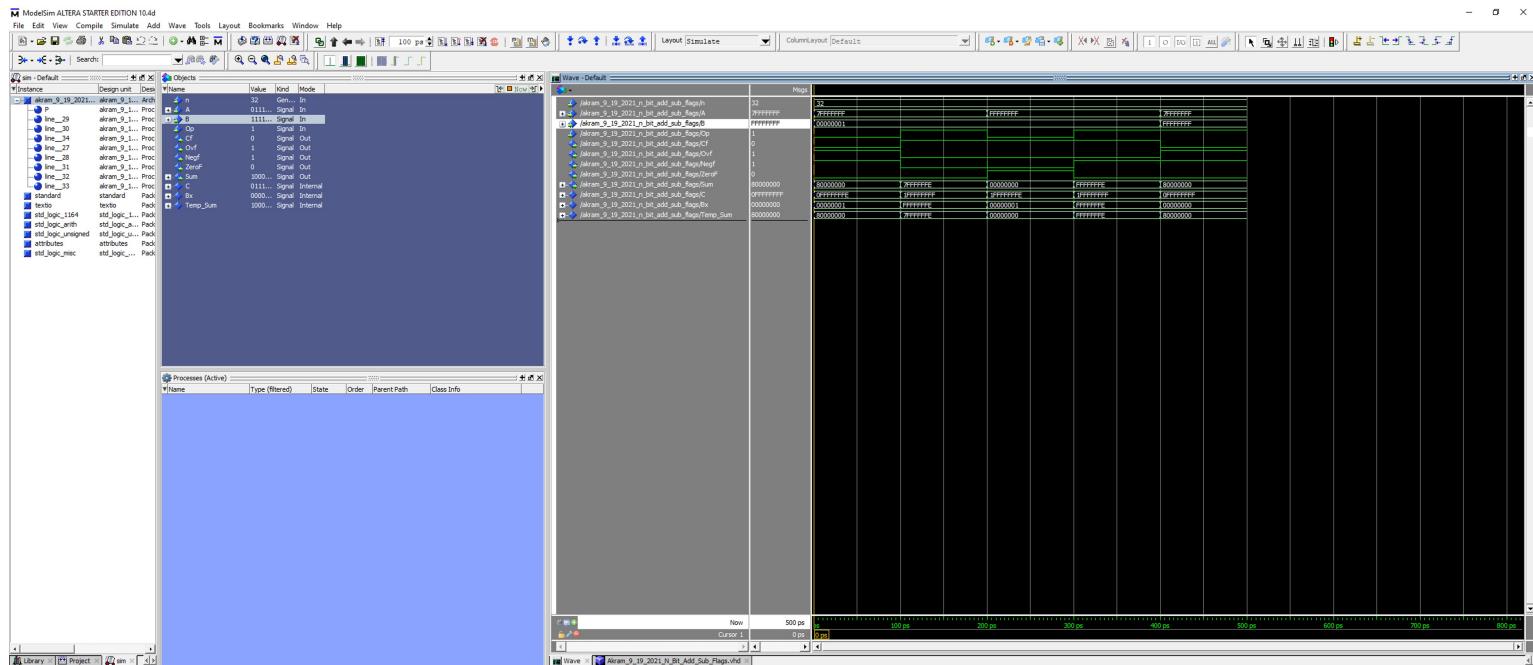
```

VSM>run
#force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 00000000000000000000000000000001 0
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 01111111111111111111111111111111 0
VSM>run
# GetModuleFileName: The specified module could not be found.

#
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/Op 1 0
VSM>run
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 11111111111111111111111111111111 0
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 0 0
VSM>run
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/Op 1 0
VSM>run
VSM>run

```

Fig 39. (Task d) A = "Most negative input" i.e. FFFFFFFF, B = 00000001, Op = 1 (subtraction), so Sum = FFFFFFFE, Carry = 1FFFFFFF.



```

VSM>run
# GetModuleFileName: The specified module could not be found.

#
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/Op 1 0
VSM>run
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 11111111111111111111111111111111 0
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 0 0
VSM>run
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/Op 1 0
VSM>run
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/A 01111111111111111111111111111111 0
force -freeze sim:/akram_9_19_2021_n_bit_add_sub_flags/B 11111111111111111111111111111111 0
VSM>run
VSM>run

```

Fig 40. (Task e) A = "Most positive input" i.e. 7FFFFFFF, B = "Most negative input" i.e. FFFFFFFF, Op = 1 (subtraction), so Sum = 80000000, Carry = 0FFFFFFF.

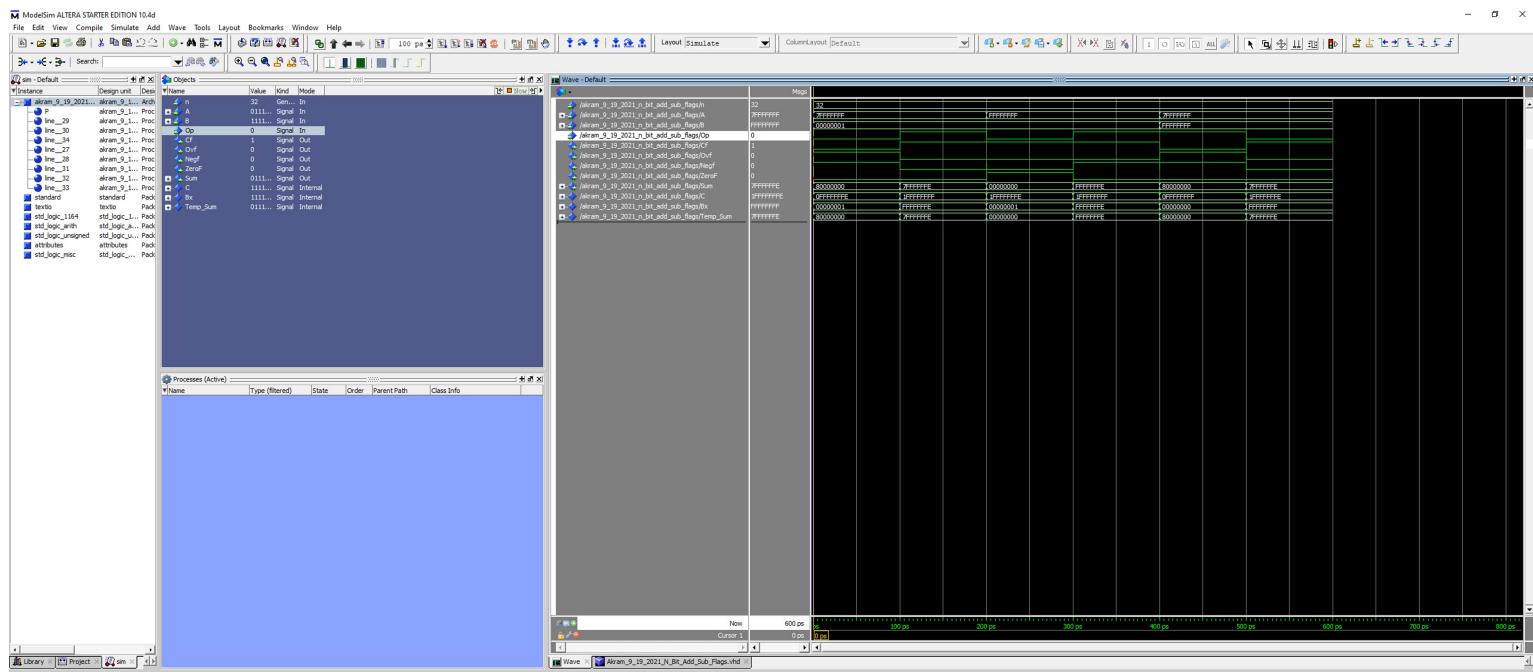


Fig 41. (Task f) A = "Most positive input" i.e. 7FFFFFFF, B = "Most negative input" i.e. FFFFFFFF, Op = 0 (addition), so Sum = 7FFFFFFF, Carry = 1FFFFFFE.

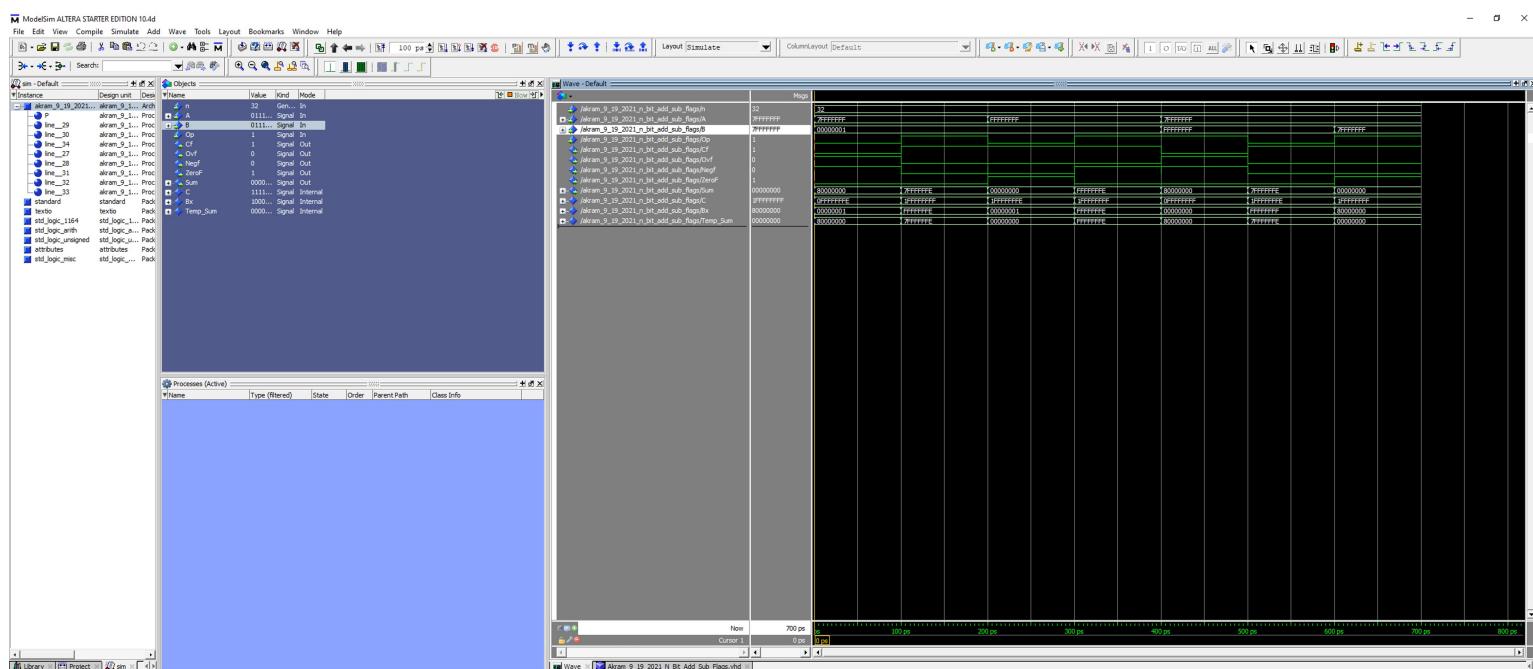


Fig 42. (Task g) A = "Most positive input" i.e. 7FFFFFFF, B = "Most positive input" i.e. 7FFFFFFF, Op = 1 (subtraction), so Sum = 00000000, Carry = 1FFFFFFF.

Task 9 DISCLAIMER: 1 adds; 0 subtracts!

Fig 43. Generated LPM as per the first tutorial in week 1 (I followed the same procedure step by step) > Compiled Successfully.

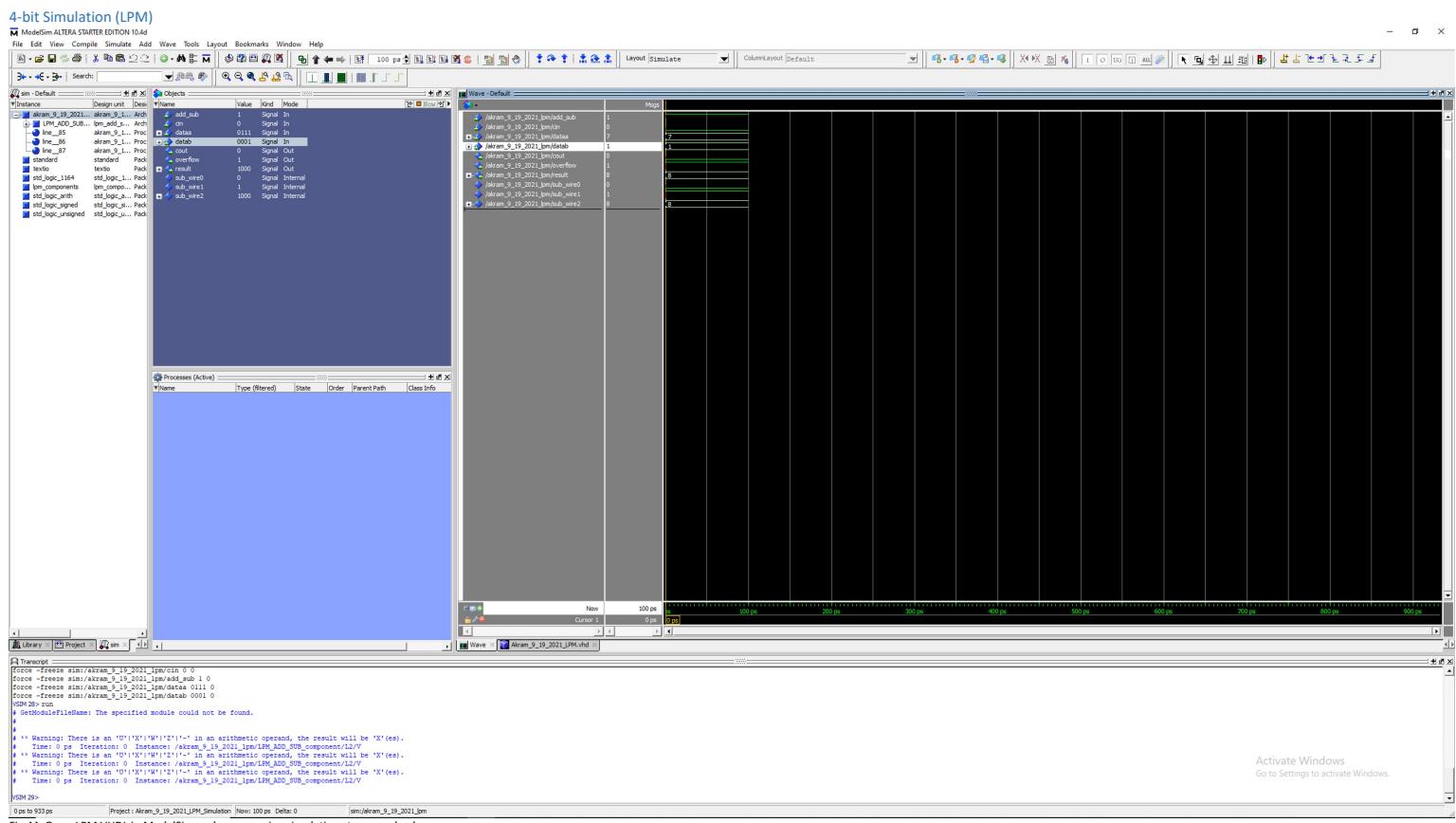


Fig 44. Open LPM VHDL in ModelSim and commencing simulations to cross check.
 (Task a) A = "Most positive input" i.e. 0111, B = 0001, Op = 1 (addition), cin = 0 so sum = 8

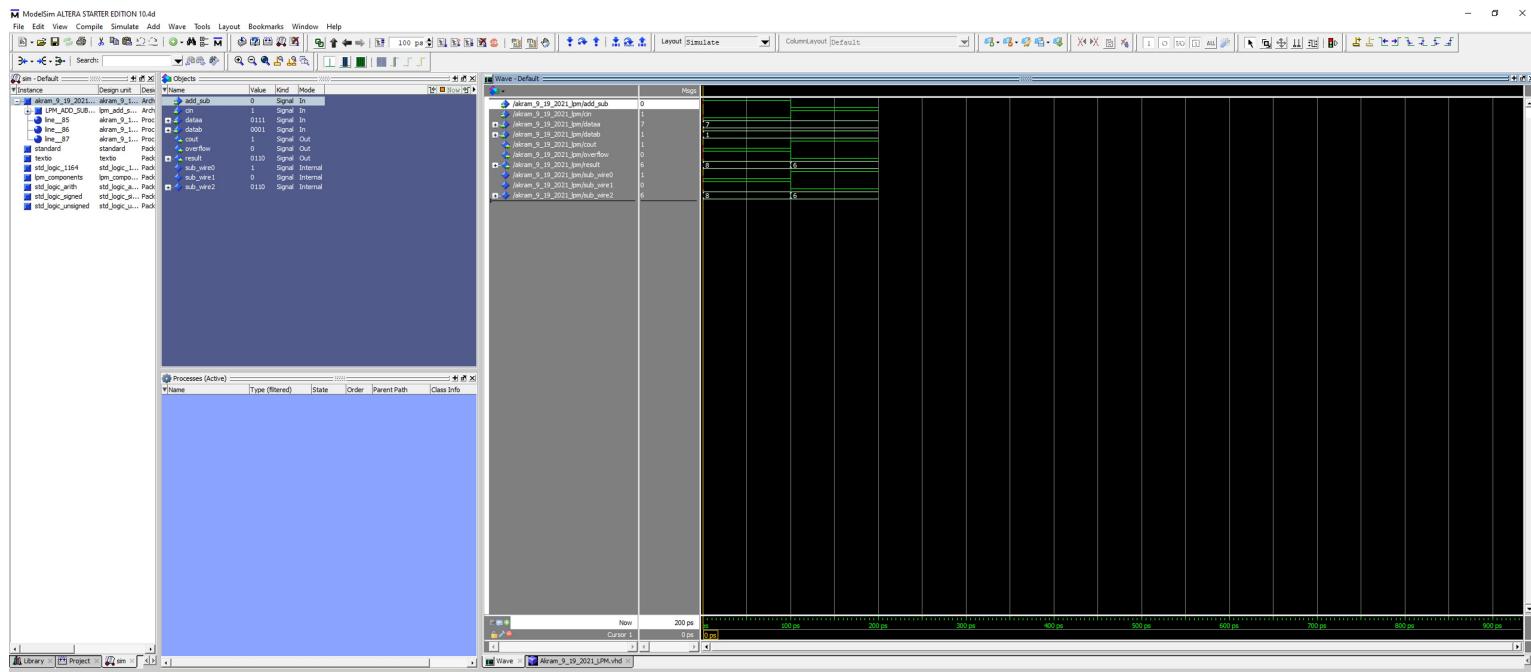


Fig 45. (Task b) A = "Most positive input" i.e. 0111, B = 0001, Op = 0 (subtraction), cin = 1 so Sum = 1, Carry = 1

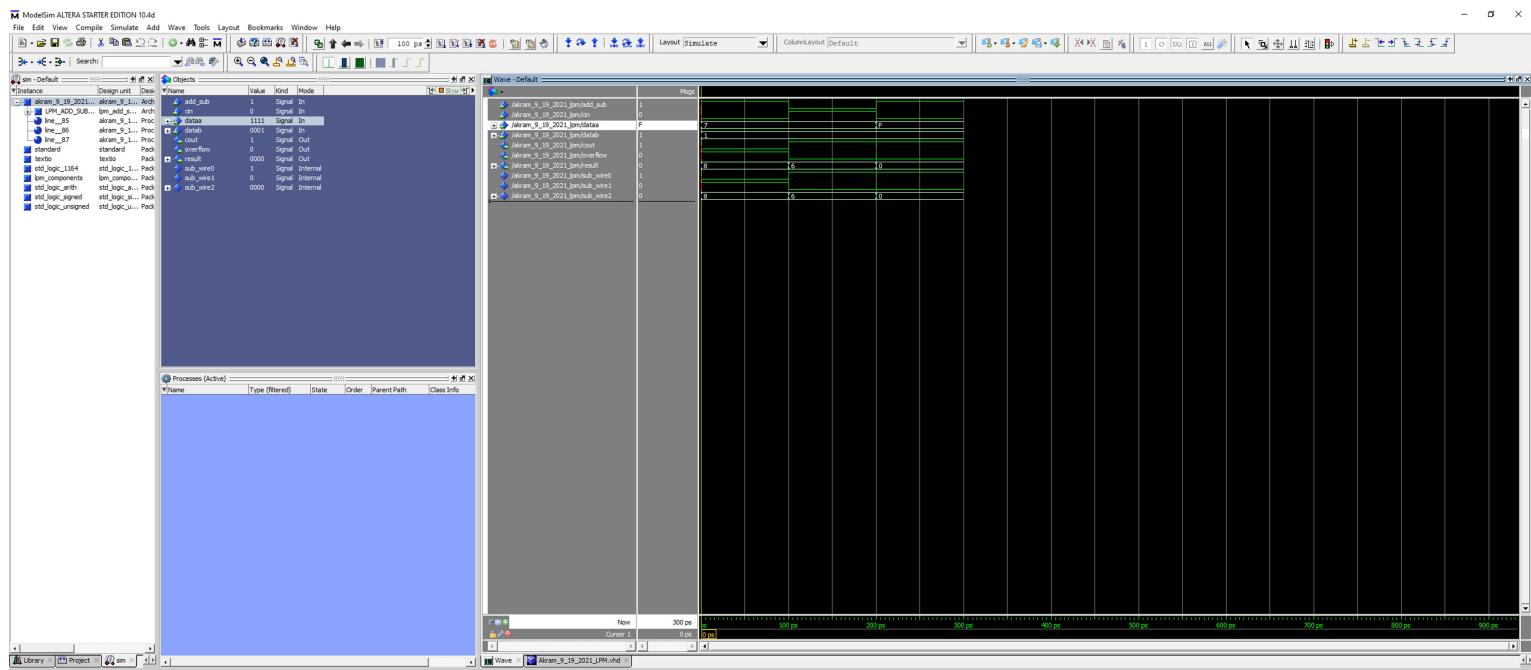
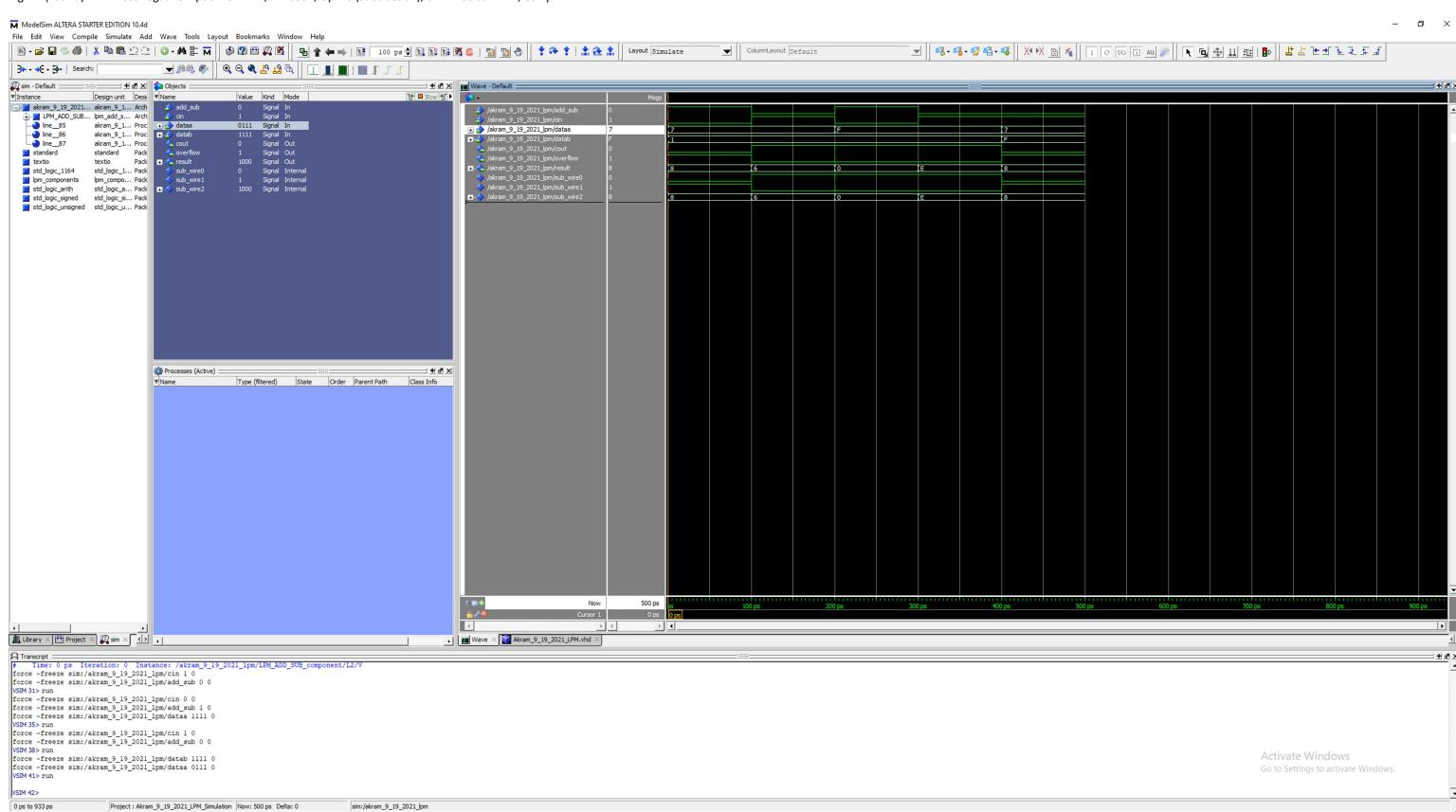
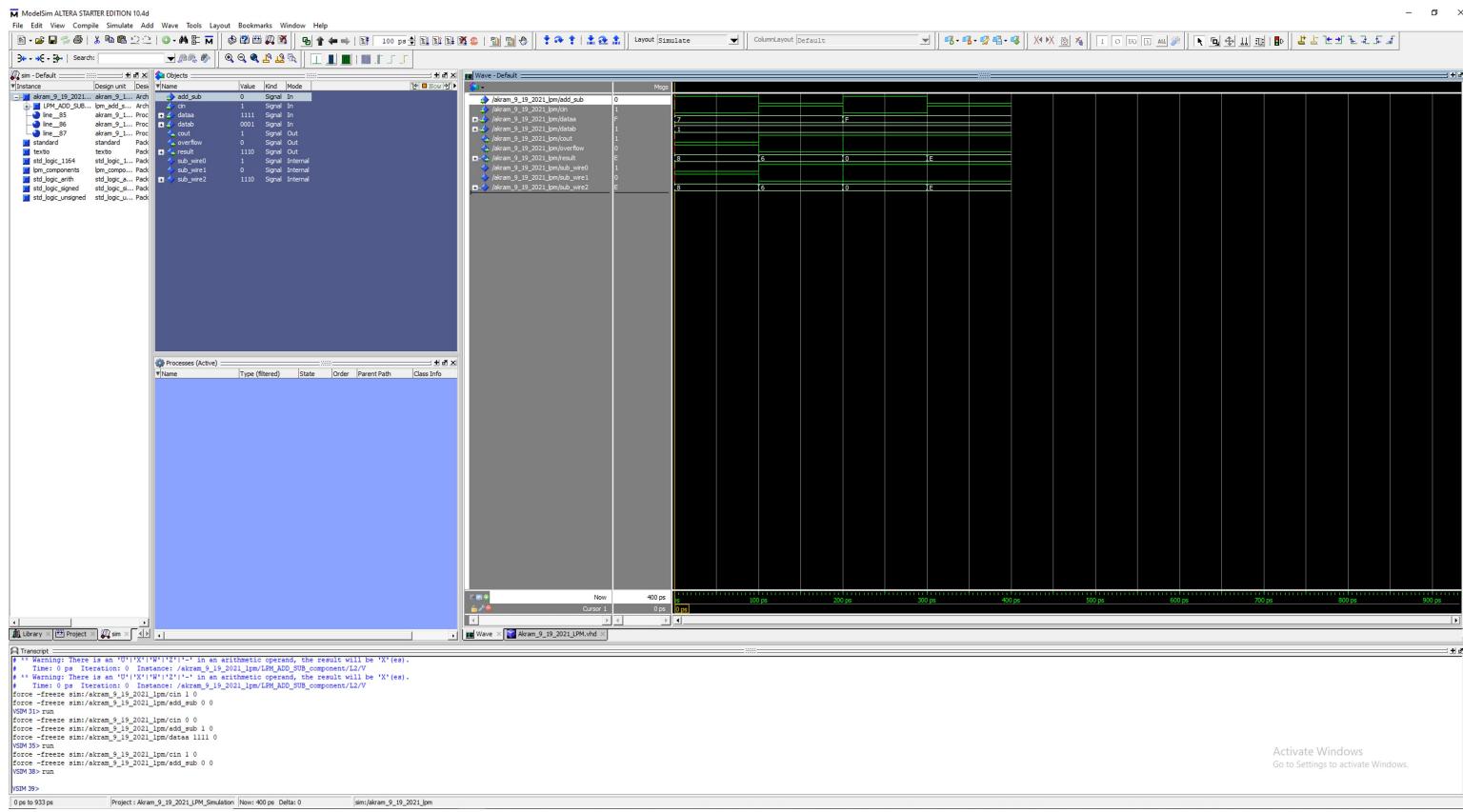
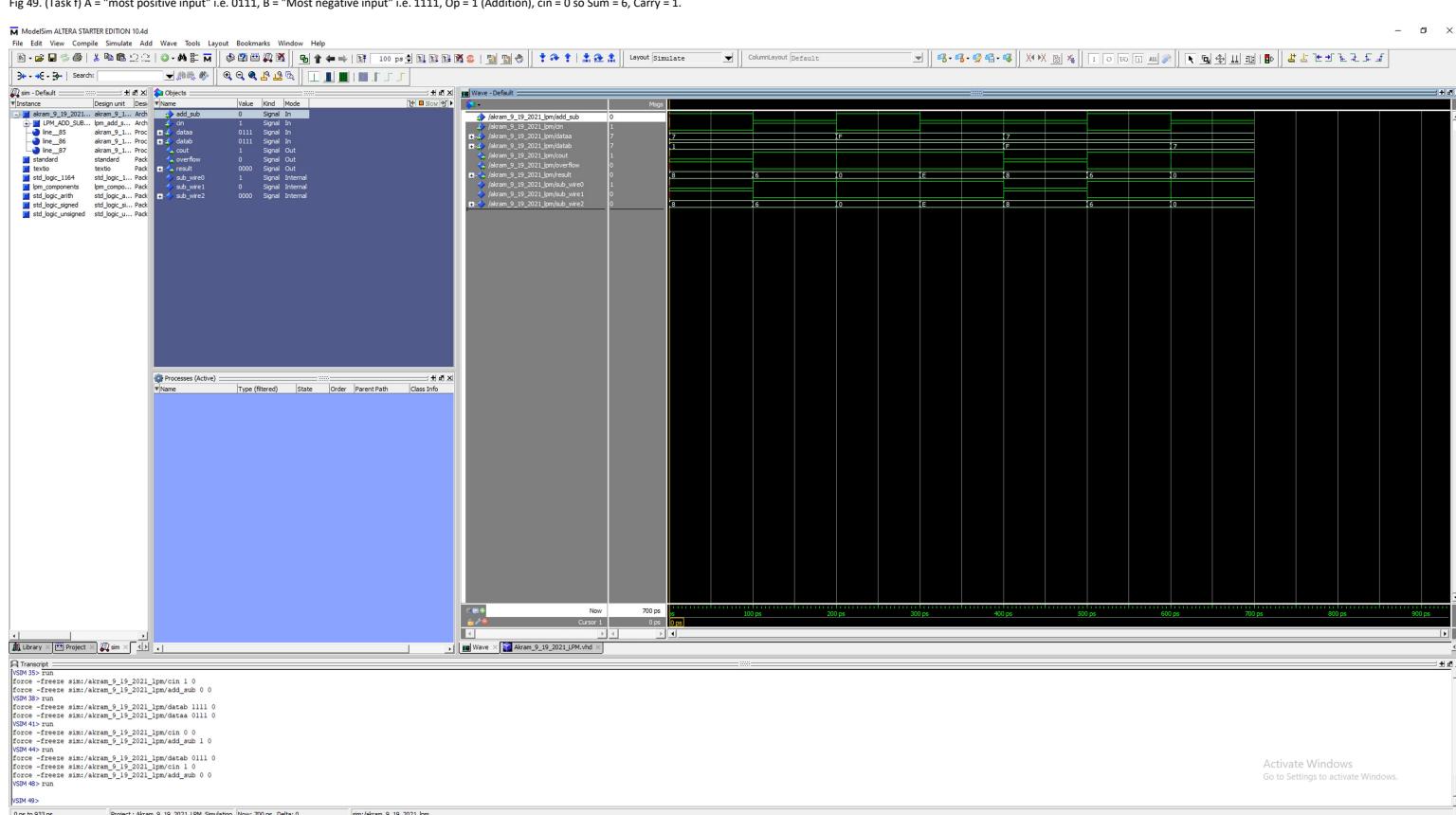
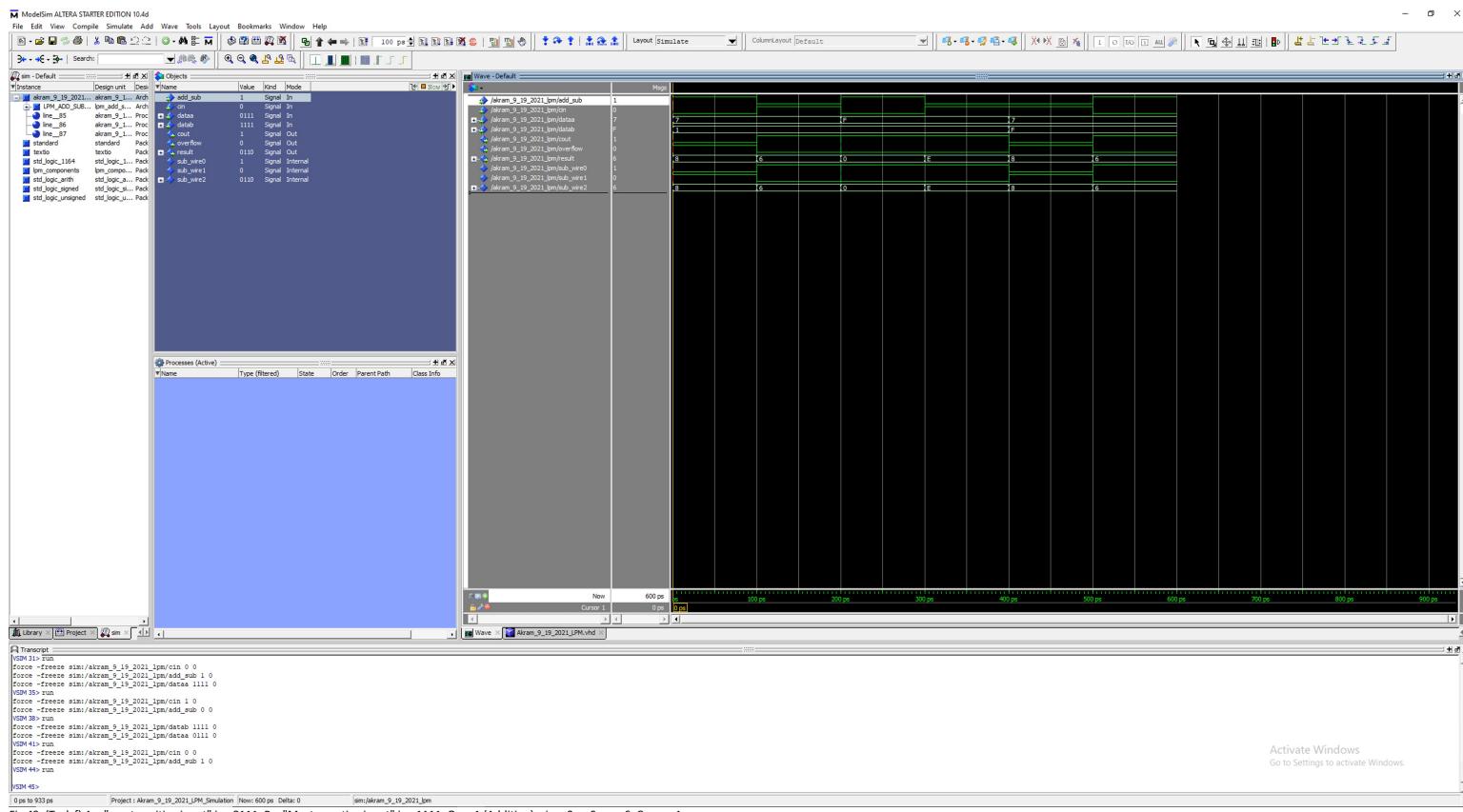


Fig 46. (Task c) A = "Most negative input" i.e. 1111, B = 0001, Op = 1 (addition), cin = 0 so Sum = 0, Carry = 1





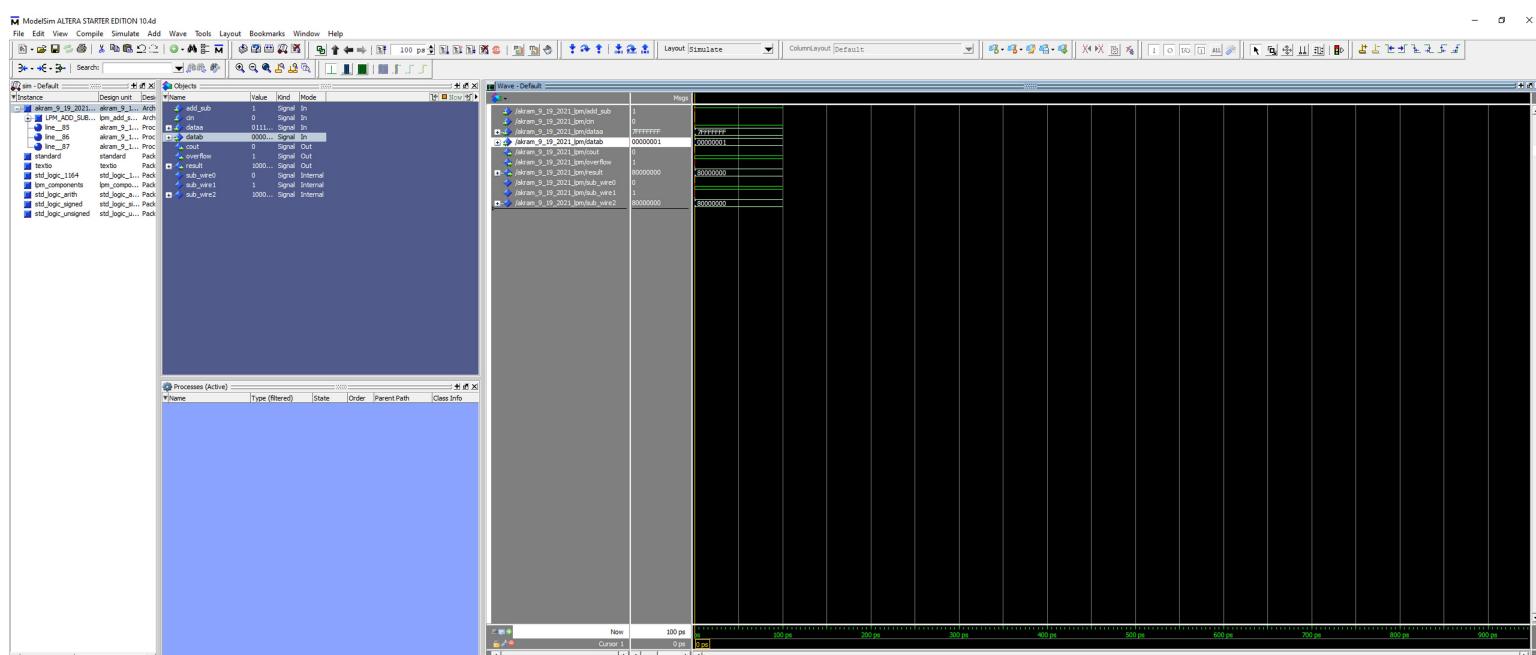
32-bit simulation a-f (LPM)

The screenshot shows the ModelSim ALTRA interface with the following details:

- File Menu:** File, Edit, View, Compile, Simulate, Add Project, Tools, Layout, Bookmarks, Window, Help.
- Project:** C:\Users\Izz\OneDrive\College\CSC342_3 Computer Organization\Labs\Lab 3\Akram_9_19_2021_LPM_Simulation
- Layout:** ColumnLayout [11Columns]
- Code Editor:** Displays the VHDL code for "akram_9_19_2021_lpm.vhd". The code includes an architecture section for "lpm" and a component section for "lpm_add_sub". It defines signals for sub_wires and components for LPM_ADD_SUB and LPM_ADD_MAP.
- Output Window:** Shows the compilation log:

```
111 -- CDM file: retrieval.info
112 --
113 -- Retrieval info: PRIVATE: CarryIn NUMERIC "1"
114 -- Retrieval info: PRIVATE: ConstantA NUMERIC "0"
115 -- Retrieval info: PRIVATE: ConstantB NUMERIC "0"
116 -- Retrieval info: PRIVATE: ConstantC NUMERIC "0"
117 -- Retrieval info: PRIVATE: ConstantD NUMERIC "0"
118 -- Retrieval info: PRIVATE: ConstantE NUMERIC "0"
119 -- Retrieval info: PRIVATE: INTERFACED_DEVICE_FAMILY STRING "Cyclone V"
120 -- Retrieval info: PRIVATE: LPM_PIPELINE NUMERIC "0"
121 -- Retrieval info: PRIVATE: MaxDepth NUMERIC "0"
122 -- Retrieval info: PRIVATE: Overflow NUMERIC "1"
123 -- Retrieval info: PRIVATE: Radius NUMERIC "10"
124 -- Retrieval info: PRIVATE: SIGNED NUMERIC "0"
125 -- Retrieval info: PRIVATE: Representation NUMERIC "0"
126 -- Retrieval info: PRIVATE: SIGN_WAFTER_DOT POSTFIX STRING "0"
127 -- Retrieval info: PRIVATE: Width NUMERIC "0"
128 -- Retrieval info: PRIVATE: ValidLsb NUMERIC "0"
```
- Bottom Status Bar:** Altra 2018.1 Windows Go to Settings to activate Windows.

Fig 51. Changed IPM length to 32 bit



```

Transport
sim/a/kram_9_19_2021_lpm_sim.vhd
sim/a/kram_9_19_2021_lpm_tb.vhdl
sim/a/kram_9_19_2021_lpm_tb.vhd
force -freeze sim/a/kram_9_19_2021_lpm_tb.m00n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m01n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m02n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m03n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m04n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m05n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m06n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m07n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m08n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m09n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m10n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m11n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m12n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m13n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m14n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m15n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m16n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m17n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m18n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m19n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m20n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m21n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m22n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m23n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m24n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m25n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m26n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m27n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m28n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m29n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m30n 0
force -freeze sim/a/kram_9_19_2021_lpm_tb.m31n 0
$ ** Warning: There is an "U'X'X'W'1?1?'"-1 in an arithmetic operand, the result will be "X'(es).
$ 0 ps Iteration 0 Instance: /a/kram_9_19_2021_lpm/lpm_ADD_STB/component/L2/V
$ ** Warning: There is an "U'X'X'W'1?1?'"-1 in an arithmetic operand, the result will be "X'(es).
$ 0 ps Iteration 0 Instance: /a/kram_9_19_2021_lpm/lpm_ADD_STB/component/L2/V
$ ** Warning: There is an "U'X'X'W'1?1?'"-1 in an arithmetic operand, the result will be "X'(es).
$ 0 ps Iteration 0 Instance: /a/kram_9_19_2021_lpm/lpm_ADD_STB/component/L2/V
$ ** Warning: There is an "U'X'X'W'1?1?'"-1 in an arithmetic operand, the result will be "X'(es).
$ 0 ps Iteration 0 Instance: /a/kram_9_19_2021_lpm/lpm_ADD_STB/component/L2/V

VSM #94
```

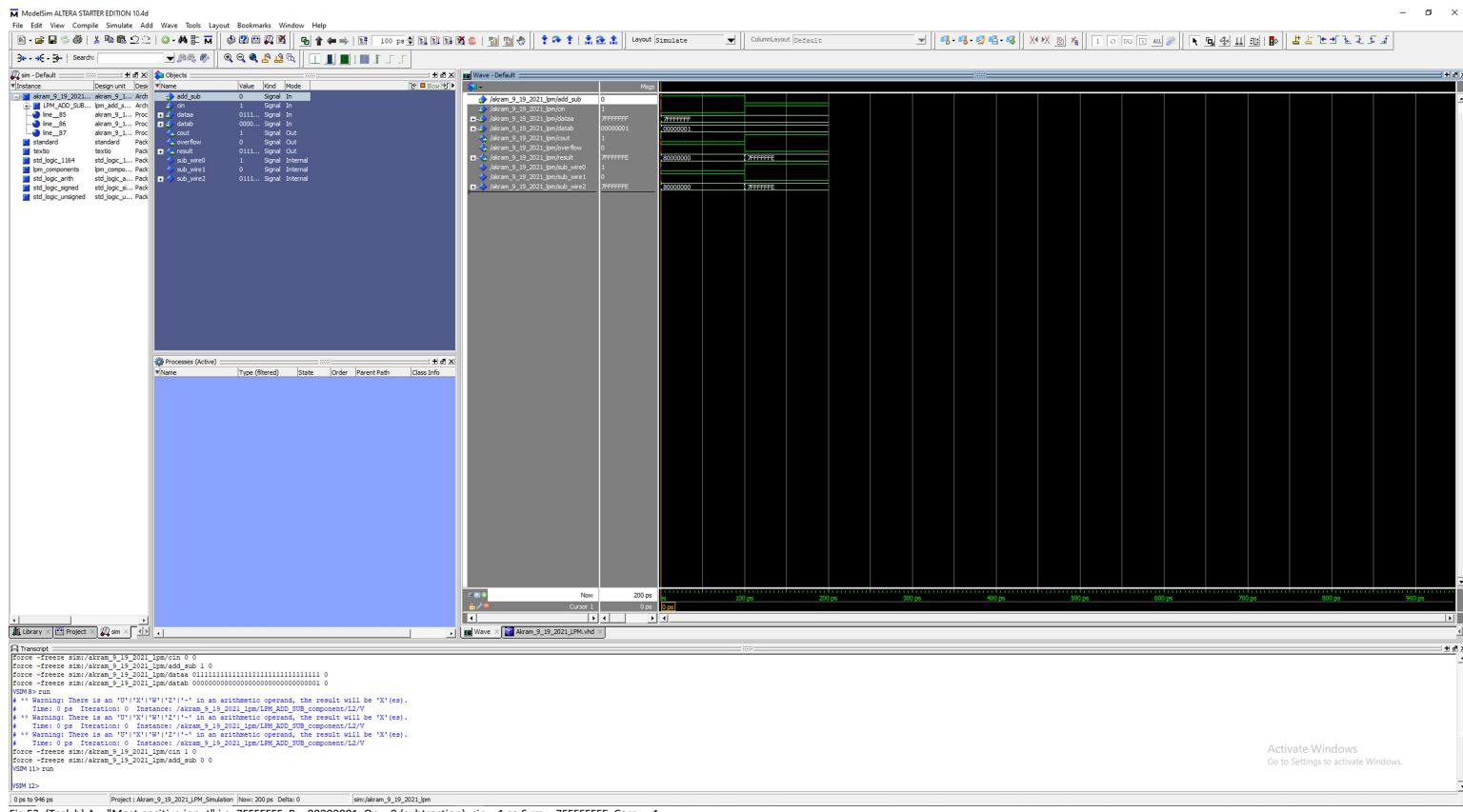


Fig 53. (Task b) A = "Most positive input" i.e. 7FFFFFFF, B = 00000001, Op = 0 (subtraction), cin = 1 so Sum = 7FFFFFFE, Carry = 1

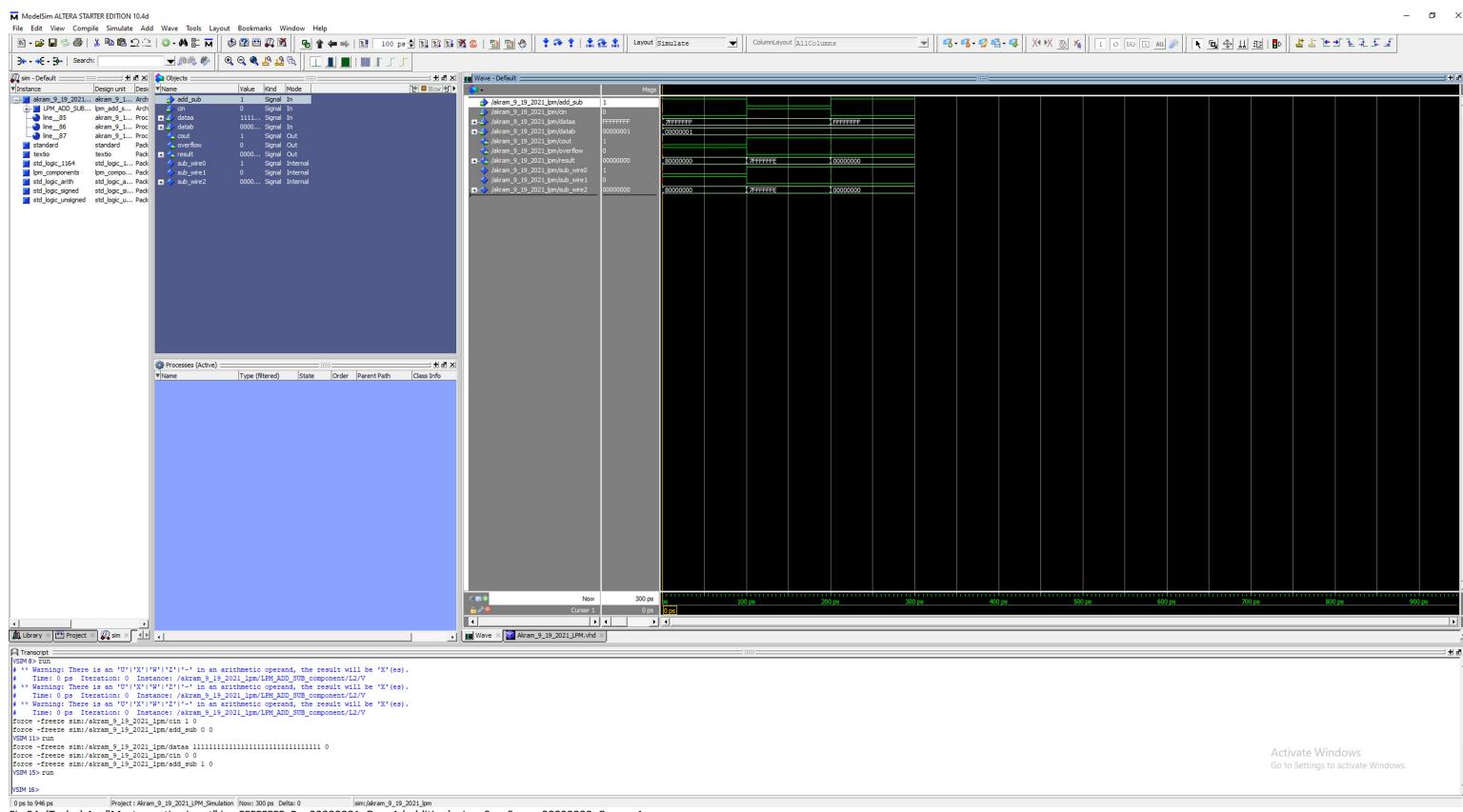
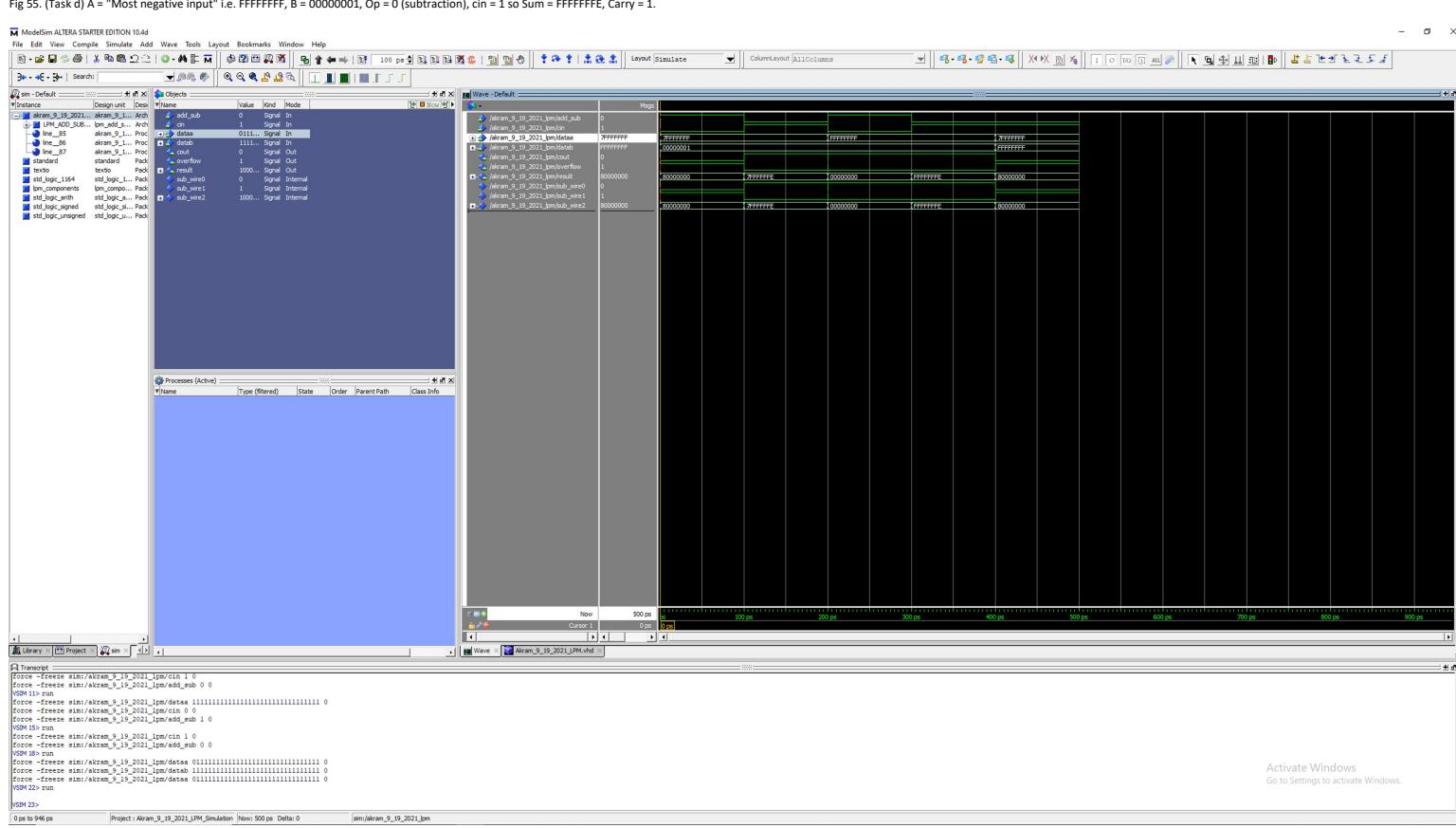
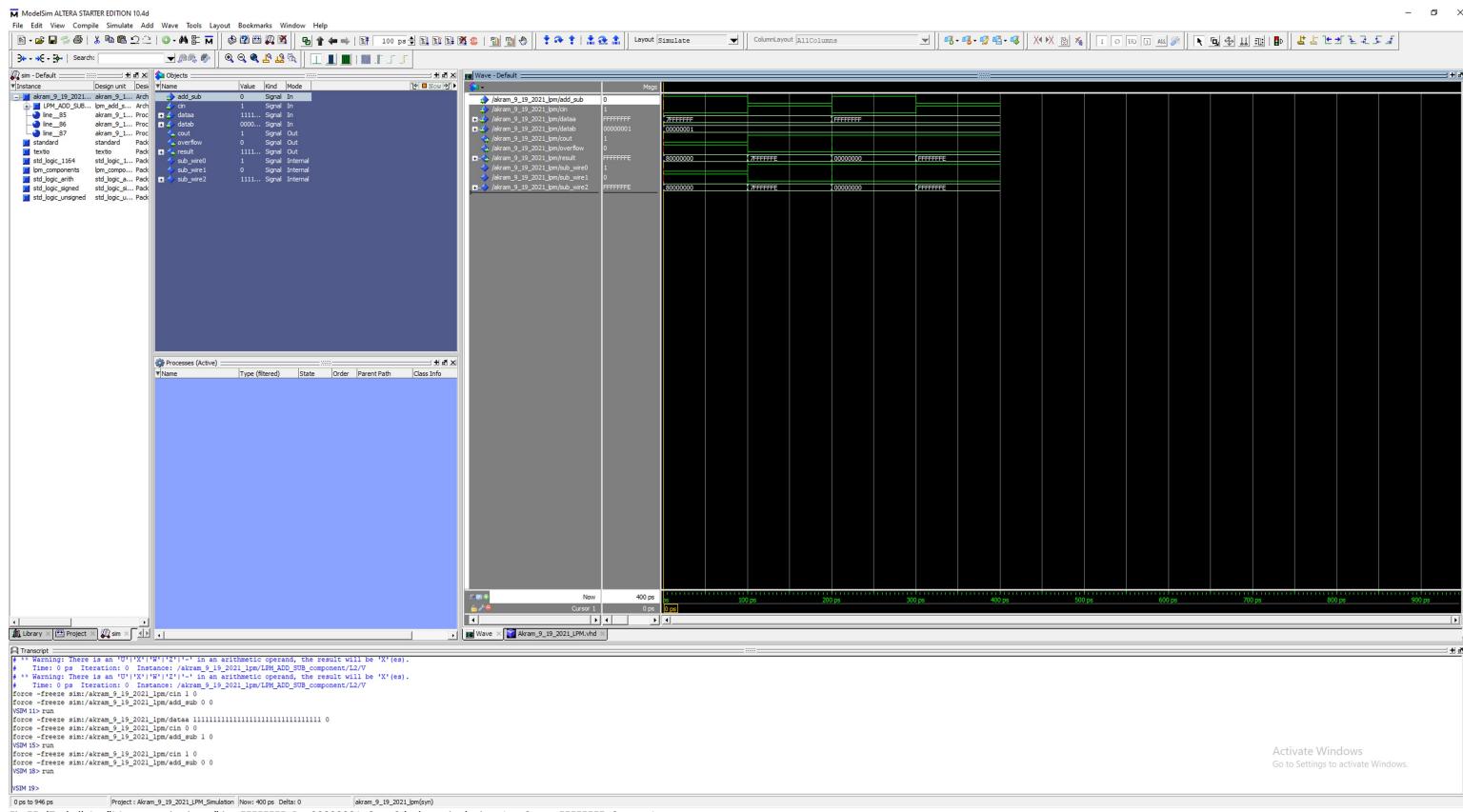


Fig 54. (Task c) A = "Most negative input" i.e. FFFFFFFF, B = 00000001, Op = 1 (addition), cin = 0 so Sum = 00000000, Carry = 1



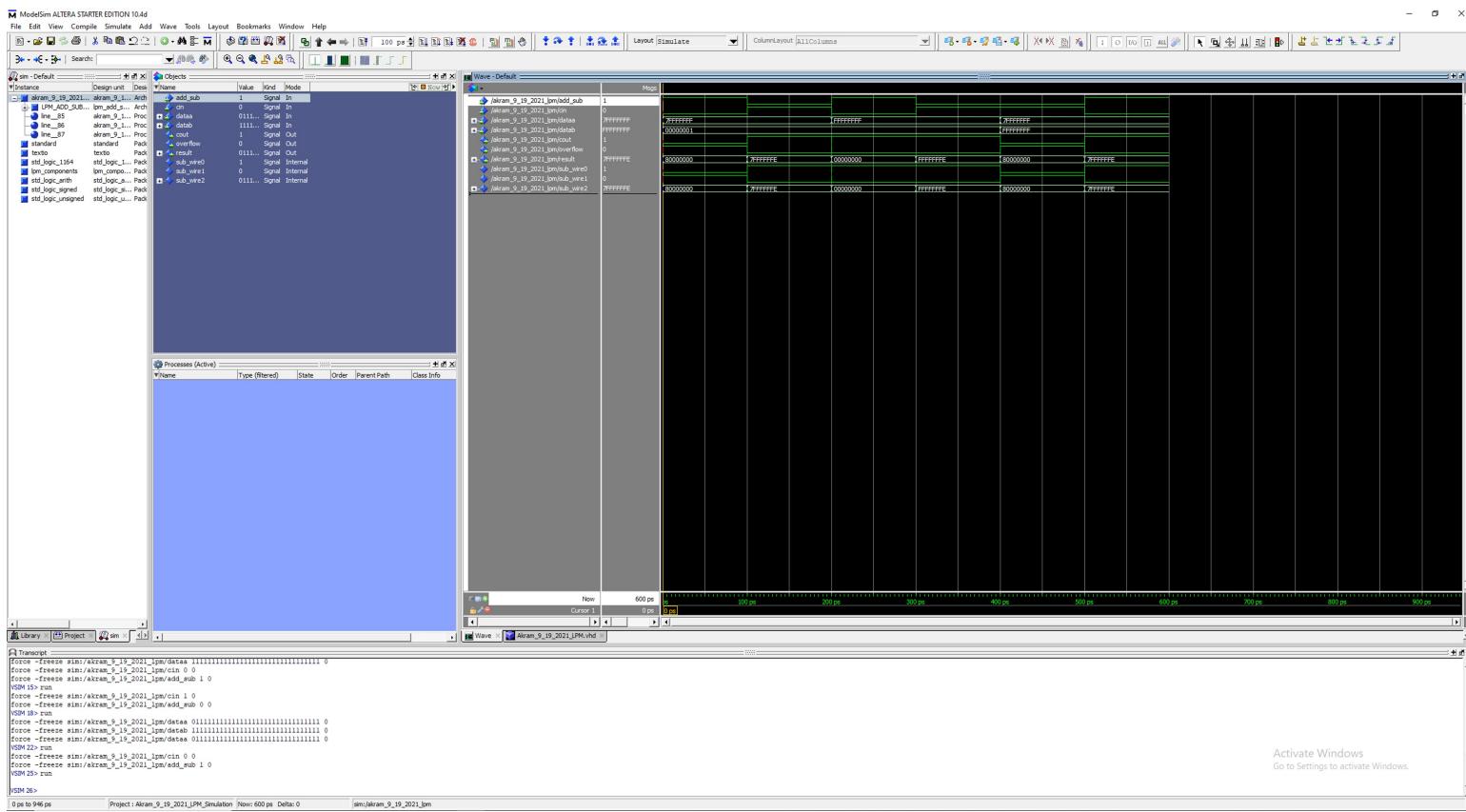


Fig 57. (Task f) A = "Most positive input" i.e. 7FFFFFFF, B = "Most negative input" i.e. FFFFFFFF, Op = 1 (addition), cin = 0 so Sum = 7FFFFFFF, Carry = 1.

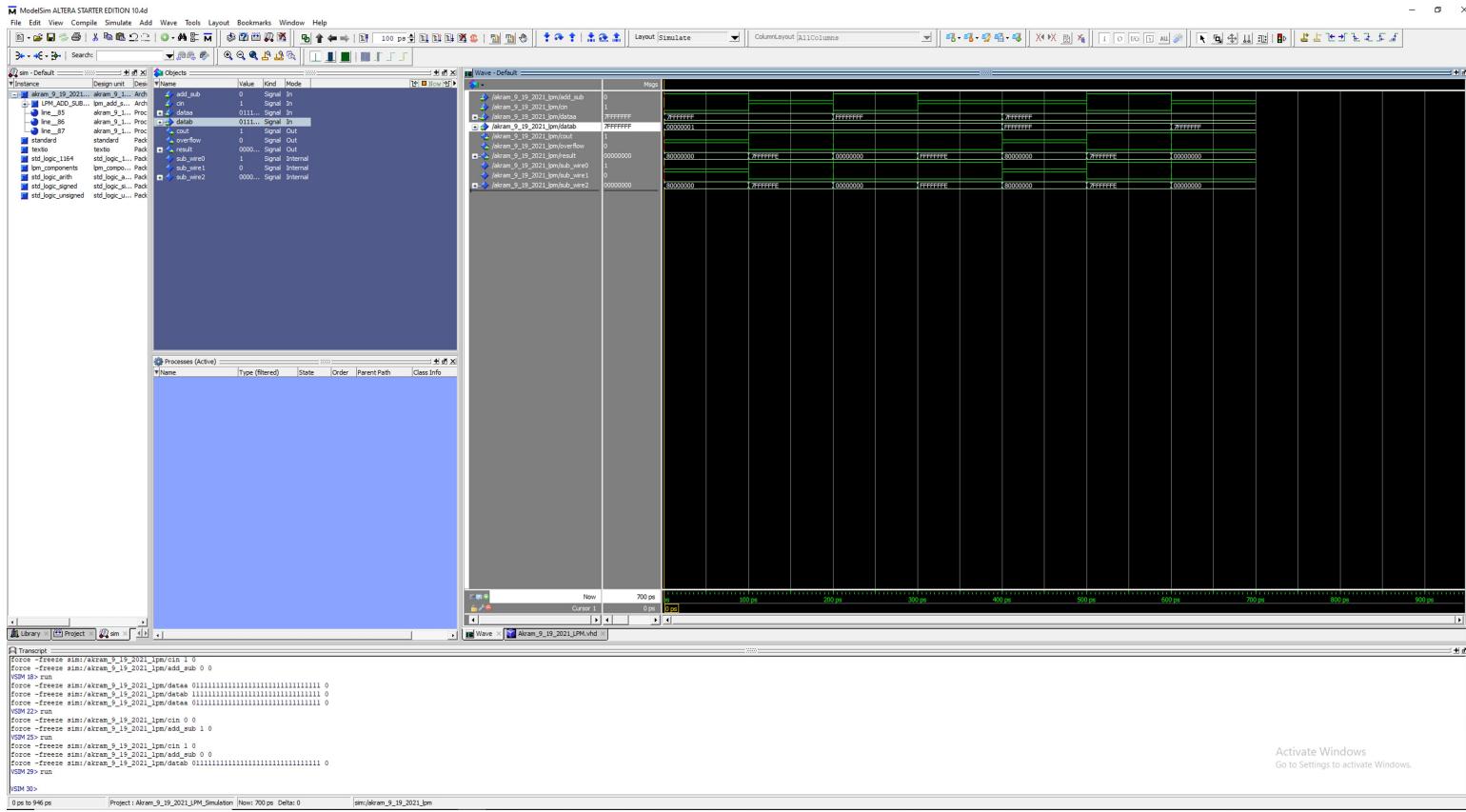


Fig 58. (Task g) A = "Most positive input" i.e. 7FFFFFFF, B = "Most positive input" i.e. 7FFFFFFF, Op = 0 (subtraction), cin = 1 so Sum = 00000000, Carry = 1.

Task 10

New Project Wizard

Summary

When you click Finish, the project will be created with the following settings:

Project directory: C:/Users/itzzy/OneDrive/College/CSC342_3 Computer Organization/Labs/Lab 3
 Project name: Akram_9_19_2021_Test_Bench
 Top-level design entity: Akram_9_19_2021_Test_Bench
 Number of files added: 0
 Number of user libraries added: 0
 Device assignments:
 Design template: n/a
 Family name: Cyclone V (E/GX/GT/SX/SE/ST)
 Device: 5CSEMA5F31C8
 Board: n/a
 EDA tools:
 Design entry/synthesis: <None> (<None>)
 Simulation: <None> (<None>)
 Timing analysis: ()
 Operating conditions:
 Core voltage: 1.1V
 Junction temperature range: 0-85 °C

< Back Next > Finish Cancel Help

Fig 59. Creating new project for Test Bench

Task 10

ModelSim ALTERA STARTER EDITION 10.4d - Custom Altera Version

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Layout (NoDesign) ColumnLayout AllColumns

Project - C:\Users\itzzy\OneDrive\College\CSC342_3 Computer Organization\Labs\Lab 3\Akram_9_19_2021_Test_Bench - StatusType [Modified]

Akram_9_19_2021_Test_Bench.vhd 09/19/2021 04:56:23...

```

1 -- Test bench
2 library ieee;
3 use ieee.std_logic_1164.all;
4
5 entity Akram_9_19_2021_Test_Bench is
6   end entity Akram_9_19_2021_Test_Bench;
7
8 architecture behav_tb of Akram_9_19_2021_Test_Bench is
9   signal A, B : std_logic;
10  signal Sum, Carry : std_logic;
11
12 begin
13
14   -- connecting test bench signals with half adder
15   UUT : entity work.Akram_9_19_2021_H_Bit_Adder
16     port map (A, B, Sum, Carry);
17
18   tb : process
19     constant period: time := ns;
20   begin
21     A <= "0000000000000000"; -- 16bits
22     wait for period;
23     assert (Sum = "1") and (Carry = "0") -- expected output
24     report "test failed for input 0000000000000000" severity error;
25
26     A <= "0000000000000001";
27     B <= "0000000000000001";
28     wait for period;
29     assert (Sum = "1") and (Carry = "0");
30     report "test failed for input 0000000000000001" severity error;
31
32     A <= "0000000000000000";
33     B <= "0000000000000001";
34     wait for period;
35     assert (Sum = "0") and (Carry = "1");
36     report "test failed for input 0000000000000000" severity error;
37
38     A <= "0000000000000001";
39     B <= "0000000000000001";
40     wait for period;
41     assert (Sum = "0") and (Carry = "1");
42     report "test failed for input 0000000000000001" severity error;
43
44     -- Fail test
45     A <= "0000000000000000";
46     B <= "0000000000000001";
47     wait for period;
48     assert (Sum = "0") and (Carry = "1");
49     report "test failed for input 0000000000000000 (fail test)" severity error;
50
51
52   wait; -- suspend process indefinitely
53   end process;
54 end behav_tb;
55 
```

Library Project

Akram_9_19_2021_Test_Bench.vhd Akram_9_19_2021_H_Bit_Add_Sub_Flags.vhd

Transcript

Compile of Akram_9_19_2021_Test_Bench.vhd failed with 14 errors.
Compile of Akram_9_19_2021_Test_Bench.vhd failed with 13 errors.
Compile of Akram_9_19_2021_Test_Bench.vhd failed with 41 errors.

ModelSim

7.0.1 (Windows) 2018.03
 Go to Settings to activate Windows.