SRAM Vs DRAM: Key Differences

RAM is an abbreviation for the term Random Access Memory. It is a type of memory that needs a constant supply of power for retaining the data present in it. It means that as soon as the power supply to the laptop or PC gets disrupted (switched off), the information stored in this memory type will be lost. Thus, it is called volatile memory, cache memory, or temporary memory of a computer system.

It is easy to read and write in RAM. Electrical signal accomplishes this process. RAM is mainly of two types:

SRAM – Static RAM is a type of semiconductor memory that stores each bit by making use of Bistable latching circuitry. This RAM type stores data using the six cells of transistor memory. It mostly serves as the cache memory for the CPU (processor).

DRAM – Dynamic RAM allows users to store every data bit in a separate capacitor residing within a particular IC (integrated circuit). It serves as the standard computer memory for any recent/modern desktop computer.

What is SRAM?

The data and information stored in transistors require a constant flow of power. Thus, because of the continuous need for power, SRAM does not need to refresh itself to remember the data stored in the memory. Because it does not demand refreshing or change in action to keep its data intact, SRAM is also known as static.

What Is DRAM?

Capacitors serve as storage units of data and information. The Capacitors storing their data in DRAM gradually discharge their memory. No energy implies that the data is lost. Thus, it needs a periodic refreshing of power in order to function. Since DRAM requires constant change or action

(meaning it requires refreshing for keeping the data intact), it is also known as dynamic. One can also use them for implementing the main memory.

Difference Between SRAM and DRAM

	SRAM	DRAM
on	Static random-access memory is a specific type of memory of a semiconductor. It makes use of bistable latching circuitry to store every bit of data. SRAM is static. A user does not have to refresh it periodically for it to perform.	Dynamic random-access memory is a type of RAM that serves as storage for every data bit within another capacitor in any given IC (integrated circuit).
General Applications	The general application areas of an SRAM are the L3 and L2 cache units in the CPU.	The DRAM works as the main memory in the computers (for example, DDR3).
Size	SRAM typically has a storage capacity of 1 MB- 16 MB.	DRAM has a usual capacity of 1 GB0 2GB, commonly found in tablets and smartphones. In most laptops, its storage capacity can be up to 4 GB- 16GB.
Position of Mem	You can find SRAM on the processor. Or it stays lodged between the processor and the main memory of any computing device.	You can find DRAM on the motherboard of a device.

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Storage Capacity	SRAM usually has a smaller size of storage.	The storage capacity of DRAM is comparatively larger.
Speed	SRAM stays in the form of on-chip memory. The access time is lesser than DRAM. Thus, it is comparatively faster.	DRAM possesses the characteristics of off-chip memory. The substantial access time is more than SRAM, and thus, it is slower.
Cost	SRAM is less cost-effective and more expensive than DRAM.	DRAM is available at a reasonable price. It is more cost-effective.
Density	SRAM is low in density and rarer.	DRAM is highly dense compared to SRAM.
Total Number of Transistors	Since SRAM has a single block of memory, including six transistors becomes necessary.	A single transistor can form a memory block with only a single transistor.
Design	It is very complicated to construct and design SRAM. It is because it uses	The DRAM is comparatively easy to implement because it also has a simplistic design. The total number of transistors present in a memory module

and Construction	various types of transistors to implement its performance.	impacts the capacity of a DRAM. Thus, the DRAM module can be six times more capable than the SRAM module (that has the same number of transistors).
Consumption of Power	The principle that SRAM follows relates to the constant change of a current direction through the switches. It has no charges like the DRAM.	The rate of power consumption is comparatively higher in DRAM as compared to SRAM.
Nature of Leaking Charge	SRAM faces no issues of leakage of charge.	The DRAM utilizes a capacitor that produces a leakage current. It makes DRAM dynamic. It's possible because a dielectric current is present inside a capacitor. A dielectric separates the constructive plates. It does not serve as a perfect insulator- thus, DRAM requires a power refresh circuitry.
Simplicity	The modules of SRAM are more straightforward when compared to the DRAM modules. One can develop easy-to-build interfaces for accessing the memory.	DRAMs are very complex as compared to SRAMs.
Ad	Consumption of power is low, and the	Manufacturing cost is low, and memory capacity is

vantage	speed of access is fast.	greater.
Disadvantage	Memory capacity is less, and manufacturing cost is fairly high.	Power consumption is high, and access speed is slow.

Designing a memory subsystem involves selecting and integrating various types of memory components, such as SRAM (Static Random-Access Memory) and DRAM (Dynamic Random-Access Memory), to meet the specific requirements of a computer system. Here's a general overview of the design considerations for a memory subsystem using both SRAM and DRAM:

1. Memory Hierarchy:
Memory subsystems often employ a hierarchical structure to balance speed, cost, and capacity. The hierarchy typically includes levels such as L1 cache, L2 cache, main memory (DRAM), and secondary storage (e.g., SSD or HDD). SRAM is often used for cache levels due to its faster access times, while DRAM is used for main memory.

2. Cache Design with SRAM:
L1 Cache: SRAM is commonly used for Level 1 (L1) caches due to its high speed and low-latency characteristics. The L1 cache is small but provides fast access to frequently used data.
L2 Cache: Depending on the design, L2 caches may also use SRAM, providing larger capacity than L1 with slightly higher latency.

3. Main Memory with DRAM:
Capacity: DRAM is used for the main memory due to its higher density and lower cost per bit compared to SRAM. DRAM allows for larger memory capacities, which is essential for storing the entire working set of data for most applications.

Refresh Cycle: DRAM requires periodic refresh cycles to maintain data integrity, as it stores charge in capacitors. The memory controller must manage these refresh cycles to prevent data loss.

4. Memory Controller:
Interface: The memory controller interfaces with the CPU and manages data transfers between the CPU and memory subsystem. It handles address decoding, read/write operations, and data transfer timings.

Memory Mapping: The memory controller maps logical addresses from the CPU to physical addresses in the memory subsystem.
5. Latency and Bandwidth Optimization:
Access Latency: SRAM provides low access latency, making it suitable for caching frequently accessed data. DRAM, while slower, provides higher density.

Memory Bus: Optimize the memory bus width and speed to balance the need for high bandwidth with the cost of the memory subsystem.

6. Error Handling:
Error Correction Code (ECC): Implement ECC in the memory subsystem to detect and correct errors in data stored in memory.
7. Power Consumption:
Power Management: Implement power-saving features in the memory subsystem to manage power consumption, especially in mobile devices or battery-powered systems.
8. Memory Interfacing:
Data Bus and Address Bus Width: Determine the appropriate data bus and address bus widths based on the system's requirements and architecture.
9. Memory Mapping:
Virtual Memory: Consider virtual memory management to provide an illusion of a larger address space than physically available memory.
10. System Integration:
Integration with CPU and I/O Devices: Ensure seamless integration with the CPU and other I/O devices, managing data transfers efficiently.
Remember that the specific requirements and constraints of the target system will heavily influence the design decisions for the memory subsystem. Additionally, advancements in memory technologies and architectures may introduce new considerations.