Digital Systems Design

Processor Logic Design

Introduction

- A computer CPU must manipulate not only data but also instruction codes and addresses coming from memory.
- The register that holds and manipulates the operation code of instructions is considered to be part of the control unit.
- Here, we will learn about the general-purpose register, commonly called an accumulator.

Processor Organization

- In a well organized processor unit, the data paths are formed by means of buses and other common lines.
- The control gates that formulate the given path are essentially multiplexers and decoders whose selection lines specify the required path.
- All organizations employ a common ALU and shifter.
- The differences in organizations are mostly manifested in the organization of the registers and their common path to the ALU.

Bus Organization

- When a large number of registers are included in a processor unit, it is most efficient to connect them through common buses or arrange them as a small memory having very fast access time.
- In the figure, there are 4 processor registers. Each register is connected to 2 MUXs to form input buses *A* and *B*.
- The result from the shifter goes through the output bus *S* into the inputs of all registers.

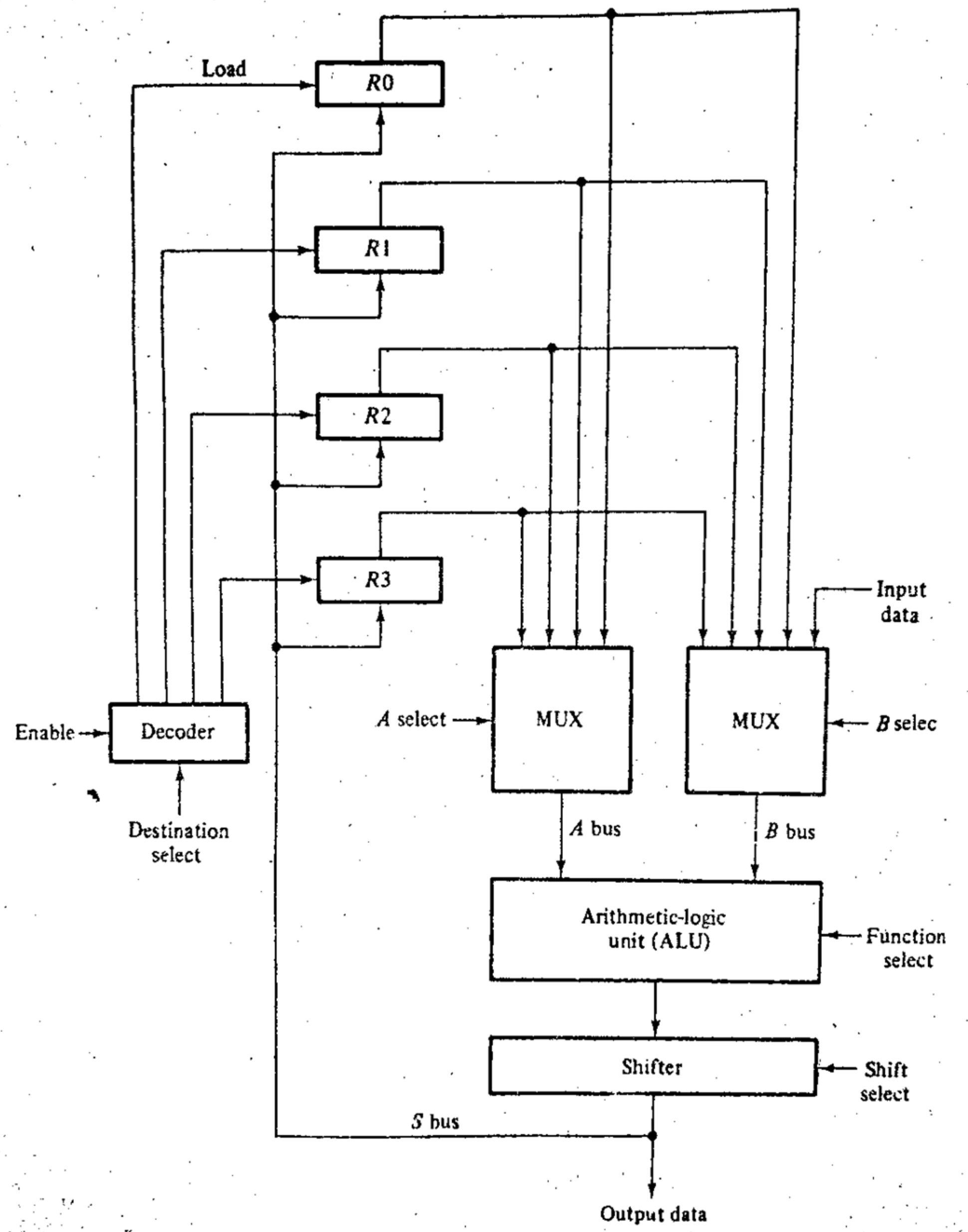


Figure 9-1 Processor registers and ALU connected through common buses

Scratchpad Memory

- The registers in a processor unit can be enclosed within a small memory unit. This memory is called scratchpad memory.
- For example, a processor unit employs 8 registers of 16 bits each. The 8 memory words can be designated *R0* through *R7*.
- A single register can be selected by means of an address to the memory unit.

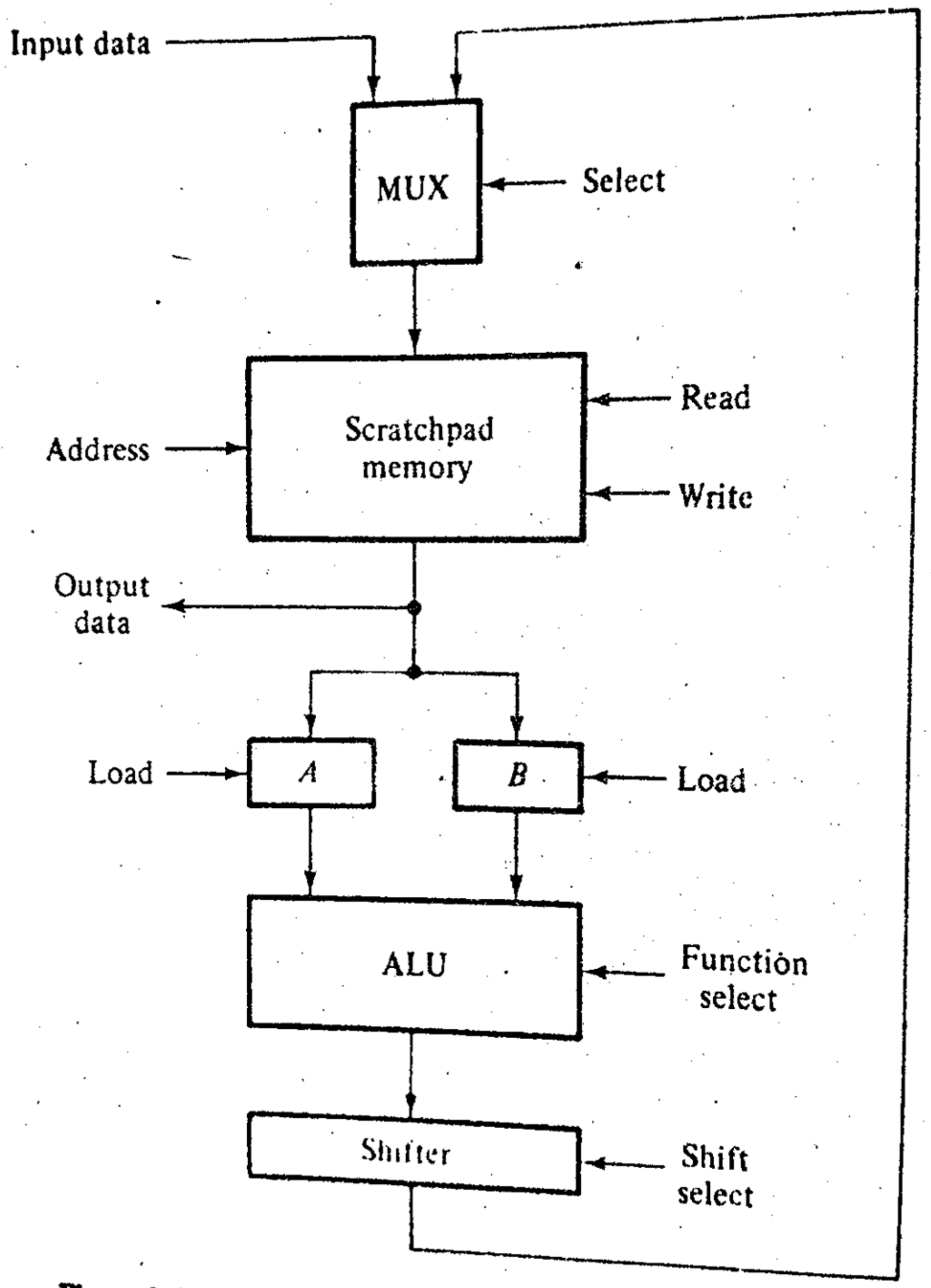


Figure 9-2 Processor unit employing a scratchpad memory

2-Port Memory

- Some processors employ a 2-port memory in order to overcome the delay caused when reading 2 source registers.
- When enabled by the memory enable (*ME*) input, new data can be written into the word specified by the *B* address.

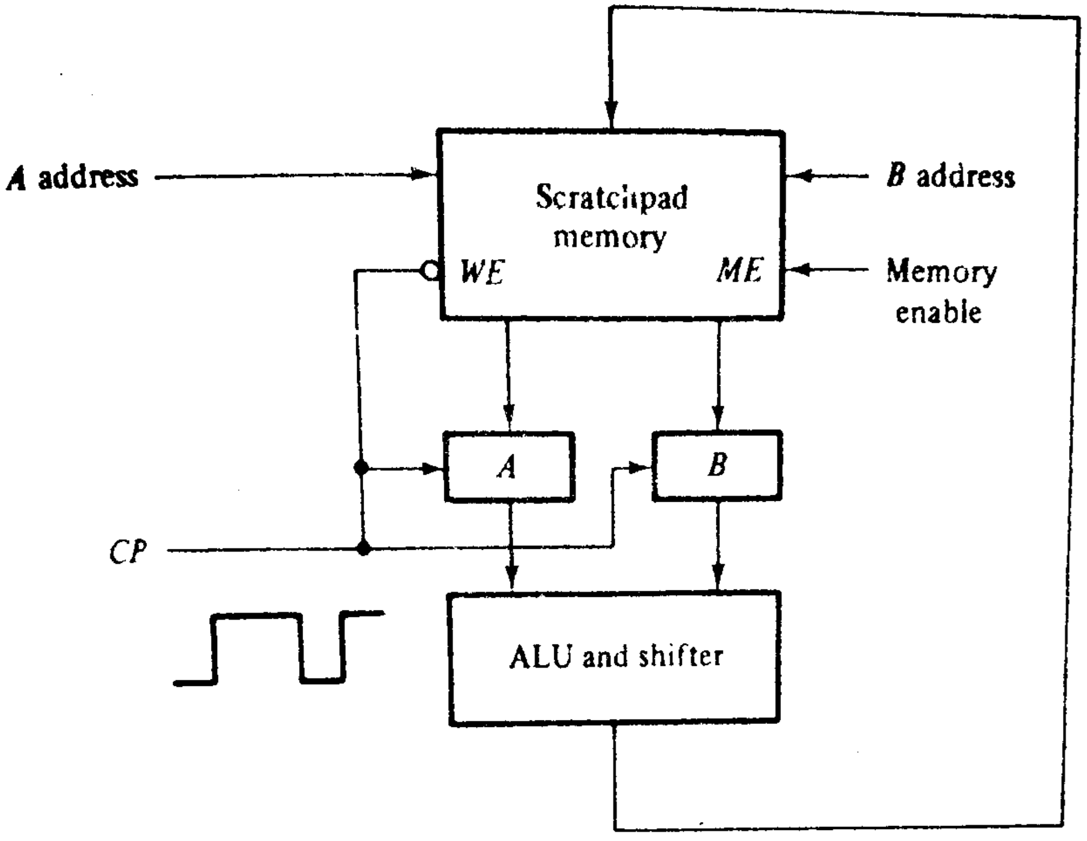
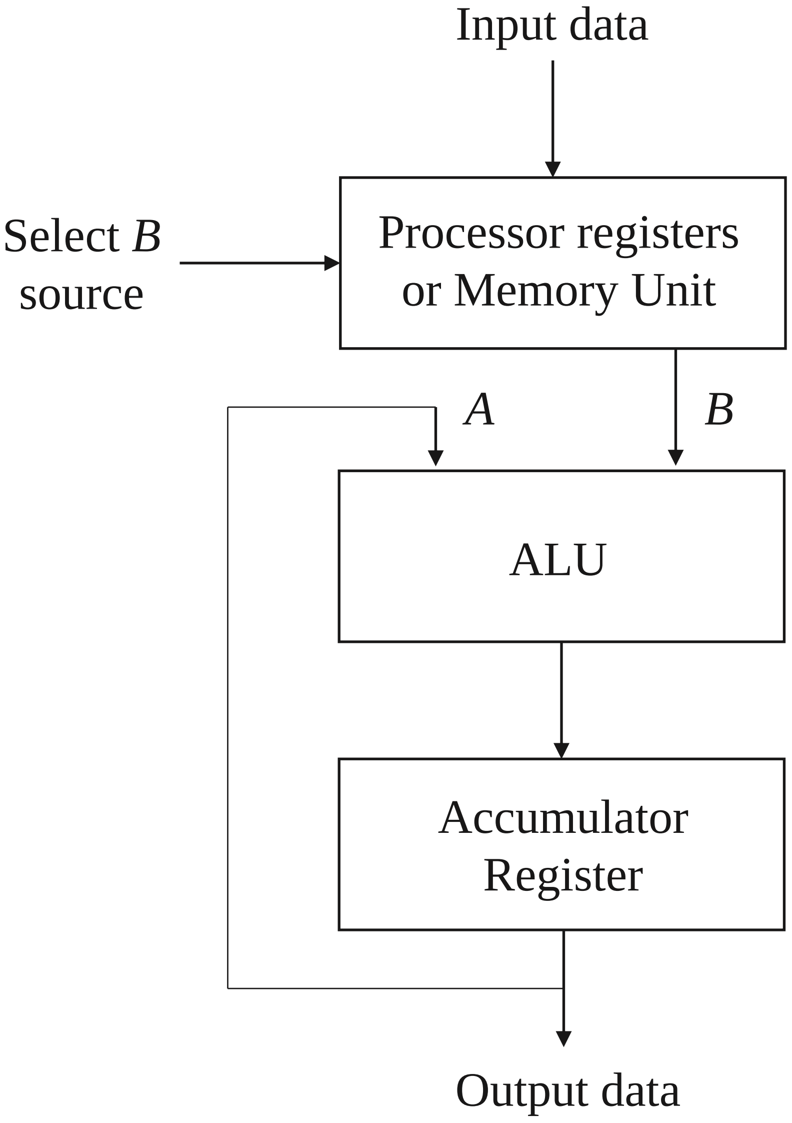


Figure 9-3 Processor unit with a 2-port memory

Accumulator Register

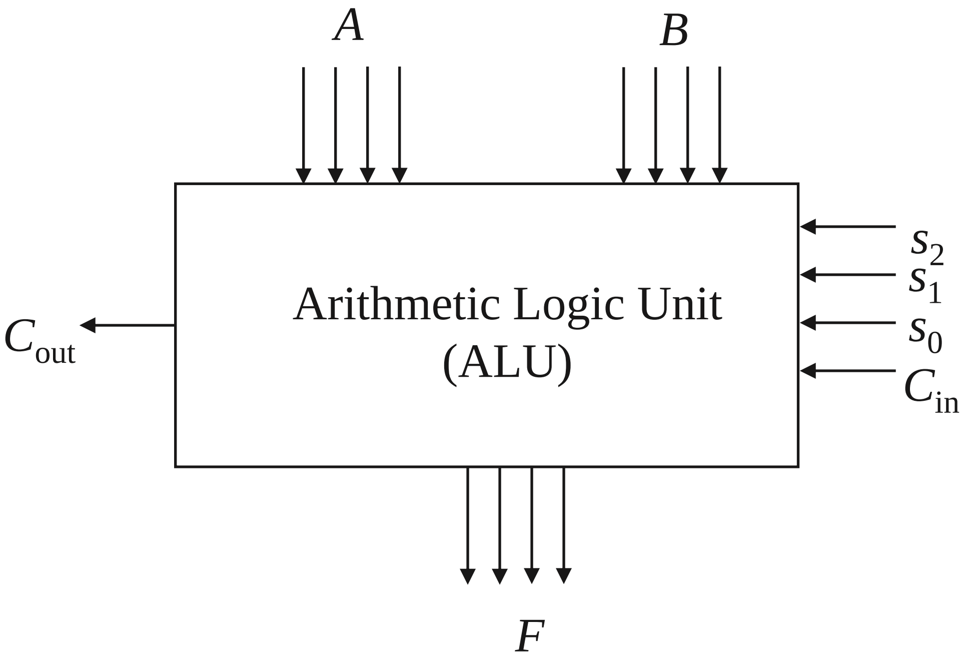
- Some processor units separate one register from all others and call it an accumulator register (*AC* or *A* register).
- It is a multipurpose register capable of performing not only the add microoperation, but many other microoperations as well.
- To form the sum of 2 numbers stored in processor unit, we need;

$$T_1: \quad A \leftarrow 0$$
$$T_2: \quad A \leftarrow A + R1$$
$$T_3: \quad A \leftarrow A + R2$$



Arithmetic Logic Unit

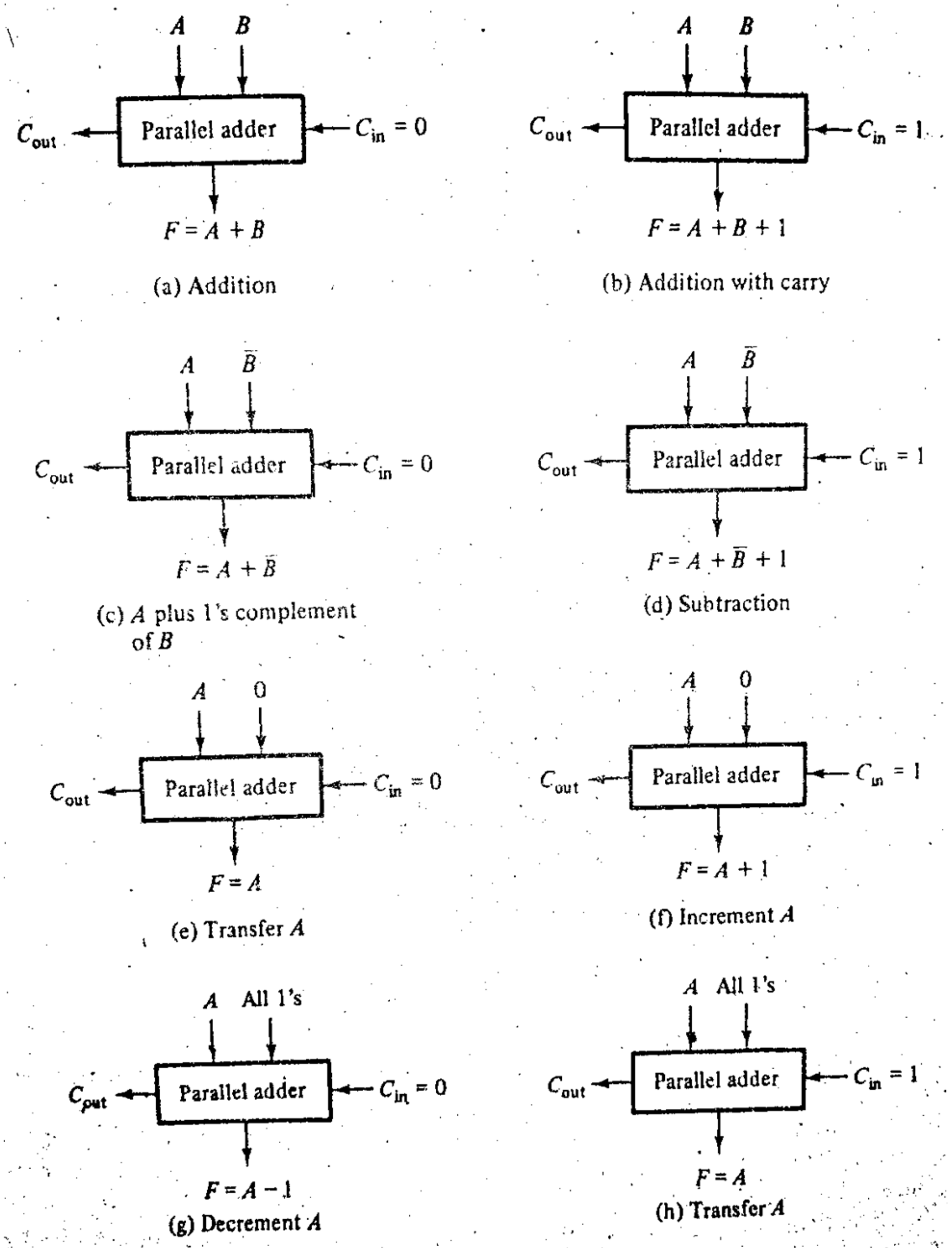
- ALU can perform a set of basic arithmetic operations and a set of logic operations.
- It has a number of selection lines to select a particular operation in the unit.
- The selection lines are decoded within the ALU so that *k* selection variables can specify up to 2^k distinct operations.



Design of Arithmetic Circui

- The basic component of the arithmetic section of an ALU is a parallel adder.
- A parallel adder is constructed with a number of full-adder circuits connected in cascade.
- The circuit that controls input B to provide the functions is called a *true/complement*, *one/zero* element.

S_1	S_0	Y_i
0	0	0
0	1	B_i
1	0	B_i'
1	1	1



(a) Addition

(b) Addition with carry

(c) *A* plus 1's complement of *B*

(d) Subtraction

(e) Transfer *A*

(f) Increment *A*

(g) Decrement *A*

(h) Transfer *A*

Figure 9-6 Operations obtained by controlling one set of inputs to a parallel adder

Design of Arithmetic Circuit

Function select			Y equals	Output equals
s_1	s_0	C_{in}		
0	0	0	0	$F = A$
0	0	1	0	$F = A + 1$
0	1	0	B	$F = A + B$
0	1	1	B	$F = A + B + 1$
1	0	0	B'	$F = A + B'$
1	0	1	B'	$F = A + B' + 1$
1	1	0	All 1’s	$F = A – 1$
1	1	1	All 1’s	$F = A$

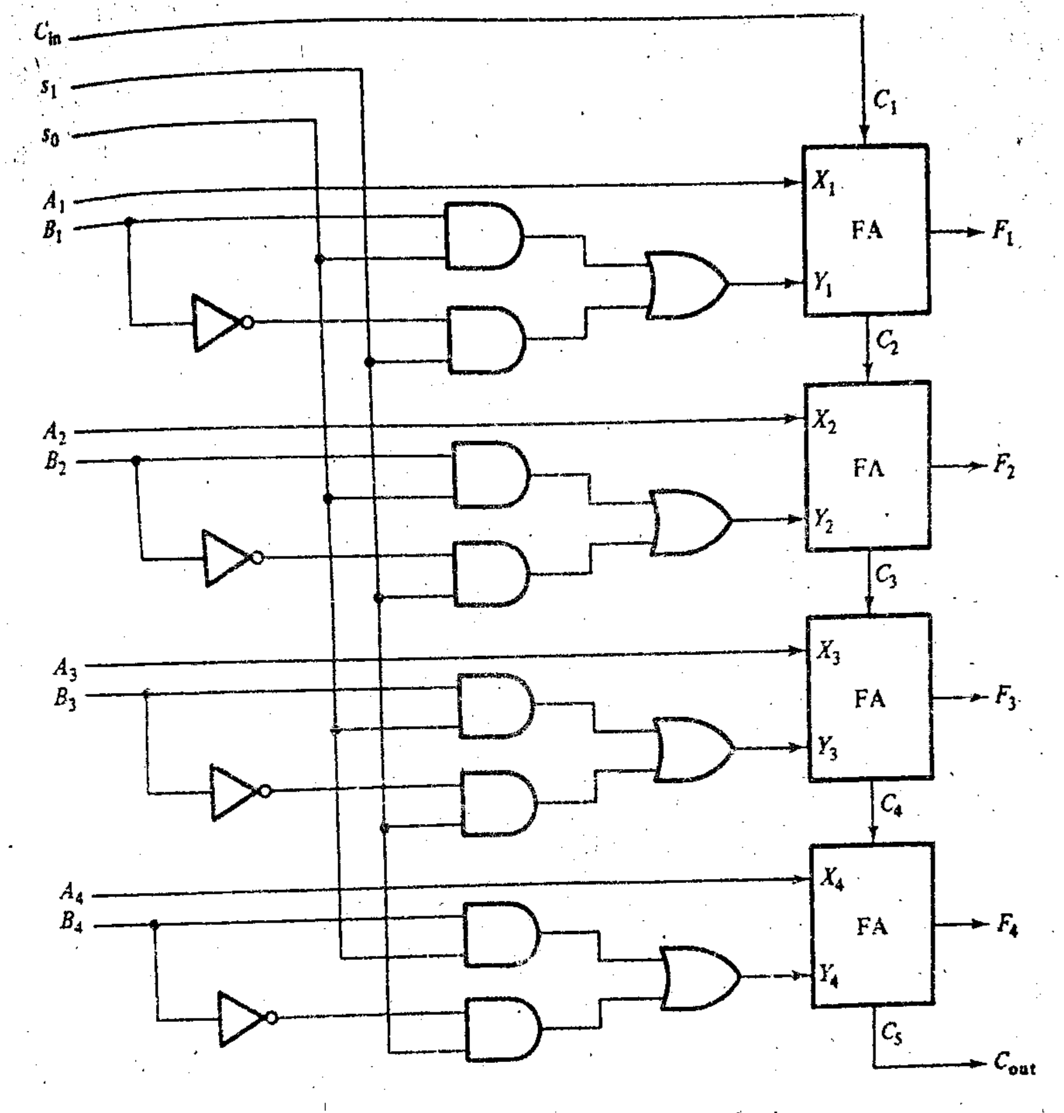


Figure 9-8 Logic diagram of arithmetic circuit

Design of Logic Circuit

s_1	s_0	Output	Operation
0	0	$F = A + B$	OR
0	1	$F = A \oplus B$	XOR
1	0	$F = AB$	AND
1	1	$F' = A'$	NOT

Design of Arithmetic Logic Unit

- To combine the two unit we need another selection line s_2.

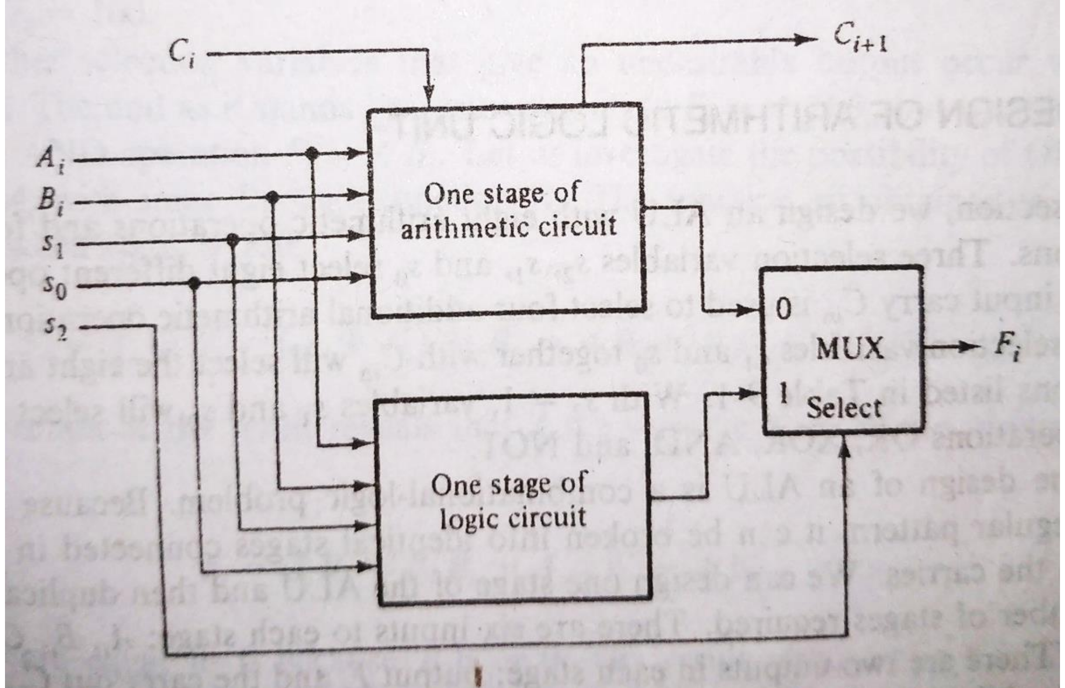


Figure 9-12 Combining logic and arithmetic circuits

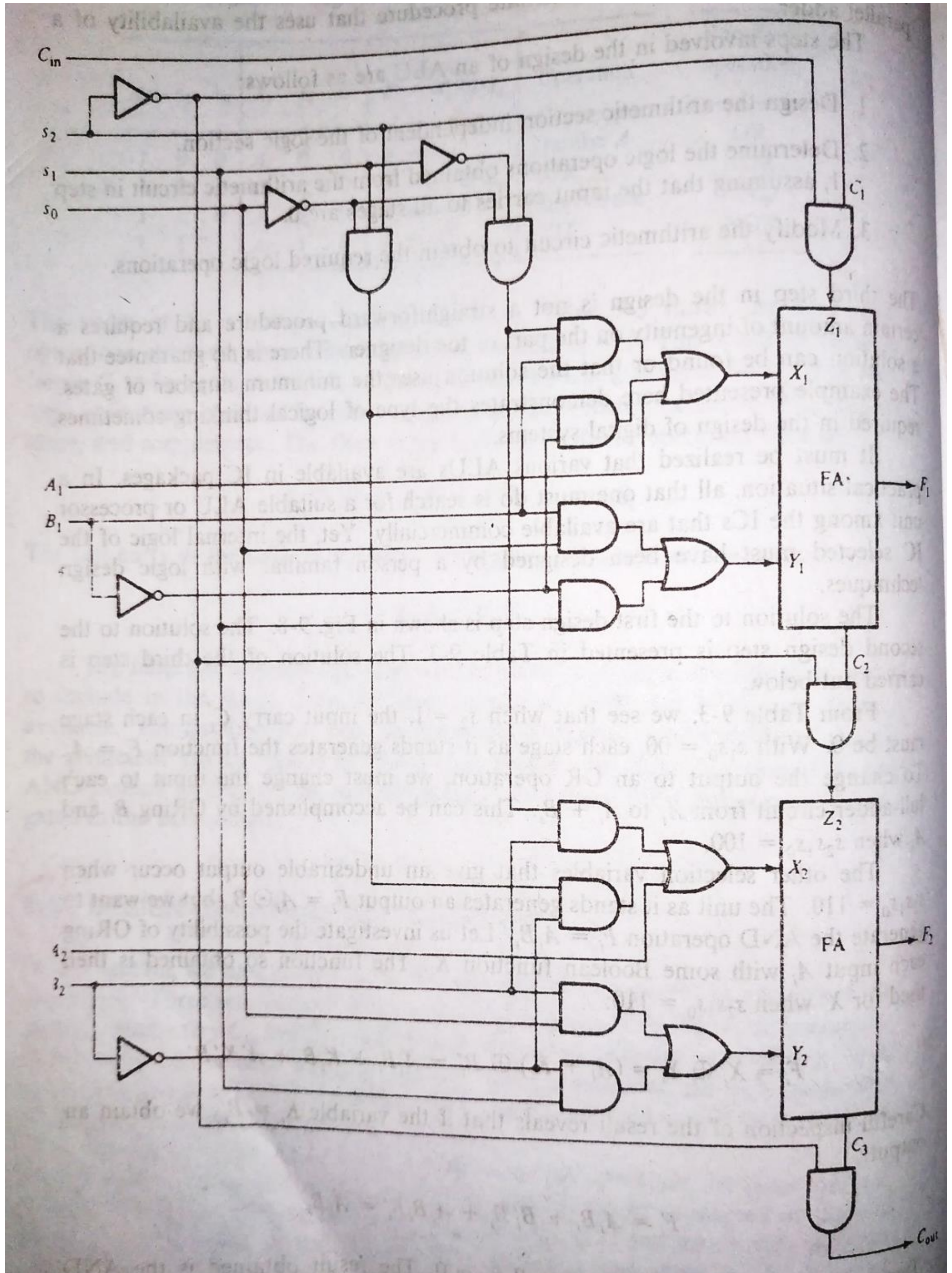


Figure 9-13 Logic diagram of arithmetic logic unit (ALU)

Status Register

- It is sometimes convenient to supplement the ALU with a status register where these status-bit conditions are stored for further analysis.
- Status-bit conditions are sometimes called *condition-code* bits or *flag* bits.

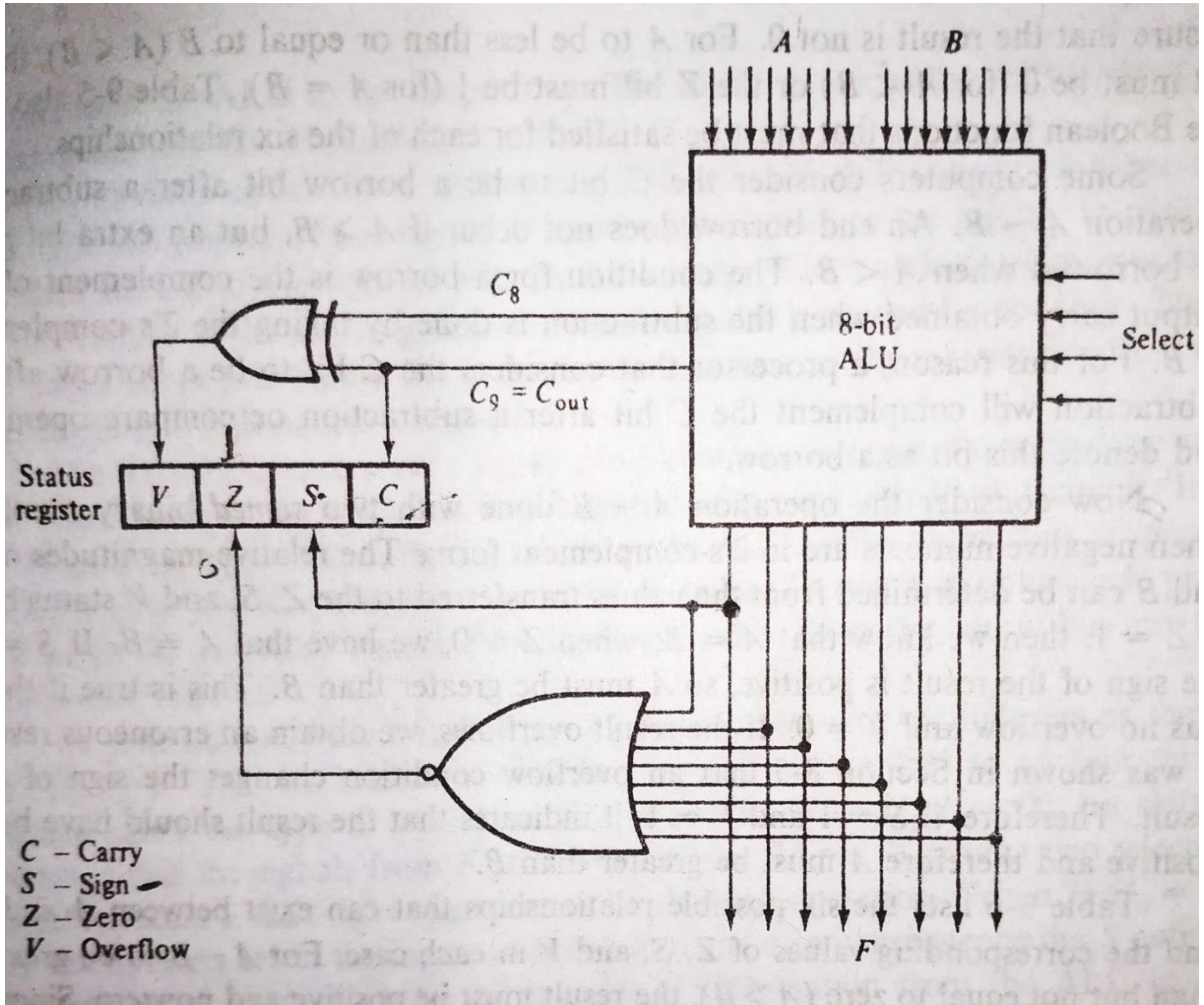


Figure 9-14 Setting bits in a status register

- The shifter may transfer the information directly without a shift, or it may shift the information to the right or to the left.
- H_2 may be employed to specify I_R or I_L during shift.

H_1	H_0	Operation
0	0	No shift
0	1	Shift right
1	0	Shift left
1	1	Assign zero

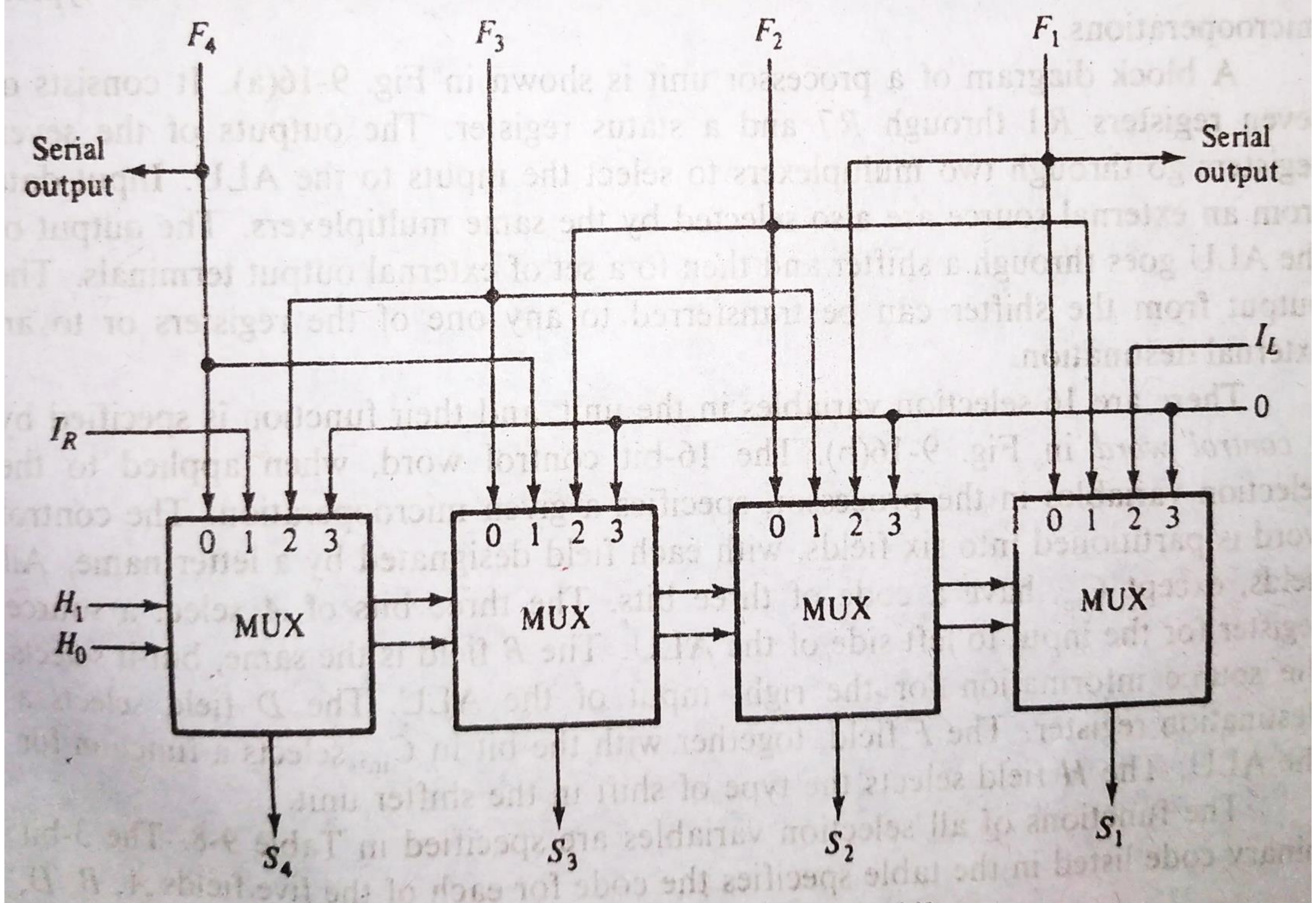
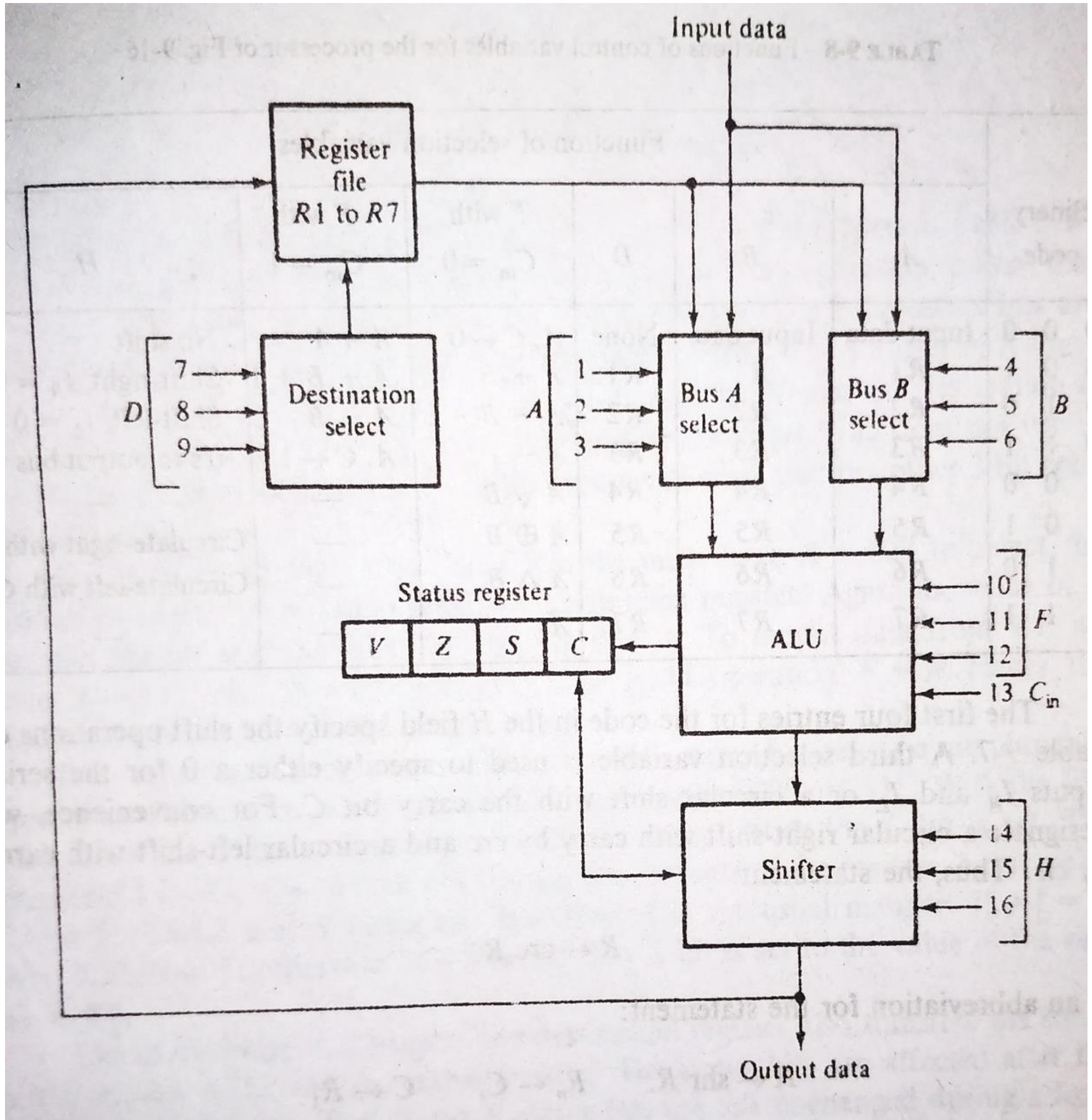


Figure 9-15 4-bit combinational-logic shifter

Processor Unit

	1..3	4..6	7..9	10..12	13	14..16
Control word	*A*	*B*	*D*	*F*	C_{in}	*H*

- The selection variables in a processor unit control the microoperations executed within the processor during any given clock pulse.
- 16 selection variables in the unit and their functions is specified by a *control word*.
- The control word is partitioned into 6 fields with each field designated by a letter name.

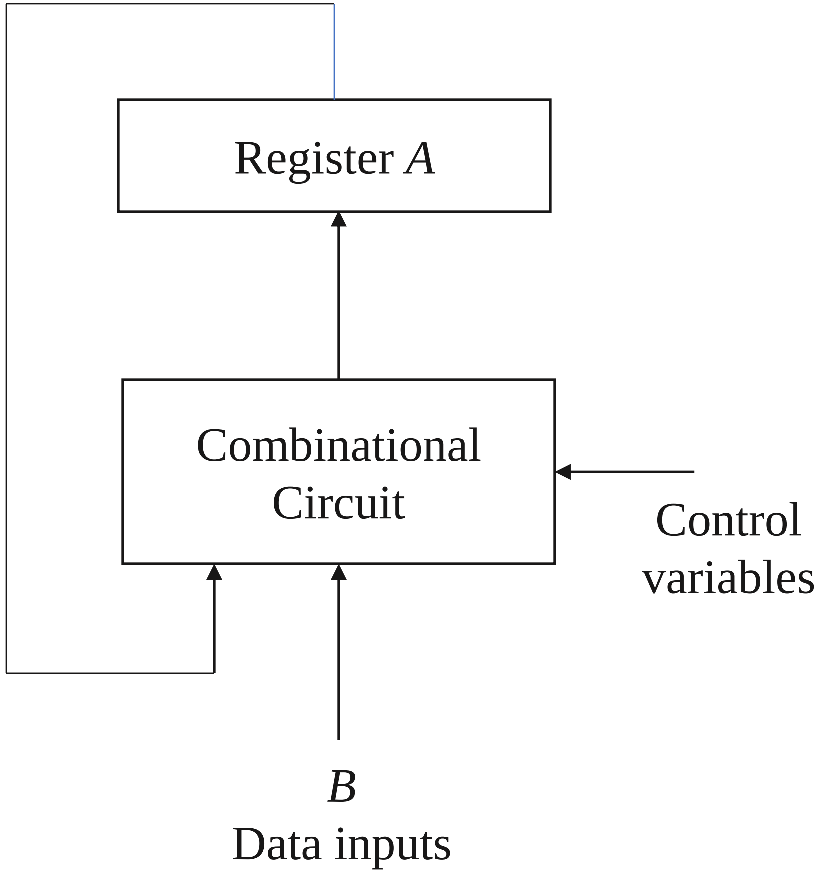


(a) Block diagram

Design of Accumulator

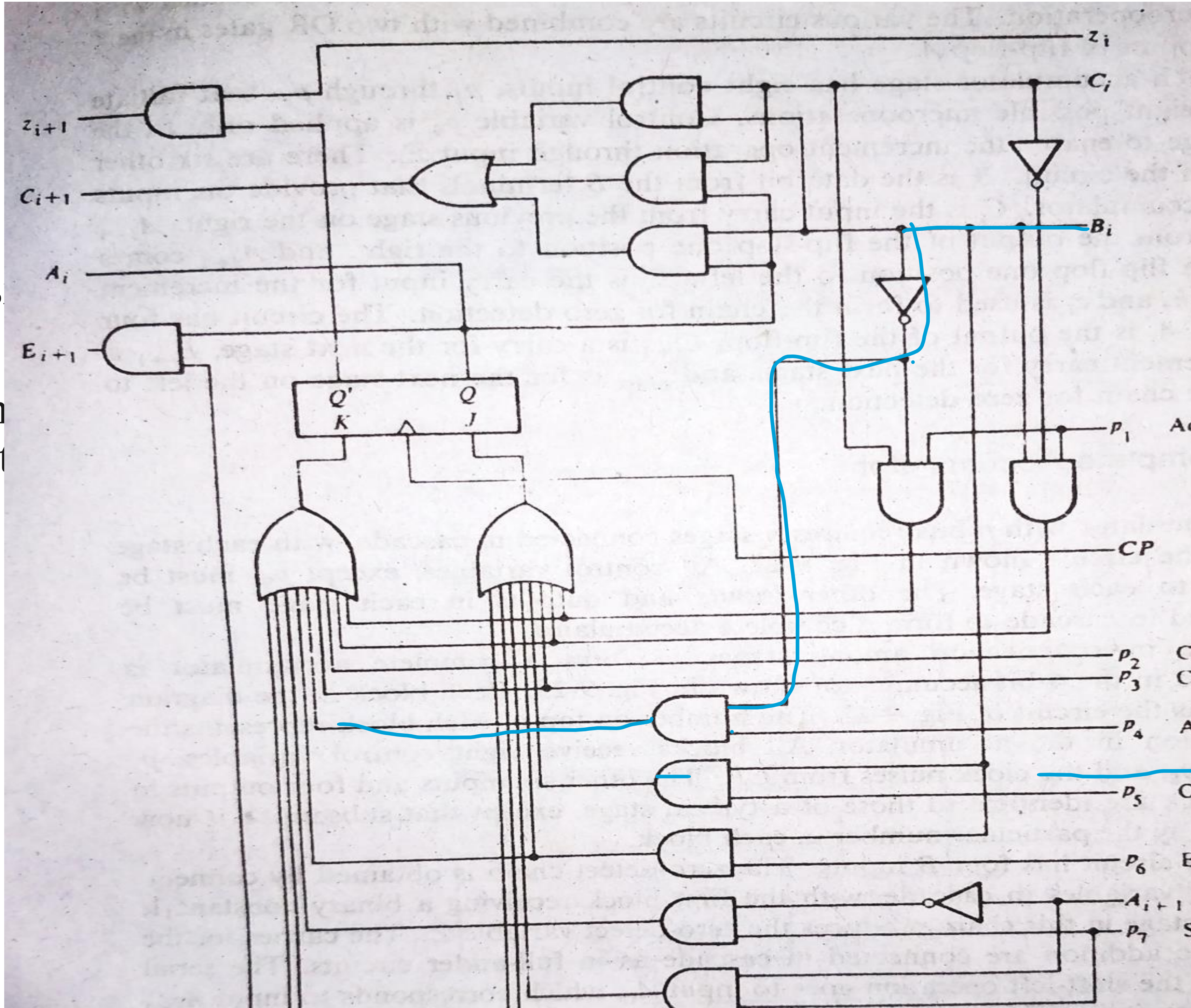
- An accumulator is a sequential circuit with *A* register and the associated combinational circuit. It requires control variables p_1 through p_9 generated by control logic circuits.

Control variable	Microoperation	Name
p_1	$A \leftarrow A+B$	Add
p_2	$A \leftarrow 0$	Clear
p_3	$A \leftarrow A'$	Complement
p_4	$A \leftarrow A \wedge B$	AND
p_5	$A \leftarrow A \vee B$	OR
p_6	$A \leftarrow A \oplus B$	Exclusive-OR
p_7	$A \leftarrow$ shr A	Shift right
p_8	$A \leftarrow$ shl A	Shift left
p_9	$A \leftarrow A+1$	Increment



One Stage of

- The register we are us flip-flops.
- We must ensure that on is enabled at any given t



Complete Accumulator

- Finally an accumulator with *n* bits requires *n* stages connected in cascade, with each stage having the circuit in the figure.

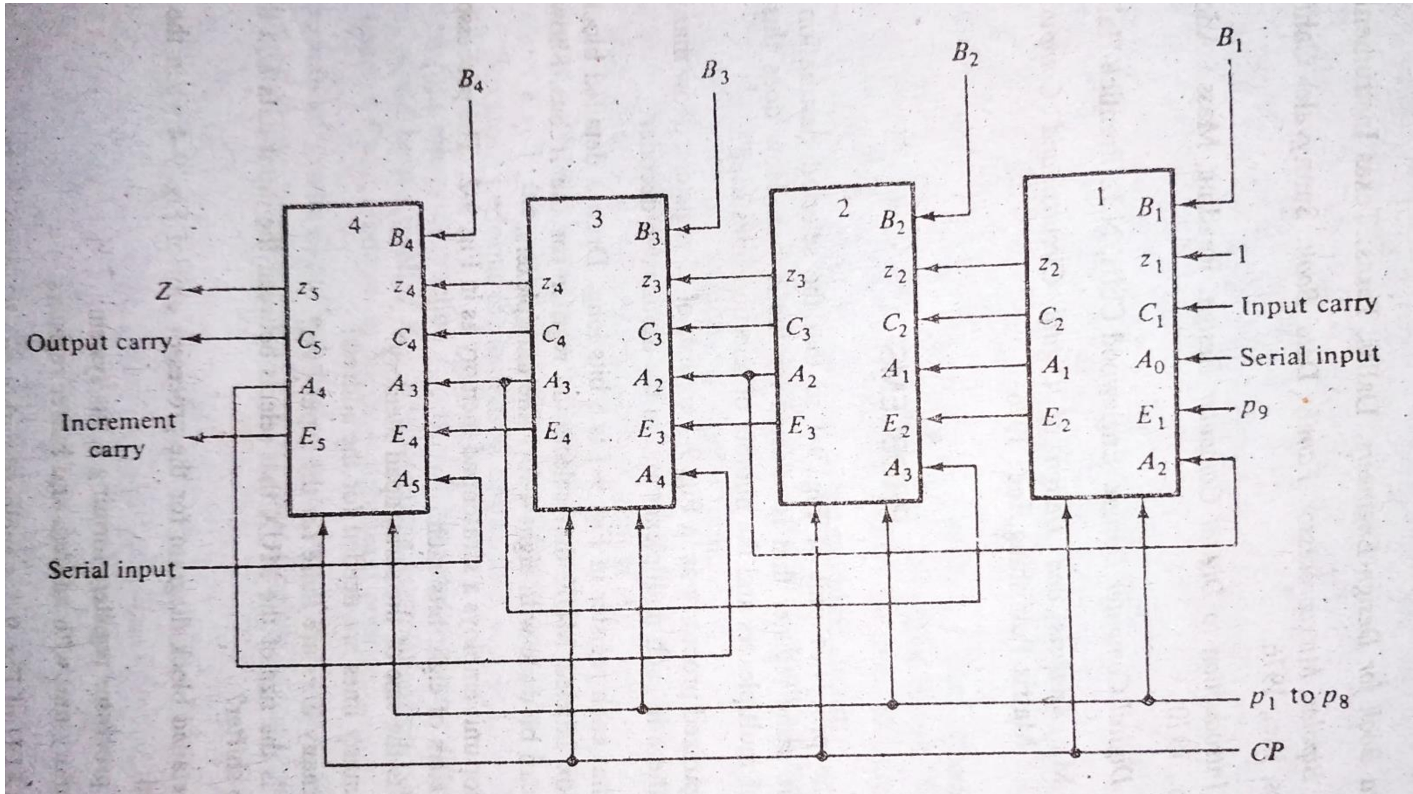


Figure 9-23 4-bit accumulator constructed with four stages