Department of Computer Science & Engineering
Midterm Examination

Course No: CSE203
Course Title: Digital Logic Design

1. Design of a sequential circuit with two *JK* flip-flops and one input, *x*. When $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

2. Design of a counter with the following repeated binary sequence: 0, 1, 2, 4, 6 using *JK* flip-flops.

3. Design of a counter with the following repeated binary sequence: 0, 1, 3, 7, 6, 4 using *T* flip-flops.

4. To reduce the number of the states in the following state table and tabulate the reduced state table.

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*f*	*b*	0	0
b	*d*	*c*	0	0
c	*f*	*e*	0	0
d	*g*	*a*	1	0
e	*d*	*c*	0	0
f	*f*	*b*	1	1
g	*g*	*h*	0	1
h	*g*	*a*	1	0

5. Design of a sequential circuit that has three *D* flip-flops A, B, C; one input, *x* and one output, *y* using the following state diagram.