



Intro to Logic Gates & Datasheets

Digital Electronics



Intro to Logic Gates & Datasheets

This presentation will

- Introduce integrated circuits (ICs).
- Present an overview of :
 - Transistor-Transistor Logic – **TTL**
 - Complementary Metal Oxide Semiconductor - **CMOS**
- Define the scale of integration and package styles.
- Describe the TTL logic gate numbering system.
- Review manufacturer datasheets.



Introduction to Integrated Circuits

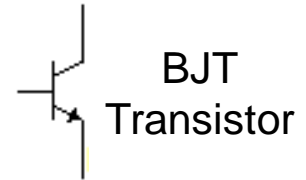
- All logic gates are available in Integrated Circuits (ICs)
- ICs are categorized in three different ways:
 - The underlying technology upon which their circuitry is based:
 - Transistor-Transistor Logic - **TTL**
 - Complementary Metal Oxide Semiconductor - **CMOS**
 - The scale of integration:
 - Small Scale Integration - **SSI**
 - Medium Scale Integration - **MSI**
 - Large Scale Integration - **LSI**
 - Very Large Scale Integration - **VLSI**
 - Package Style
 - Through-Hole Technology - **THT**
 - Dual Inline Packages - **DIP**
 - Surface-Mount Technology - **SMT**
 - Small Outline IC - **SOIC**
 - Plastic Leaded Chip Carrier - **PLCC**
 - Quad Flat Pack - **QFP**



TTL Vs. CMOS Logic

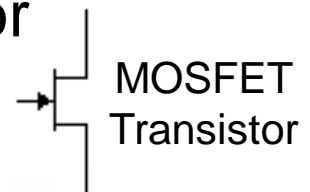
TTL: Transistor-Transistor Logic

- Constructed from Bipolar Junction Transistors (BJT)
- Advantages:
 - *Faster than CMOS*
 - *Not sensitive to damage from electrostatic-discharge*
- Disadvantages:
 - *Uses more power than CMOS*



CMOS: Complementary Metal Oxide Semiconductor

- Constructed from Metal Oxide Semiconductor Field-Effect Transistors (MOSFET)
- Advantages:
 - *Uses less power than TTL*
- Disadvantages:
 - *Slower than TTL*
 - *Very sensitive to damage from electrostatic-discharge*



IC Density of Integration

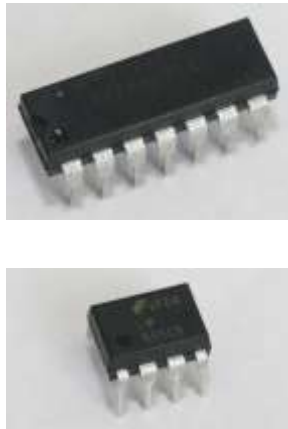
Density of Integration / Complexity	Gates per IC
SSI: Small-Scale Integration <ul style="list-style-type: none">• Logic Gates (AND, OR, NAND, NOR)	<10
MSI: Medium-Scale Integration <ul style="list-style-type: none">• Flip Flops• Adders / Counters• Multiplexers & De-multiplexers	10 – 100
LSI: Large-Scale Integration <ul style="list-style-type: none">• Small Memory Chips• Programmable Logic Device	100 – 10,000
VLSI: Very Large-Scale Integration <ul style="list-style-type: none">• Large Memory Chips• Complex Programmable Logic Device	10,000 – 100,000
ULSI: Ultra Large-Scale Integration <ul style="list-style-type: none">• 8 & 16 Bit Microprocessors	100,000 – 1,000,000
GSI: Giga-Scale Integration <ul style="list-style-type: none">• Pentium IV Processor	>1,000,000



Package Styles

Through-Hole Technology (THT)

DIP: Dual Inline Package



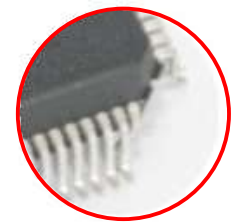
NOTE: For most commercial application, the DIP package has become obsolete. However, it is still the package of choice for educational applications because it can be used with proto-boards.

Surface Mount Technology (SMT)

SOIC: Small Outline IC



QFP: Quad Flat Pack



PLCC: Plastic Leaded Chip Carrier



Through-Hole Technology (THT)

- THT components have pins that are inserted into holes drilled in the PCB and soldered on the reverse side of the board.
- Advantages:
 - Designs with THT components are easier to hand-assemble than SMT-based designs because THT components are much larger.
 - THT components can be used in proto-boards.
- Disadvantages:
 - Designs with TMT components are significantly larger than SMT-based designs.
 - Most high-end electronics components (i.e., microprocessors) are not available in THT package styles.



Surface Mount Technology (SMT)

- SMT components are mounted on the surface of the PCB, so no holes need to be drilled.
- Primary Advantages:
 - Designs with SMT components are smaller than THT-based designs because SMT components are significantly smaller and have much higher pin counts than THT components.
 - Also, SMT components can be mounted on both sides of the PCB.
- Primary Disadvantages:
 - Designs with SMT components are more expensive to manufacture because the process is significantly more sophisticated than THT-based designs.
 - SMT components can not be used in a proto-boarding.



TTL Logic Sub-Families

TTL Series	Infix	Example	Comments
Standard TTL	none	7404	Original TTL gates. Slowest, uses a lot of power. (obsolete)
Low Power	L	74L04	Optimized to consume less power than "Standard". (obsolete)
Schottky	S	74S04	First to utilizes the Schottky transistor. Optimized for speed, but consumes a lot of power. (obsolete)
Low-Power Schottky	LS	74LS04	Faster and lower power consumption than the L & LS subfamilies. The type that is used throughout this course.
Advanced Schottky	AS	74A S04	Very fast, uses a lot of power.
Advanced Low-Power Schottky	ALS	74ALS04	Very good speed-power ratio. Quite popular member of this family.



TTL Logic Gate Numbering System

DM 74 LS 08 N

Package Style (i.e., N=DIP)

Logic Function (i.e., 04 = Inverter, 08 = AND Gate, etc.)

Logic Sub-family (i.e., LS = Low Power Schottky)

74-Series TTL

Manufacturer

- DM = Fairchild Semiconductor
- SN = Texas Instruments

Manufacturer Datasheets

A manufacturer datasheet for a logic gate contains the following information:

- General Description
- Connection (pin-out) Diagram
- Function Table
- Operating Conditions
- Electrical Characteristics
- Switching Characteristics
- Physical Dimensions

General Description

FAIRCHILD
SEMICONDUCTOR™

DM74LS08
Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

August 1986
Revised March 2000

DM74LS08 Quad 2-Input AND Gates

Ordering Code:

Order Number	Package Number	Package Description
DM74LS08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in tape and reel. Specify by appending the suffix letter 'X' to the ordering code.

Connection Diagram

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

DM74LS08

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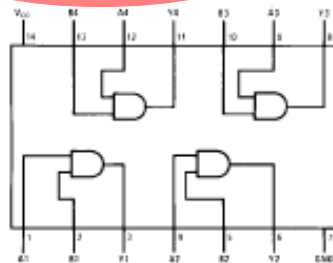
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Connection Diagram



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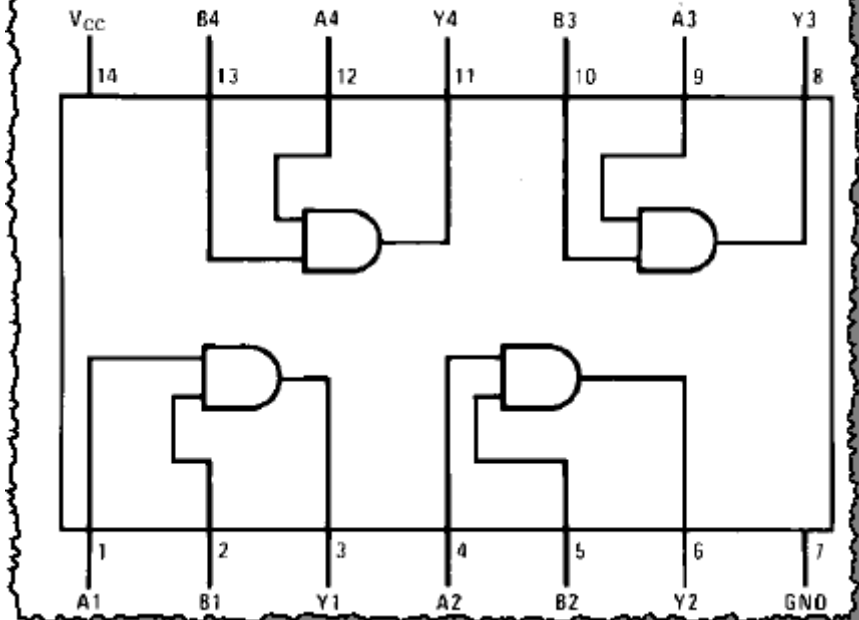
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Connection Diagram



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Recommended Operating Conditions

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The 'Absolute Maximum Ratings' are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The 'Recommended Operating Conditions' table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

LOW-to-HIGH Level Output	4	13	5	18	ns
HIGH-to-LOW Level Output	3	11	5	18	ns

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.



Electrical Characteristics

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The 'Absolute Maximum Ratings' are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The 'Recommended Operating Conditions' table will define the conditions for actual device operation.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max},$ $V_{IH} = \text{Min}$	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max},$ $V_{IL} = \text{Max}$		0.35	0.5	V
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 7V$			0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7V$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$			-0.36	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	-20		-100	mA
I_{CCH}	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}$		2.4	4.8	mA
I_{CCL}	Supply Current with Outputs LOW	$V_{CC} = \text{Max}$		4.4	8.8	mA



Switching Characteristics

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The 'Absolute Maximum Ratings' are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The 'Recommended Operating Conditions' table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{OH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R _L = 2 kΩ				Units
		C _L = 15 pF		C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

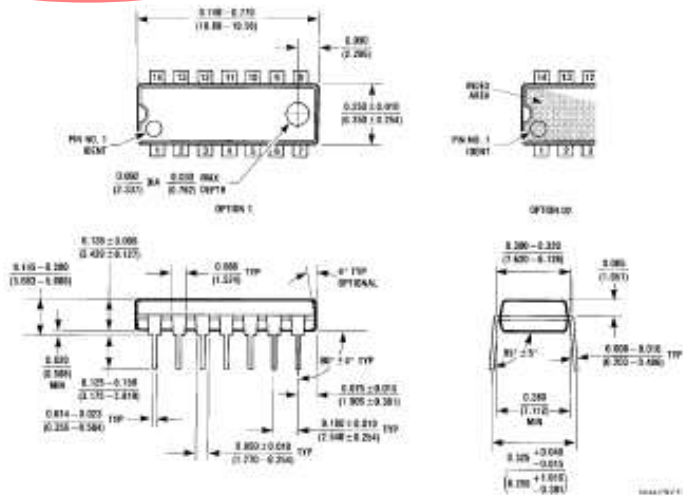
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.



Physical Dimensions

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DM74LS08 Quad 2-Input AND Gates



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A



Physical Dimensions

