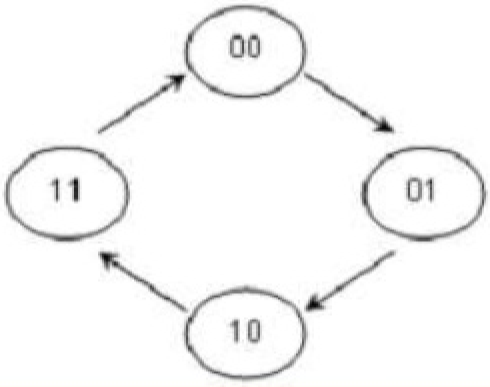
CHAPTER 2

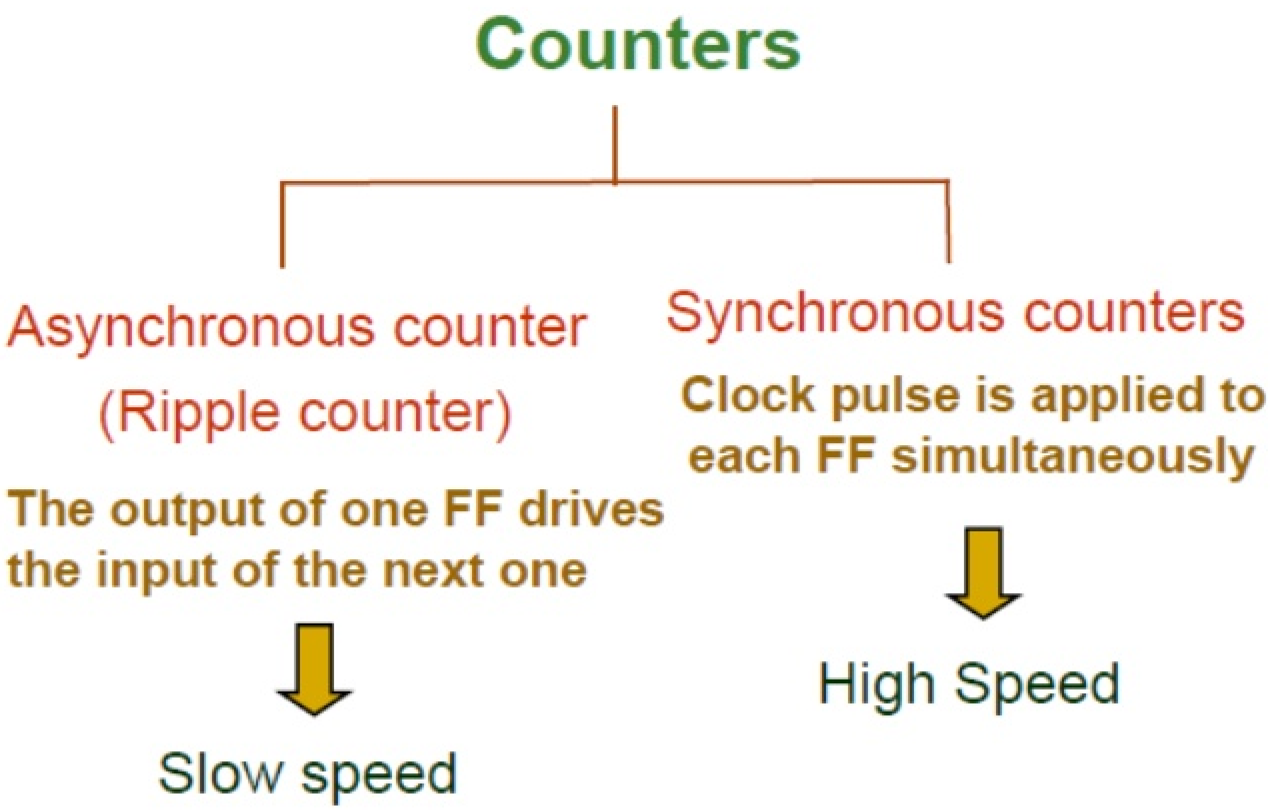
COUNTER

Introduction

- Counter

- A counter is a sequential logic circuit consisting of a set of flip-flops which can go through a sequence of states.





Counters

Asynchronous counter (Ripple counter)

The output of one FF drives the input of the next one

Slow speed

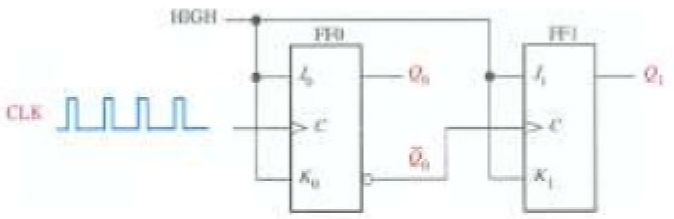
Synchronous counters

Clock pulse is applied to each FF simultaneously

High Speed

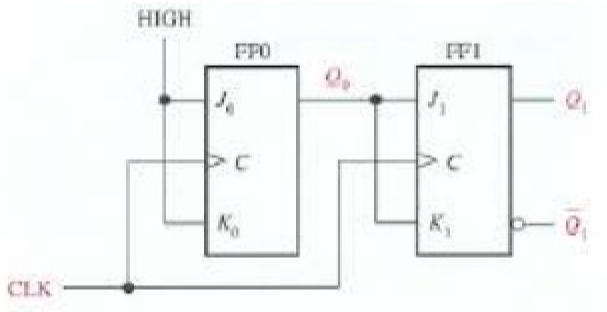
Introduction (continue)

- Counters are formed by connecting flip-flops together
- Types of counter are;
  - Asynchronous
    - Also known as ripple counter
    - The first flip-flop is driven by external clock while the successive flip-flops by the output of preceding flip-flop



Introduction (continue)

- Synchronous
  - All flip-flops are simultaneously driven by common clock



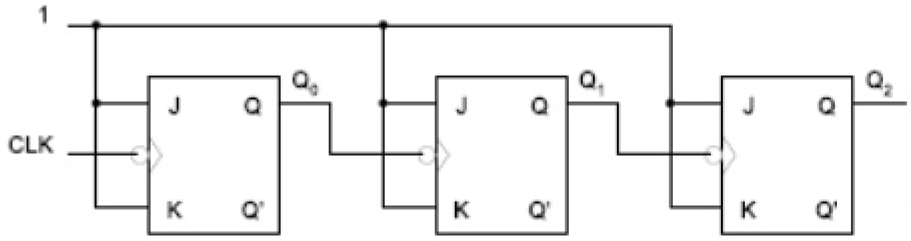
- Each type of counter are classified by;
  - Sequence i.e up or down
  - Number of states i.e 2-bit will have 4 states (2^N)
  - Number of flip-flops i.e same as number of bits

Asynchronous counter

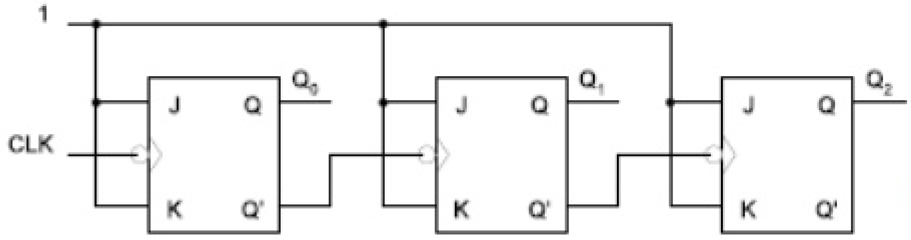
Asynchronous counter

- Also known as ripple counter. Ripple counters are the simplest type of binary counters because they require the fewest components to produce a given counting operation.
- Each FF output drives the CLK input of the next FF.
- FFs do not change states in exact synchronism with the applied clock pulses.
- *There is delay between the responses of successive FFs.*
- It is also often referred to as a *ripple counter* due to the way the FFs respond one after another in a kind of rippling effect.

Up counter and down counter for negative edge clock

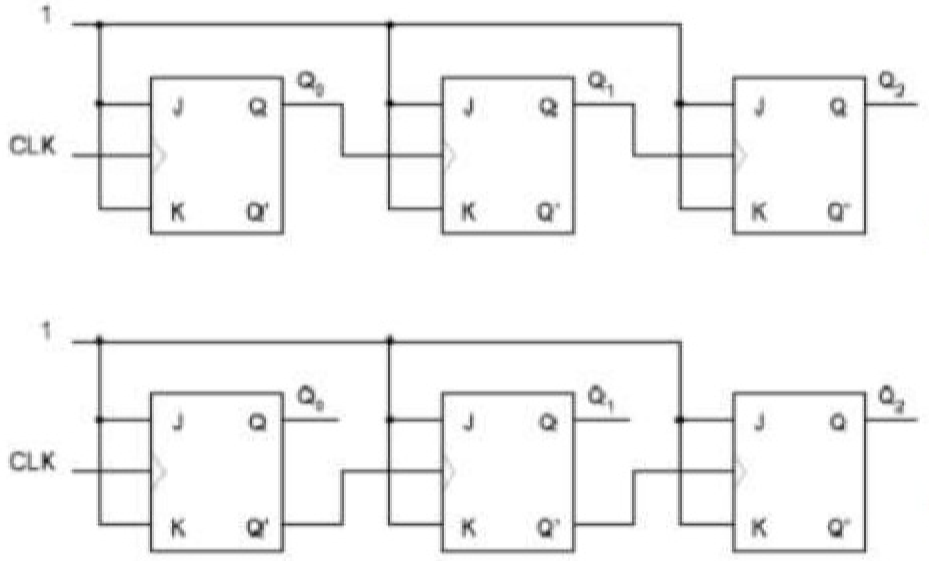


3-bit binary up counter



3-bit binary down counter

Up counter and down counter for positive edge clock

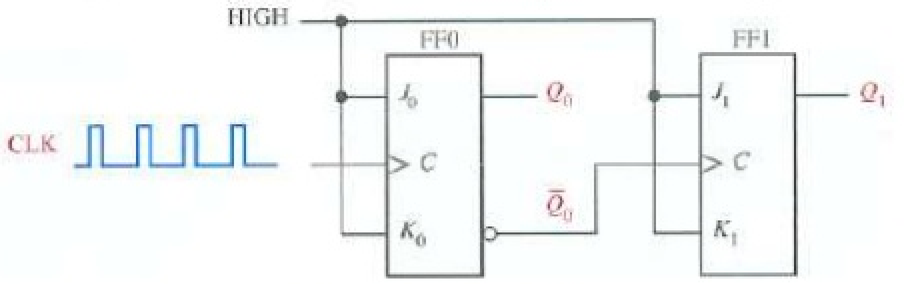


3-bit binary down counter

3-bit binary up counter

Asynchronous Counter Operation

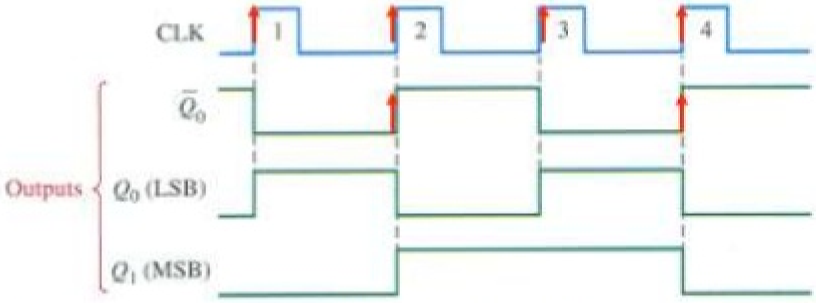
- For example, 2-bit asynchronous binary counter using J-K FF



- CLK is only connected to 1st FF0, LSB FF
- The 2nd FF clock is driven by $\overline{Q_0}$ of 1st FF
- Both FF input are always HIGH
- Q_0 changes state at the positive-edge clock
- Q_1 change at the positive-edge of the $\overline{Q_0}$
- Note that the two FFs do not triggered at the same time because clock and Q_0 transitions do not occur at the same time

Asynchronous Counter Operation (continue..)

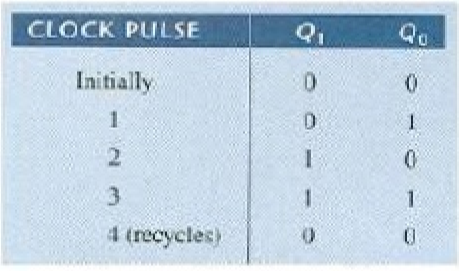
- Timing diagram for 2-bit asynchronous binary counter



- Four clock pulses are applied, assume initially all LOW
- Q_0 (LSB) is always toggle at positive-edge clock (J and K are HIGH)
- $\overline{Q_0}$ is reciprocal of Q_0
- Q_1(MSB) is toggle at positive-edge of Q_0
- At 4th clock pulse, the counter is recycle to its original state (both FF are LOW)

Asynchronous Counter Operation (continue..)

- Binary state sequence for 2-bit asynchronous binary counter

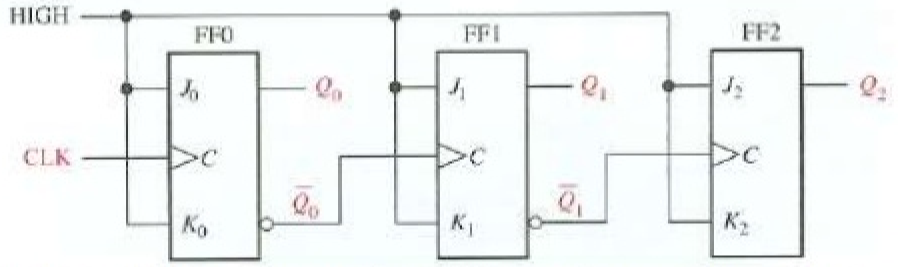


CLOCK PULSE	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

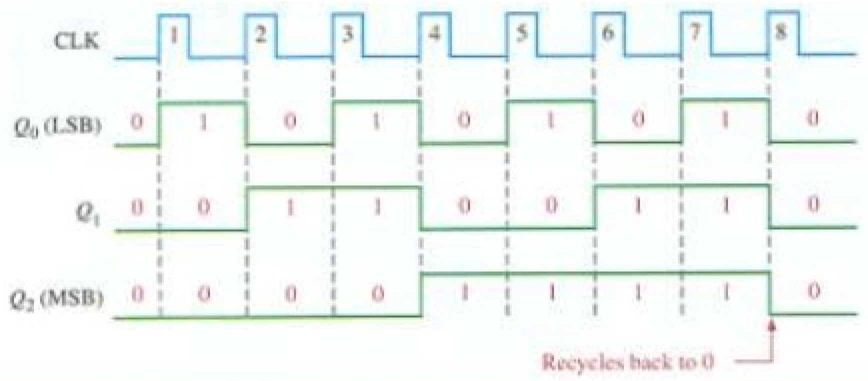
- The counter is in up sequence (Q_1 is MSB, Q_0 is LSB)
- Count from 0 to 3 in binary sequence
- The term ‘recycle’ refers to the transition from final state to original state
- Therefore, 2-bit asynchronous counter has four state and consists of two FF

A 3-bit Asynchronous Binary Counter

- Draw 3-bit asynchronous up counter using J-K FFs

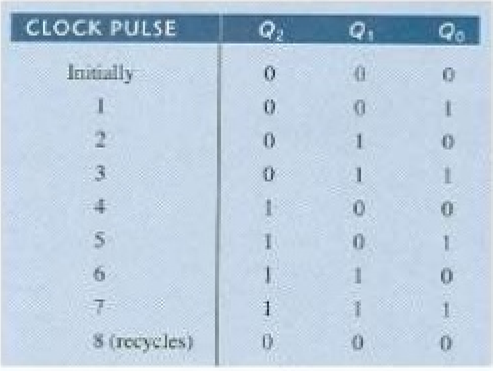


- Sketch the timing diagram for 3-bit asynchronous up counter



A 3-bit Asynchronous Binary Counter (continue..)

- Tabulate the state sequence for 3-bit asynchronous up counter



CLOCK PULSE	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

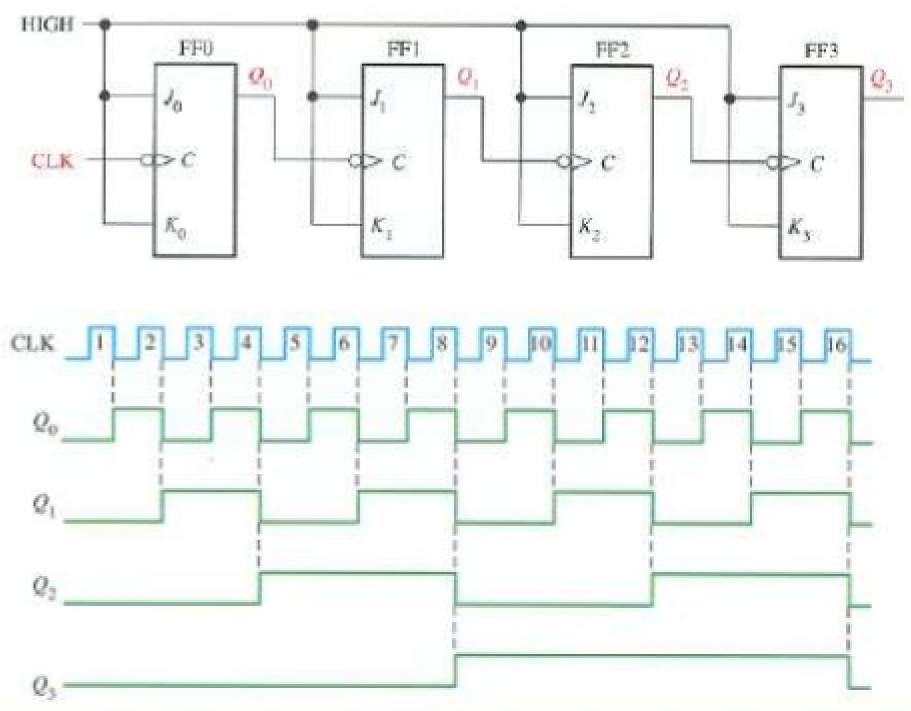
- Conclusion, 3-bit asynchronous up counter consists of three J-K FFs and counts from 0 to 7 (8 states)

Disadvantages of asynchronous counter (continue)

- Asynchronous counters are not useful at very high frequencies, especially for counters with large number of bits.
- Another problem caused by propagation delays in asynchronous counters occurs when we try to electronically detect (decode) the counter’s output states.

Exercise: A 4-bit Asynchronous Binary Counter

☞ Draw the timing diagram for 4-bit asynchronous up counter given below

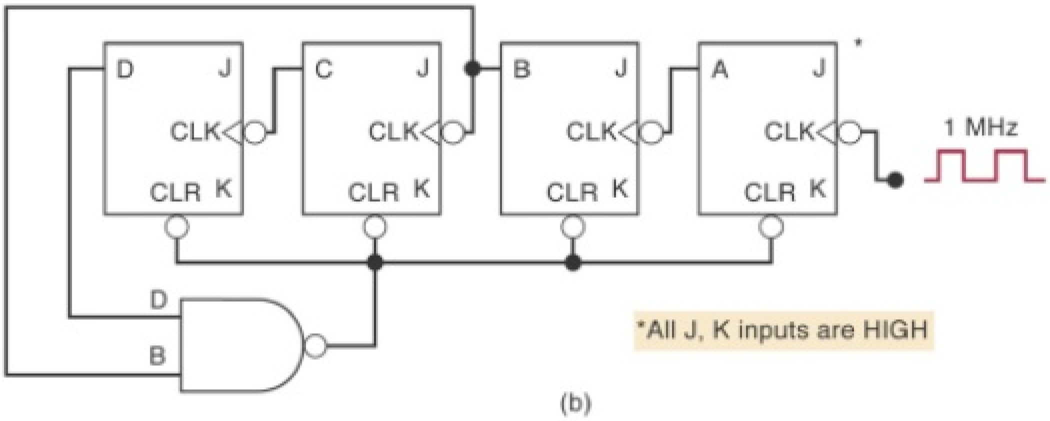


Asynchronous MOD counter

- MOD number is generally equal to the number of states that the counter goes through in each complete cycle before it recycles back to its starting state.
- MOD number can be increased simply by adding more FFs to counter. MOD number = 2^N

Changing the MOD number

Construct a MOD-10 counter that will count from 0000 through 1001.

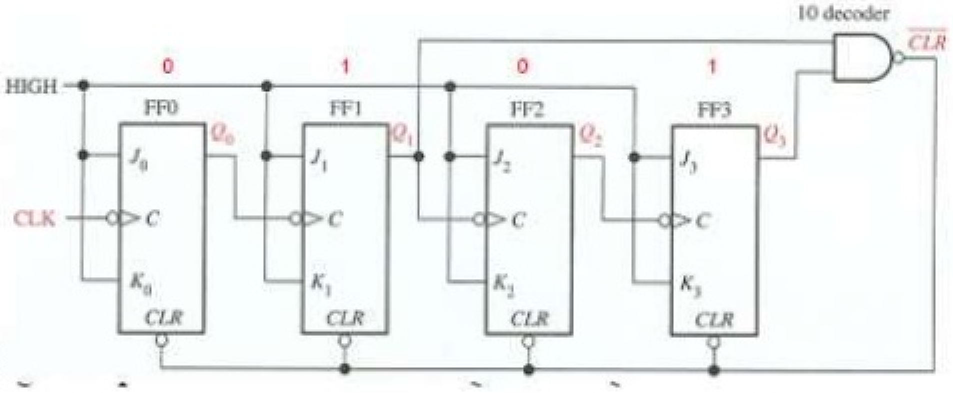


*All J, K inputs are HIGH

(b)

Asynchronous Decade Counter

- Counters can be designed to have a number of states in their sequence that is less than the maximum of 2N. This type of sequence is called a **truncated sequence.**
- For example, asynchronous modulus ten (MOD-10) counter or decade counter



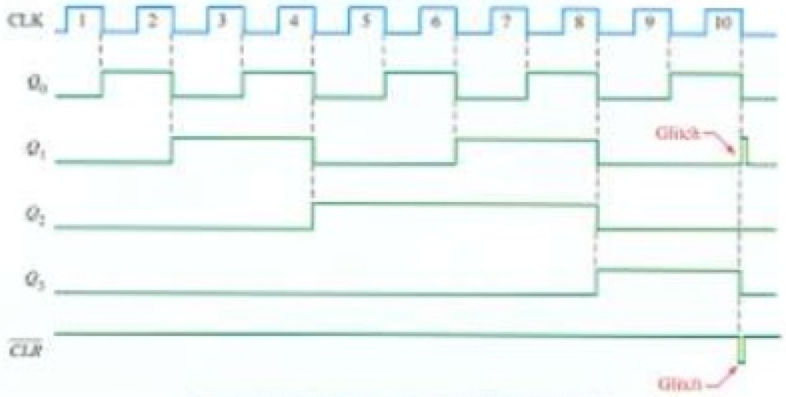
- NANI

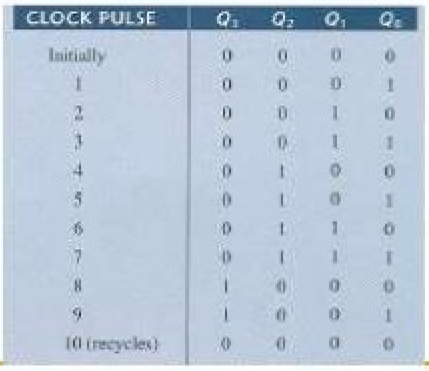
☑—Note that 10 is 1010 which is Q_3 AND Q_1 are HIGH

- CLR is produced and then reset all FFs to recycle
- The counter count again

Asynchronous Decade Counter (continue..)

- Timing diagram and binary state sequence for decade counter

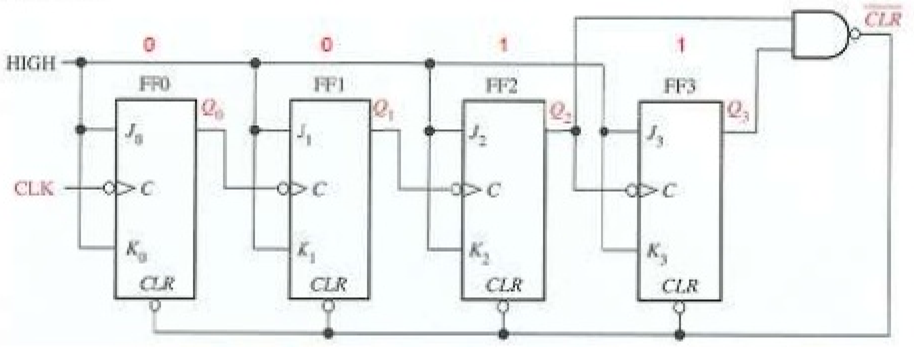


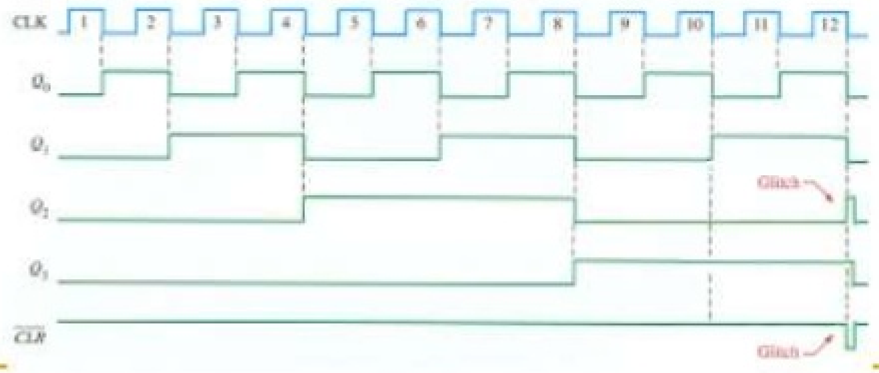


CLOCK PULSE	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

Asynchronous Decade Counter Exercise

- Modify MOD-10 asynchronous counter to have MOD-12 and draw the timing diagram (1100)



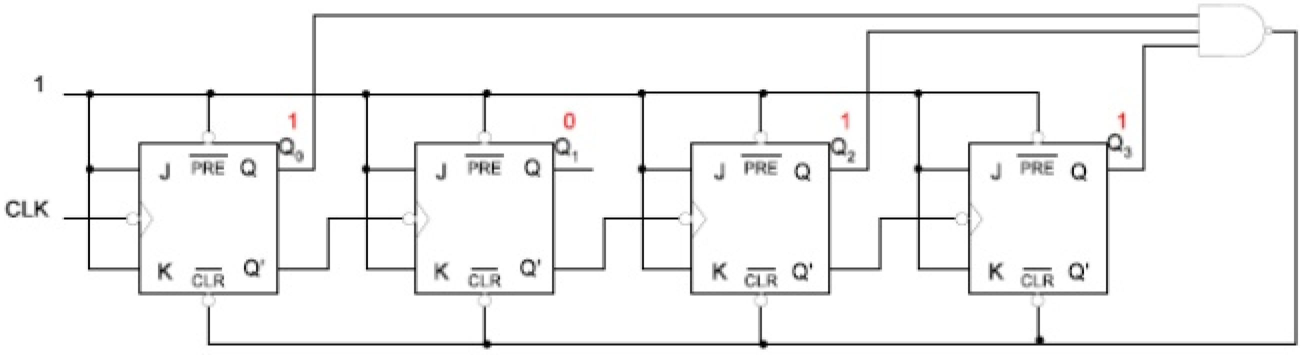


Exercise (continue)

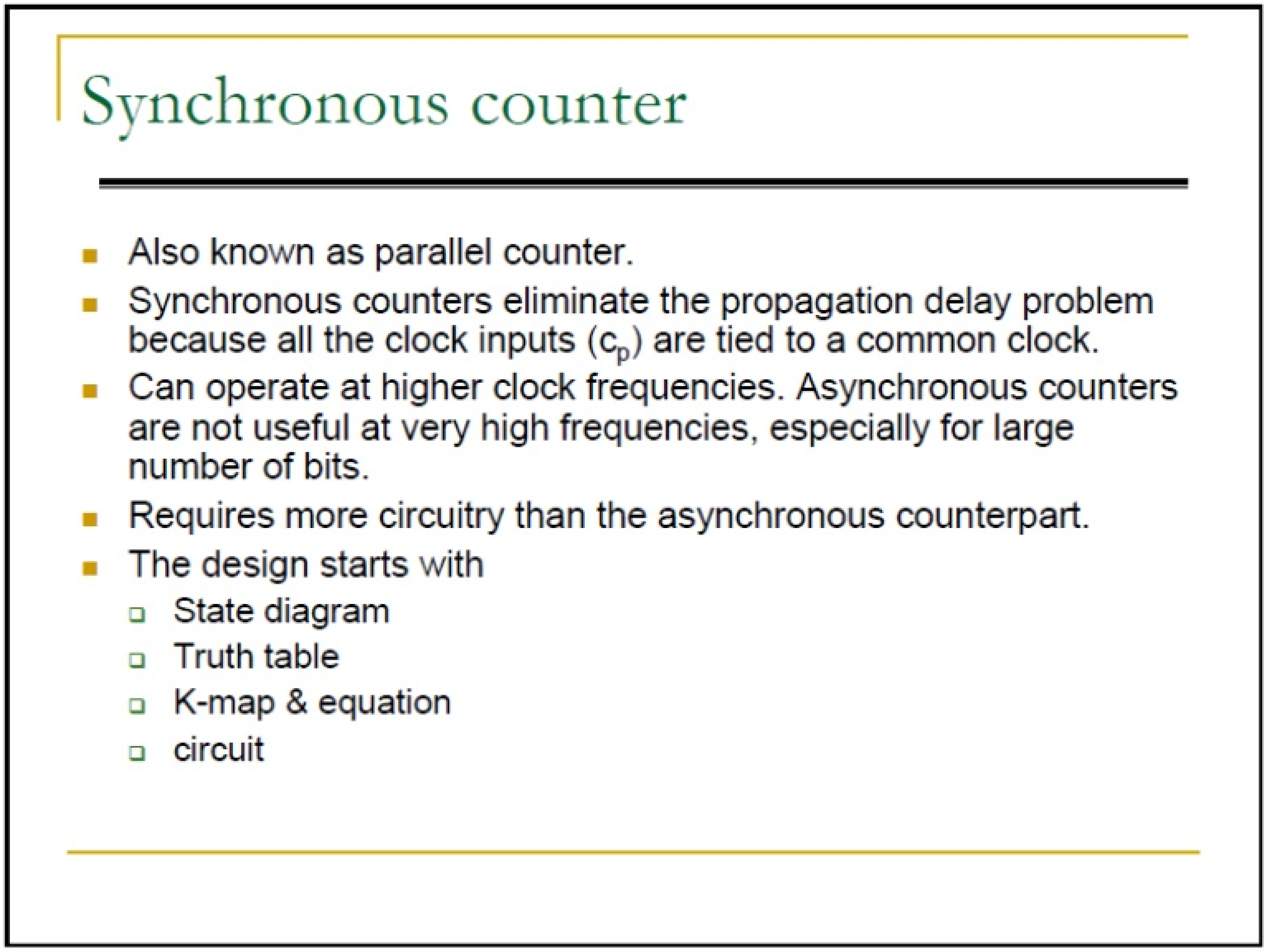
2. Draw the circuit for asynchronous counter according to these attributes:

- MOD 13 counter using JK flip-flops.
- Negative edge triggered
- Down counter
- Active low preset and clear input

Answer:

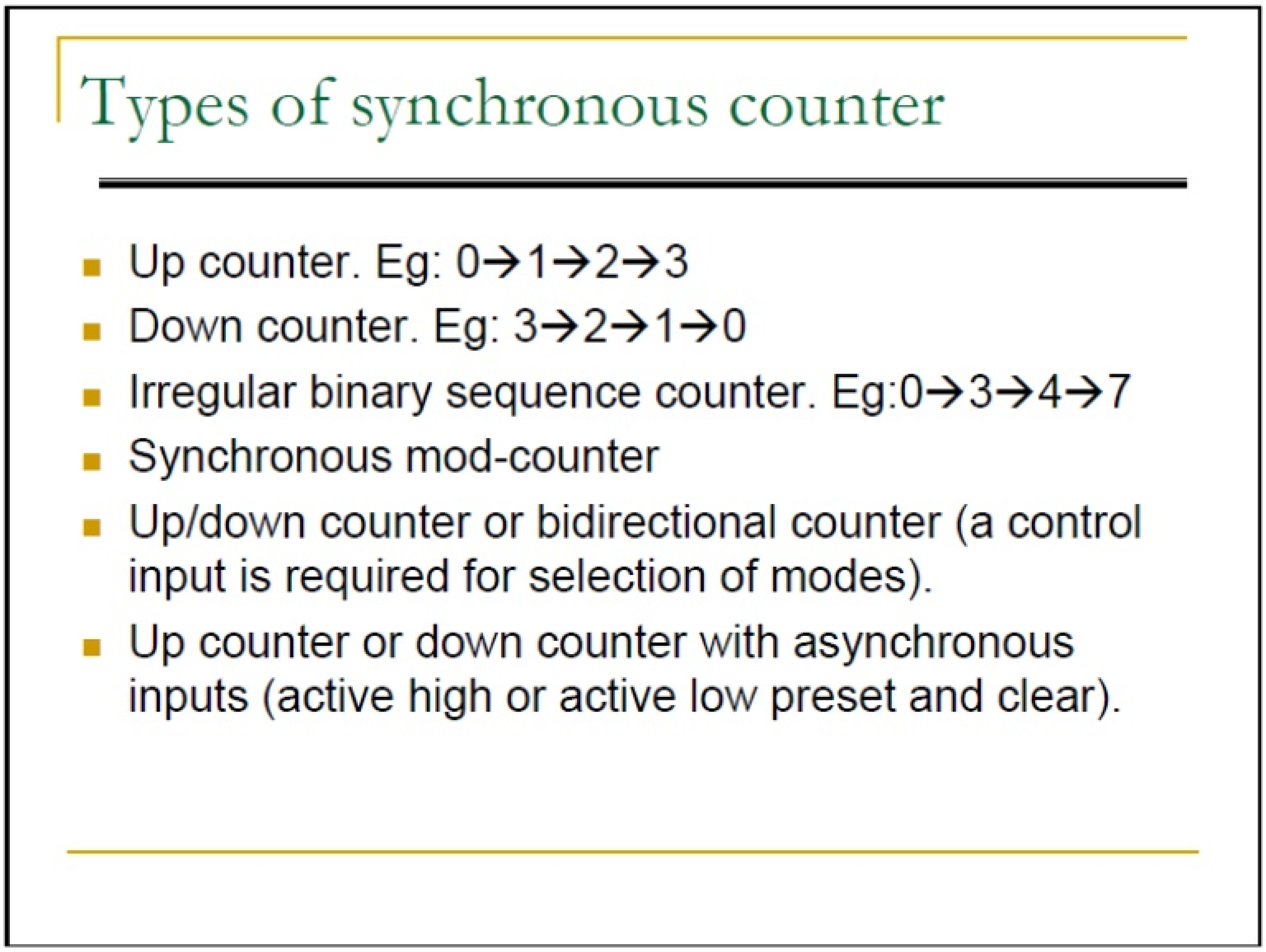


Synchronous counter



Synchronous counter

- Also known as parallel counter.
- Synchronous counters eliminate the propagation delay problem because all the clock inputs (c_p) are tied to a common clock.
- Can operate at higher clock frequencies. Asynchronous counters are not useful at very high frequencies, especially for large number of bits.
- Requires more circuitry than the asynchronous counterpart.
- The design starts with
  - State diagram
  - Truth table
  - K-map & equation
  - circuit



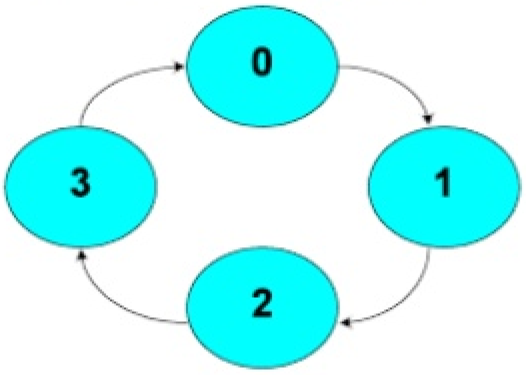
Types of synchronous counter

- Up counter. Eg: 0→1→2→3
- Down counter. Eg: 3→2→1→0
- Irregular binary sequence counter. Eg:0→3→4→7
- Synchronous mod-counter
- Up/down counter or bidirectional counter (a control input is required for selection of modes).
- Up counter or down counter with asynchronous inputs (active high or active low preset and clear).

Design step for synchronous up counter

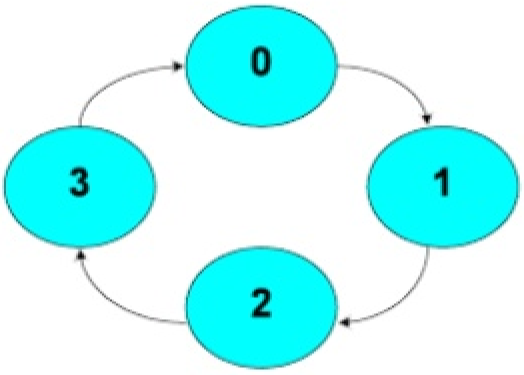
Example: Design a 2 bit counter using D, T and JK flip-flop based on the sequence 0→1→2→3.

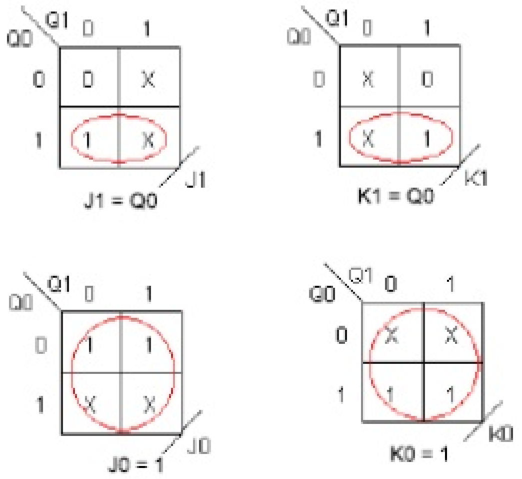
Step 1: Draw the state diagram



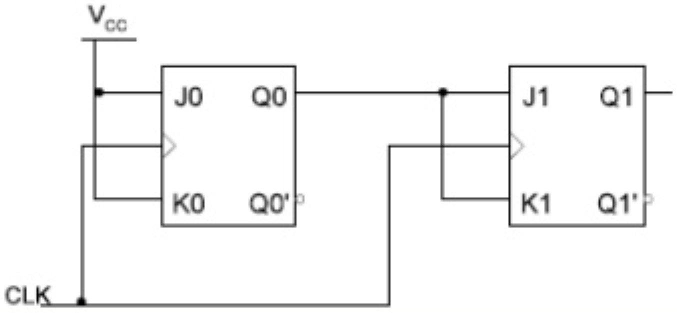
Up counter using JK flip-flop

- Using JK flip-flop



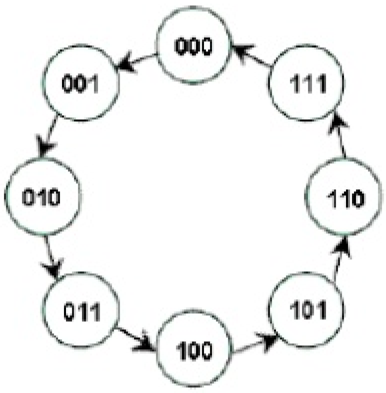


Present state		Next state		Flip-flop inputs			
Q1	Q0	Q1	Q0	J1	K1	J0	K0
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1



Design of Synchronous Counter Exercise 1

- Design a counter to produce 3-bit binary counter using J-K FF
  - ☑ State diagram
  - ☑ State and excitation tables



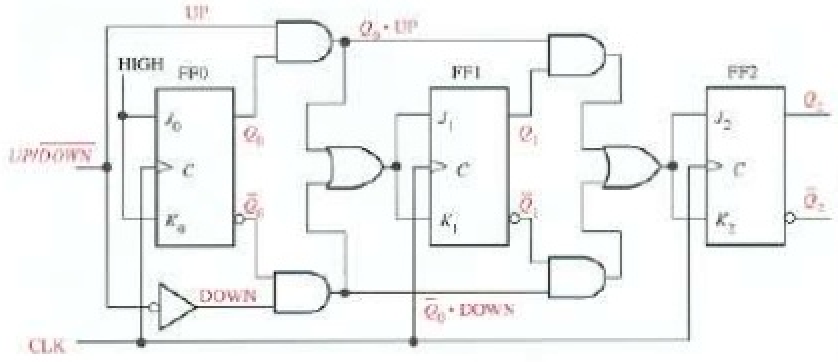
PRESENT STATE			NEXT STATE			FLIP-FLOP INPUTS		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2 K_2	J_1 K_1	J_0 K_0
0	0	0	0	0	1	0 X	0 X	1 X
0	0	1	0	1	0	0 X	1 X	X 1
0	1	0	0	1	1	0 X	X 0	1 X
0	1	1	1	0	0	1 X	X 1	X 1
1	0	0	1	0	1	X 0	0 X	1 X
1	0	1	1	1	0	X 0	1 X	X 1
1	1	0	1	1	1	X 0	X 0	1 X
1	1	1	0	0	0	X 1	X 1	X 1

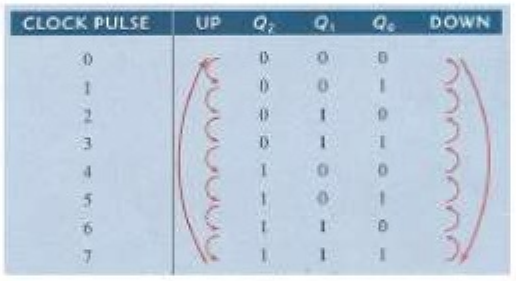
Topic:

- Up/down counter or bidirectional counter
- Cascaded counter
  - Asynchronous cascaded counter
  - Synchronous cascaded counter
- Counter decoding
  - Decoding glitches
  - Strobing technique

Up/Down Synchronous Counter (bidirectional counter)

- Bidirectional counters, also referred to as UP/DOWN counters, are capable of progressing in either direction through any given count sequence. Recall that in general, bidirectional counters can be reversed at any point in their count sequence.
- Capable to count in either direction through a certain sequence
- For example 3-bit up/down synchronous counter
  ☑ Able to count from 0 to 7 or 7 to 0





CLOCK PULSE	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

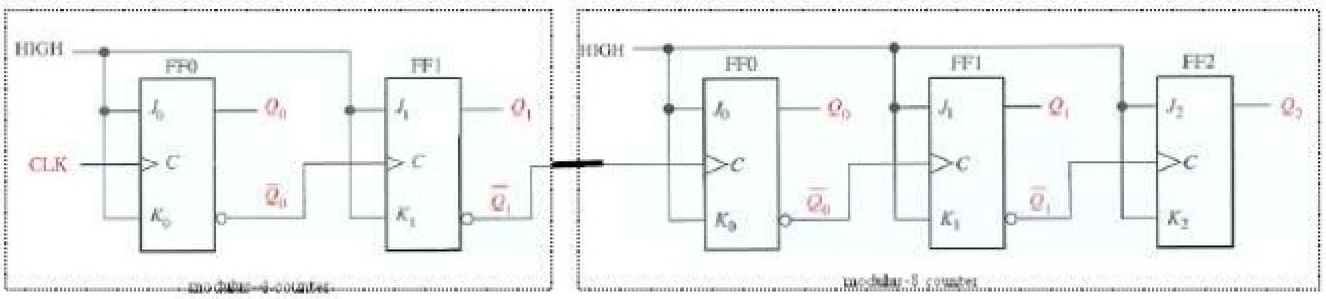
Cascaded Counters

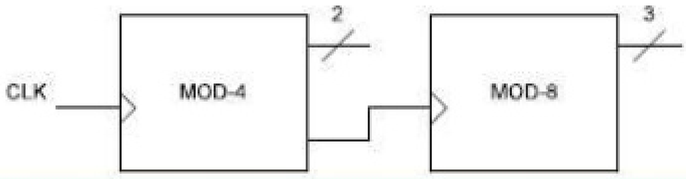
- Counters can be connected to achieve higher modulus operation.
- Cascading means that the last stage output of one counter drives the input of the next counter.
- A **mod-M** and a **mod-N** counter in cascade give a **mod-MN** counter.
- 2 types of cascading: **Asynchronous cascading** and **synchronous cascading**

Cascaded Counters (continue)

Asynchronous cascading

Two asynchronous counters connected in cascade for a 2 bit and a 3 bit ripple counter. The overall modulus of the two cascaded counters is 4 x 8 = 32; that is they act as a divide-by-32 counter.





Decade Counters/BCD counters

- Decade counter
  - Any counter has 10 distinct states, no matter what the sequence.
- BCD counter
  - A decade counter counts in sequence from 0000 (zero) through 1001(decimal 9).