Bangabandhu Sheikh Mujibur Rahman Science and Technology University, Gopalganj
Department of computer Science & Engineering
2nd Year 1st Semester B.Sc. Engg. Examination-2014
Course: CSE210 (Digital Logic Design)

Full Marks: 70 Times: 4 Hours

N.B.:
i. Answer **SIX** questions, taking any **THREE** from each section
ii. All questions are all of equal values
iii. Use **separate answer script** for each section

Section- A

			Marks
1.	a)	What is a flip-flop?	2
	b)	Describe the operation of clocked J-K flip-flop with circuit diagram.	5
	c)	Describe the characteristics of flip-flop.	$4\frac{2}{3}$
2.	a)	What is a multiplexer?	2
	b)	Draw the circuit diagram and show the truth table of 16 inputs multiplexer.	6
	c)	What are the some major applications of multiplexer?	2
	d)	Show how the 74LS138 decoder can be used as 1-8 line demultiplexer.	$1\frac{2}{3}$
3.	a)	What is a ripple counter? Why asynchronous counter is referred to as a ripple counter?	3
	b)	Design and implement a MOD-14 asynchronous counter using J-K flip-flop.	$5\frac{2}{3}$
	c)	What are the advantages of synchronous counter over asynchronous counter?	3
4.	a)	What is a timer?	1
	b)	Draw the internal diagram of a 555 timer.	5
	c)	Explain the operation of a 555 timer as monostable multivibrator.	$5\frac{2}{3}$

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Section - B

Marks

5. a) What is the difference between level triggered and edge triggered? 3

   b) What do you mean by Schmit-trigger circuit? Where it is used? 3

   c) Does a J-K flip-flop have any ambiguous input conditions? Justify your answer. 2

   d) What is the limitation of S-R flip-flop? 2

   e) Why D latch is called a transparent latch? $1\frac{2}{3}$

6. a) What is a decoder? 2

   b) What is the function of a decoder's enable input(s)? $1\frac{2}{3}$

   c) Describe the operation of a 1- of – 8 decoder with circuit diagram. 6

   d) What is the difference between DeMUX and Decoder? 2

7. a) i) Determine fmax for the mod-16 synchronous counter, if tpd for each FF is 50 ns and tpd for each AND gate is 20 ns. 3
   ii) What must be done to convert this counter to MOD-32?
   iii) Determine fmax for the MOD-32 parallel counter.

   b) Design a synchronous counter using J-K flip-flop to count the following sequence $8\frac{2}{3}$
   $0 \rightarrow 2 \rightarrow 4 \rightarrow 5 \rightarrow 1 \rightarrow 7 \rightarrow 6$

8 a) What do you mean by step size and percentage resolution of a DAC? 3

   b) A 10- bit DAC has a step size of 10 mV. Determine the full scale output voltage and the percentage resolution. 2

   c) Briefly discuss digital- ramp AD converter. $6\frac{2}{3}$