

Digital System (Lecture + Note)

P-type Semiconductor

extrinsic type of semiconductor

when a trivalent impurity (B , Al) is added to an intrinsic or pure semiconductor (Si , Ge) it is said to be a p-type semiconductor. A p-type semiconductor has more holes than electrons.

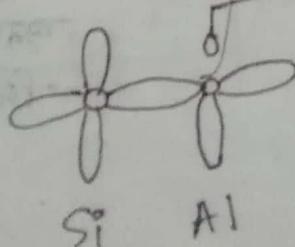
($Si+Al$)

n-type Semiconductor

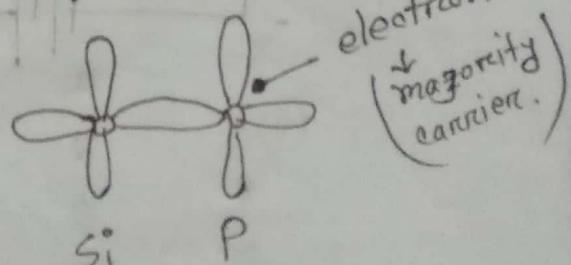
n-type semiconductor is a tetravalent semiconductor (outer most orbital has 4 electrons) doped with (P , As , Sb)

A n-type semiconductor has more electron than holes.

($Si+P$)

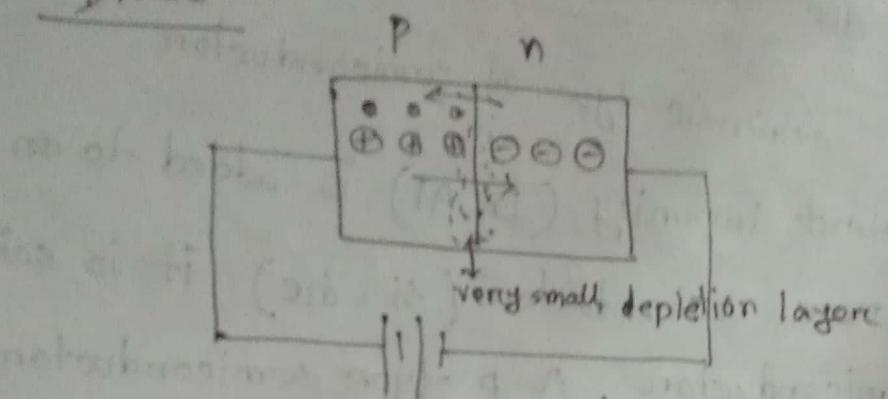


P-type



n-type

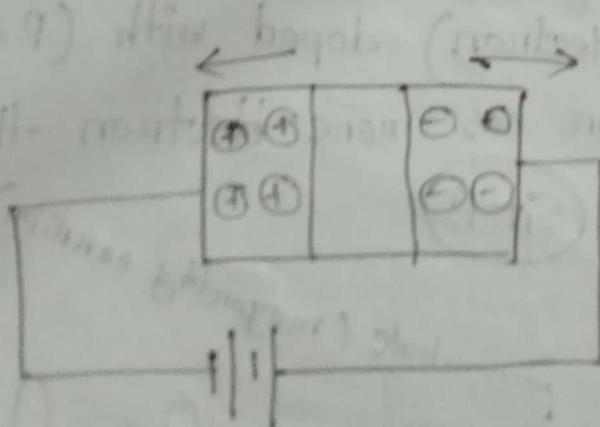
Diode



Forward Bias:

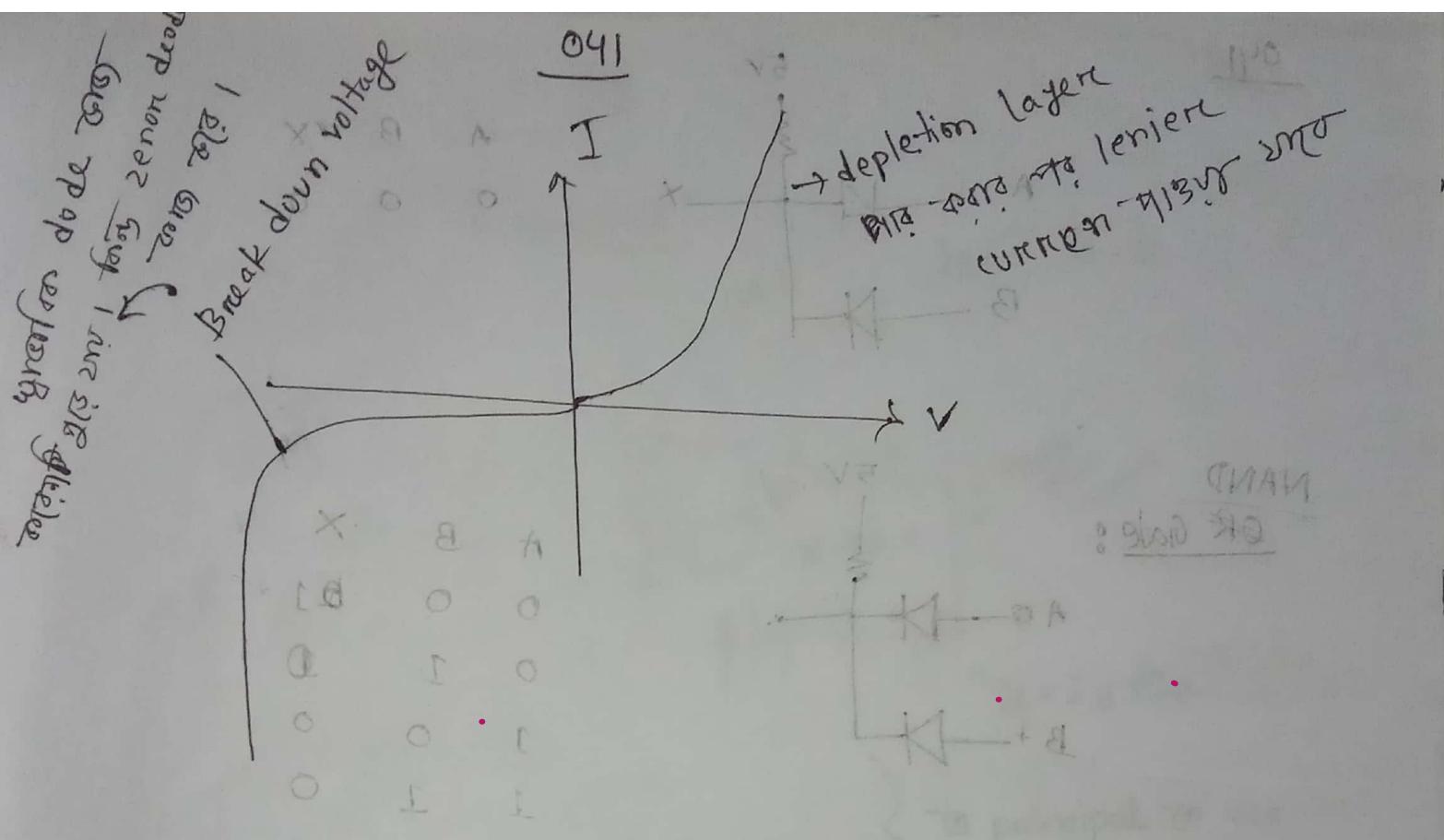
depletion layer କିମ୍ବା ରତ୍ନ
ରେ ଏ ହେଉ - ବୁଝାଯାଇଲେ,
- ଏକଥିରେ ଏକା ପୋଟିଅନ୍ତର୍ଗତ
depletion layer କିମ୍ବା ରତ୍ନ
ଅଧିକ ଆବଶ୍ୟକ ଏ ଫ୍ଲୋ - କାରଣରେ,

depletion layer - କେ ଅଭାବ - କାର୍ଯ୍ୟ (carrier energy କେବଳ ଶୁଣ
ଦେବାରେ) ଏବଂ କୁଣ୍ଡଳ ଫ୍ଲୋ କାର୍ଯ୍ୟ (short circuit) କେବଳ ଜର୍କାତ୍ କାର୍ଯ୍ୟ

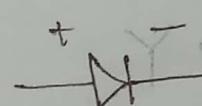


depletion layer କୁଣ୍ଡଳ
କାର୍ଯ୍ୟ କାର୍ଯ୍ୟ

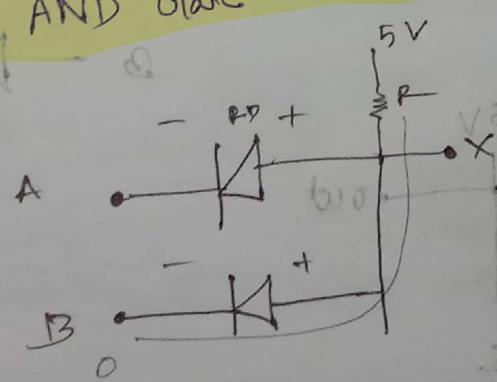
- ଅନୁଭବ ଏ ପ୍ରକାଶ କାର୍ଯ୍ୟ
- ଏବଂ ଅନେକ କୁଣ୍ଡଳ voltage
- ଦିଅି - ହେବେ ।



Symbol of diode:



Drawing AND Gate with diode:



5V (1)
0V (0)

X	5(1)
A	5
B	0
5	0
0	5
0	0

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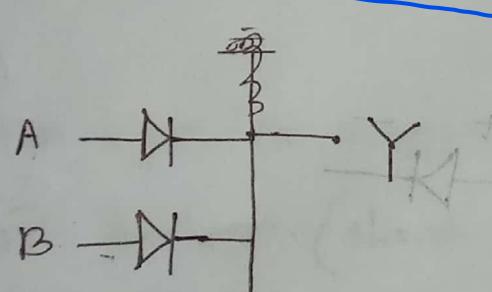
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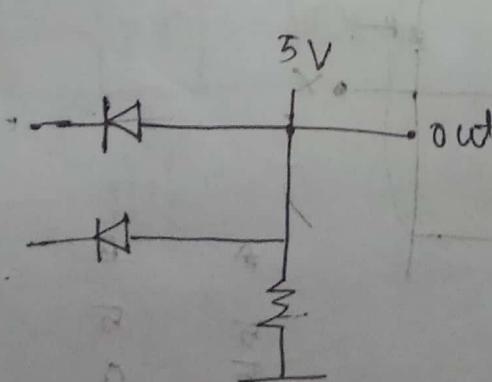
80%

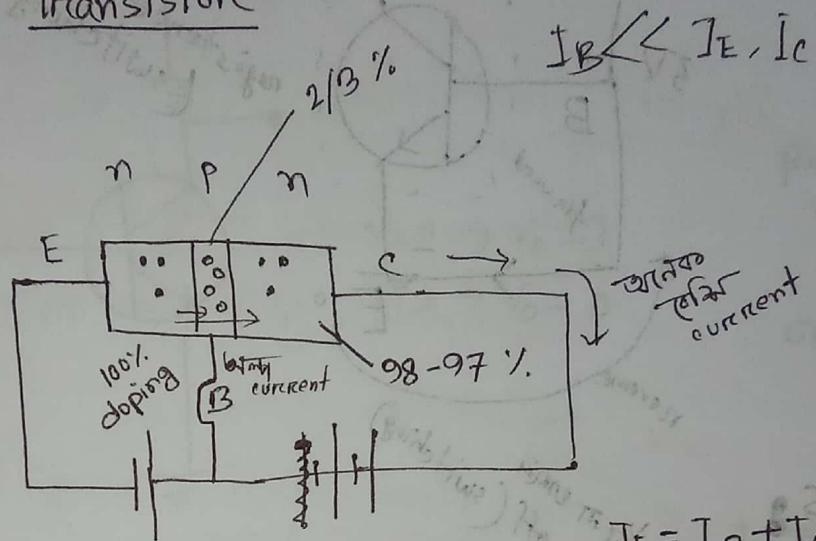
OR Gate :

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



AND :



Transistor

$$I_E = I_B + I_C$$

E, B (forward)

B, C (Reverse)

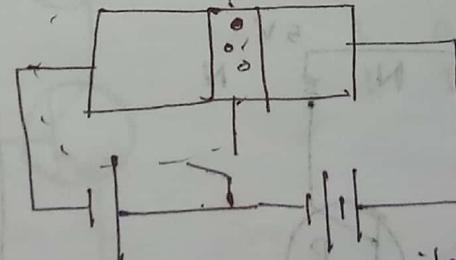
transistor

৷ ফোর্বে

বিদ্যুৎ বাতি হচ্ছে।

} **প্রাথমিক ব্যবহার**
করে - অধিক সামগ্ৰ্য
current পাওয়া হচ্ছে।
অনেক Amplifier ফেচের
কাট করে।

$$I_E \approx I_B$$



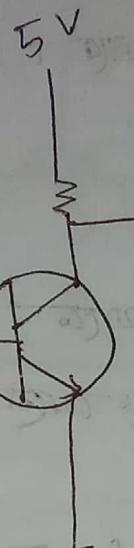
অ্যান্ড switch ফেচের কাট করে।

-এটা ID টে নিপত্তি করে IE ১০

current টে IB টে পার্য কৰা হয়।

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single-transistor logic

$$\frac{5 \times H}{H + R} \approx 5$$

$$R \ll H$$

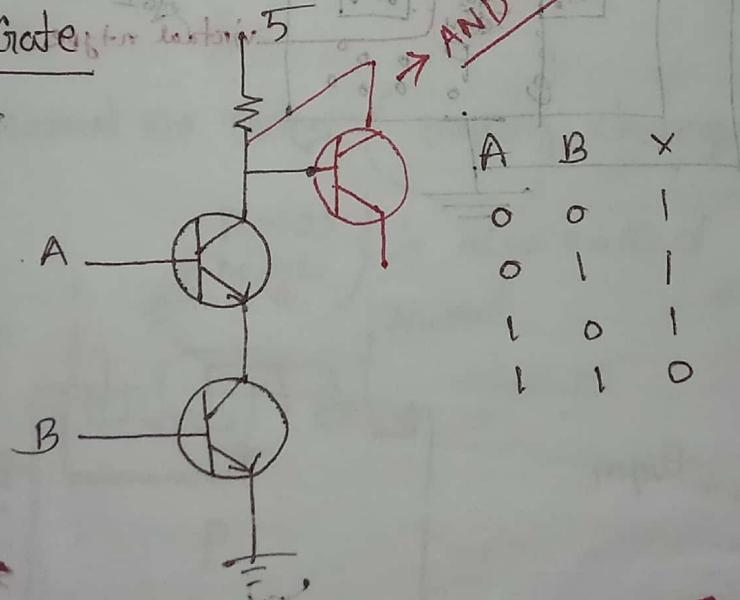
0.2 m conductor
200 m²

0.2 m

$$\frac{5 \times 0}{0 + R} = 0$$

(T 3720M)

NAND Gate



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

$$\begin{cases} 1 \rightarrow 0 \\ 0 \rightarrow 1 \end{cases}$$

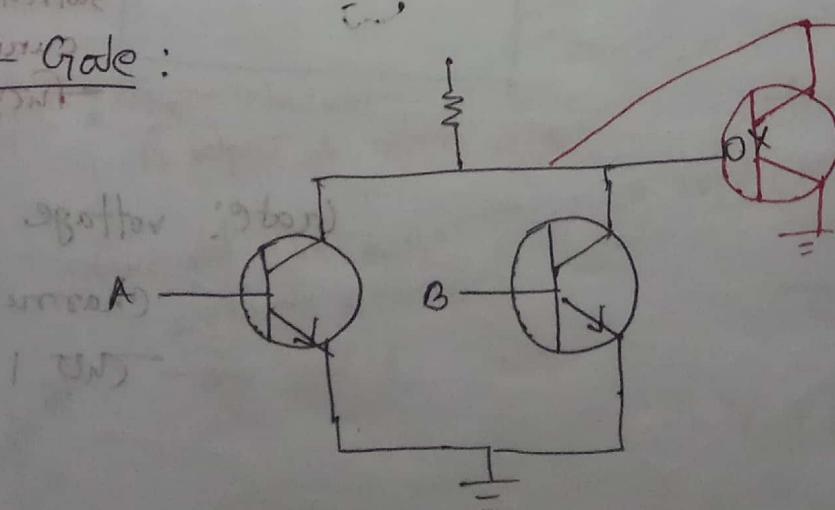
Not
20
20
20
20

no power or not true

not true then output

1 will be out

(OR Gate)



A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

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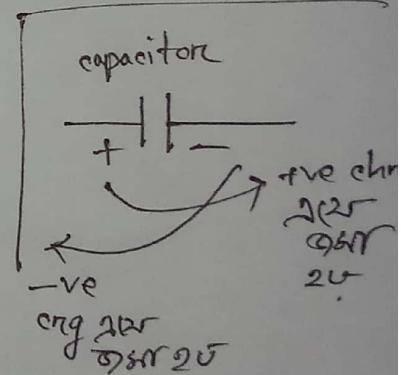
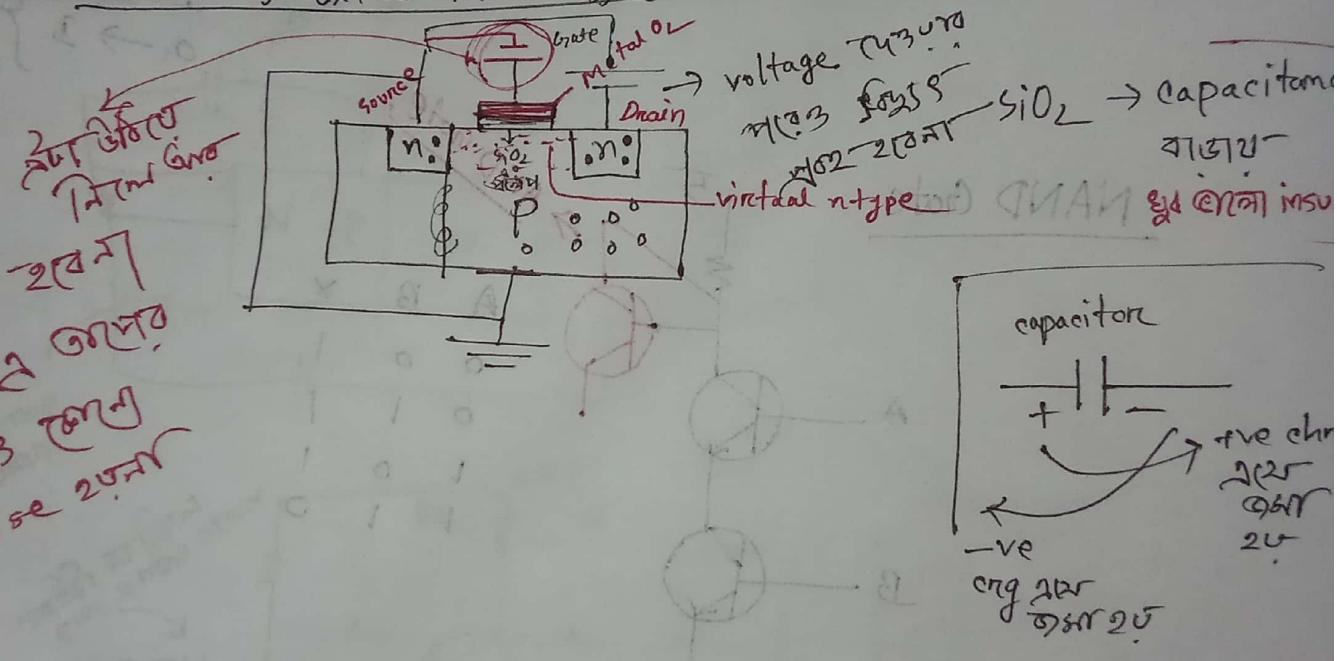
IPO

Note: NAND NOR কোর্সের মধ্যে একটি বিষয় হাতে

Bipolar Transistor

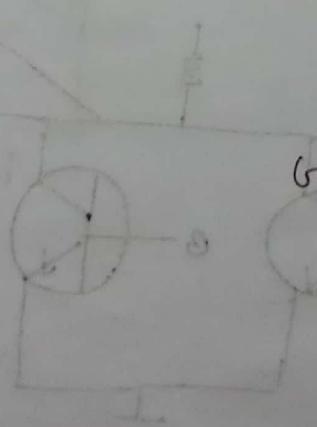
২ পথের diode এবং (majority/minority carrier) temperature এর দ্বারা আলো ছেড়ে করেন।

Metal of Oxide Field Effect Transistor (MOSFET)



(Storage)

X	0	A
+	0	0
0	-	0
0	0	1

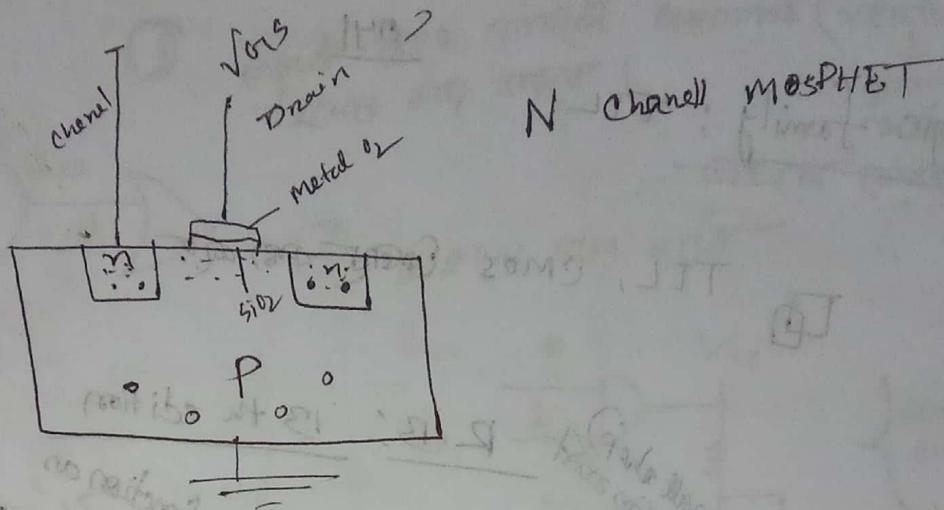


switch এর কাজ করা
current এর switch
fizik এবং

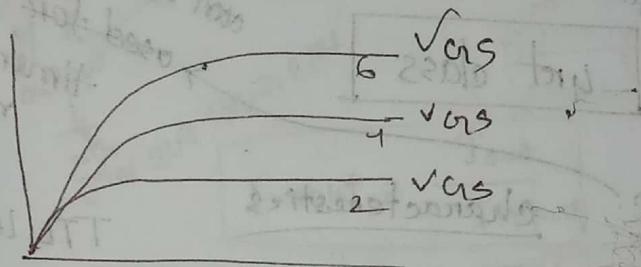
gate: voltage Apply করুন
channel (gate) খুলুন
ব্যুৎ।

14/09/2020

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N channel MOSFET



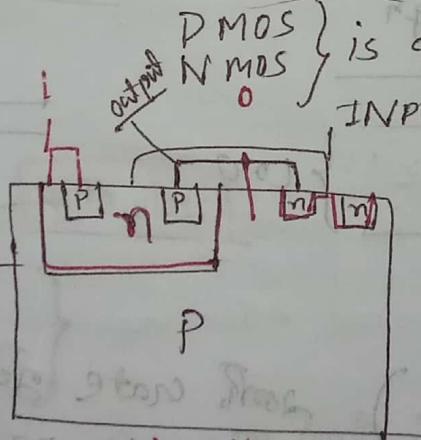
complementary
metal oxide semiconductor

P channel \Rightarrow V_{GS} (Doping change + (+ve, -ve charge))

D MOS
N MOS } is also called.

CMOS :

CMOS INVERTER



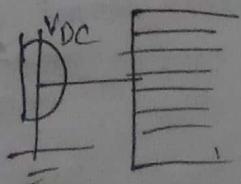
input $\geq 0 \text{ volt} \Rightarrow \text{out} = 1$

transistor-transistor logic

CMOS \Rightarrow output $\leq 0.75 \text{ volt}$
input $\geq 0.75 \text{ volt}$

current \downarrow

T-TL : - D E



Used complementary
and symmetrical
pairs of P-type and
N-type MOSFET

PMOS $(0-1.5)$ low logic state
Both $(2.5-5)$ high

Ground $\geq 2.0 \text{ volt}$
connect
 $\geq 2.0 \text{ volt}$

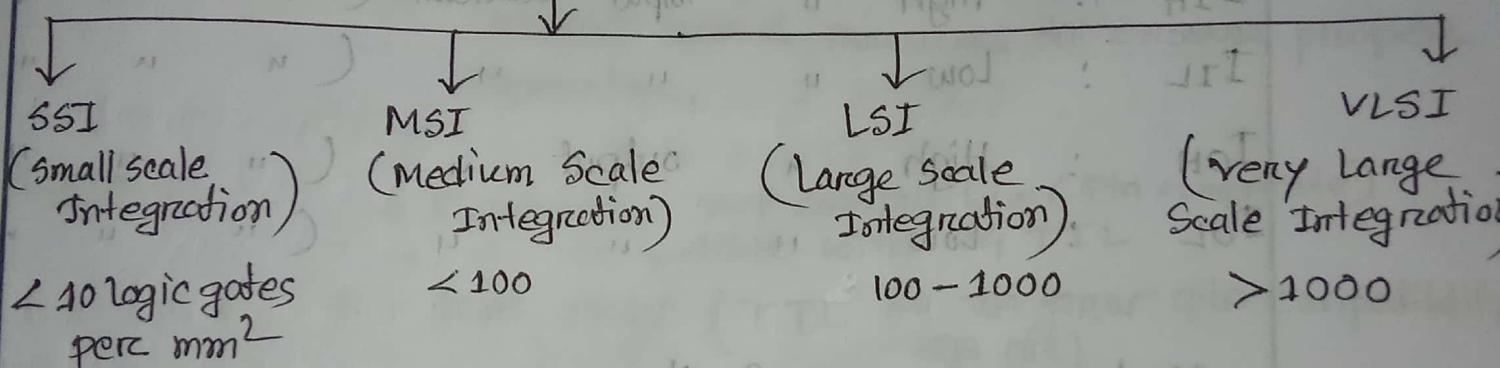
IC (Integrated Circuit)

Date :

IC consist transistorz, registerz, capacitorz, diode

An Integrated circuit (IC), sometimes called a chip, microchip or microelectronic circuit is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, diodes and transistors are fabricated.

Based on logic gates present :



Characteristics of IC :

- Fan out
- Power Dissipation
- Propagation Delay
- Noise Margin
- Fan in
- Operating temperature
- Power Supply requirements

Symbol Definition

V_{IH} : High state input voltage, (logic 1)

V_{IL} : Low state " (logic 0)

V_{OH} : High " output " (logic 1)

V_{OL} : Low " " (logic 0)

I_{IH} : High " input current (input voltage logic 1)

I_{IL} : Low " " " (input voltage logic 0)

I_{OH} : High " output " (output voltage logic 1)

I_{OL} : Low " " " (output voltage logic 0)

Most common IC families :

* TTL

* CMOS

TTL :

→ Most popular and widely used

→ operate from +5V supply

→ labeling system starting with 54 or 74

Ex: 7400, 7401, 74121

→ High → +5V, Low or Ground

7400 = standard series

74L00 = low power series (low I)

74H00 = High power series

74S00 = Schottky series

74LS00 = low power Schottky series

Date :

Some term compare between IC's

Pin compatible: Pin configuration are the same.

Functionally Equivalent: logic ^{function} perform they perform are exactly same.

Electrically compatible: can be connected directly to each other without special measures to ensure proper operation.

midrange = 7.2-1

CMOS:

C → Electrically not compatible (Pin compatible)
T → " compatible with 74 TTL

40 = pure CMOS (TTL 74 এর মাঝে pin compatibility)
গুলি (জু)

74C = 74 TTL এর মাঝে pin compatible

74HC = High speed (Electrically not compatible)

74HCT = pin compatible ~~but connection not possible.~~
and

74HCT \leftrightarrow 74

74AC = Most Advance, electrically not compatible

74ACT = " " " compatible with 74 TTL

If TTL series, power = V_{cc} (collector voltage)

CMOS " , power = V_{DD} (Drain voltage)

* V_{cc} \rightarrow Supply Voltage $\rightarrow +5V$

Not logic voltage

Supply voltage is used to run IC

where $V_{DD} = 3-18V$

Note: সার্ভিসে তে TTL এর
সময়ে গুলি কালো
+5V APPLY কর
-22,

* Ground pin uses

$$\text{Logic } 0 \rightarrow (\text{For TTL}) = 0 - 2V$$

Transistor used 25, or depletion layer logic 25 voltage নামে, 0 থেকে 25 পরিমাণ voltage স্বতন্ত্র logic = 0

5i,

$0 - 0.8 = 0$	logic
$2 - 5 = 1$	"

$0.8 - 2$ শত TTL ckts generally ফিল্ড 0 or 1 25
 \rightarrow Uncertain

For CMOS : প্রযুক্তির কাজের ফল

$$\text{logic } 0 = 0 - 1.5$$

$$\text{logic } 1 = 3.5 - 5$$

1 - 3.5 = Uncertain

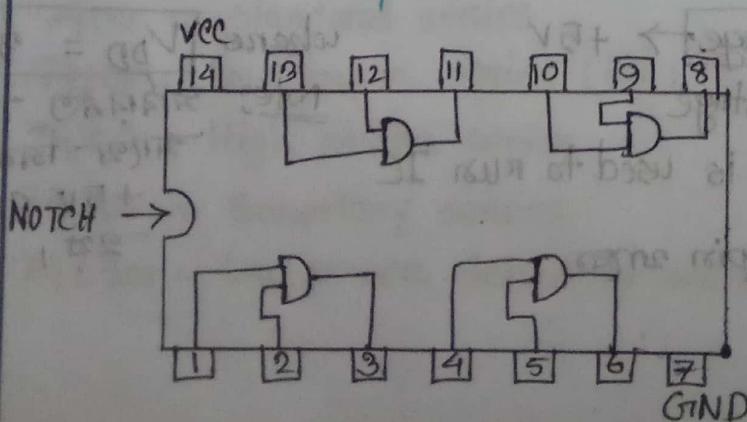
Note: কোনো IC এর input -এ কোনো কিছুই না দেও জান
 0 বা 1 যেকোথেকে floating এর uncertain
 unconnected input. TTL PF = 0PF

→ situation (f) logic high = 5H PF

→ TTL or logic 1 → CMOS or floating input
 বরবর
 PF ↔ TSHPF
 IC -এ অতি হো।

IC Datasheet:

(i) SN 74LS08 → IC PF কি কাজ করে (Quad 2-input AND gate)
 company name TTL Scattky
 Low power consumption

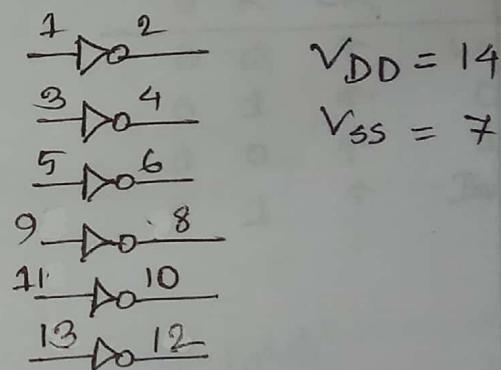
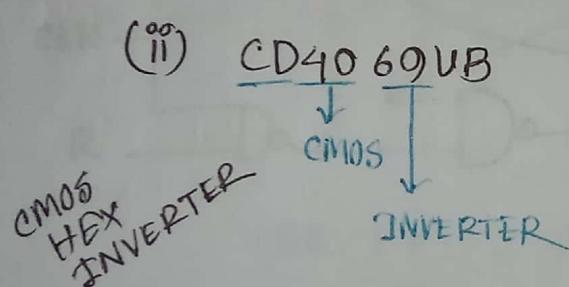


Guaranteed operating ranges

	Min	TYP	Max
Vcc	4.75	5	5.25 V
TA	-25	25	75 °C
I _{OH}	-	-0.4 mA	
I _{OL}	-	8.0 mA	

Date :

	<u>Typ</u>	<u>Max</u>
V_{IH}	$\frac{M_{IO}}{2} V$	
V_{IL}		$0.8 V$
V_{OH}	$2.4 V$	$3.5 V$
V_{OL}		$0.25 - 0.35$ $0.4 - 0.5$
I_{IH}		$0.1 \text{ mA} - 20 \text{ mA}$
I_{IL}		-0.4



• Sequen~~tial~~ Synchronous sequential circuits that use clock pulse in the inputs of memory elements are called clocked sequential circuits.

The memory elements used in clocked sequential circuits are called flip-flops.

A flip-flop circuit can maintain a binary state indefinitely until directed by an input signal to switch states.

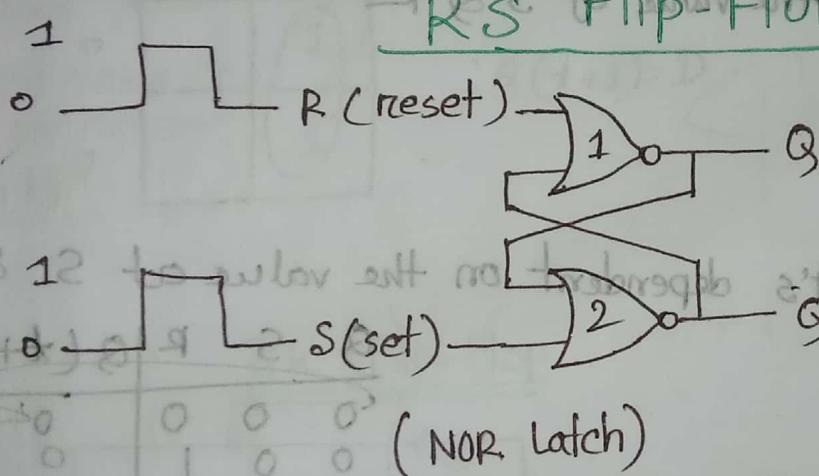
The major differences among various types of flip-flops are in the number of inputs they possess in the manner in which the inputs affect the binary state.

স্থায়ী: একটি অবস্থা স্থায়ী এবং অন্য অবস্থা নিষ্কৃত-গ্রহণ গ্রহণ করে অবস্থার পরিস্থিতিক পরিবর্তনকারী মাল্টিপ্লিকেশনের বলা হয়। তাই জার্জ প্রাদী মাল্টিপ্লিকেশনে ফিপ-প্রস্তাৱ বলা হচ্ছে। ফিপ-প্রস্তাৱ একটি বিনারি এক বিনারি ডিজিটের বর্তনী বা একটি বাইনারি বিট (0 অথবা 1) অঙ্গকৰণ কৰাতে পারে।

ফিপ-প্রস্তাৱের ইনপুটে কোনো কেজি দিলে আউটপুটে তা অনিদিষ্টভাবে অঙ্গকৰণ আকুন। ফিপ-প্রস্তাৱ বন্ধন কৰা হলে এ প্রিসাপ প্ৰদান কৰা কৰা থলে ইনপুটের কেজি কৰিয়ে নিলেও আউটপুট প্ৰদান কৰিবিবিত্ত-থাকে। প্ৰতিটি ফিপ-প্রস্তাৱ 2P output এবং একটি একাধিক input থাকে। output একটি অক্টি (ON) অথবা LOW (OFF) অবস্থা-থাকে।

- Each Flip-Flop has two outputs, Q and Q' , and two inputs, set and reset.
- The cross coupled connection from output of one gate to the input of other gate constitutes a feedback path. So this circuit is an asynchronous circuit.
- This type of flip-flop sometimes called direct-coupled RS flip-flop or SR latch.

RS Flip-Flop



S	R	Q	\bar{Q}
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

indeterminant

(After $S=1$, $R=0$)
(After $S=0$, $R=1$)

Nor gate ഏ പോതുമെന്നോളെ എൻഡ് ഇപ്പ് ഇപ്പ് സീറ്റ് അല്ലെങ്കിൽ 1 വരുമ്പോൾ ഓട്ടു ദാഖല് ചെയ്യാം

Note
ഘട്ടന

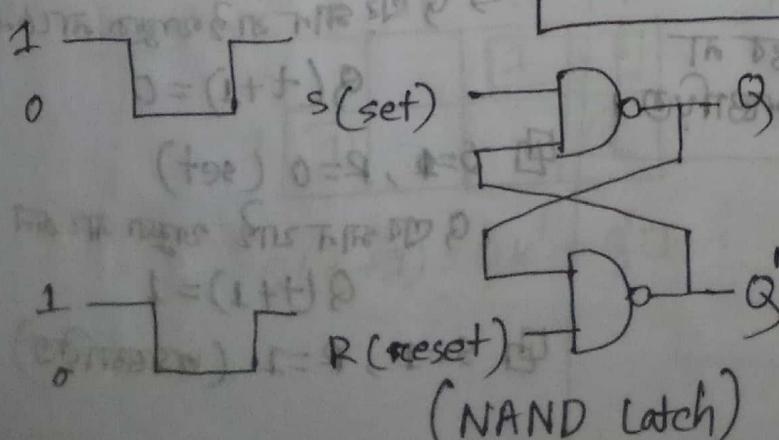
$S=0, R=0$ (no change; previous state same)

$S=0, R=1$ (Reset), $Q(t+1) = 0$

$S=1, R=0$ (set), $Q(t+1) = 1$

$S=1, R=1$ is indeterminant because

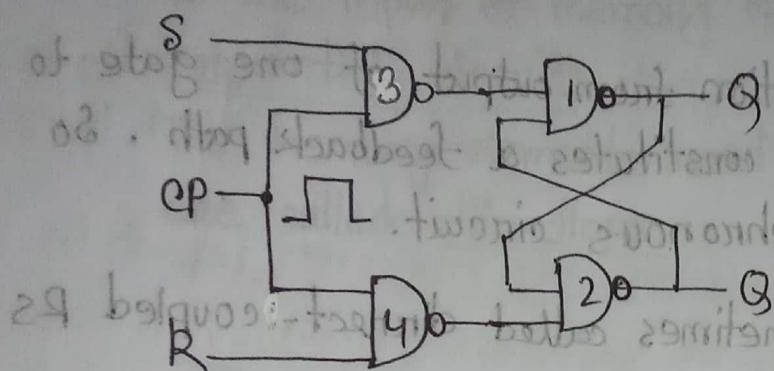
$Q = Q'$ is not possible.



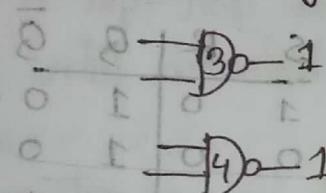
S	R	Q	\bar{Q}
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

indeterminant

Output of clocked RS flip-flop



If $CP = 0$ ignored the value of S & R



If $CP = 1$, then it's dependent on the value of S & R

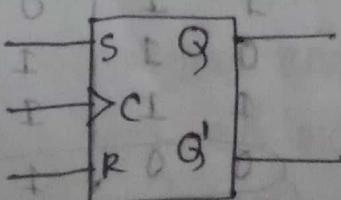
		Q	SR	Q(t)	Q(t+1)
		00	01	11	10
S	R	0		X	1
		1	1	X	1

Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	1
0	1	0	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

$$Q(t+1) = S + QR'$$

Note: $SR = 0$ (always)

$SR = 1$ when $S = 1$, $R = 1$ असत्ता न होने के लिए यह जरूरी है।



block diagram

Note

• $S = 0, R = 0$ (No change) $Q(t+1) = Q(t)$

• $S = 0, R = 1$ (Reset)

• Q एवं जान या उपकृत नहीं करें

$$Q(t+1) = 0$$

• $S = 1, R = 0$ (Set)

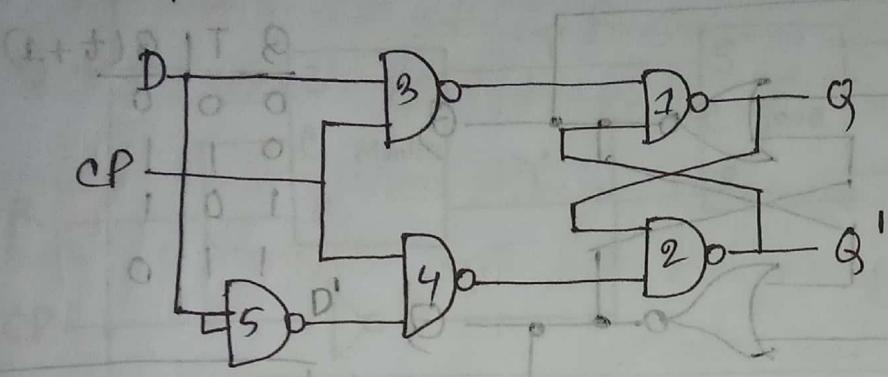
• Q एवं जान या उपकृत नहीं करें

$$Q(t+1) = 1$$

• $(S = 1), R = 1$ (असत्ता न होने के लिए यह जरूरी है।)

D Flip-Flop

1st input $\rightarrow D$

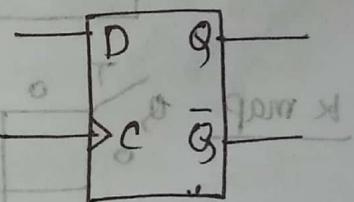
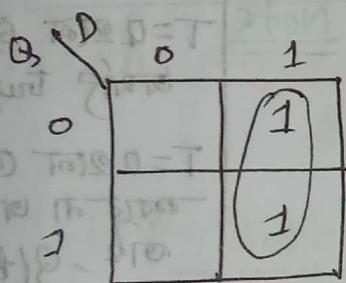


Note:

$D=0$ (reset) $\rightarrow Q(t+1)=0$
 $D=1$ (set) $\rightarrow " = 1$

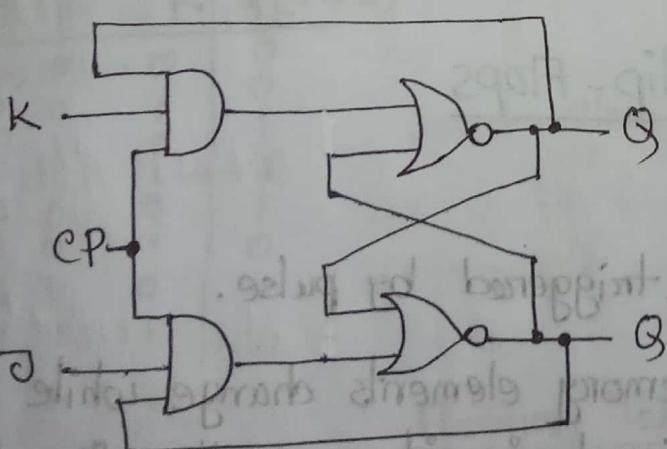
Q	D	$Q(t+1)$
0	0	0
0	1	1
1	0	0
1	1	1

$$\therefore Q(t+1) = D$$



Block Diagram

JK Flip-Flop



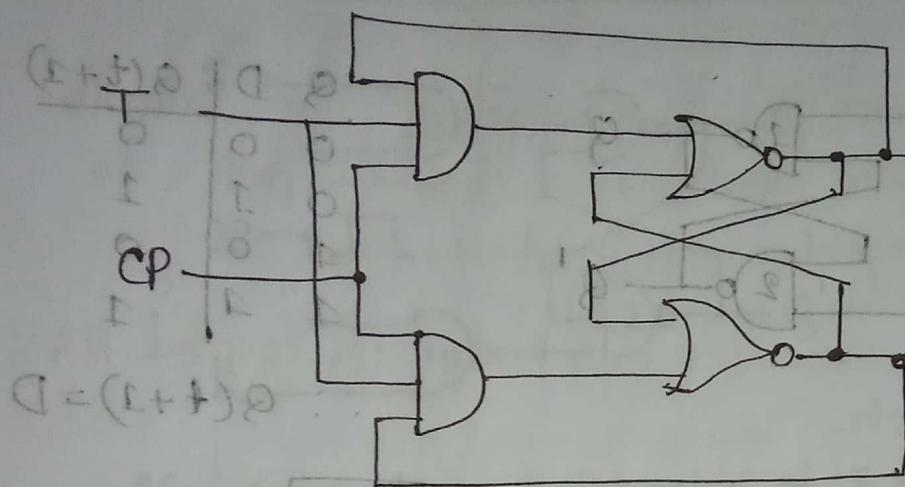
J	K	00	01	11	10
0	0	0	0	1	1
1	0	1	1	1	0

$$\therefore Q(t+1) = QK' + Q'J$$

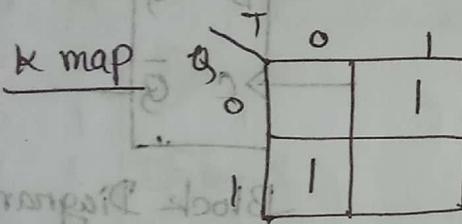
Note

- $J=0, K=0, Q(t+1)=Q$
- $J=0, K=1, Q(t+1)=0$ (reset)
- $J=1, K=0, Q(t+1)=1$ (set)
- $J=1, K=1, Q(t+1)=Q'$

Flip Flop



Q	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0



Note

$T = 1$ तें $Q(t+1) = Q$
बाँधे त्रिकोण ($Q(t)$) आए

$T = 0$ तें बोना त्रिकोण
बाँधे ना अस्ति तो आए
 $Q^2 - Q(t+1) = Q$

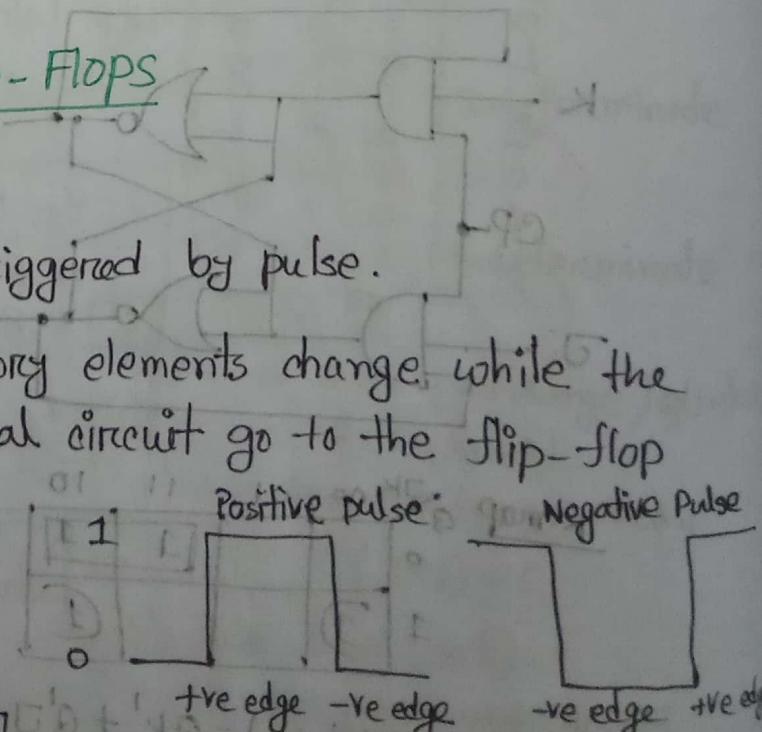
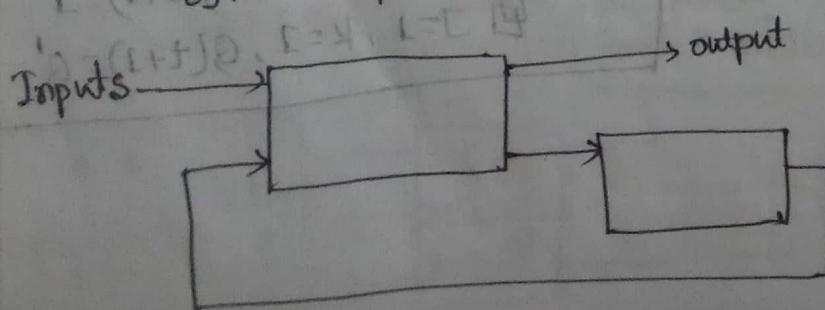
$$Q(t+1) = TQ' + \bar{T}Q$$

Triggering of Flip-Flops

(action)
कार्यक्रम

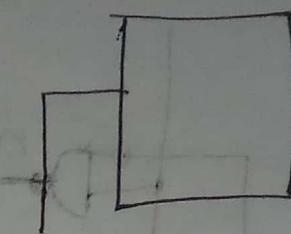
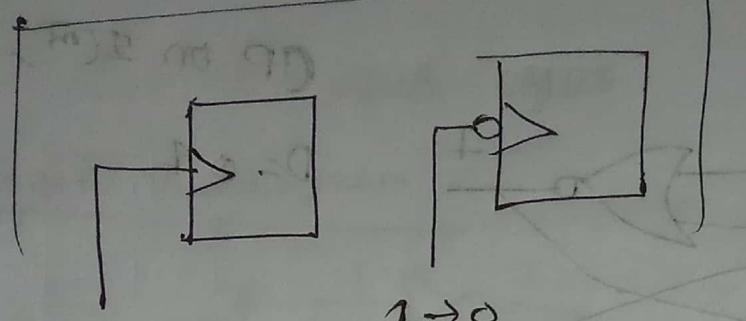
■ Clocked flip flops are triggered by pulse.

■ (clock). The outputs of memory elements change while the outputs of combinatorial circuit go to the flip-flop after a pulse transition.



Triggering
Method

edge Trigger



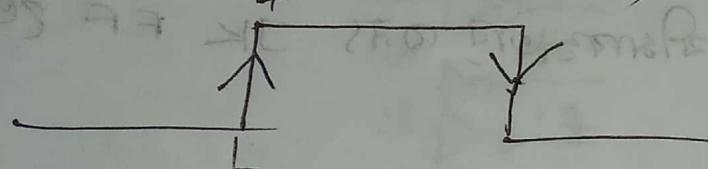
Level Triggering

$0 \rightarrow 1$

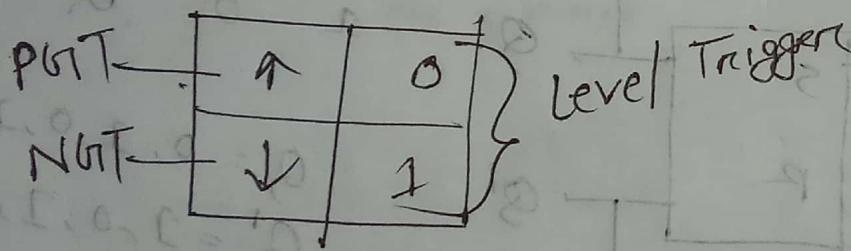
$1 \rightarrow 0$

NGT

PGT (Positive going Trigger)



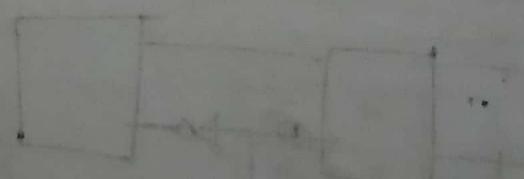
{ when the signal goes
to low to high or
high to low there
will be changed



Next: FF Register, memory Design.

latch
involve level edge

FF
PGT / NGT



Flip-Flop Excitation Table

- During the design process, we usually know the transition from present state to next state and wish to find the input conditions that will cause the required transition.
- For this reason, we need a table called an excitation table, lists the required inputs for a given change of state.

<u>(a) RS :</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>S</u>	<u>R</u>
0	0	0	X	
0	1	0		
1	0	1		
1	X	0		

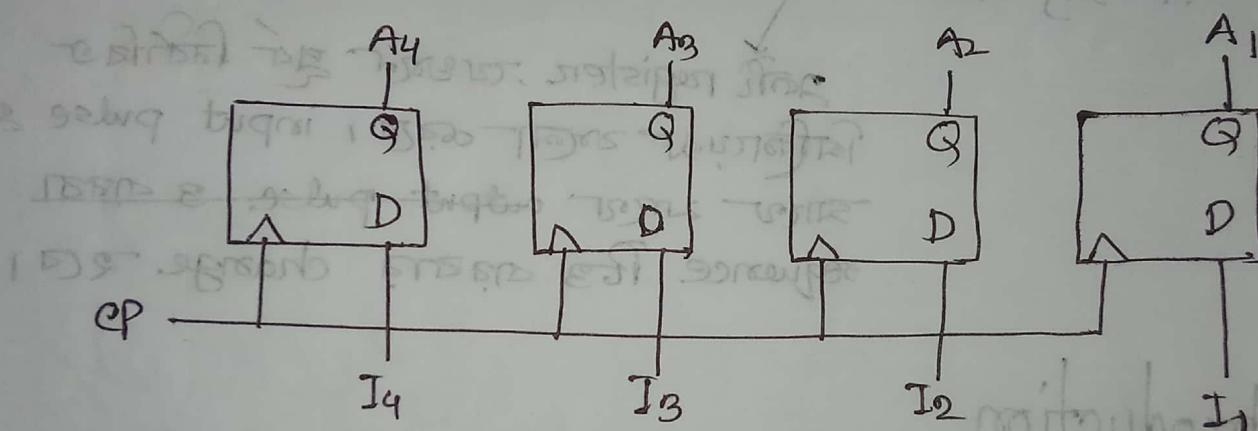
<u>(b) JK :</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>J</u>	<u>K</u>
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

<u>(c) D :</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>D</u>	<u>(d) T :</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>T</u>
0	0	0	0	0	0	0	0
0	1	0	1	0	0	1	1
1	0	0	0	b	1	0	1
1	1	1	1	b	1	1	0
				b			
				a			

Register

The simplest possible register is one that consists of only flip flop without any external gates.

The clock pulse input, CP, enables all flip-flops so that the information presently available can be transferred into 4 bit register.



(4 bit register with D flip flop)

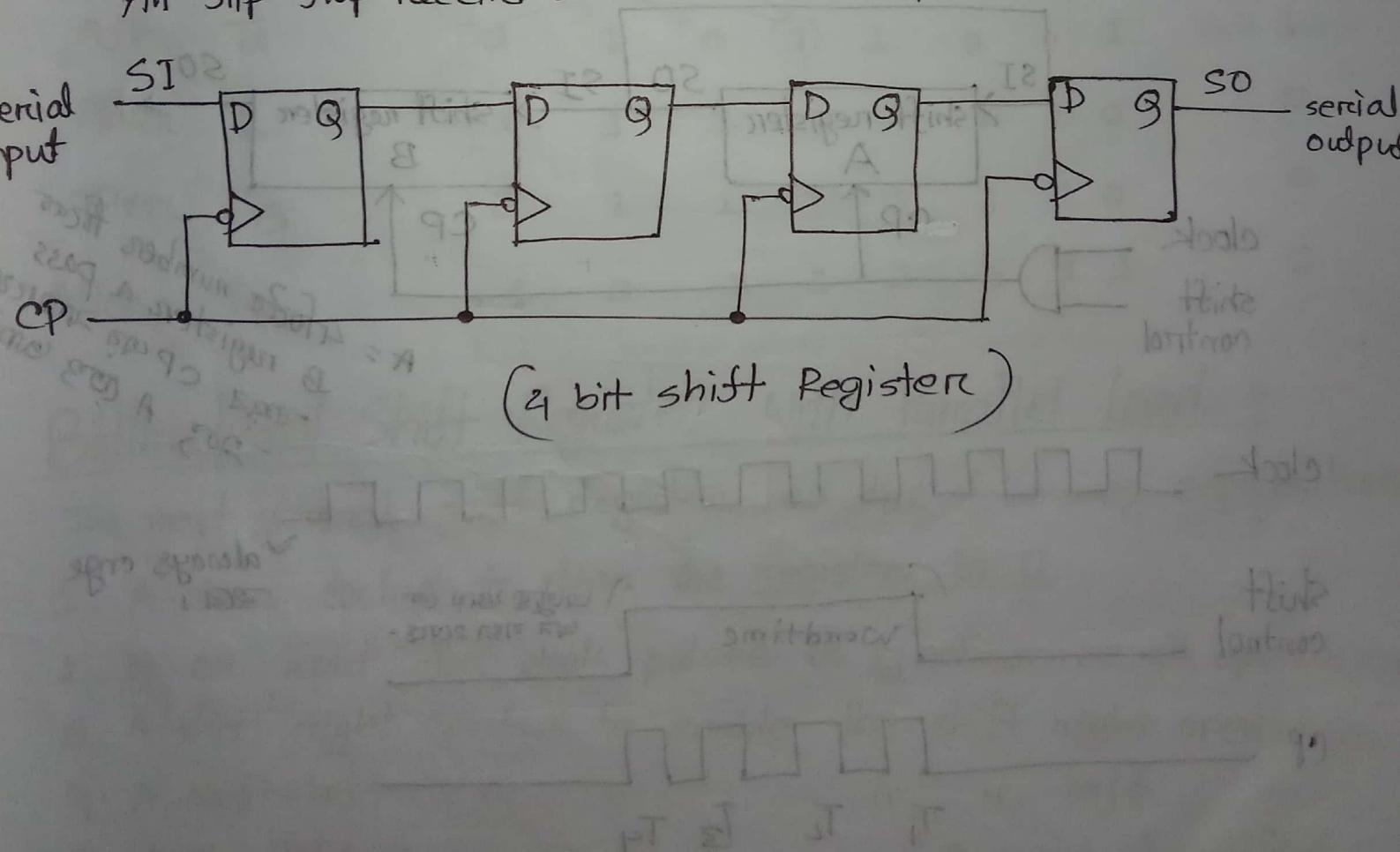
Shift Register

Instrumentation

A register capable of shifting its binary information either to the right or to the left is called shift register.

~~✓~~ The logical configuration of a shift register consists of a chain of flip flops connected in cascade (right or left) with the output of one flip-flop connected to the input of the next flip-flop.

All flip flop receive a common clock pulse.



Difference Between Latch and Flipflop

level sensitive	edge sensitive
faster	slower
less number of gate	more number of gate

PLA < PAL

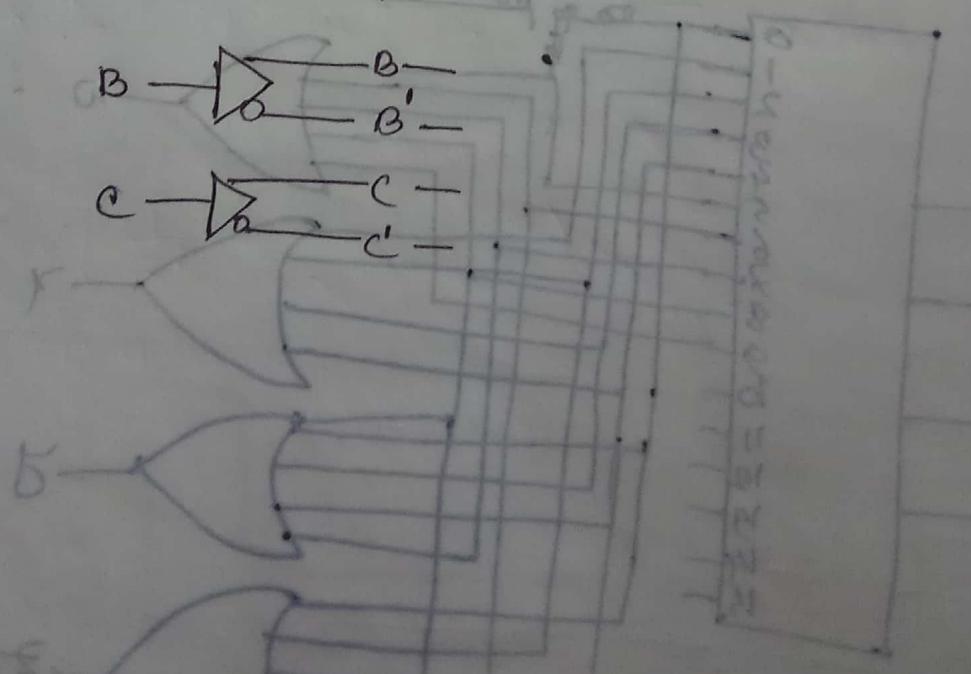
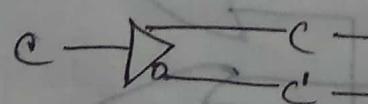
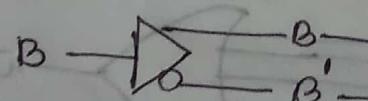
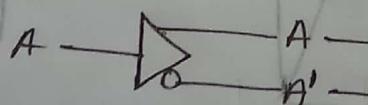
PLA

It is a type of fixed architecture logic device with programmable AND gates followed by programmable OR gates.

Step-1	A	B	C	Y_1	Y_2
	0	0	0		
	0	0	1		
	0	1	0		
	0	1	1		
	1	0	0		
	1	0	1		
	1	1	0		
	1	1	1		

$$\left. \begin{aligned} \text{Step-2: } Y_1 &= A\bar{B}\bar{C} + A\bar{B}C + ABC \\ &= \underline{A\bar{B}} + \underline{AC} \\ Y_2 &= \underline{BC} + \underline{AC} \end{aligned} \right\}$$

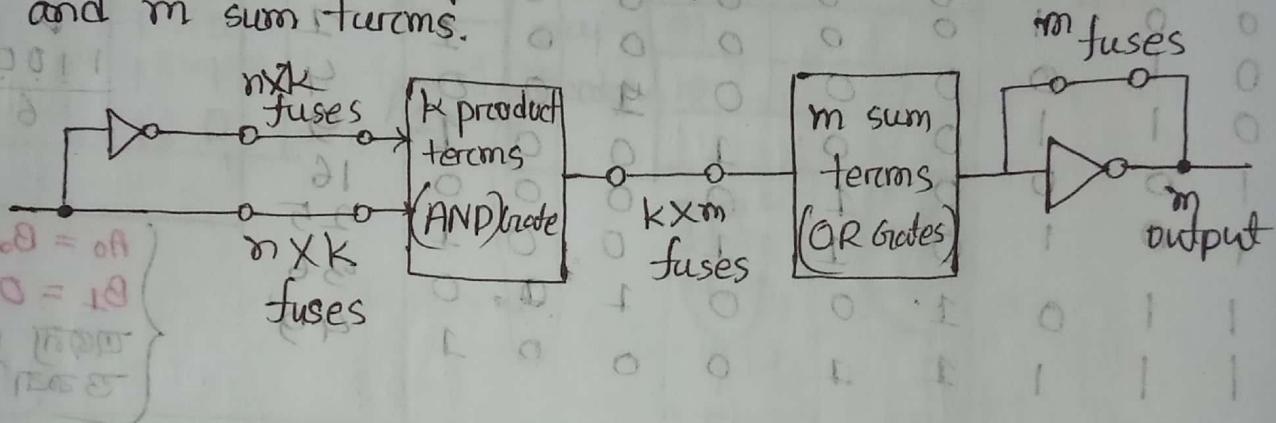
Step-3 No. of input buffer.
= No. of variable = 3



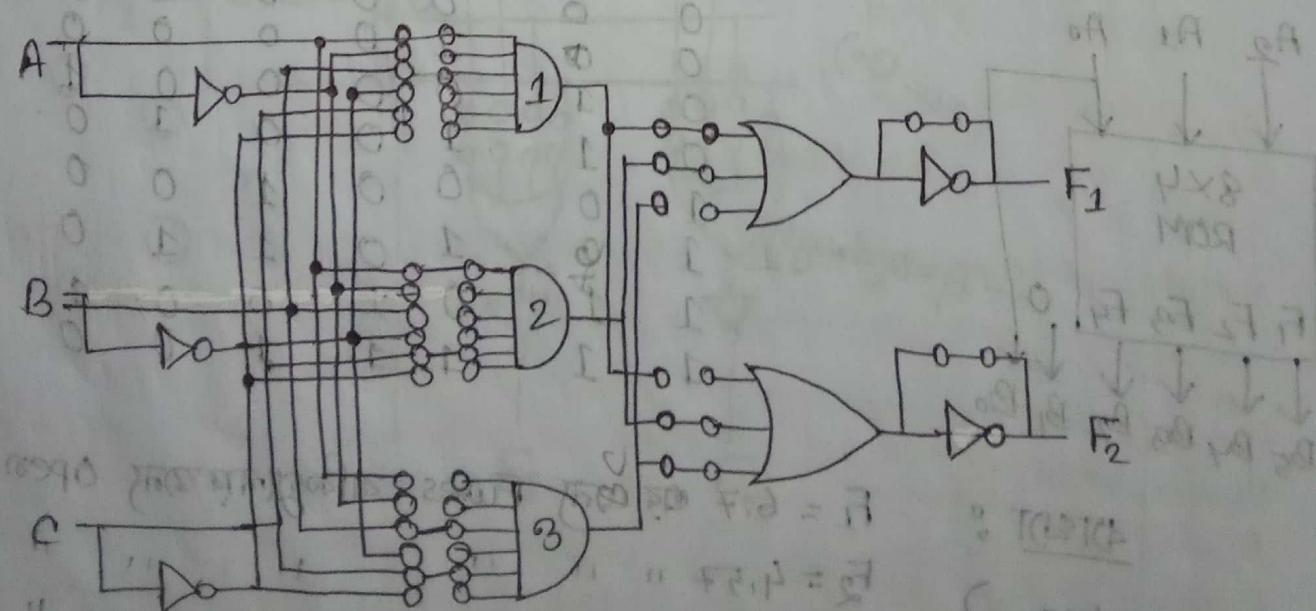
Programmable Logic Array:

- * A combinational circuit may have don't care conditions which become address inputs that will never occur.
- * It is more economical to use a second type of LSJ component called a programmable logic array.

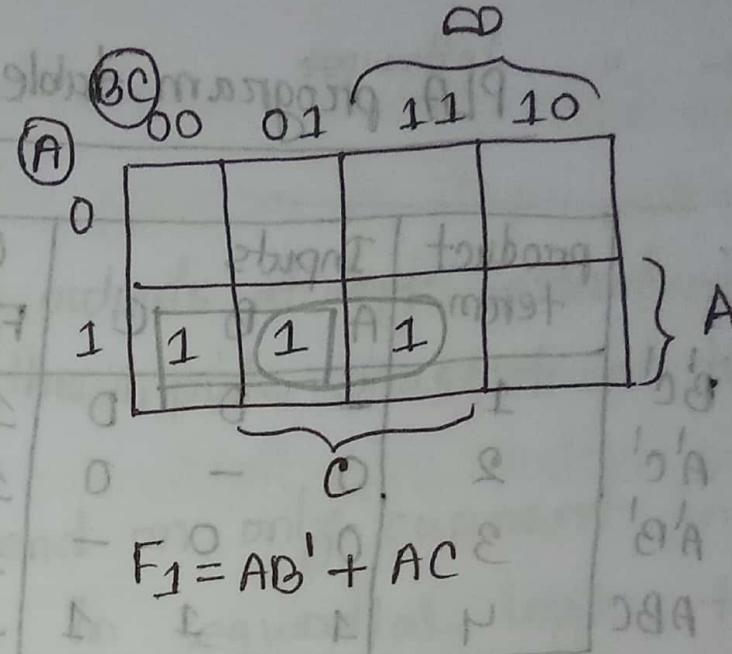
It consists of n inputs, m outputs, k product terms and m sum terms.



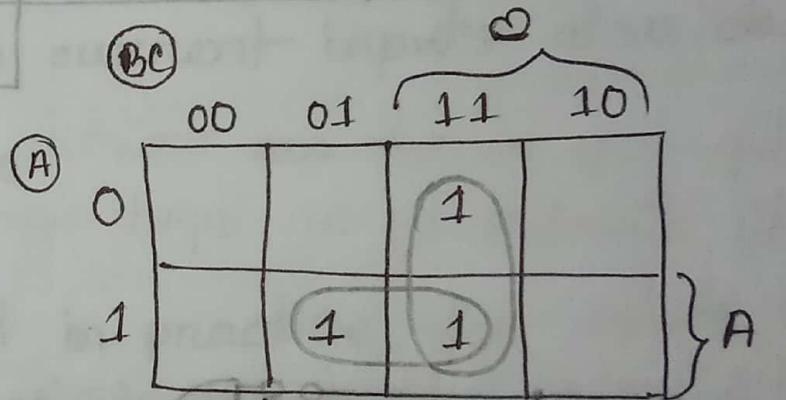
PLA with three inputs, three product terms and two outputs implemented with combinational circuit.



A	B	C	F	F_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1



Product term	Inputs			Outputs	
	A	B	C	F_1	F_2
AB'	1	1	0	1	-
AC	2	1	-	1	1
BC	3	-	1	-	1
				T	T
					T/C



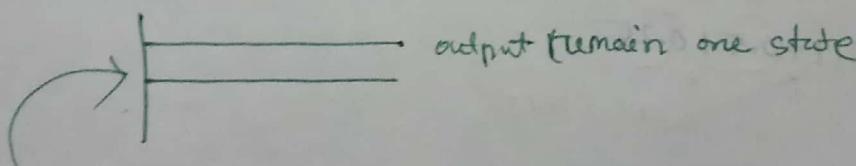
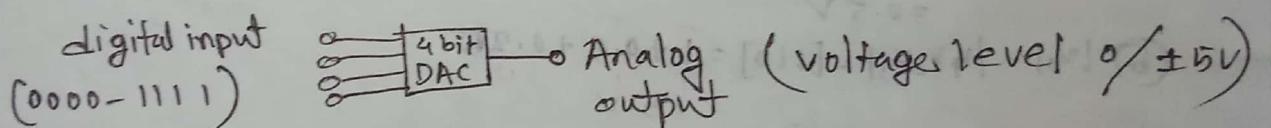
$F_2 = AC + BC$

Comparator : (Compare two voltage)

Op-amp comparator circuit is an open loop circuit. Because open loop op-amp have very high voltage gain, so small difference in input signals are detected. Here two signals which are to be compared are connected to the two input terminals. Output will be either $+V_{CC}$ or $-V_{CC}$. This op-amp comparator circuit is used as an interface between analog and digital circuit.

Ans: V_1, V_2 compare \rightarrow if $V_o = -ve \quad V_1 > V_2$
if $V_o = +ve \quad V_1 < V_2$

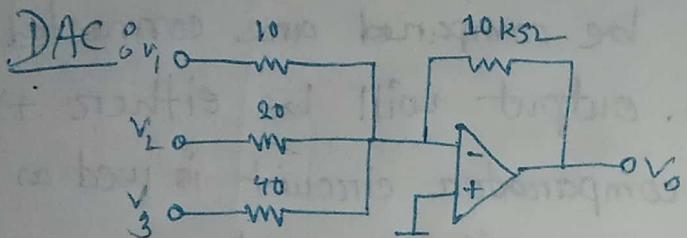
Converters : Digital to analog converter current to voltage converter.



Monostable multivibrator : Its output is in only one stable state. It is also known as one shot multivibrator. In a monostable multivibrator, the output pulse duration is determined by the Rc time constant and is $T = 1.11 R C$.

Bistable Multivibrator : A bistable vibrator is a circuit with an oscillating output. It doesn't need any external triggering and it has got no stable state. It is a type of regenerative oscillator.

Bistable Multi-vibrator: A bistable multi-vibrator is a circuit with two stable states. High and low. generally, a switch is required for toggling between the high and low state of the output.



- ① $(-V_o) = \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3$
- $= V_1 + 0.5V_2 + 0.25V_3$
- ② $|V_o|$ for $|V_1, V_2, V_3| = [010]$
- ③ $|V_o|$ for $|V_1, V_2, V_3| = [110]$
- ④ $|V_o| = 1.25$ what should do
- ⑤ $|V_o| = 1.75$ -- -- --

$$[V_1, V_2, V_3] = [010] = \cancel{0} + \cancel{0.5} + \cancel{0.25}$$

$$\cancel{0} + \cancel{0.5} + \cancel{0.25}$$

$$= 0.5V$$

$$⑥ |V_o| - |V_1, V_2, V_3| = [110] = \cancel{1} + \cancel{0.5} + \cancel{0.25}$$

$$⑦ |V_o| - |V_1, V_2, V_3| = \cancel{1} + \cancel{0.5} + \cancel{0.25} = 1.5V$$

$$⑧ |V_o| = |V_1, V_2, V_3| = \begin{bmatrix} 1 & 0 & 1 \end{bmatrix} = 1.25$$

$$1 + 0 + 1 = 1.25$$

High state (logic 1) Low state (logic 0)

(1111...0000)

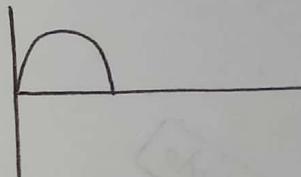
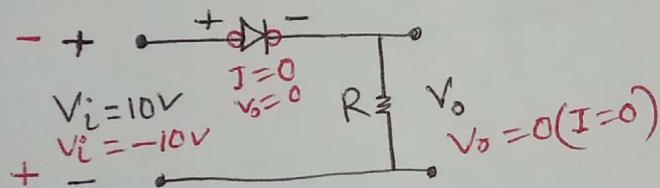
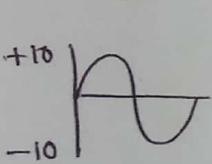
Multibitvibrator: An electronic device used to implement two state device like oscillator, timer, FF.

Clipper Circuit :

- यह circuit होना एक वेव एवं निपट्टे
- अंमेके remove करने या कटे जाने
- अतः clipper circuit बने।

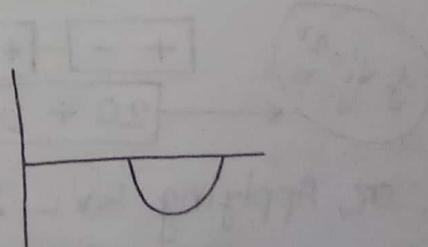
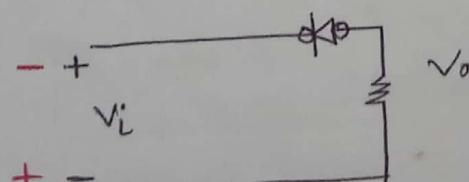
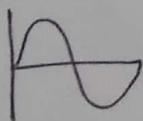
Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.

①

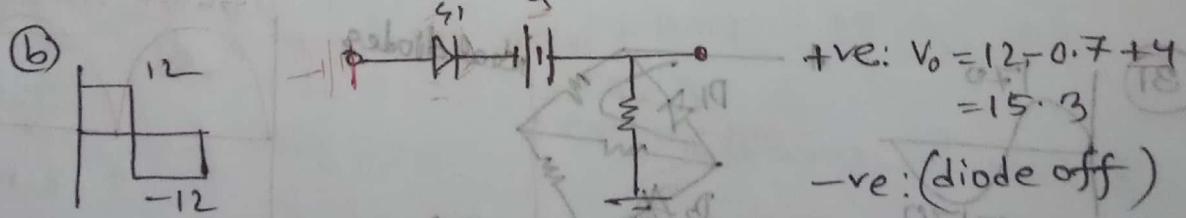
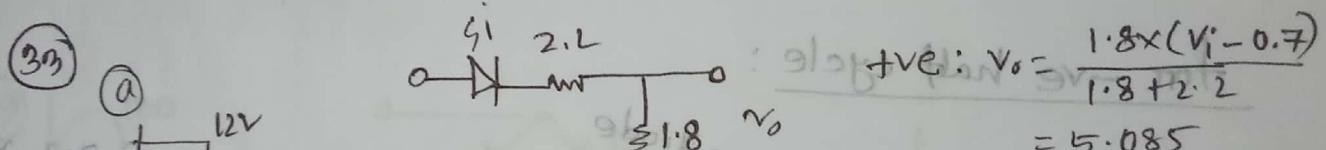
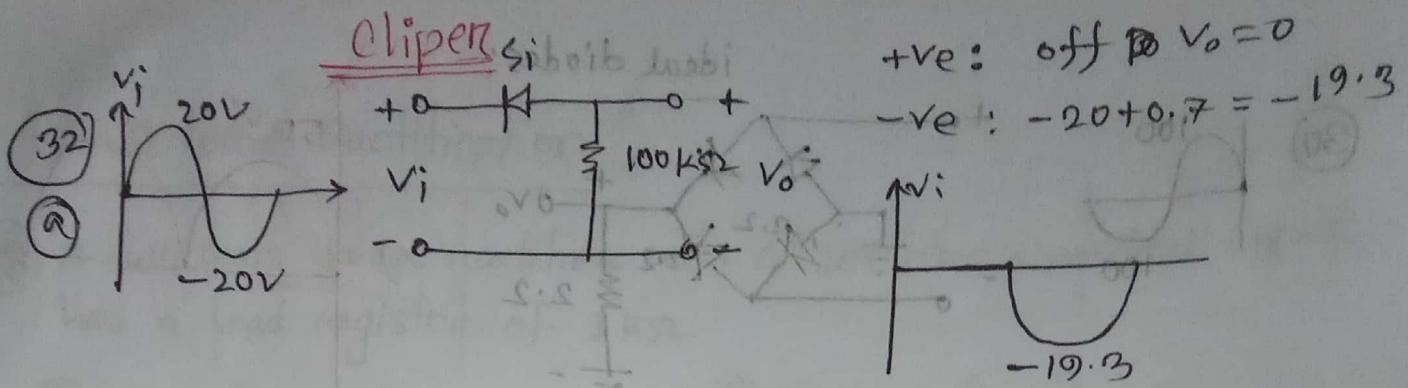


forward
reverse (off 2एवं गाव)

②



diode off
diode off active



$$\sqrt{52.27} = \frac{(0.81 \times 1.1)}{5.5 + 1.1} = \text{answer}$$

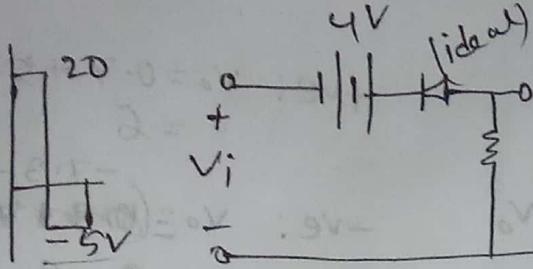
$$\sqrt{52.27} = \frac{0.81 \times 1.1}{5.5 + 1.1} = \text{answer}$$

: (110.0): step 110.0

$$1.1 = 5.5 \parallel 3.8$$

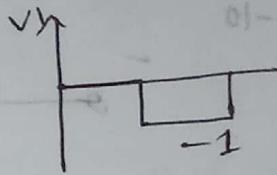
(34)

@

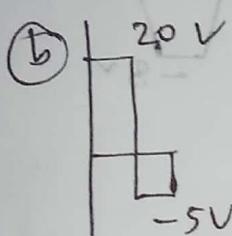


$$+ve: v_o = 0 \text{ (diode off)}$$

$$-ve: 2v_o = 5 - 4 + v_o = 0 \\ \Rightarrow v_o = -1 \\ 5 \times 4 = v_o$$

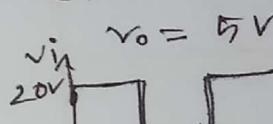


(b)

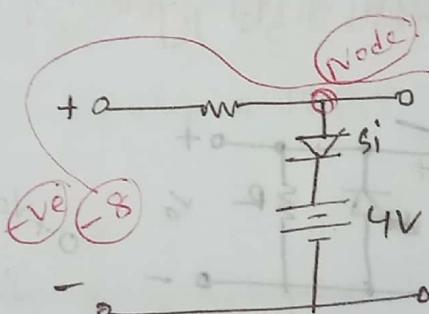
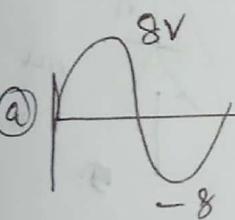


$$+ve: v_o = 20V$$

$$-ve: (\text{diode off})$$

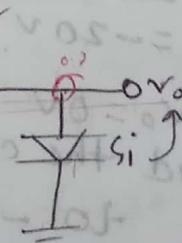
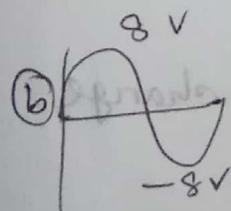
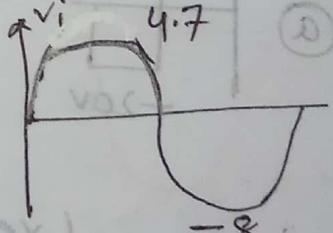


(35)



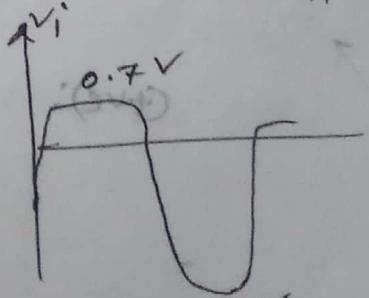
$$+ve: v_o = 4 + 0.7 = 4.7$$

$$-ve: v_o = -8 \text{ V} = v_i$$



$$+ve: v_o = 0.7$$

$$-ve: v_o = -8 - 3 = -11$$



~~to give total voltage across Node 2 & 3~~
 diode ~~will remain open~~ ~~Node 2 & 3~~ ~~voltage across~~
~~will be 0V~~ ~~Node 2 & 3~~ ~~voltage across~~
~~total voltage across 2 & 3~~