DIGITAL LOGIC DESIGN

by

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Definitions

- Switching network
  - One or more inputs
  - One or more outputs
    - Two Types
      - Combinational
        - The output depends only on the present values of the inputs
        - Logic gates are used
      - Sequential
        - The output depends on present and past input values

Boolean Algebra

- **Boolean Algebra** is used to describe the relationship between inputs and outputs
- **Boolean Algebra** is the logic mathematics used for understanding of digital systems

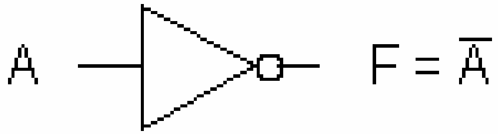
Basic Operations

- **COMPLEMENT (INVERSE)**

$$0^{'} = 1 \quad \text{and} \quad 1^{'} = 0$$

$$A^{'} = 1 \quad \text{if} \quad A = 0 \quad \text{and} \quad A^{'} = 0 \quad \text{if} \quad A = 1$$

A	F
0	1
1	0



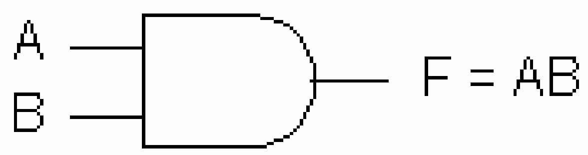
0 is low voltage

1 is high voltage

Basic Operations

- **AND**

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1



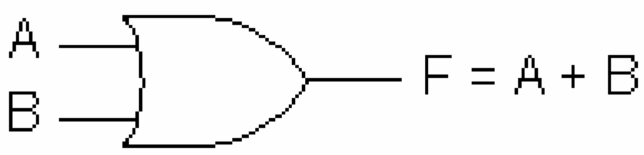
F is 1 if and only if

A and B are both 1

Basic Operations

- **OR**

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1



F is 1 if and only if

A or B (or both) are 1

Basic Theorems

$$X + 0 = X \qquad X \cdot 1 = X$$

$$X + 1 = 1 \qquad X \cdot 0 = 0$$

$$X + X = X \qquad X \cdot X = X$$

$$(X')' = X \qquad X + XY = X$$

$$X + X' = 1 \qquad X(X + Y) = X$$

Let's prove each one

Simplification Theorems

1. $XY + XY' = X$
2. $(X+Y)(X+Y') = X$
3. $X + XY = X$
4. $X(X+Y) = X$
5. $(X+Y')Y = XY$
6. $XY' + Y = X + Y$

- **Proof 6.**

  R.H.S. = $X+Y$

  $= X(Y+Y')+Y(X+X')$

  $= XY+XY'+XY+X'Y$

  $= XY+XY'+X'Y$

  $= (X+X')Y+XY'$

  $= Y+XY'$

  = L.H.S.

Truth Table

- It can represent a boolean function
- For possible input combinations it shows the output value
- There are 2^n rows (*n* is the number of input variables)
- It ranges from 0 to $2^n - 1$

Examples

- Show the truth table for

$$F = X' + YZ$$

- Show the followings by constructing truth tables

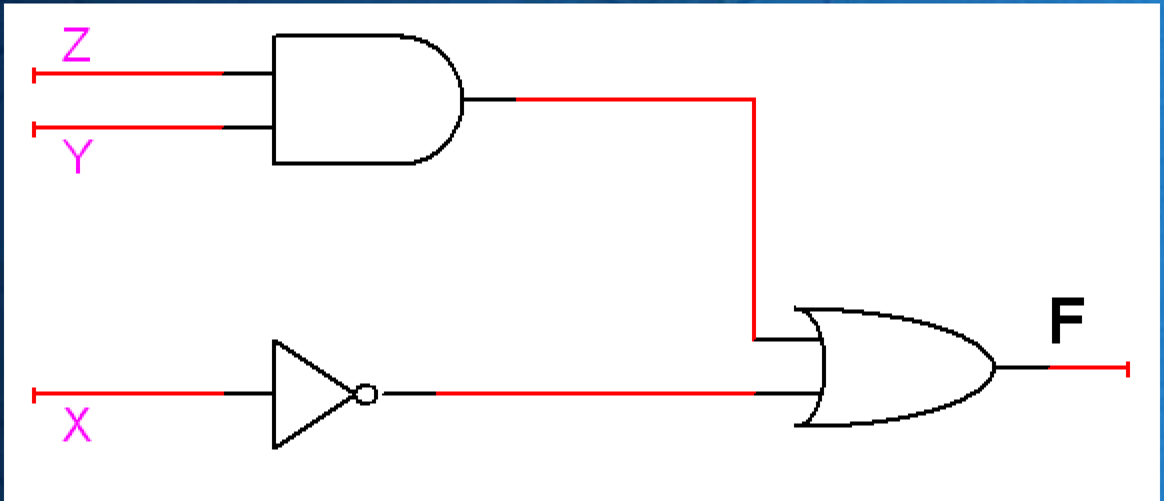
$$X(Y+Z) = XY + XZ$$

$$X + YZ = (X+Y)(X+Z)$$

Example

- Draw the network diagram for

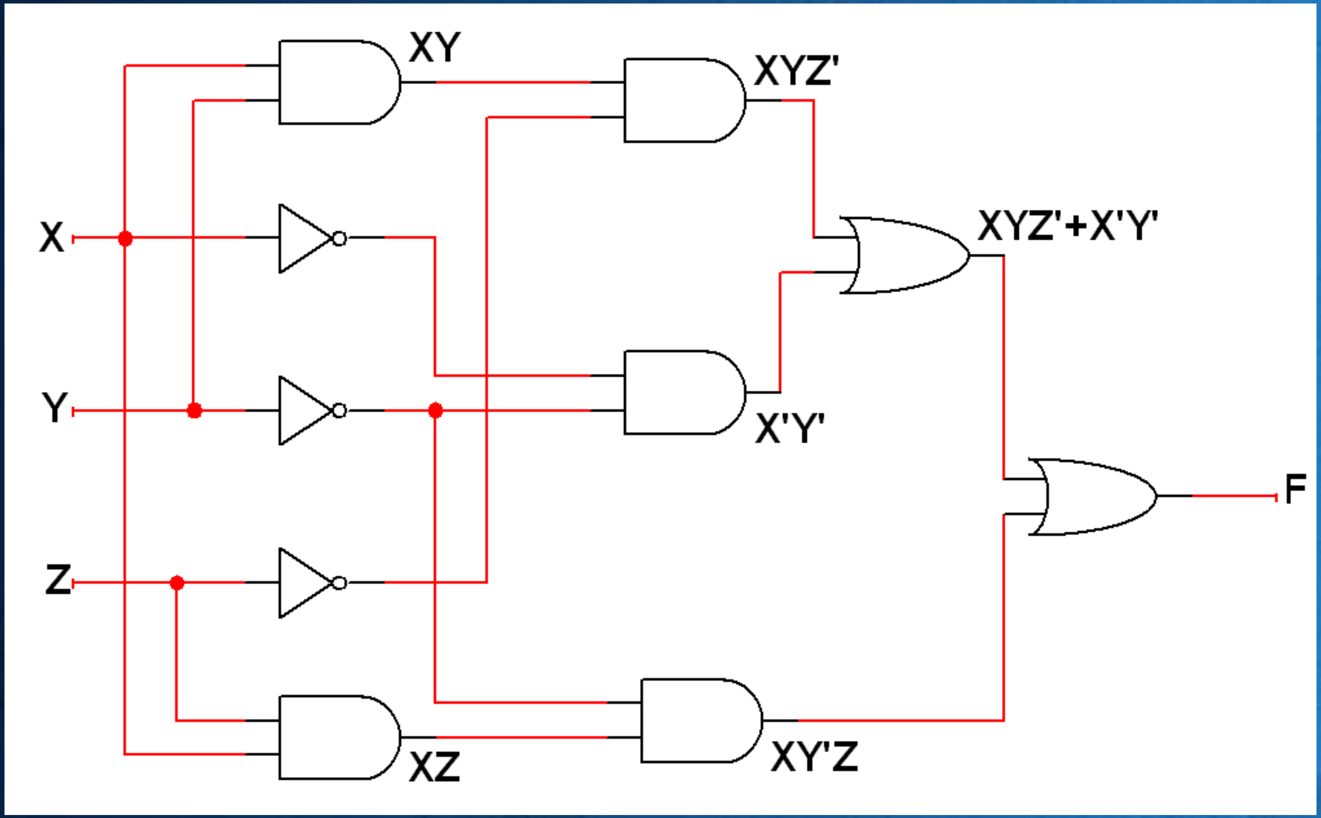
$$F = X' + YZ$$



Example

- Draw the network diagram for

$$F = XYZ' + XY'Z + X'Y'$$



Operator Precedence

- Parenthesis
- NOT
- AND
- OR

Inversion

$$(X+Y)' = X'Y'$$
$$(XY)' = X' + Y'$$

Prove with the truth tables…

$$(X_1 + X_2 + \ldots + X_n)' = X_1' X_2' \ldots X_n'$$
$$(X_1 X_2 \ldots X_n)' = X_1' + X_2' + \ldots + X_n'$$

- **The complement of the product is the sum of the complements**
- **The complement of the sum is the product of the complements**

Examples

- **Find the complements of**

$$[(A' + B)C']' = ?$$

$$[(AB' + C)D' + E]' = ?$$

$$\left[A + ((BC')' + D)'\right]'' = ?$$

Study Problems

1. Draw a network to realize the following by using only one AND gate and one OR gate

$$Y = ABCD + ABCE + ABCF$$

2. Draw a network to realize the following by using two OR gates and two AND gates

$$F = (V + W + X)(V + X + Y)(V + Z)$$

3. Prove the following equations using truth table

$$W'XY + WZ = (W' + Z)(W + XY)$$

$$(A + C)(AB + C') = AB + AC'$$

Solution of problem 2

L.H.S.=(V+X+W)(V+X+Y)(V+Z)

=[(V+X)+W(V+X)+Y(V+X)+WY](V+Z)

=[(V+X)(1+W+Y)+WY](V+Z)

=(V+X+WY)(V+Z)

This can be implemented by two OR gates and two AND gate.

Minterms

- Consider variables *A* and *B*
- Assume that they are somehow combined with AND operator
- There are 4 possible combinations

$$AB, \quad A'B, \quad AB', \quad A'B'$$

- Each of those terms is called a minterm (standard product)
- In general, if there are n variables, there are 2^n minterms

Exercise

- **List the minterms for 3 variables**

A	B	C	Minterm	Designation
0	0	0	$A'B'C'$	m_0
0	0	1	$A'B'C$	m_1
0	1	0	$A'BC'$	m_2
0	1	1	$A'BC$	m_3
1	0	0	$AB'C'$	m_4
1	0	1	$AB'C$	m_5
1	1	0	ABC'	m_6
1	1	1	ABC	m_7

Maxterms

- Consider variables *A* and *B*
- Assume that they are somehow combined with OR operator
- There are 4 possible combinations

$$A+B, \quad A^{'}+B, \quad A+B^{'}, \quad A^{'}+B^{'}$$

- Each of those terms is called a maxterm (standard sums)
- In general, if there are n variables, there are 2^n maxterms

Exercise

- List the maxterm for 3 variables

A	B	C	Maxterm	Designation
0	0	0	A+B+C	M_0
0	0	1	A+B+C'	M_1
0	1	0	A+B'+C	M_2
0	1	1	A+B'+C'	M_3
1	0	0	A'+B+C	M_4
1	0	1	A'+B+C'	M_5
1	1	0	A'+B'+C	M_6
1	1	1	A'+B'+C'	M_7

Example

- **Express *F* in the sum of minterms and product of maxterms formats**

$$F = A + BC'$$

$$\begin{aligned}
F = A + BC' &= A(B + B')(C + C') + (A + A')BC' \\
&= ABC + ABC' + AB'C + AB'C' + ABC' + A'BC' \\
&= ABC + ABC' + AB'C + AB'C' + A'BC' \\
&= m_7 + m_6 + m_5 + m_4 + m_2 \\
&= \sum(2,4,5,6,7) \\
&= \prod(0,1,3)
\end{aligned}$$

Sum-of-Products

- **All products are the product of single variable only**

$$AB' + CD'E + AC'E' \quad \leftarrow \text{YES}$$

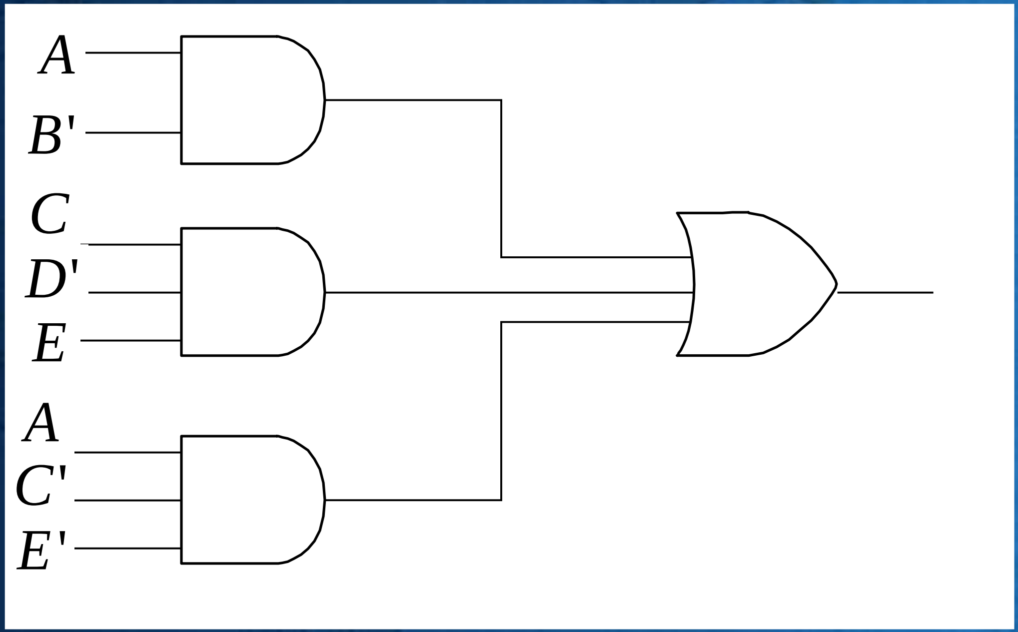
$$A + B' + C + D'E \quad \leftarrow \text{YES}$$

$$(A+B)CD + EF \quad \leftarrow \text{NO}$$

Sum-of-Products

- **One or more AND gates feeding a single OR gate at the output**

$$AB' + CD'E + AC'E'$$



Product-of-Sums

- **All sums are the sums of single variables**

$$(A+B')(C+D'+E)(A+C'+E')$$ ← YES

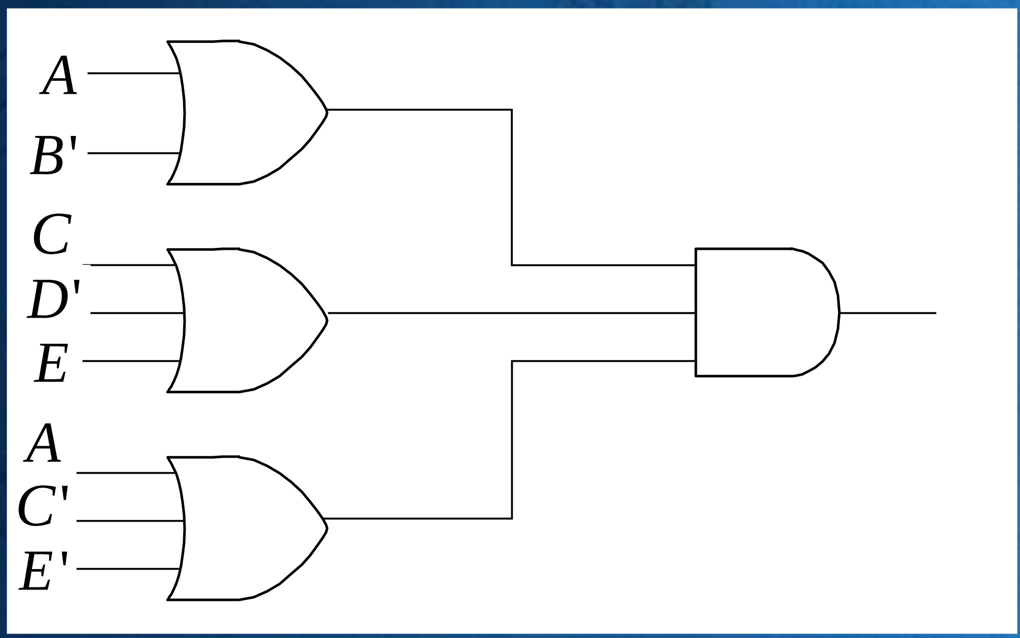
$$AB'C(D'+E)$$ ← YES

$$(A+B)(C+D)+EF$$ ← NO

Product-of-Sums

- **One or more OR gates feeding a single AND gate at the output**

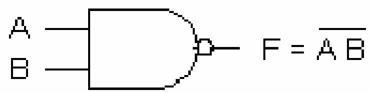
$$(A+B')(C+D'+E)(A+C'+E')$$



Logic Gates

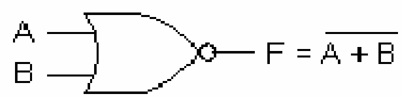
$F = A \uparrow B$

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



NAND

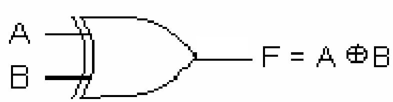
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0



NOR

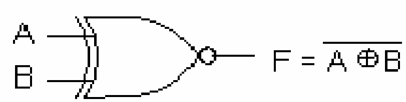
$F = A \downarrow B$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0



Exclusive-OR (XOR)

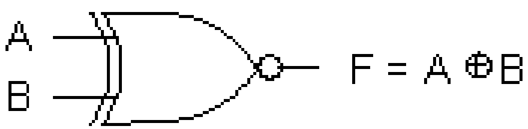
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1



Exclusive-NOR (XNOR)

Exclusive-OR

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0



Exclusive-OR (XOR)

$$A \oplus 0 = A$$

$$A \oplus 1 = A'$$

$$A \oplus A = 0$$

$$A \oplus A' = 1$$

$$A \oplus B = B \oplus A$$

$$(A \oplus B) \oplus C = A \oplus (B \oplus C) = A \oplus B \oplus C$$

$$A(B \oplus C) = AB \oplus AC$$

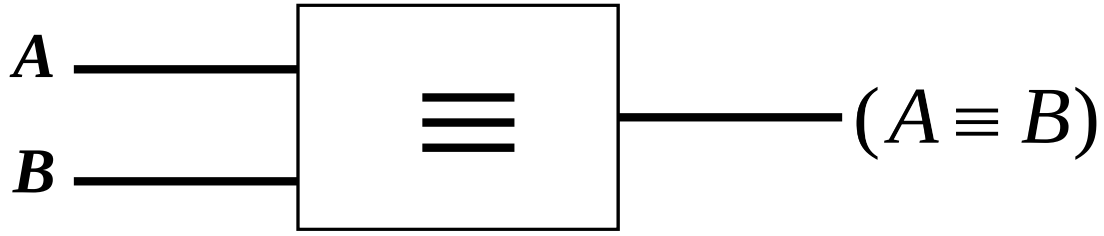
$$(A \oplus B)' = A \oplus B' = A' \oplus B = AB + A'B'$$

$$A \oplus B = 1 \Leftrightarrow A = 1 \quad \text{or} \quad B = 1 \quad \text{but not both}$$

Equivalence

- **Equivalence is the complement of exclusive-OR**

$$(A \oplus B)' = (A'B + AB')' = (A + B')(A' + B) =$$
$$= AB + A'B' = (A \equiv B)$$



$$F = (A'B \equiv C) + (B \oplus AC')$$

Simplify it…

Integrated Circuits

- SSI (Small Scale)
  - Less than 10 gates in a package
- MSI (Medium Scale)
  - 10-1000 gates in a package
- LSI (Large Scale)
  - 1000s of gates in a single package
- VLSI (Very Large Scale)
  - Hundred of thousands of gates in a single package

Study Problems

- **Course Book Chapter – 2 Problems**
  - 2 – 1
  - 2 – 3
  - 2 – 5
  - 2 – 8
  - 2 – 12
  - 2 – 14

Questions