PROJECT SAIC

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GROUP:2331
YEAR: III

Theme

This project presents 4 stages, the first one is a non-inverting amplifier with a single ended voltage, the second stage contains a low pass Sallen Key circuit, the third stage has a circuit with a PGA with RG parallel and switches and the last stage represents a full wave rectifier with two op-amps. The op-amp I used for the project is ADA4077 which has a max supply of -/+20V.

STAGE 1 -Non-inverting amplifier

A non-inverting amplifier circuit with a single-ended voltage source uses an operational amplifier (op-amp) to amplify an input voltage, providing an output voltage that is in-phase with the input. The input voltage is connected to the non-inverting terminal of the op-amp, while a feedback resistor network is used to determine the amplification factor, allowing the circuit to produce a scaled version of the input. The requirements for this project were

STAGE 2 - Low pass Sallen-Key

A Sallen-Key filter is a type of active filter circuit commonly used in electronics to implement low-pass and high-pass filters. It typically consists of an operational amplifier (op-amp) configured in a specific arrangement with resistors and capacitors to achieve the desired frequency response. The Sallen-Key topology is known for its simplicity and versatility, making it a popular choice for designing second-order filters in various electronic applications. The gain for the circuit is 1 and Rin min is 2k ohms.

STAGE 3 - PGA RG paralel

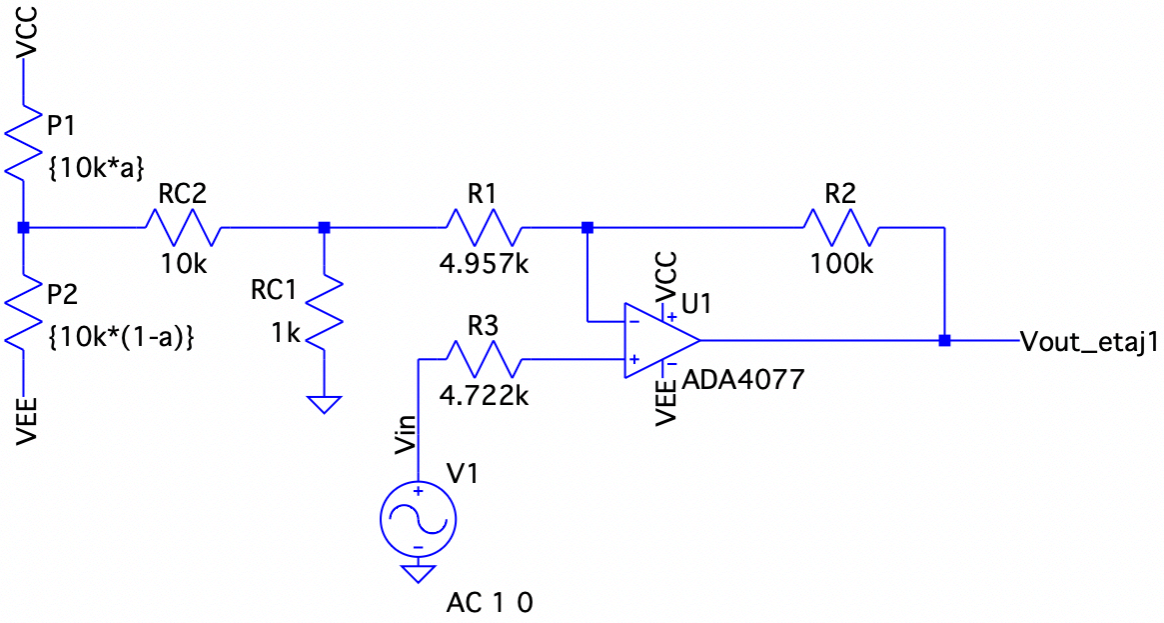
A PGA (Programmable Gain Amplifier) RG parallel circuit involves the use of parallel resistors (RG) in a configuration that enables programmable gain settings for the amplifier. By changing the combination of resistors in parallel, the circuit allows for flexible adjustment of the gain, making it suitable for applications where variable amplification is required, such as in instrumentation and communication systems.

STAGE 4 -Full wave rectifier

A precision full-wave rectifier is a circuit designed to rectify both the positive and negative halves of an AC signal accurately, providing a full-wave rectified output with minimal voltage drop. One common implementation of a precision full-wave rectifier is based on an operational amplifier (op-amp) and diodes.

Sizing

STAGE 1



$$A_V = \frac{R_2}{R1 + R_{C-EQ}}; R_{C1} << R1; R_{C2} << RC2$$

$$R_{C-EQ} = RC1 \quad (R_{C2} + a \cdot P \quad (1-a) \cdot P)$$

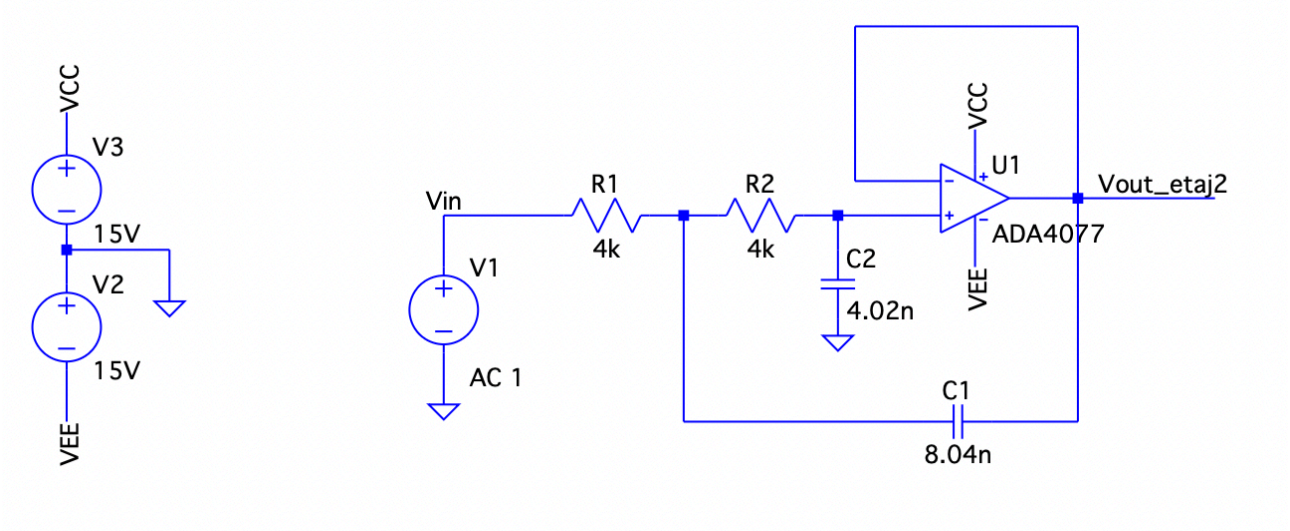
Assume: $a = 0.49; P = 10k; R_{C2} = 10k; RC1 = 1k; R_2 = 100k$

$$(0.49 \cdot 10k) \quad (1 - 0.49) * 10k = \frac{4.9k \cdot 5.1k}{4.9k + 5.1k} = 2.499 => R_{C-EQ} = 925$$

$$A_v = 18 => \frac{R_2}{R_1 + R_{C-EQ}} = 17 => R_1 = 4.957k$$

$$R_3 = R_2 \quad R_1 => R_3 = 4.722K$$

STAGE 2



LPF Sallen Key

$$H_0 = A_{DC} = 1; \omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}; Q = \frac{\sqrt{R_1 R_2}}{R_1 + R_2}\sqrt{\frac{C_1}{C_2}}$$

f0 [Hz]	w0[rad/sec]	Q	H0[V/V]
7,00E+03	4,40E+04	7,07E-01	1,00E+00

varianta 1

C1[F]	set C2[F]	set R1 = R2[ohm]
8,04E-09	4,02E-09	4,00E+03

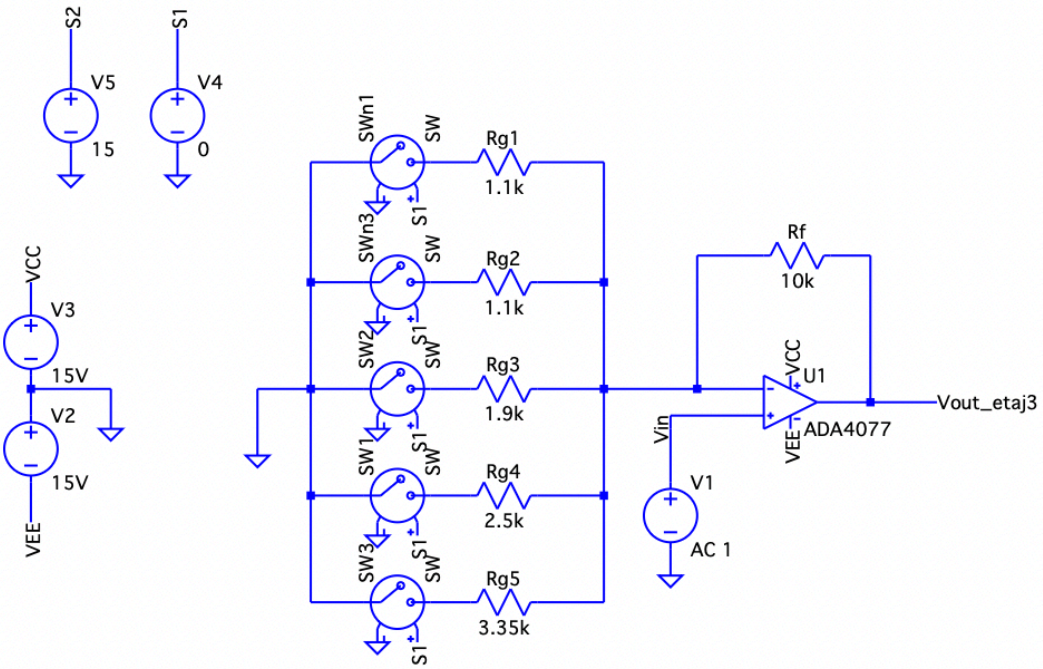
$$C_1 = \frac{2Q}{\omega_0 R}; C_2 = \frac{C_1}{4Q^2} = \frac{1}{2Q\omega_0 R}$$

varianta 2

C1[F]	set C2[F]	R1 = R2[ohm]
2,00E-10	1,00E-10	1,61E+05

$$C_1 = \frac{2Q}{\omega_0 R}; C_2 = \frac{C_1}{4Q^2} = \frac{1}{2Q\omega_0 R}$$

STAGE 3



$$Avv = 1 + \frac{R_f}{R_g}; R_f = 10k$$

$$20dB = 10V => R_G = \frac{10k}{9} = 1.1k = R_{g1}$$

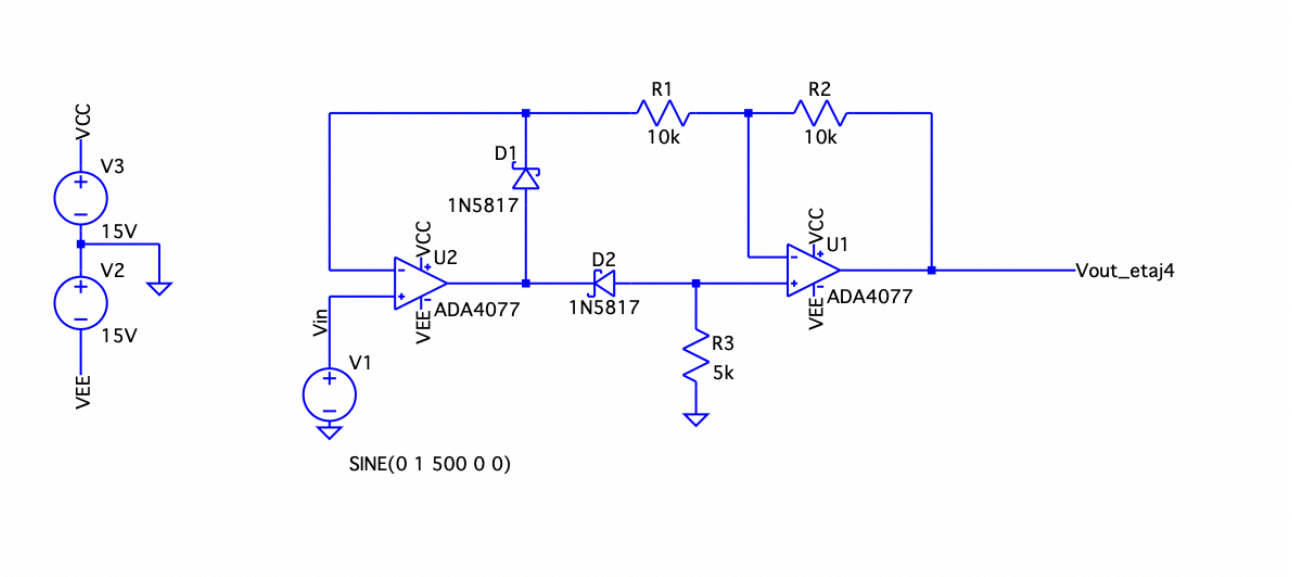
$$18dB = 7.94V => R_G = \frac{10k}{96.94} = 1.4k = R_{g2}$$

$$16dB = 6.03V => R_G = \frac{10k}{5.03} = 1.9k = R_{g3}$$

$$14dB = 5.01V => R_G = \frac{10k}{4.01} = 2.5k = R_{g4}$$

$$12dB = 3.98V => R_G = \frac{10k}{2.98} = 3.35k = R_{g5}$$

STAGE 4



$V_{out} = V_{in}; V_{in} < 0$

$V_{out} = -V_{in}; V_{in} > 0$

$R_1 = R_2 = 10k$

$R_3 = \frac{R}{2} = 5k$

Characterization

STAGE 1

```
Operating Bias Point Solution:
V(n003)                    9.96116    voltage
V(vout_etaj1)              14.0853    voltage
V(vcc)                          15    voltage
V(vee)                         -15    voltage
V(n004)                    12.2171    voltage
V(n002)                    1.58653    voltage
V(n001)                   0.557223    voltage
V(vin)                          20    voltage
I(R1)                   0.00168946    device_current
I(Rc2)                  0.00010293    device_current
I(R2)                  4.12416e-05    device_current
I(Rc1)                  -0.00158653   device_current
I(R3)                   0.00164821    device_current
I(P1)                   0.00294751    device_current
I(P2)                   0.00305044    device_current
I(V2)                   -0.00349174   device_current
I(V3)                   -0.00338878   device_current
I(V1)                   -0.00164821   device_current
Ix(u1:1)                0.00164821    subckt_current
Ix(u1:2)                -0.00164822   subckt_current
Ix(u1:3)                0.000441272   subckt_current
Ix(u1:4)                 -0.0004413   subckt_current
Ix(u1:5)                -4.12416e-05  subckt_current
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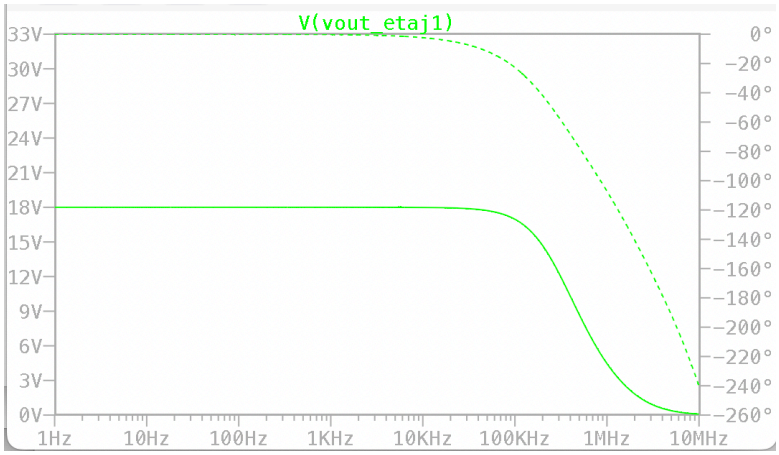
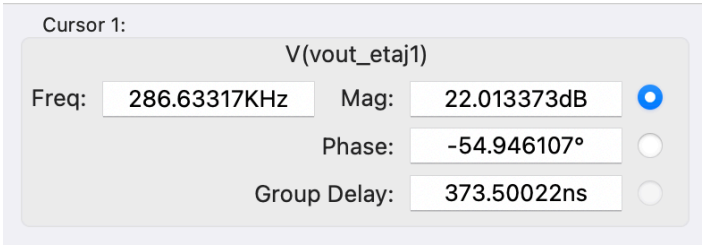
DCOP

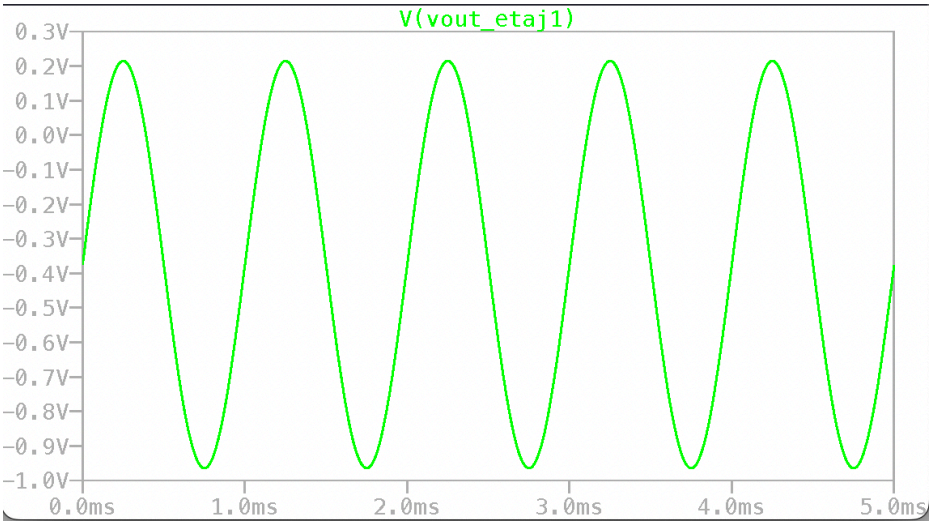
Gain=18



AC analysis



Bandwidth



Transient analysis

STAGE 2

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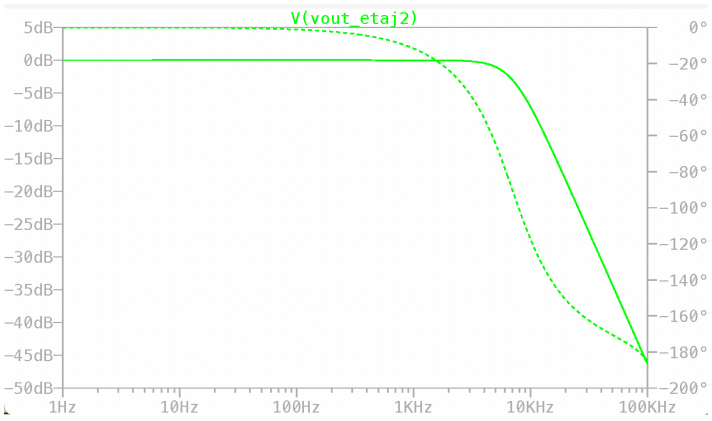
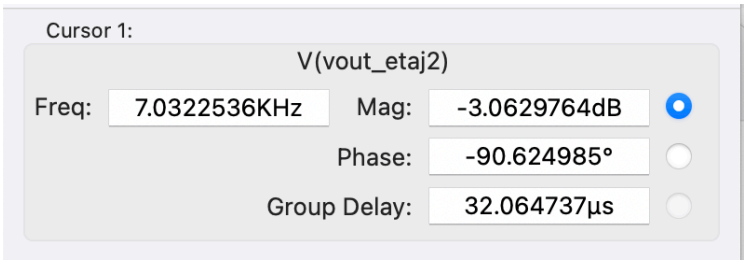
Operating Bias Point Solution:
V(vin)                          20    voltage
V(n001)                      16.9755  voltage
V(n002)                      13.9509  voltage
V(vout_etaj2)                12.6228  voltage
V(vcc)                          15    voltage
V(vee)                         -15    voltage
I(C2)                   5.60827e-20   device_current
I(C1)                   -3.4995e-20   device_current
I(R1)                  -0.000756136   device_current
I(R2)                  -0.000756136   device_current
I(V1)                  -0.000756136   device_current
I(V2)                   0.000356084   device_current
I(V3)                   0.000356109   device_current
Ix(u1:1)                0.000756136   subckt_current
Ix(u1:2)               -0.000756137   subckt_current
Ix(u1:3)               -0.000356109   subckt_current
Ix(u1:4)                0.000356083   subckt_current
Ix(u1:5)                0.000756137   subckt_current
```

DCOP

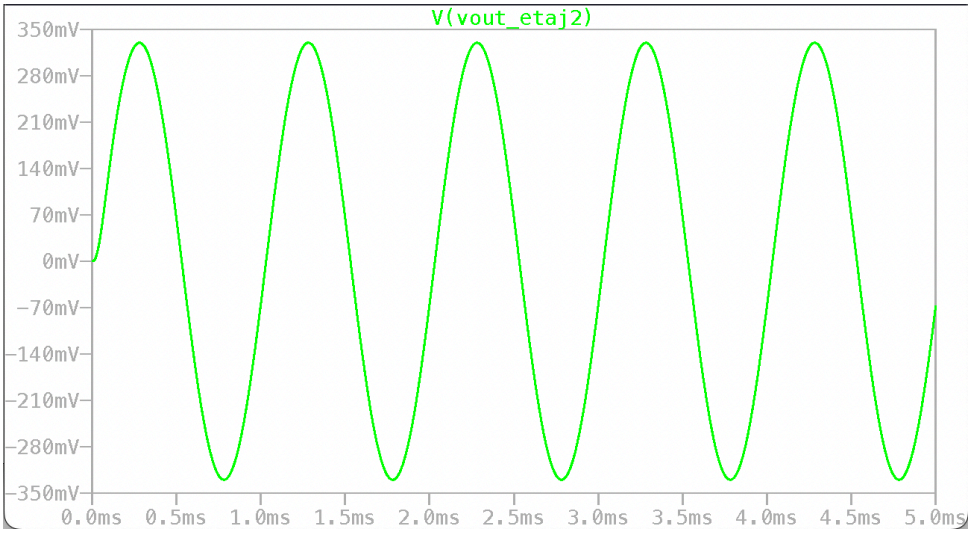
H0=1



AC analysis



Bandwidth



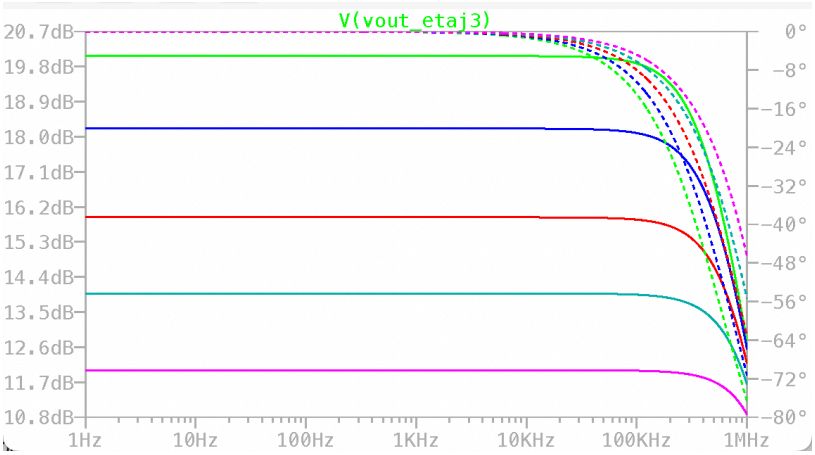
Transient analysis

STAGE 3

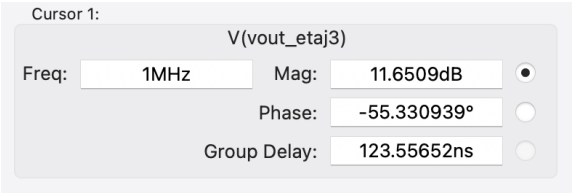
```
Operating Bias Point Solution:
V(n002)                    8.9152   voltage
V(vout_etaj3)            -13.9978   voltage
V(vcc)                         15   voltage
V(vee)                        -15   voltage
V(vin)                         20   voltage
V(n005)                    8.9152   voltage
V(n006)                    8.9152   voltage
V(s1)                           0   voltage
V(s2)                          15   voltage
V(n003)                    8.9152   voltage
V(n001)                0.00809736   voltage
V(n007)                    8.9152   voltage
V(n004)                    8.9152   voltage
I(Rf)                  -0.0022913   device_current
I(Rg3)                1.78304e-11   device_current
I(Rg4)                1.78304e-11   device_current
I(Rg1)                1.78304e-11   device_current
I(Rgn)                 0.00809736   device_current
I(Rg5)                1.78304e-11   device_current
I(Rg2)                1.78304e-11   device_current
I(Sw2)                1.78304e-11   device_current
I(Sw1)                1.78304e-11   device_current
I(Swn1)               1.78304e-11   device_current
I(Swn2)                0.00809736   device_current
I(Sw3)                1.78304e-11   device_current
I(Swn3)               1.78304e-11   device_current
I(V1)                  -0.0103887   device_current
I(V2)                   0.00189132   device_current
I(V3)                   0.00189129   device_current
I(V4)                           0   device_current
I(V5)                           0   device_current
Ix(u1:1)                0.0103887   subckt_current
Ix(u1:2)               -0.0103887   subckt_current
Ix(u1:3)               -0.00189129   subckt_current
Ix(u1:4)                0.00189132   subckt_current
Ix(u1:5)                0.0022913   subckt_current
```

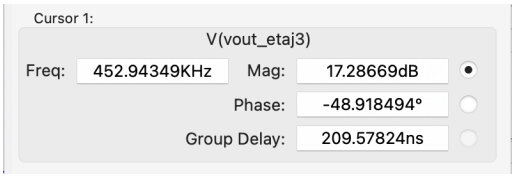
DCOP

GAIN

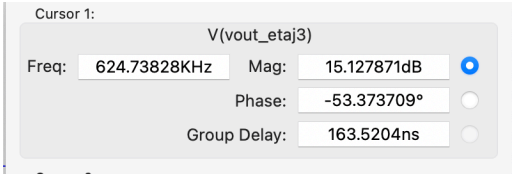


AC analysis

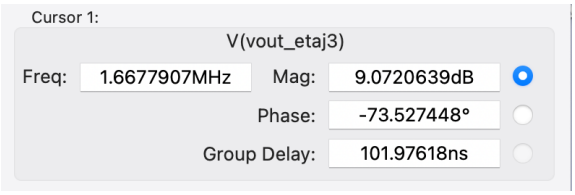




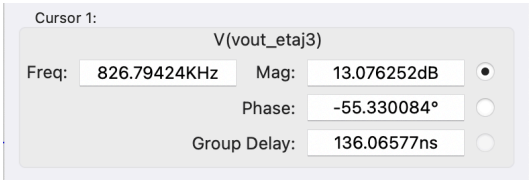
20dB



14dB

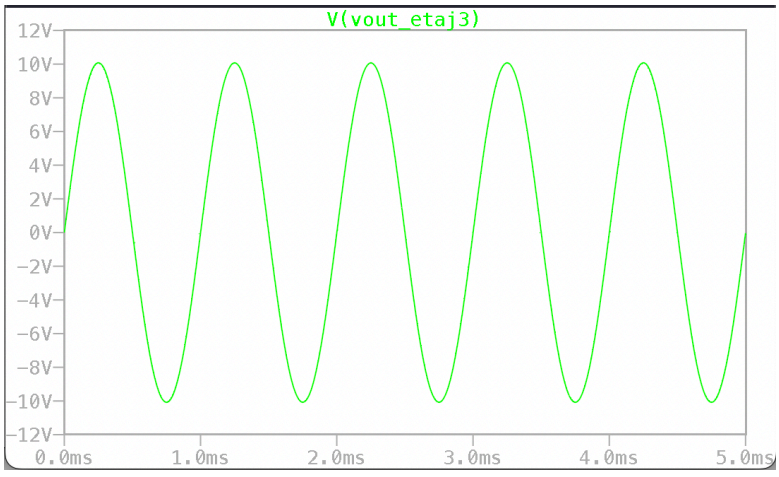


18dB



12dB

16dB



Transient Analysis

STAGE 4

```
Operating Bias Point Solution:
V(n002)                  -10.7283   voltage
V(vout_etaj4)             -14.039   voltage
V(vcc)                         15   voltage
V(vee)                        -15   voltage
V(n004)                  -13.7556   voltage
V(n001)                   16.6033   voltage
V(n003)                  -13.9369   voltage
V(vin)                         20   voltage
I(D1)                   -3.17e-05   device_current
I(D2)                  0.00515321   device_current
I(R2)                  0.000331071  device_current
I(R1)                  0.00273316   device_current
I(R3)                  -0.00275112  device_current
I(V1)                  -0.00276486  device_current
I(V2)                  0.00471603   device_current
I(V3)                  0.00471597   device_current
Ix(u1:1)               -0.00240209  subckt_current
Ix(u1:2)               0.00240209   subckt_current
Ix(u1:3)               6.89311e-05  subckt_current
Ix(u1:4)               -6.89029e-05 subckt_current
Ix(u1:5)               0.000331071  subckt_current
Ix(u2:1)               0.00276486   subckt_current
Ix(u2:2)               -0.00276486  subckt_current
Ix(u2:3)               -0.00478491  subckt_current
Ix(u2:4)               0.00478494   subckt_current
Ix(u2:5)               0.00518491   subckt_current
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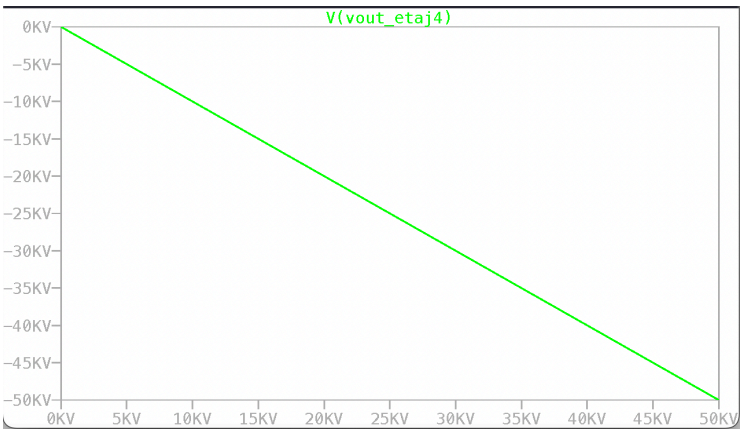
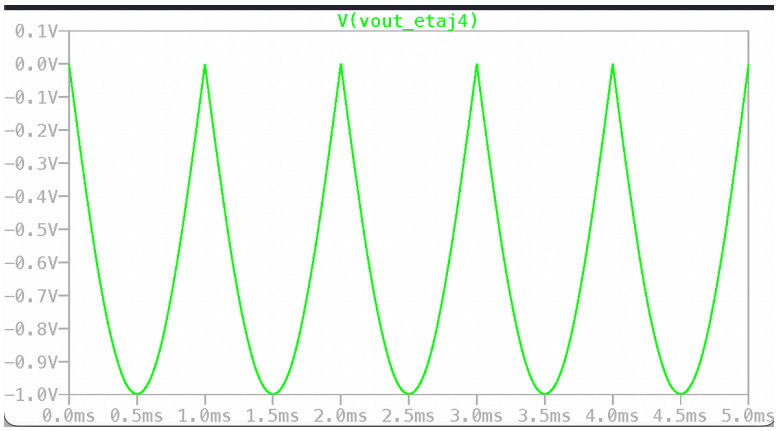
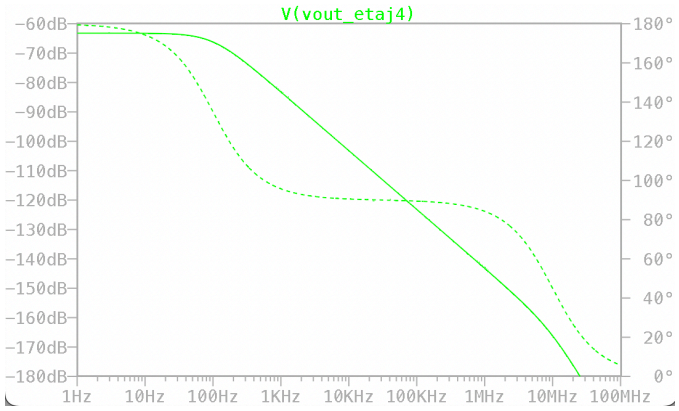


DCOP

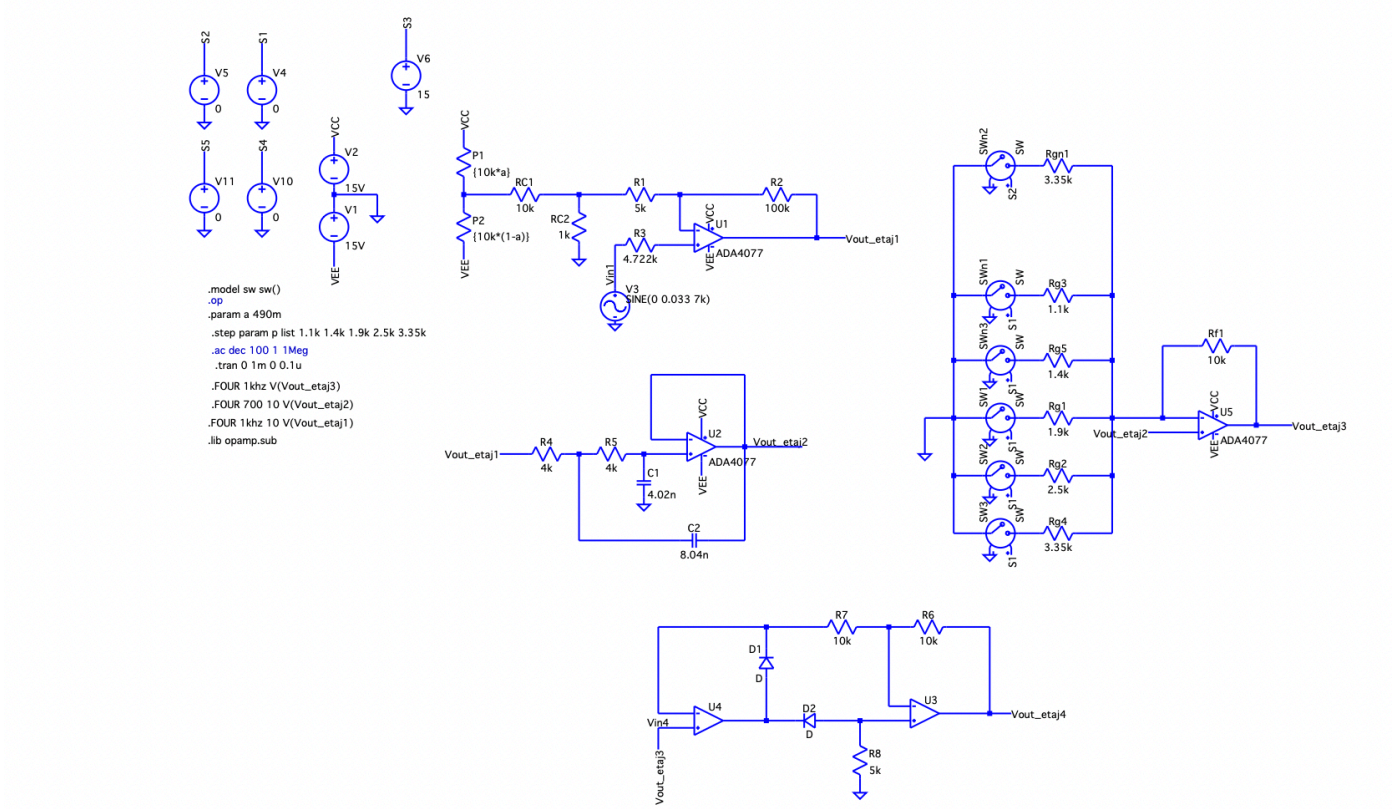


Transient analysis



AC analysis

Verification and characterization of the analog interface



CONCLUSION

Stage	1	2	3	4
Gain (measured)	17,99	1	20,1-18,2-15,9-13,9-12,02	1
Gain (specified)	18	1	20-18-16-14-12	1
BW (measured)	187kHz	7,03kHz	452-624-826kHz-1-1.66MHz	-
BW (specified)	-	7kHz	-	-

The initial three stages of the circuit demonstrate commendable performance, exhibiting the specified gains as anticipated. However, upon scrutinizing the output from the final stage, discrepancies and errors become apparent, necessitating a thorough examination and potential refinement to ensure consistent and reliable operation across all stages of the circuit.