BCS HIGHER EDUCATION QUALIFICATIONS
BCS Level 4 Certificate in IT

April 2011

EXAMINER'S REPORT

Computer & Network Technology

Overall comments

Many candidates ignored comments made in previous reports in following instructions on completing the front of the scripts. It is important for candidates to indicate which questions they attempted. Candidates failed to write the question number at the top of every page of the scripts. Centres and course providers must impress this rule on their candidates as omission of vital information causes problems during marking. The level of English was bad in some centres, hence the inability for candidates to express themselves clearly. It was also noted that some candidates used red ink. This should not happen since it conflicts with marking of scripts.

While marking scripts, it was felt that candidates did not seem to have studied the various topics well in some centres. Course providers must endeavour to explore this syllabus in depth. Computer and Network Technology is a core aspect of an IT Professional. Gaps in knowledge with regards to this area can pose serious problems in understanding more advanced and specialist IT concepts. If in doubt, course providers must seek clarification from the BCS examination's office.

In some centres, many candidates did not attempt the correct number of questions. Consequently, they were not able to score enough marks to achieve a pass grade.

Detailed questions' report

As in previous sittings, many candidates and course providers did not analyse past trends for this paper. Some elements of the paper have been examined during previous sittings. If candidates had paid attention to this, they would have been better prepared, and accordingly written good answers. It is also worth mentioning that candidates seemed to ignore the amount of marks allocated to questions in section A and B. When writing answers, candidates must carefully keep in mind that questions 1, 2, 3 and 4 carry 30 marks each. Accordingly, candidates must write sufficiently in-depth answers to attract these marks. Short answers which lack depth did not enable candidates to score well in section A.

Section A

A1. a) A computer can deal with input and output in several ways; for example, programmed I/O, DMA, and interrupt-driven I/O.

Explain what we mean by the expression *interrupt-driven I/O* used in the above statement. Your answer should include a detailed description of how a peripheral uses an interrupt (hardware exception) to request attention and how the computer deals with (services) that request. Your answer should include the role of the operating system in this process. It will be necessary to draw one or more diagrams to illustrate this activity.

(24 marks)

b) In the context of interrupt handling, what is the meaning of

i) prioritized interrupts
ii) vectored interrupts

(6 marks)

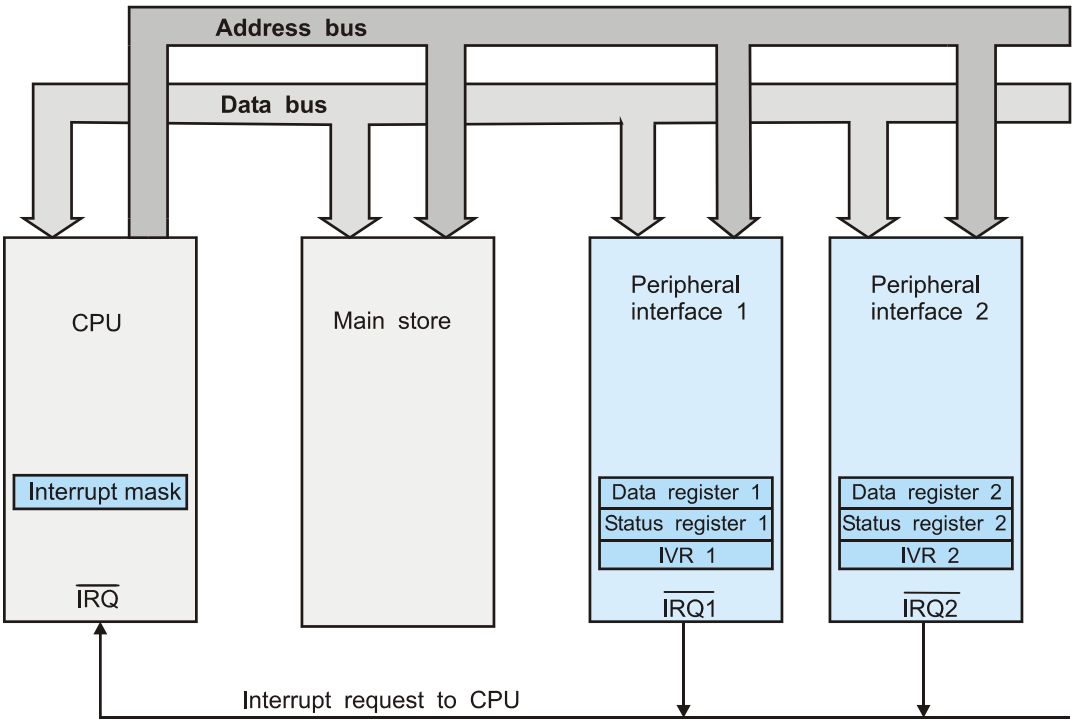
Answer Pointers

a)

Computers implement interrupt-driven in various ways. However, the basic principles are similar in all machines. About 60 to 70% of the marks should be awarded for a basic/minimal description with additional marks awarded for greater detail – especially if actual systems are described.

In a computer using interrupt-driven input/output, the computer performs tasks normally and does not carry out any explicit I/O activity as part of a program until an I/O device signals that it is ready to take part in a data exchange. That is, the I/O device initiates the I/O transaction; this is the key to interrupt-driven I/O.

The diagram below describes a simple I/O structure. The essential part is a common interrupt request line, IRQ, that connects all peripherals to the computer. When any peripheral requires attention it asserts (drives) the IRQ line and the CPU detects this event.



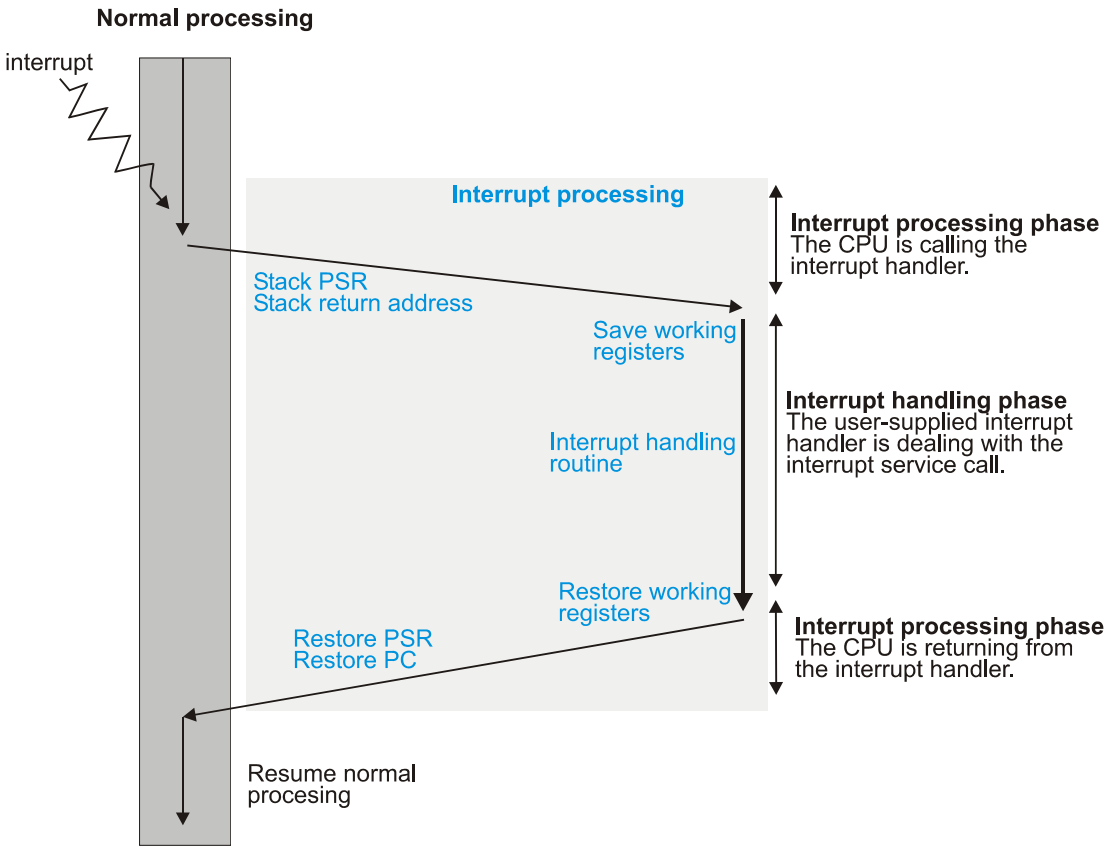
The CPU may or may not respond to an interrupt request. The request may be masked (turned off or disabled) if the CPU is busy executing a higher priority task. It is the function of the operating system to turn on and off responses to interrupts. NOTE – there are ways of assigning priority to peripherals and that is the subject of the part (b) answer. Should a candidate include prioritization in this section, appropriate credit should be given.

When the CPU responds to an interrupt, it must save the current machine context (the program counter, the processor status word and – optionally – the contents of registers). These are often saved on the system stack. The CPU then determines the cause of the interrupt (usually by polling each possible peripheral in turn by reading its interrupt status bit). When the interrupting device is located, control is passed to the appropriate interrupt handler (the operating system usually plays a role in determining the location of the interrupt handler).

After the interrupt has been processed, a return from interrupt is made and the saved registers, status word, and program counter restored. The figure below demonstrates the basic interrupt handling sequence. Note that the processor (via the operating system) must reset the state of the interrupting device to avoid a second (and infinite sequence of) interrupt when the interrupt has been serviced.

NOTE – in some modern computer systems, interrupt request lines are not used. Instead, there is a message-passing bus. In this case the peripheral transmits an interrupt request message to the CPU. A message passing bus avoids the need for separate interrupt and arbitration (etc) sub-buses.

Note that interrupts can be nested so that an interrupt can be interrupted.



b)

i. In a system with prioritized interrupts, there are more than one interrupt request lines from interrupting devices (peripherals). For example, there may be seven peripherals each with its own interrupt request line. These lines can be prioritized so that each device has its own interrupt level. Consequently, a, say, level 5 interrupt will take precedence over levels 1 to 4, and a level 6 interrupt will be able to interrupt a level 5. By prioritizing interrupt levels, it is not necessary for the operating system to poll each possible interrupter in turn. NOTE – some operating systems have complex priority arrangements; for example, a rotating priority where the current high-priority device becomes the lowest priority device – this ensured fairness.

ii. In an interrupt driven system, the processor detects an interrupt request but does not know which peripheral made the request. In a system with vectored interrupts, it then broadcasts an interrupt acknowledge to all interrupters. The device that interrupted responds by transmitting a key (interrupter number) to the processor. The operating

system uses this key to get the address (i.e., vector) of the appropriate interrupt handler. NOTE – some form of hardware prioritization is necessary to ensure that only one interrupter responds to the interrupt acknowledge.

A2. Over the past 40 years, personal computers and computers in small offices have become much more powerful and are able to store vast amount of data. An equally significant change has been the degree of connectivity between computer and peripherals and other computers.

Write an account of the way in which connectivity has changed over the past three decades and describe the basic principles and properties of some of the technologies involved. Your answer should cover both long-distance connectivity and local connectivity.

(30 marks)

Answer Pointers

This is a very open-ended question and candidates were given credit for their understanding of the issues involved. Marks were awarded for both breadth of knowledge and depth of knowledge. Any reasonable interpretation of this question was accepted.

Candidates were expected to cover long distance communications using technologies that have not changed radically over the last three decades (e.g., landlines, microwave links, fibre optics, and satellite links). Typical characteristics are:

Satellite: latency 500-700 ms point to point or 1,000-1,400ms round-trip. Bandwidth up to about 900 Mb/s for a single beam. However, for individual users, the bandwidth ranges from about 9,600 bps to about 144 kbits/s.

Microwave: Microwave links are really terrestrial versions of satellite links that use high frequency radio waves in the range 1 GHz to 30 GHz. They are point to point and line of sight. The latency is relatively small and bandwidths of the order of 150 MHz are possible.

Fibre optic link: Fibre optic links use a fine fibre of glass that transmits information at optical frequencies by exploiting the propagation of light in a tube (using total internal reflection). Fibre optic cables are relatively cheap, not line-of-sight, cannot be eavesdropped upon, have a low attenuation per mile, a low latency, and bandwidths in the Gbps range; for example, 40 Gbps links are used in some urban areas to connect communities.

The most significant change to computer/data communications in the last few decades has been at the local level from the domestic to industrial to metropolitan scales. Three decades ago long distance links often relied on modems operating across the telephone network at 1,200 bps to 9,600 pbs and 10 Mbps (expensive) Ethernets.

In the last few years, short-range data links have become pervasive with very low-cost 1 Gbps Ethernet links for both domestic and industrial use, high bandwidth fibre optic links and ADSL links (ADSL uses modified telephone technology to provide downstream data rates of 24 mbps and upstream data rates of 3.3 Mbps. Note that the link is duplex but does not have equal bandwidth in both directions).

Probably the most significant innovation in recent years is WiFi technology that provides a short range radio link to connect digital devices with each other and the Internet. WiFi is based on the IEEE 802.11 standard which has been updated over the years. Originally (1997), WiFi had a bandwidth of 20 Mbps and a data rate of 1 MHz per data stream. By 2009 the 802.11n standard was specifying data rates up to 150 Mbps per stream. The range is typically 70m indoors and up to 250m outdoors. WiFi operates in the 2.4 GHz band and (now) in the 5GHz band as well.

WiFi is associated with two issues. One is security – not all links are appropriately encoded and the other is pollution. The proliferation of WiFi enabled devices is leading to bandwidth congestion (there is only a limited range of WiFi frequencies available).

Another similar technology is Bluetooth. This is rather similar to WiFi in principle but is used for very short links such as keyboard to computer or cell phone to earpiece.

A3. A circuit has four natural binary encoded inputs D, C, B, A where D is the most-significant bit. These values represent 0 to 15 in decimal. It has a single output X.

A designer wishes to construct a logic circuit using AND, OR, and NOT gates that will provide a 1 output if the input on D, C, B, A is either less than four or in the range 10 to 12 inclusive.

a) Construct a truth table with four inputs, D, C, B, A in the range 0 0 0 0 to 1 1 1 1 and an output X.

(6 marks)

b) Using Boolean algebra write down an expression (unsimplified) for X.

(6 marks)

c) By means of Boolean algebra or a Karnaugh map write down a simplified Boolean expression for X.

(6 marks)

d) Draw a circuit using AND, OR, and NOT gates to implement the simplified Boolean expression for X.

(6 marks)

e) If each gate has a delay of 2ns (the time between the inputs being available and the corresponding output valid) what is the worst case (longest) time between inputs becoming valid and output X valid.

(6 marks)

Answer Pointers

a)

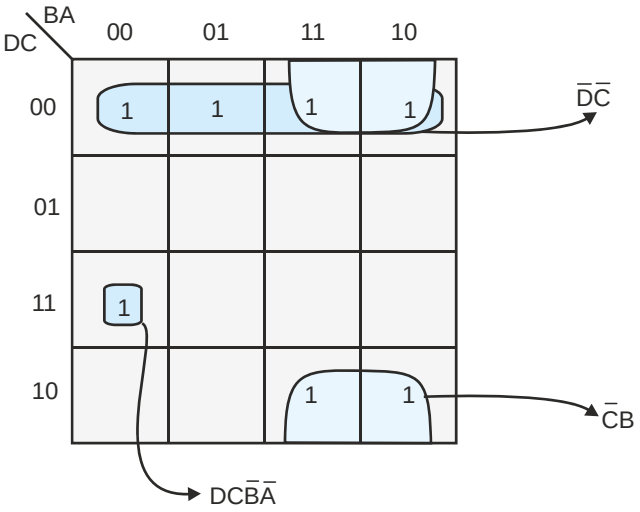
N	D	C	B	A	Less than 4	Ten to 12	F
0	0	0	0	0	1	0	1
1	0	0	0	1	1	0	1
2	0	0	1	0	1	0	1
3	0	0	1	1	1	0	1
4	0	1	0	0	0	0	0
5	0	1	0	1	0	0	0
6	0	1	1	0	0	0	0
7	0	1	1	1	0	0	0
8	1	0	0	0	0	0	0
9	1	0	0	1	0	0	0
10	1	0	1	0	0	1	1
11	1	0	1	1	0	1	1
12	1	1	0	0	0	1	1
13	1	1	0	1	0	0	0
14	1	1	1	0	0	0	0
15	1	1	1	1	0	0	0

b)

F = D!.C!.B!.A! + D!.C!.B!.A + D!.C!.B.A! + D!.C!.B.A + D.C!.B.A! + D.C!.B.A + D.C.B!.A!

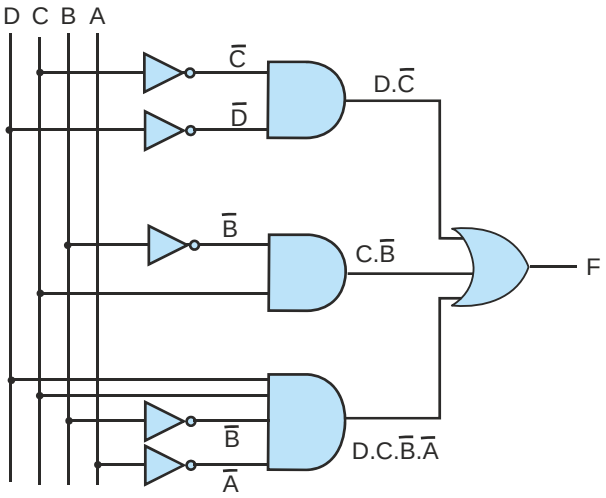
(note use of A! to indicate NOT A)

c)



The function is F = D!.C! + C!.B + D.C.B!.A!

d)



e)

The longest delay path is three gates (invertor, AND, OR) in series = 3 x 2 = 6 ns.

A4. a) With the aid of diagrams draw the structure of a computer at the level of registers, buses and functional units and explain the sequence of actions that take place when an instruction is read from memory and executed.

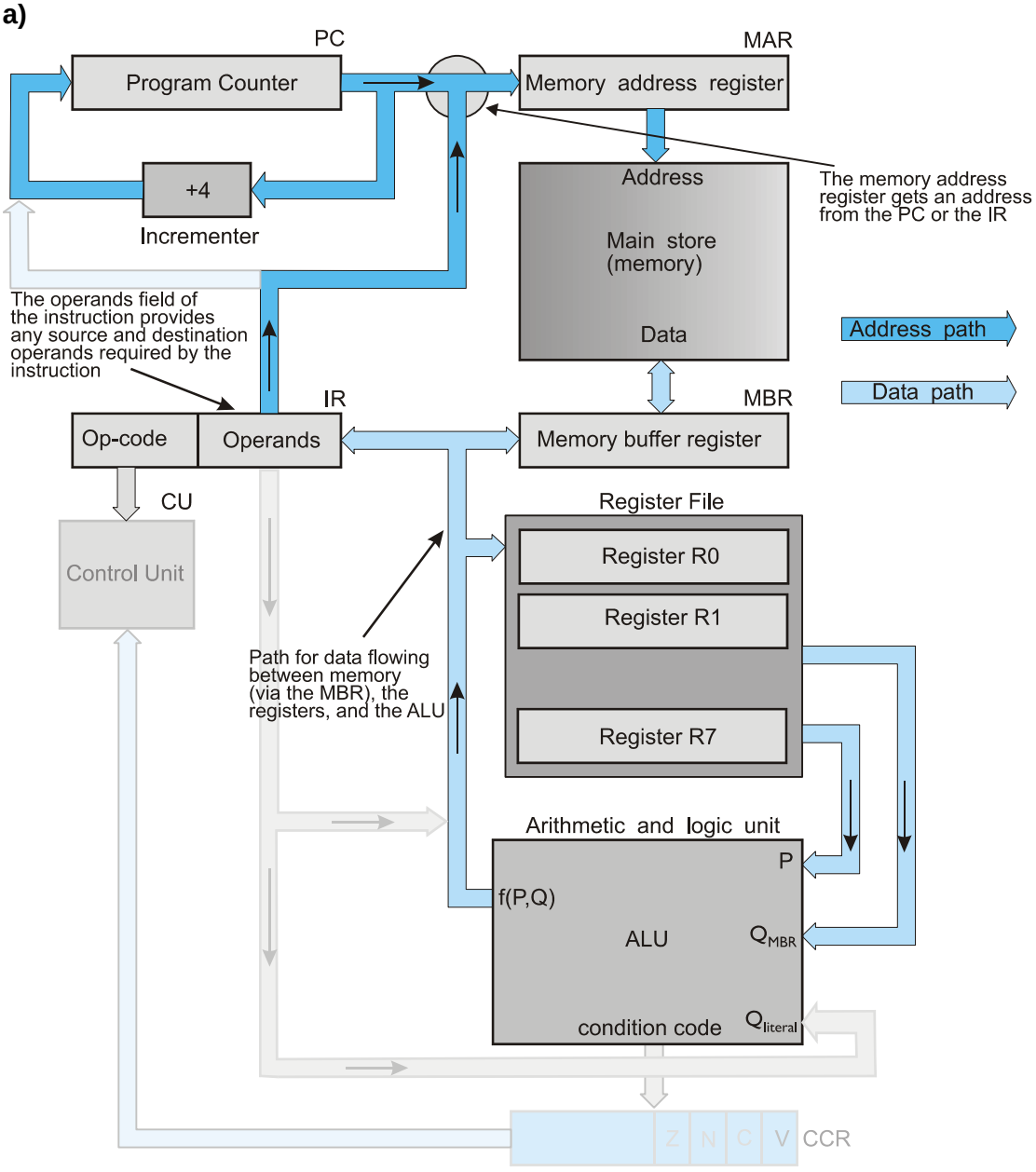
(22 marks)

b) Computers (microprocessors) are often described as being RISC or CISC; for example, Intel's Pentium and core i7 computers are broadly CISC machines and ARM, the PowerPC, MIPS and SPARC are RISC machines.

Briefly explain the difference between RISC and CISC machines and describe the fundamental characteristic of each machine.

(8 marks)

a)



A computer consists of a number of registers that each hold a word, buses that connect registers, and an ALU (arithmetic logic unit) that performs operations on data. Note that the term execution unit is often used today rather than ALU.

Candidates needed to explain the nature of the fetch/execute cycle in order to gain a pass mark.

Initially, at the start of an instruction, the program counter contains the address in memory of the next instruction to be executed. The program counter, PC, points at the next instruction.

The contents of the PC are fed to a memory address register, MAR, where it is held while the actual instruction is read from memory to get its op-code. At the same time the contents of the program counter are incremented to point at the next instruction.

NOTE: In the diagram the program counter is shown as being incremented by 4 because it is assumed that instructions are 32 bits or 4 bytes. In a CISC processor, the program counter is incremented by the size of the instruction in bytes – this may be from 2 to 10. Candidates are not required to know this, but credit was given if a candidate pointed this out.

The instruction from memory is fed to the instruction register where it is held while it is decoded. The sequence of operations so far are:

[MAR] ← [PC]
[PC] ← [PC] + 4
[IR] ← [M[MAR]]

This corresponds to the fetch cycle and is the same for each instruction.

When the instruction is decoded, the control unit generates the operation necessary to implement the current instruction. For example, if it is ADD R1,mem which means add the contents of memory location 'mem' to register R1, the operation [R1] ← [R1] + [M[IR]] is executed.

Computers can perform conditional operations (IF THEN ELSE) which appear as conditional branches (e.g., BEQ abc) at the machine level. These are implemented by testing the output of the ALU (for zero, not zero, carry, overflow etc) and using the result of that test (true or false) to either load the program counter with the next address in sequence (the default case) or whether to load the PC with a branch address from the operand field of the IR.

b)

The terms RISC and CISC once implied two different classes of computer. Today, many of the characteristics of RISC machines have been incorporated in CISC architectures like Intel's Pentium and iCore machines. However, there are specific features associated with RISC and CISC technologies.

The CISC concept was only formalized after the introduction of RISC processors in the 1980s. CISC machines are Intel's 8-bit processors, '386, '486, Intel's Pentium and later members of the IA32 family – as well as the Motorola 68K family. They are characterised by having so called complex instruction sets with a memory to register format (e.g. ADD D1,Mem or ADD Mem,D1). They also tend to support complex memory addressing modes. Instructions are of variable size – for example the 68K has instruction sizes ranging from 2 to 10 bytes. They also generally have relatively small register sets and often several special purpose registers.

The key feature of the RISC (reduced instruction set computer) is that it has a regular instruction size – typically four bytes/ 32 bits. This means that all instructions are the same size and therefore it is possible to read instructions ahead of processing (difficult with CISC instructions as they are of different sizes). RISC machines are called load/store machines because they support only two memory operations LOAD register and STORE register.

RISC processors use pipelined execution; that is, execution is split into four or more phases (fetch instruction, decode it, fetch operand, execute instruction, store result). This means that four (or more) instructions may be being executed at the same time. A RISC processor with n stages can, at best, execute instructions n times faster than a non-pipelined equivalent. Note that branch/jump instructions degrade RISC performance and that RISC pipelining techniques are applied to all modern CISC processors.

Section B

B5. a) Explain why it is necessary to use a data communications protocol to control a data link.

(6 marks)

b) What role does TCP play in a data transmission system?

(6 marks)

Answer Pointers

a) A data communications protocol is used to establish standardised agreement/rules between computer devices for the purpose of data transmission.

b) TCP is a transport layer protocol used by applications that require guaranteed delivery. It is a sliding window protocol that provides handling for both timeouts and retransmissions.

B6. a) Describe the factors that need to be considered as to whether to use a laser or an ink jet printer.

(6 marks)

b) Explain the operation of a laser printer.

(6 marks)

Answer Pointers

a) Factors include volume of print to be produced, speed of printing, running costs

b) A brief explanation of how the laser printer uses laser beam and a ‘toner’ type of ink to produce output was expected.

B7. With reference to computer security, explain each of the terms below:

a) Firewall

(6 marks)

b) Data Encryption

(6 marks)

Answer Pointers

a) A combination of hardware, software and security mechanisms to restrict the flow of information in and out of a computer system.

b) The translation of data into a secret code before transmission. The receiving computer must be able to decrypt the data transmitted.

B8. Wireless computing (Wi-Fi) has changed the way people use computers and associated devices.

a) Using Wi-Fi as an example, describe how wireless computing operates.

(8 marks)

b) Give four examples of typical devices that make use of Wi-Fi

(4 marks)

Answer Pointers

a) Wi-Fi – wireless network which uses radio waves to provide wireless high speed internet and network communication. The Wi-Fi alliance uses network standards such as 802.11 for network communication.

b) Laptop computers, PDA, wireless printer, mobile phone (not proprietary devices such as Iphone or Blackberry).

B9. a) Explain the importance of IP addressing in computer networks.

(6 marks)

b) What are the differences between an intranet and an extranet?

(6 marks)

Answer Pointers

a) An identifier for a device on a TCP/IP network. Networks using the TCP/IP protocol route messages based on the IP address of the destination. The format of an IP address is a 32-bit numeric address written as four numbers separated by periods. Each number can be zero to 255. For example, 1.160.10.240 could be an IP address. IP addressing enable devices in a network to interconnect to each other so that data can be transmitted.

b) An intranet is a network based on TCP/IP protocols (an internet) which belongs to an organisation. The intranet is used to share information between users internally. An extranet on the other hand is practically an intranet but which is partially accessible to authorised users from outside the organisation.

B10. Explain the terms below as applied to operating systems.

a) Multi user

(3 marks)

b) Multi tasking

(3 marks)

c) Multi processing

(3 marks)

d) Real Time

(3 marks)

Answer Pointers

a) Two or more users simultaneously using a computer system

b) Several tasks which are handled by the computer system at the same time

c) More than one process/program running at the same time

d) An operation which takes place and produces immediate results/output.

B11. There has been considerable development in the way computer networks are set up and used. One area which has become popular is *cloud computing*. Briefly describe *cloud computing*. Using suitable examples, explain potential uses of cloud computing.

(12 marks)

Answer Pointers

Cloud computing is based on the use of large group of servers to handle information technology resources. Users are able to use massive data centres and systems found in different locations. With the widespread use of the internet and associated technology, organizations are making use of cloud computing to share information and resources in business.

B12. Briefly, explain the following processor related terms.

a) Logic gate

(4 marks)

b) Memory Address Register

(4 marks)

c) Bus

(4 marks)

Answer Pointers

a) A type of electronic circuit which is used in computing to regulate the flow of electricity. This forms the basis of the Boolean logic operations in computers.

b) A register which is used to store the memory address from which data will be fetched from the CPU.

c) A set of wires which are used to carry data from one side of the computer to the other. The bus provides a very important medium of data transfer in computing.