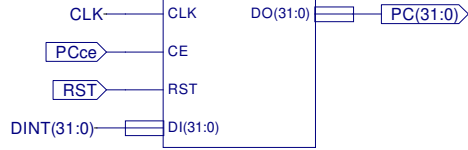


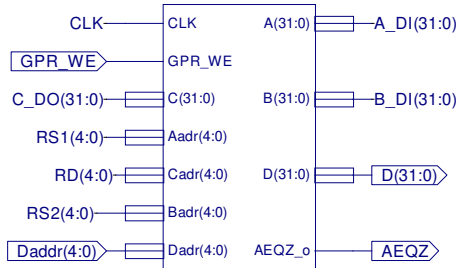
## Reg\_C REG32CE



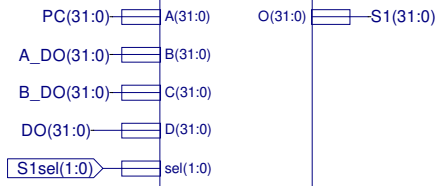
## PC Reg REG32RST



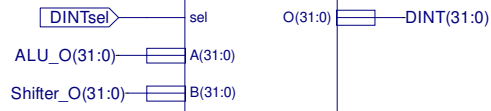
## GPR\_env



## S1 MUX MUX4\_32bit



## DINT MUX MUX32bit



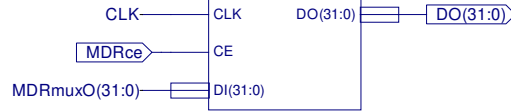
## A MUX MUX32bit



## MDR MUX MUX32bit



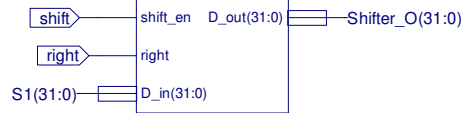
## MDR REG32CE



## Reg\_A REG32CE



## shifter



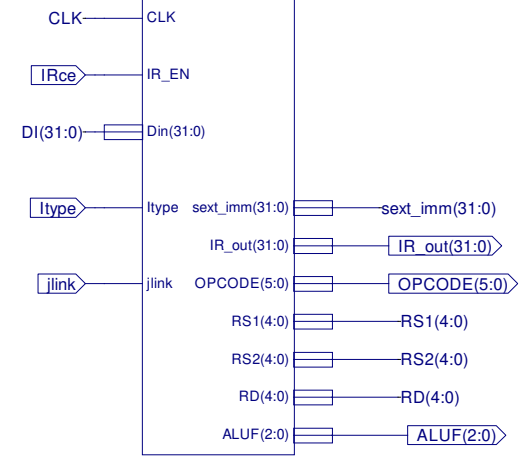
## MAR REG32CE



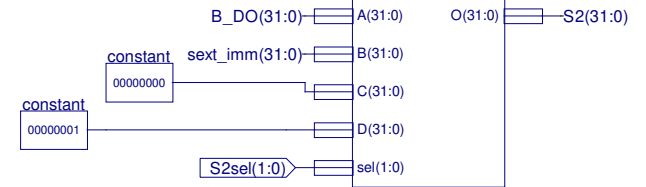
## 8 MSB to Zero DLX\_MMU



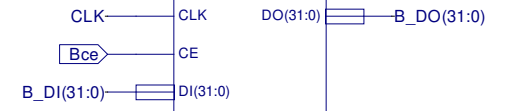
## IRenv



## S2 MUX MUX4\_32bit



## Reg B REG32CE



## DLX\_ALU

