CS311 - Computer Architecture Lab

Assignment 6 - Report

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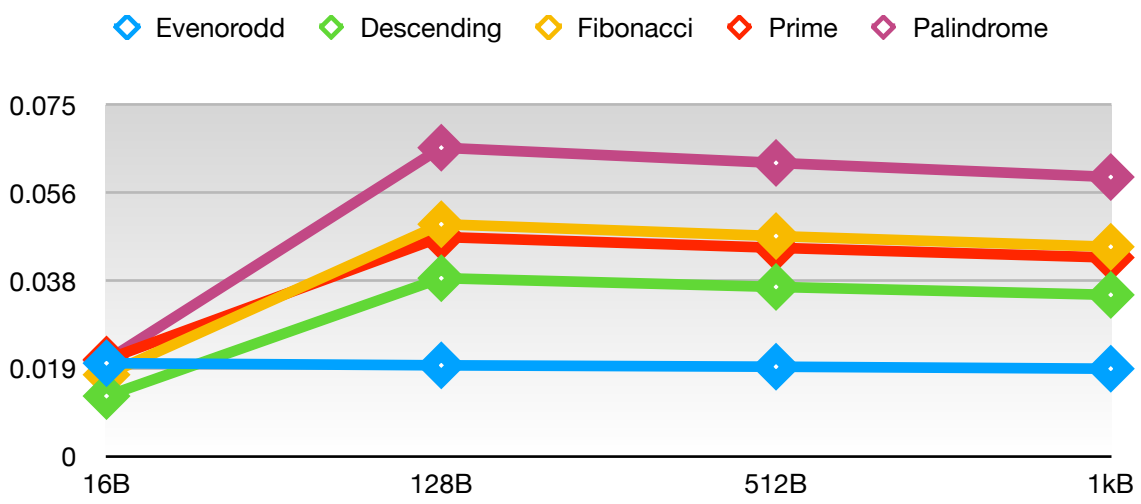
1. **Problem 1:** When L1i-cache is changed.

L1d=1kB	Evenorodd	Descending	Fibonacci	Prime	Palindrome
No. of instructions	5	188	67	28	47
	16 B				
Cycles	252	13741	3858	1358	2302
IPC	0.01984127	0.012808383	0.017366512	0.020618556	0.020417029
	128B				
Cycles	258	4945	1352	598	713
IPC	0.019379845	0.0380182	0.049556214	0.04682274	0.065918654
	512B				
Cycles	262	5201	1425	629	750
IPC	0.01908397	0.036146894	0.047017545	0.044515103	0.06266667
	1kB				
Cycles	268	5458	1498	660	788
IPC	0.018656716	0.03444485	0.0447263	0.042424243	0.05964467



2. **Problem 2:** When L1d-cache is changed.

L1i=1kB	Evenorodd	Descending	Fibonacci	Prime	Palindrome
No. of instructions	5	188	67	28	47
	16 B				
Cycles	268	5458	1498	660	788
IPC	0.018656716	0.03444485	0.0447263	0.042424243	0.05964467
	128B				
Cycles	268	5458	1498	660	788
IPC	0.018656716	0.03444485	0.0447263	0.042424243	0.05964467
	512B				
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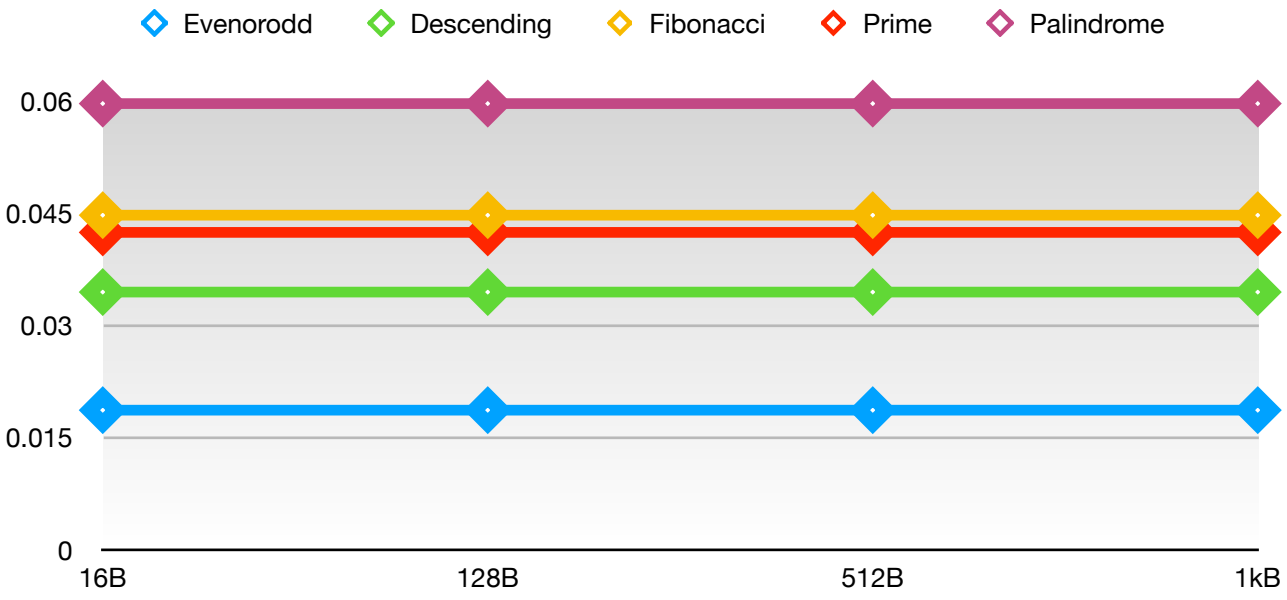

3. Problem 3:

When CacheLd is constant and CacheLi is varying, Evenorodd.asm has no loops, and hence the IPC decreases on increase of cache size (since it increases latency also). For the remaining benchmarks, the IPC changes based on the number of loops in the benchmark.
When CacheLi is constant and CacheLd is varying, all benchmarks except descending.asm have constant IPC. This is because descending.asm has multiple instances of writing and reading from main memory whereas the other benchmarks do not.

4. Problem 4:

We have chosen descending.asm as the benchmark. When L1-i cache is changed from 16B to 128B, the hit rate goes above
As cache size increases, hit rate increases as expected and then becomes constant as enough cache is present for the program.

5. Problem 5:

We have chosen descending.asm as the benchmark. When L1-d cache is changed from 16B to 128B, the hit rate above.
As the cache size increases, here the hit rate remains constant as the number of memory accesses are less.