



**FUNDAÇÃO EDSON QUEIROZ**  
**UNIVERSIDADE DE FORTALEZA**  
ENSINANDO E APRENDENDO

# Aula 13

## Módulos de Suporte a CPU

**Microcontroladores PIC18 – Programação em C**



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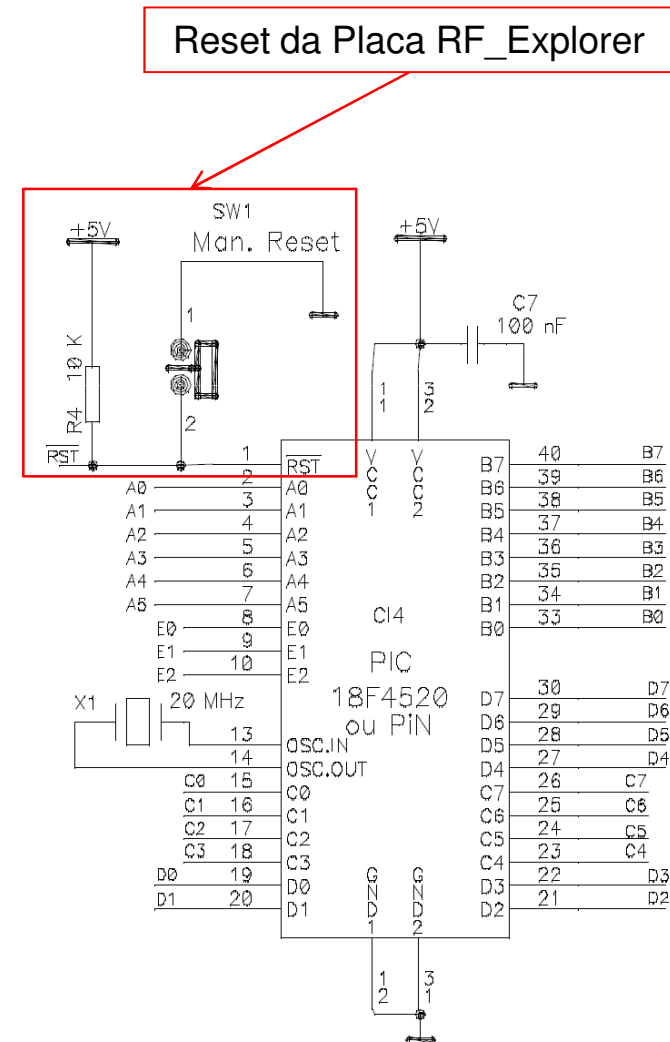
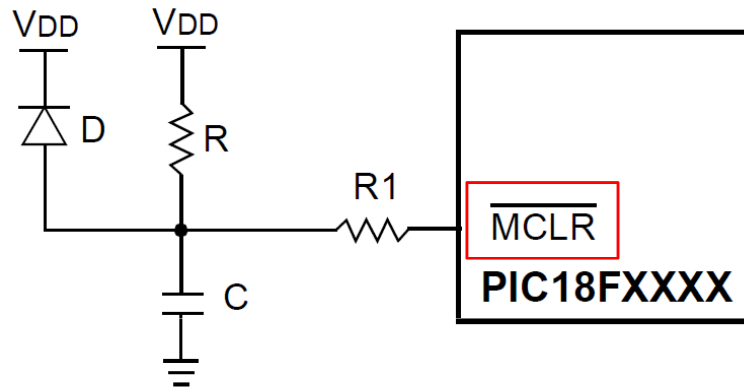
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# Sistema de Reset

- ❑ O sistema de reset dos PIC18F4520 é responsável por **iniciar a CPU** e **periféricos** em um estado predefinido após um dos seguintes eventos:
  1. **Botão de Reset** durante a operação normal (**MCLR**);
  2. **Alimentação Inicial do chip** (*Power-on reset* ou **POR**);
  3. **Timer de Inicialização** (Power-up timer ou **PWRT / PUT**);
  4. **Timer de partida do oscilador** (*Oscillator start-up timer* ou **OST**);
  5. **Queda de alimentação** (*Brown-out reset* ou **BOR**);
  6. **Reset** provocado pelo watchdog (**WDT**);
  7. **Reset por software** via instrução RESET;

# 1. Master Clear (MCLR)



## 6. Registradores do Watchdog

### REGISTRADORES DE CONFIGURAÇÃO

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	00-- 0111
300002h CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	PWRTEN	---1 1111
300003h CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	---1 1111
300005h CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX	1--- -011
300006h CONFIG4L	DEBUG	XINST	—	—	—	LVP	—	STVREN	10-- -1-1
300008h CONFIG5L	—	—	—	—	CP3 <sup>(1)</sup>	CP2 <sup>(1)</sup>	CP1	CP0	---- 1111
300009h CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah CONFIG6L	—	—	—	—	WRT3 <sup>(1)</sup>	WRT2 <sup>(1)</sup>	WRT1	WRT0	---- 1111
30000Bh CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch CONFIG7L	—	—	—	—	EBTR3 <sup>(1)</sup>	EBTR2 <sup>(1)</sup>	EBTR1	EBTR0	---- 1111
30000Dh CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(2)</sup>
3FFFFFh DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(2)</sup>

R/P-1	U-0	U-0	U-0	U-0	R/P-0	R/P-1	R/P-1
MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX
bit 7							bit 0

bit 7

**MCLRE:** MCLR Pin Enable bit

1 = MCLR pin enabled; RE3 input pin disabled

0 = RE3 input pin enabled; MCLR disabled

## 2. Power-on Reset (POR)

- Circuito interno ao PIC que o mantém em reset até que VDD alcance tensão suficiente quando a tensão de alimentação é ligada;
- A tensão deve alcançar algo em torno de 1,2V - 1,7V;
- Serve para o PIC funcionar corretamente;
- Não possui um registrador de configuração;

### 3. Power-up Timer (PWRT ou PUT)

- Temporizador que mantém em **reset** o PIC por **72 ms após a alimentação** ser ligada;
- Permite que a tensão da fonte se **estabilize**;
- Também permite que o oscilador principal estabilize antes que o PIC entre em funcionamento;
- É ativado pelo bit de configuração “Power Up Timer”;
- É uma proteção adicional ao POR, evitando travamentos já na inicialização;

### 3. Registradores do PWRT

#### REGISTRADORES DE CONFIGURAÇÃO

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	00-- 0111
300002h CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	PWRTEN	---1 1111
300003h CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	---1 1111
300005h CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX	1--- -011
300006h CONFIG4L	DEBUG	XINST	—	—	—	LVP	—	STVREN	10-- -1-1
300008h CONFIG5L	—	—	—	—	CP3 <sup>(1)</sup>	CP2 <sup>(1)</sup>	CP1	CP0	---- 1111
300009h CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah CONFIG6L	—	—	—	—	WRT3 <sup>(1)</sup>	WRT2 <sup>(1)</sup>	WRT1	WRT0	---- 1111
30000Bh CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch CONFIG7L	—	—	—	—	EBTR3 <sup>(1)</sup>	EBTR2 <sup>(1)</sup>	EBTR1	EBTR0	---- 1111
30000Dh CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(2)</sup>
3FFFFFh DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(2)</sup>

U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	BORV1 <sup>(1)</sup>	BORV0 <sup>(1)</sup>	BOREN1 <sup>(2)</sup>	BOREN0 <sup>(2)</sup>	PWRTEN <sup>(2)</sup>
bit 7							bit 0

bit 0

**PWRTEN:** Power-up Timer Enable bit<sup>(2)</sup>

1 = PWRT disabled

0 = PWRT enabled

## 4. OST

- Mantém o PIC resetado até que 1024 ciclos do oscilador ocorram depois do PUT
- Assegura que o cristal ou ressonador tenha iniciado e estabilizado



## 4. Registradores do OST

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### REGISTRADORES DE CONFIGURAÇÃO

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	00-- 0111
300002h	CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	PWRTEN	---1 1111
300003h	CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	---1 1111
300005h	CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX	1--- -011
300006h	CONFIG4L	DEBUG	XINST	—	—	—	LVP	—	STVREN	10-- -1-1
300008h	CONFIG5L	—	—	—	—	CP3 <sup>(1)</sup>	CP2 <sup>(1)</sup>	CP1	CP0	---- 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	—	—	—	—	WRT3 <sup>(1)</sup>	WRT2 <sup>(1)</sup>	WRT1	WRT0	---- 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	—	—	—	—	EBTR3 <sup>(1)</sup>	EBTR2 <sup>(1)</sup>	EBTR1	EBTR0	---- 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(2)</sup>
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(2)</sup>

## 4. Registradores do OST

### REGISTRADORES DE CONFIGURAÇÃO

R/P-0	R/P-0	U-0	U-0	R/P-0	R/P-1	R/P-1	R/P-1
IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 7      **IESO:** Internal/External Oscillator Switchover bit

1 = Oscillator Switchover mode enabled

0 = Oscillator Switchover mode disabled

bit 6      **FCMEN:** Fail-Safe Clock Monitor Enable bit

1 = Fail-Safe Clock Monitor enabled

0 = Fail-Safe Clock Monitor disabled

bit 5-4      **Unimplemented:** Read as '0'

bit 3-0      **FOSC<3:0>:** Oscillator Selection bits

11xx = External RC oscillator, CLKO function on RA6

101x = External RC oscillator, CLKO function on RA6

1001 = Internal oscillator block, CLKO function on RA6; port function on RA7

1000 = Internal oscillator block, port function on RA6 and RA7

0111 = External RC oscillator, port function on RA6

0110 = HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)

0101 = EC oscillator, port function on RA6

0100 = EC oscillator, CLKO function on RA6

0011 = External RC oscillator, CLKO function on RA6

0010 = HS oscillator

0001 = XT oscillator

0000 = LP oscillator

## 4. Registradores do OST

### REGISTRADORES DE CONFIGURAÇÃO

R/P-1	U-0	U-0	U-0	U-0	R/P-0	R/P-1	R/P-1
MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX
bit 7							bit 0

bit 2

**LPT1OSC:** Low-Power Timer1 Oscillator Enable bit

1 = Timer1 configured for low-power operation

0 = Timer1 configured for higher power operation

## 5. BOR

- Reseta o PIC quando a tensão de alimentação cai abaixo de **4V por aproximadamente 100us**;
- Quando a tensão de alimentação volta ao valor nominal, o BOR permite o PIC seja reiniciado;
- É ativado pelo bit de configuração “Brown Out Detect”
- Circuito de proteção onde a queda de tensão de alimentação é comum, evitando travamentos;

## 5. Registradores do BOR / BOREN

### REGISTRADORES DE CONFIGURAÇÃO

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	00-- 0111
300002h	CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	PWRTEN	---1 1111
300003h	CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	---1 1111
300005h	CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX	1--- -011
300006h	CONFIG4L	DEBUG	XINST	—	—	—	LVP	—	STVREN	10-- -1-1
300008h	CONFIG5L	—	—	—	—	CP3 <sup>(1)</sup>	CP2 <sup>(1)</sup>	CP1	CP0	---- 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	—	—	—	—	WRT3 <sup>(1)</sup>	WRT2 <sup>(1)</sup>	WRT1	WRT0	---- 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	—	—	—	—	EBTR3 <sup>(1)</sup>	EBTR2 <sup>(1)</sup>	EBTR1	EBTR0	---- 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(2)</sup>
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(2)</sup>

BOR Configuration		Status of SBOREN (RCON<6>)	BOR Operation
BOREN1	BOREN0		
0	0	Unavailable	BOR disabled; must be enabled by reprogramming the Configuration bits.
0	1	Available	BOR enabled in software; operation controlled by SBOREN.
1	0	Unavailable	BOR enabled in hardware in Run and Idle modes, disabled during Sleep mode.
1	1	Unavailable	BOR enabled in hardware; must be disabled by reprogramming the Configuration bits.

## 6. Watcdog (WDT)

- Sua função é **proteger** o sistema contra possíveis **travamentos**, fazendo com que o sistema reinicie e volta a funcionar;
- Circuito **temporizador** acionado por um oscilador próprio;
- Quando ocorre o timeout (estouro), provoca um **reset** no programa se o PIC estiver no modo normal;
- WDT deve ser **zerado** antes do timeout, senão o sistema reiniciará;
- Em modo sleep provoca um **wake-up**;
- É ativado pelo bit de configuração **“Watchdog Timer - WDT”**

## 6. Registradores do Watchdog

### REGISTRADORES DE CONFIGURAÇÃO

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	00-- 0111
300002h	CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	PWRTEN	---1 1111
300003h	CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	---1 1111
300005h	CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX	1--- -011
300006h	CONFIG4L	DEBUG	XINST	—	—	—	LVP	—	STVREN	10-- -1-1
300008h	CONFIG5L	—	—	—	—	CP3 <sup>(1)</sup>	CP2 <sup>(1)</sup>	CP1	CP0	---- 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	—	—	—	—	WRT3 <sup>(1)</sup>	WRT2 <sup>(1)</sup>	WRT1	WRT0	---- 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	—	—	—	—	EBTR3 <sup>(1)</sup>	EBTR2 <sup>(1)</sup>	EBTR1	EBTR0	---- 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(2)</sup>
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(2)</sup>



## 6. Registradores do Watchdog

U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN
bit 7			bit 0				

Pode ser configurado um fator de prescaler, para variar o timeout entre **4 ms a 131.072s (2.18 minutos)**, como mostrado na tabela ao lado:

bit 7-5

bit 4-1

**Unimplemented:** Read as '0'**WDTPS<3:0>:** Watchdog Timer Postscale Select bits

1111 = 1:32,768

1110 = 1:16,384

1101 = 1:8,192

1100 = 1:4,096

1011 = 1:2,048

1010 = 1:1,024

1001 = 1:512

1000 = 1:256

0111 = 1:128

0110 = 1:64

0101 = 1:32

0100 = 1:16

0011 = 1:8

0010 = 1:4

0001 = 1:2

0000 = 1:1

bit 0

**WDTEN:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled (control is placed on the SWDTEN bit)

# Sistema de Reset

- ❑ Os eventos anteriores provocam a reinicialização geral da CPU e dos periféricos para a seguinte condição:
  1. **CPU:** o registrador é carregado com o valor 0x000000 e a execução do programa tem início a partir deste endereço;
  2. **Portas de E/S:** todos os pinos são configurados como entrada (TRISx = 0xFF, exeto TRISE que inicializado com 0x07);
  3. **Timers:** *timer* 0 inicia operando, os demais *timers* são desativados;
  4. **ADC:** desativado, pinos de entrada no modo analógico;
  5. **Comparadores Analógicos:** desativados, pinos de entrada no modo analógico;
  6. **Demais periféricos:** desativados;

# Registadores SFR de Reset

FFFh	TOSU	FDFh	INDF2 <sup>(1)</sup>	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2 <sup>(1)</sup>	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2 <sup>(1)</sup>	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2 <sup>(1)</sup>	FBCh	CCPR2H	F9Ch	— <sup>(2)</sup>
FFBh	PCLATU	FDBh	PLUSW2 <sup>(1)</sup>	FBHh	CCPR2L	F9Bh	OSCTUNE
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	— <sup>(2)</sup>
FF9h	PCL	FD9h	FSR2L	FB9h	— <sup>(2)</sup>	F99h	— <sup>(2)</sup>
FF8h	TBLPTRU	FD8h	STATUS	FB8h	BAUDCON	F98h	— <sup>(2)</sup>
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	PWM1CON <sup>(3)</sup>	F97h	— <sup>(2)</sup>
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	ECCP1AS <sup>(3)</sup>	F96h	TRISE <sup>(3)</sup>
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD <sup>(3)</sup>
FF4h	PRODH	FD4h	— <sup>(2)</sup>	FB4h	CMCON	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	HLVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	— <sup>(2)</sup>
FF0h	INTCON3	FD0h	RCON	FB0h	SPBRGH	F90h	— <sup>(2)</sup>
FEFh	INDF0 <sup>(1)</sup>	FCFh	TMR1H	FAFh	SPBRG	F8Fh	— <sup>(2)</sup>
FEeh	POSTINC0 <sup>(1)</sup>	FCEh	TMR1L	FAEh	RCREG	F8Eh	— <sup>(2)</sup>
FEDh	POSTDEC0 <sup>(1)</sup>	FCDh	T1CON	FADh	TXREG	F8Dh	LATE <sup>(3)</sup>
FECh	PREINC0 <sup>(1)</sup>	FCCh	TMR2	FACH	TXSTA	F8Ch	LATD <sup>(3)</sup>
FEBh	PLUSW0 <sup>(1)</sup>	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	— <sup>(2)</sup>	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	— <sup>(2)</sup>
FE7h	INDF1 <sup>(1)</sup>	FC7h	SSPSTAT	FA7h	EECON2 <sup>(1)</sup>	F87h	— <sup>(2)</sup>
FE6h	POSTINC1 <sup>(1)</sup>	FC6h	SSPCON1	FA6h	EECON1	F86h	— <sup>(2)</sup>
FE5h	POSTDEC1 <sup>(1)</sup>	FC5h	SSPCON2	FA5h	— <sup>(2)</sup>	F85h	— <sup>(2)</sup>
FE4h	PREINC1 <sup>(1)</sup>	FC4h	ADRESH	FA4h	— <sup>(2)</sup>	F84h	PORTE <sup>(3)</sup>
FE3h	PLUSW1 <sup>(1)</sup>	FC3h	ADRESL	FA3h	— <sup>(2)</sup>	F83h	PORTD <sup>(3)</sup>
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA

# Registadores SFR de Reset: RCON

R/W-0	R/W-1 <sup>(1)</sup>	U-0	R/W-1	R-1	R-1	R/W-0 <sup>(2)</sup>	R/W-0
IPEN	SBOREN	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7	0	1					bit 0

Após o Reset

As interrupções são desabilitadas e as prioridades são configuradas como altas;

Os flags em RCON permitem detectar a origem do evento do reset e tomar providências necessárias.

Indicador de reset por inicialização (POR, PWRT e OST)

**IPEN:** Interrupt Priority Enable bit

1 = Enable priority levels on interrupts  
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

**SBOREN:** BOR Software Enable bit<sup>(1)</sup>

If BOREN1:BOREN0 = 01:

1 = BOR is enabled

0 = BOR is disabled

If BOREN1:BOREN0 = 00, 10 or 11:

Bit is disabled and read as '0'.

**Unimplemented:** Read as '0'

**$\overline{RI}$ :** RESET Instruction Flag bit

1 = The RESET instruction was not executed (set by firmware only)

0 = The RESET instruction was executed causing a device Reset (must be set in software after Brown-out Reset occurs)

**$\overline{TO}$ :** Watchdog Time-out Flag bit

1 = Set by power-up, CLRWDI instruction or SLEEP instruction

0 = A WDT time-out occurred

**$\overline{PD}$ :** Power-Down Detection Flag bit

1 = Set by power-up or by the CLRWDI instruction

0 = Set by execution of the SLEEP instruction

**$\overline{POR}$ :** Power-on Reset Status bit

1 = A Power-on Reset has not occurred (set by firmware only)

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

**$\overline{BOR}$ :** Brown-out Reset Status bit

1 = A Brown-out Reset has not occurred (set by firmware only)

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

**RI, POR e BOR** devem ser setados por software em "1".

# FSRs Watchdog: WDTCON e RCON

## WDTCON

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SWDTEN <sup>(1)</sup>
bit 7							bit 0

bit 7-1

**Unimplemented:** Read as '0'

bit 0

**SWDTEN:** Software Controlled Watchdog Timer Enable bit<sup>(1)</sup>

1 = Watchdog Timer is on

0 = Watchdog Timer is off

## RCON

R/W-0	R/W-1 <sup>(1)</sup>	U-0	R/W-1	R-1	R-1	R/W-0 <sup>(2)</sup>	R/W-0
IPEN	SBOREN	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 3

 $\overline{TO}$ : Watchdog Time-out Flag bit

1 = Set by power-up, CLRWDT instruction or SLEEP instruction

0 = A WDT time-out occurred

# FSRs OST: OSCCON

## OSCCON

R/W-0	R/W-1	R/W-0	R/W-0	R <sup>(1)</sup>	R-0	R/W-0	R/W-0
IDLEN	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0
bit 7							bit 0

bit 7 **IDLEN:** Idle Enable bit

- 1 = Device enters an Idle mode on *SLEEP* instruction
- 0 = Device enters Sleep mode on *SLEEP* instruction

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits

- 111 = 8 MHz (INTOSC drives clock directly)
- 110 = 4 MHz
- 101 = 2 MHz
- 100 = 1 MHz<sup>(3)</sup>
- 011 = 500 kHz
- 010 = 250 kHz
- 001 = 125 kHz
- 000 = 31 kHz (from either INTOSC/256 or INTRC directly)<sup>(2)</sup>

bit 3 **OSTS:** Oscillator Start-up Timer Time-out Status bit<sup>(1)</sup>

- 1 = Oscillator Start-up Timer (OST) time-out has expired; primary oscillator is running
- 0 = Oscillator Start-up Timer (OST) time-out is running; primary oscillator is not ready

bit 2 **IOFS:** INTOSC Frequency Stable bit

- 1 = INTOSC frequency is stable
- 0 = INTOSC frequency is not stable

bit 1-0 **SCS<1:0>:** System Clock Select bits

- 1x = Internal oscillator block
- 01 = Secondary (Timer1) oscillator
- 00 = Primary oscillator

FSRs OST: OSCTUNE

# OSCTUNE

R/W-0	R/W-0 <sup>(1)</sup>	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTSRC	PLLEN <sup>(1)</sup>	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7			bit 0				

**bit 7**      **INTSRC:** Internal Oscillator Low-Frequency Source Select bit  
               1 = 31.25 kHz device clock derived from 8 MHz INTOSC source (divide-by-256 enabled)  
               0 = 31 kHz device clock derived directly from INTRC internal oscillator

**bit 6**      **PLEN:** Frequency Multiplier PLL for INTOSC Enable bit<sup>(1)</sup>  
               1 = PLL enabled for INTOSC (4 MHz and 8 MHz only)  
               0 = PLL disabled

**bit 5**      **Unimplemented:** Read as ‘0’

**bit 4-0**     **TUN<4:0>:** Frequency Tuning bits  
               011111 = Maximum frequency  
               •                          •  
               •                          •  
               000001  
               000000 = Center frequency. Oscillator module is running at the calibrated frequency.  
               111111  
               •                          •  
               •                          •  
               100000 = Minimum frequency

# FSRs OST: T1CON

## T1CON

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	<b>T1RUN</b>	T1CKPS1	T1CKPS0	<b>T1OSCEN</b>	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **RD16:** 16-Bit Read/Write Mode Enable bit  
 1 = Enables register read/write of Timer1 in one 16-bit operation  
 0 = Enables register read/write of Timer1 in two 8-bit operations

bit 6 **T1RUN:** Timer1 System Clock Status bit  
 1 = Device clock is derived from Timer1 oscillator  
 0 = Device clock is derived from another source

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits  
 11 = 1:8 Prescale value  
 10 = 1:4 Prescale value  
 01 = 1:2 Prescale value  
 00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable bit  
 1 = Timer1 oscillator is enabled  
 0 = Timer1 oscillator is shut off  
 The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2 **T1SYNC:** Timer1 External Clock Input Synchronization Select bit  
When TMR1CS = 1:  
 1 = Do not synchronize external clock input  
 0 = Synchronize external clock input  
When TMR1CS = 0:  
 This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit  
 1 = External clock from pin RC0/T1OSO/T13CKI (on the rising edge)  
 0 = Internal clock (Fosc/4)

bit 0 **TMR1ON:** Timer1 On bit  
 1 = Enables Timer1  
 0 = Stops Timer1



## Detectores de Alta/Baixa Tensão (HLVD)

- O PIC18F4520 incluem também um circuito especial para detecção da elevação ou diminuição da tensão de alimentação, chamado HLVD ()

# Registadores SFR do HLVD - HDLDCON

R/W-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
VDIRMAG	—	IRVST	HLVDEN	HLVDL3 <sup>(1)</sup>	HLVDL2 <sup>(1)</sup>	HLVDL1 <sup>(1)</sup>	HLVDL0 <sup>(1)</sup>
bit 7							bit 0

bit 7 **VDIRMAG:** Voltage Direction Magnitude Select bit

1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)

0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

**0 - Queda de Tensão**  
**1 - Aumento de Tensão**

bit 6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit

1 = Indicates that the voltage detect logic will generate the interrupt flag at the specified voltage range

0 = Indicates that the voltage detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 4 **HLVDEN:** High/Low-Voltage Detect Power Enable bit

1 = HLVD enabled

0 = HLVD disabled

bit 3-0 **HLVDL<3:0>:** Voltage Detection Limit bits<sup>(1)</sup>

1111 = External analog input is used (input comes from the HLVDIN pin)

1110 = Maximum setting

.

.

.

0000 = Minimum setting

**0000 - 2,17V**  
**0001 - 2,23V**  
**...**

**1111 - 5V**

# Registadores do HLVD

## PIR2

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF
bit 7						bit 0	

bit 2

**HLVDIF:** High/Low-Voltage Detect Interrupt Flag bit

1 = A high/low-voltage condition occurred (direction determined by VDIRMAG bit, HLVDCON&lt;7&gt;)

0 = A high/low-voltage condition has not occurred

## PIE2

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE
bit 7						bit 0	

bit 2

**HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit

1 = Enabled

0 = Disabled

## IPR2

R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP
bit 7						bit 0	

bit 2

**HLVDIP:** High/Low-Voltage Detect Interrupt Priority bit

1 = High priority

0 = Low priority

# Reset / Código-fonte - 1

```

1  #include <p18f4520.h>
2  #include <stdio.h>
3
4  #pragma config OSC = XT, WDT = ON, WDTPS = 1, MCLRE = ON
5  #pragma config DEBUG = OFF, LVP = OFF, PWRT = ON, BOREN = OFF
6
7  #define TECLA_S1    PORTBbits.RB0
8  #define TECLA_S2    PORTBbits.RB1
9  #define TECLA_S3    PORTBbits.RB2
10 #define LED_L1     LATBbits.LATB0
11 #define LED_L2     LATBbits.LATB1
12 #define LED_L3     LATBbits.LATB2
13
14 void verifica_RCON(void)
15 {
16     if (!RCONbits.TO)    // se o watchdog causou um reset
17     {
18         ClrWdt();        // apaga TO
19         LED_L1=1;        // liga o led L1
20     }
21     if (!RCONbits.RI)    // se foi um reset por software
22     {
23         RCONbits.RI=0;    // apaga o flag
24         LED_L2=1;        // liga o led L2
25     }
26     if (!RCONbits.POR)    // se foi um POR
27     {
28         RCONbits.POR=0;    // apaga o flag
29         LED_L3=1;        // liga o led L3
30     }
31 }
32

```

## Reset / Código-fonte - 2

```

33 void atraso(void)
34 {
35     unsigned char aux;
36     for (aux=255;aux;aux--) ClrWdt();
37 }
38
39 void main(void)
40 {
41     verifica_RCON(); // verifica os flags do RCON
42     ADCON1 = 0x0F;   // desliga entradas analógicas
43     while(1)
44     {
45         TRISB = 0;   // todos os pinos da porta B como saídas
46         atraso();     // chama a função de atraso
47         TRISB = 0x0F; // pinos RB0 a RB3 como entradas
48         if (!TECLA_S1) Reset(); // se S1 pressionada, executa reset por software
49         if (!TECLA_S2) while(1); // se S2 pressionada, entra em loop e espera wa
50         if (!TECLA_S3) LATB=0;   // se S3 pressionada, apaga os leds
51     }
52 }
53

```

**A tecla S1:** Provoca a execução de uma instrução RESET, ressetando o chip;

**A tecla S3:** permite apagar os LEDs;

**A tecla S2:** Provoca a entrada em um loop infinito, isso faz com que ocorra o estouro da contagem do watchdog e o consequente reset;

# Oscilador / Código-fonte - 1

```

1  #include <p18f4520.h>
2  #include <stdio.h>
3  #include "pic_simb.h"
4
5  #pragma config OSC=INTIO67, WDT = OFF, MCLRE = ON
6  #pragma config DEBUG = OFF, LVP = OFF, PWRT = ON, BOREN = OFF
7
8  #define L1    LATBbits.LATB0
9  #define S2    PORTBbits.RB1
10 #define S3    PORTBbits.RB2
11
12 void atraso(void)
13 {
14     unsigned char cnt1,cnt2;
15     for (cnt1=255;cnt1;cnt1--)    // loop externo
16     {
17         // se S2 pressionada, inverte IRCF0 (4MHz <-> 8MHz)
18         if (!S2) OSCCONbits.IRCF0 = !OSCCONbits.IRCF0;
19         // se S3 pressionada, inverte PLEN (clock*1 ou clock*4)
20         if (!S3) OSCTUNEbits.PLEN = !OSCTUNEbits.PLEN;
21         for (cnt2=255;cnt2;cnt2--);    // loop interno
22     }
23 }
24

```

Alterna-se as frequências de operação de 8MHz e 4MHz;

Liga ou desliga o PLL e com isso alterando a frequência de piscagem do LED (alternado entre 16MHz e 4 Mhz);

## Oscilador / Código-fonte - 2

```
25  main()
26  {
27      OSCCON = 0x70;      // clock = INTRC (8MHz)
28      TRISBbits.TRISB0 = 0;  // configura RB0 como saída
29      ADCON1 = 0x0F;      // desliga entradas analógicas
30  while(1)
31  {
32      LATBbits.LATB0 = 1;    // RB0 = 1
33      atraso();             // chama a função de atraso
34      LATBbits.LATB0 = 0;    // RB0 = 0
35      atraso();             // chama a função de atraso
36  }
37 }
```

## Próxima Aula

# **Aula 14**

## Interrupções