Design Graph LAB3

Advanced CPU architecture and Hardware Accelerators Lab

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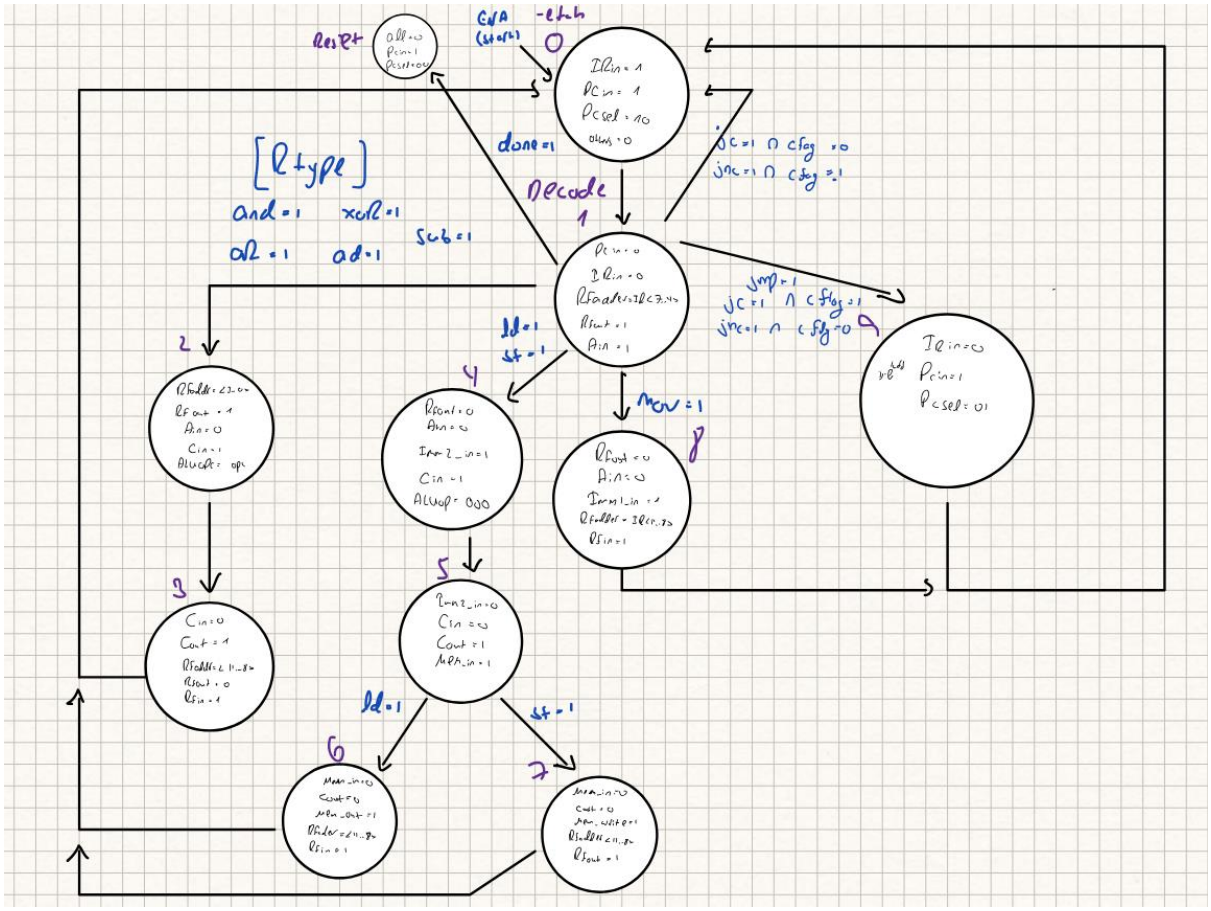
25/6/24

FSM:



States controls:

STATE		output														
		IRin	Pcin	Pcsel	RFaddr	RFout	RFin	OPC	Ain	Cin	Cout	Imm1_in	Imm2_in	Mem_in	Mem_out	Mem_wr
reset		0	0	0	0	0	0	0000	0	0	0	0	0	0	0	0
Fetch	State 0	1	1	10	0	0	0	0000	0	0	0	0	0	0	0	0
Decode	State 1	0	0	0	IR<7..4>	1	0	0000	1	0	0	0	0	0	0	0
Rtype	State 2	0	0	0	IR<3..0>	1	0	IR<15..12>	0	1	0	0	0	0	0	0
	State 3	0	0	0	IR<11..8>	0	1	0000	0	0	1	0	0	0	0	0
Itype	State 4	0	0	0	0	0	0	IR<15..12>	0	1	0	0	1	0	0	0
	State 5	0	0	0	0	0	0	0000	0	0	1	0	0	1	0	0
	State 6	0	0	0	IR<11..8>	0	1	0000	0	0	0	0	0	0	1	0
	State 7	0	0	0	IR<11..8>	1	0	0000	0	0	0	0	0	0	0	1
	State 8	0	0	0	IR<11..8>	0	1	0000	0	0	0	1	0	0	0	0
Jtype	State 9	0	0	01	0	0	0	0000	0	0	0	0	0	0	0	0