module	in			out			
	line name	sorce	ena_signal	line name	data	target	ena_signal
IR	Din_IR	Prog Memory <15..0>	IRin	Dout_IR_a	IR <11..8>	Din_Rfadder_a	*
				Dout_IR_b	IR<7..4>	Din_Rfadder_b	*
				Dout_IR_c	IR <3..0>	Din_Rfadder_c	*
				Op_IR	IR <15..12>	Din_Decoder	*
				IR_sign1	IR <7..0>	Din_Sighn Ext1	*
				IR_sign2	IR <3..0>	Din_Sighn Ext2	*
Rfadder	Din_Rfadder_a	Dout_IR_a	Rfaddr (mux)	Dout_Rfadder	Din_Rfadder&mux	writeAddr_REG , readAddr_REG	*
	Din_Rfadder_b	Dout_IR_b					
	Din_Rfadder_c	Dout_IR_c					
Registers	writeAddr_REG	Dout_Rfadder	*	Dout_REG	REG[ADDRESS]	BUS<15..0>	Rfout
	readAddr_REG	Dout_Rfadder	*				
	Din_Registers	BUS<15..0>	Rfin				
Reg A	Din_A	BUS<15..0>	Ain	Dout_A	REG A <15..0>	X_a	*
ALU	X_a	Dout_A	*	ALU_res	ALU result <15..0>	Din_C	*
	X_b	BUS<15..0>	*	ALU_Cflag	ALU cflag	Control Unit - Cflag	*
	OPC_ALU	OPC signal	*	ALU_Zflag	ALU zflag	Control Unit - Zflag	*
				ALU_Nflag	ALU zflag	Control Unit - Nflag	
Reg C(ms)	Din_C	Dout_A	Cin	Dout_C	Reg C(ms)<15..0>	BUS<15..0>	Cout
Sighn Ext1	Din_Sighn_Ext1	IR_sign1	*	Dout_Sighn_Ext1	0#8 &Din_Sighn_Ext1	BUS<15..0>	Imm1_in
Sighn Ext2	Din_Sighn_Ext2	IR_sign2	*	Dout_Sighn_Ext2	0#12 &Din_Sighn_Ext1	BUS<15..0>	Imm2_in
Decoder	Din_Decoder	Op_IR	*	status signals	decoder&Din_Decoder	Control Unit - Cflag	*
PC	Din_PC	Dout_PC_adder	PCin	Dout_PC	REG PC <15..0>	readAddr_ITCM	*
						PC_adder	
PC_adder	Din_PC_adder	Dout_PC	Pccel	Dout_PC_adder	Din_PC_adder&adder&mux	Din_PC	*
Prog Memory (ITCM)	wren_ITCM	TB_ena	*	Dout_ITCM	ITCM[Dout_PC_adder]	Din_IR	*
	Din_ITCM	TB_datain	*				*
	writeAddr_ITCM	TB_addr	*				*
	readAddr_ITCM	Dout_PC_adder	*				*
Data Memory (DTCM)	RmemAddr (mux)	BUS<15..0>	*	Dout_DTCM	DTCM[adress]	BUS<15..0>	Mem_out
		TB	*				
	WmemAddr (mux)	BUS<15..0>	Mem_in				
		TB	*				
	WmemData(mux)	BUS<15..0>	*		DTCM[adress]	TB	*
		TB	*				
	memEn	Mem_wr	*				
		TB	*				