PREPERATION REPORT LAB2

Advanced CPU architecture and Hardware Accelerators Lab

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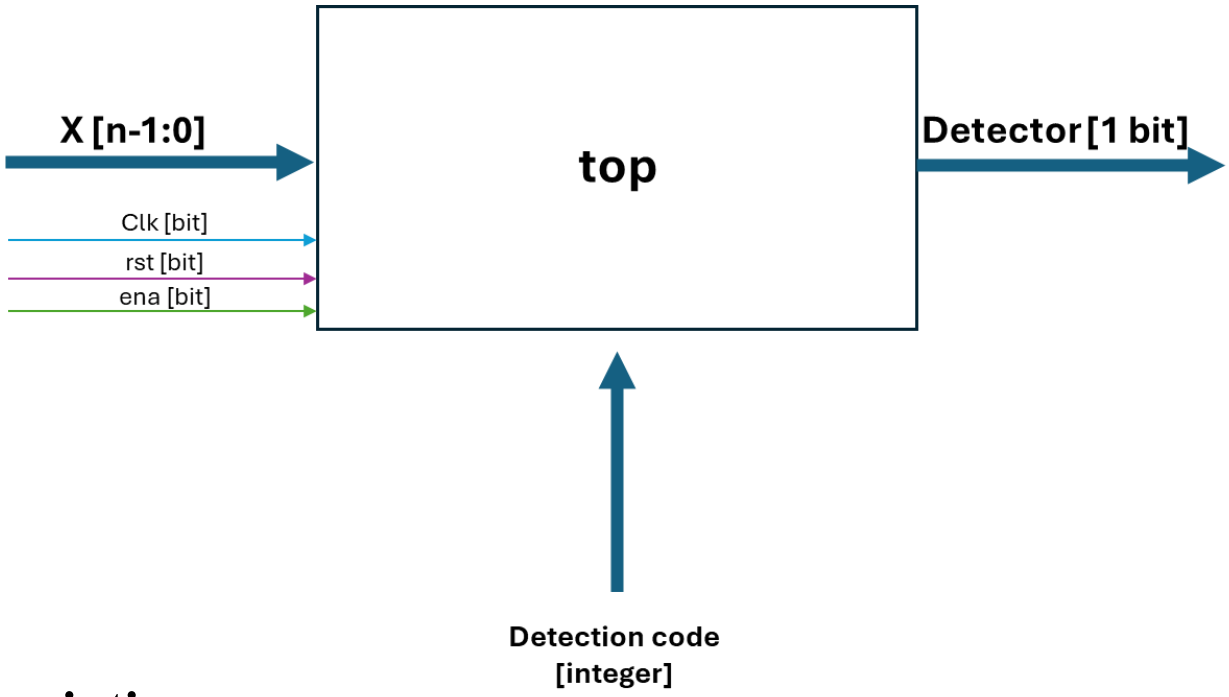
TOP:



Description:

This module encapsulates three processes, which will be elaborated upon subsequently. The module receives an N-bit series of signals representing integer values and a detection code signal of integer type at time J. Additionally, the module has three more 1-bit signal inputs: clk, rst, and ena. The module outputs a signal referred to as the "detector." If the series of numbers maintains the specified condition, the detector bit is set.

Ports in:

- **X** - An N-bit series of signals
- **Detection code** – A integer input signal designated as the mode selector determines the condition thar the module check .

  "0" – X[j-1] – X[j-2] =1

  "1" – X[j-1] – X[j-2] =2

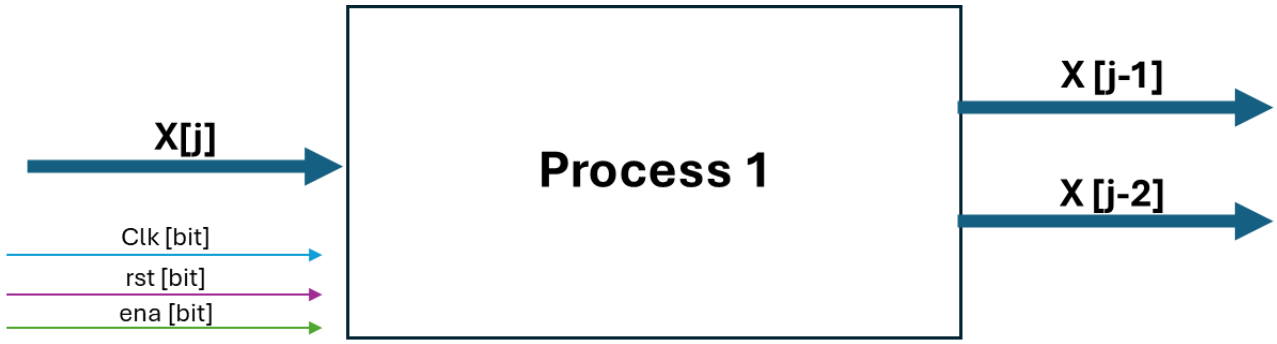
  "2" – X[j-1] – X[j-2] =3

  "3" – X[j-1] – X[j-2] =4
- **clk** – A clock bit input signal to the FF.
- **rst** – A reset bit input signal to the FF.
- **ene** – A enable bit input signal to the FF.

Ports out:

- **detector** - 1 bit signal that set if the series of numbers maintains the specified condition.

Process 1:

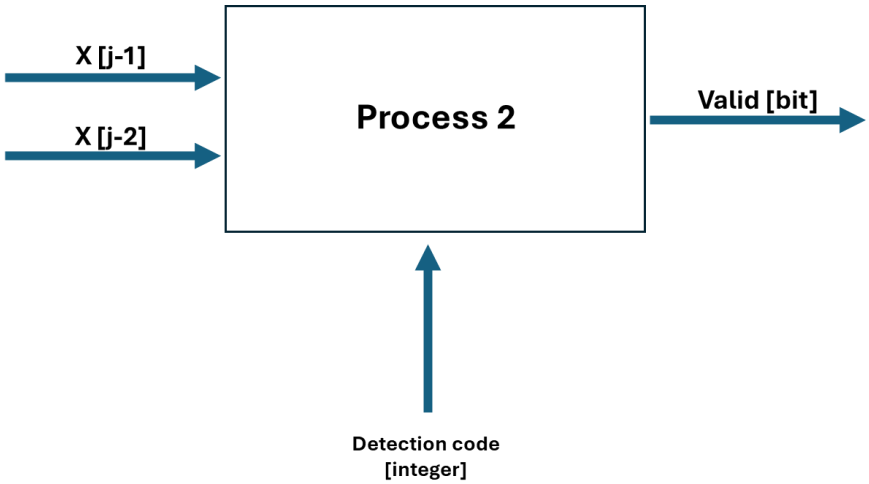


The described process involves taking an input signal x[j]x[j]x[j] and using two chained flip-flops (FF) to generate two output signals: x[j−1] and x[j−2]

This mechanism operates under the following conditions:

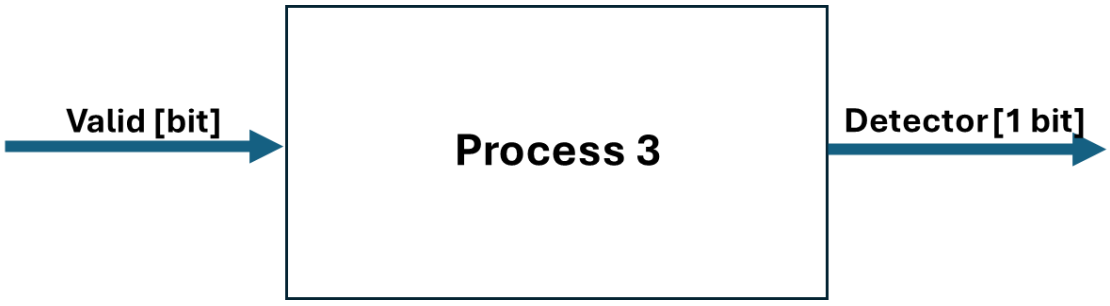
- **Clock Signal (clk):** The process is synchronous, meaning it operates on the rising or falling edge of a clock signal.
- **Enable Signal (ena):** The process is active only when the enable signal is set.
- **Reset Signal (rst):** When the reset signal is set, the output signals are forced to z

Process 2:



The described process involves receiving two signals, X[j−1]X[j-1]X[j−1] and X[j−2]X[j-2]X[j−2], and assessing whether their difference complies with a predetermined condition. It proceeds by augmenting the X[j−2]X[j-2]X[j−2] signal with a detection code and a carry, then evaluates whether the result matches X[j−1]X[j-1]X[j−1]. If equality is achieved, the valid bit is activated.

Process 3:



The described process involves receiving a valid bit and counting the consecutive occurrences where the valid bit is set for mmm clock cycles. Once mmm consecutive valid bits are detected, the detector bit is activated. Additionally, the process is controlled by clock (clk), enable (ena), and reset (rst) signals.

- **Clock Signal (clk):** Synchronizes the operation of the process.
- **Enable Signal (ena):** Controls whether the process is active.
- **Reset Signal (rst):** Resets the process and its internal counters.

Result analysis:

Upon running a simulation for this module, we observe that the results align with our expectations.