PREPERATION REPORT LAB3

Advanced CPU architecture and Hardware Accelerators Lab

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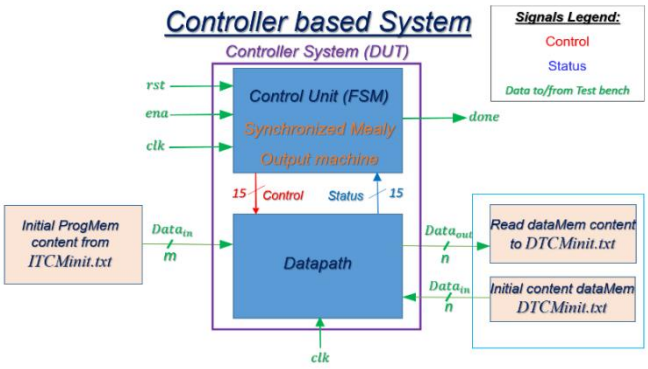
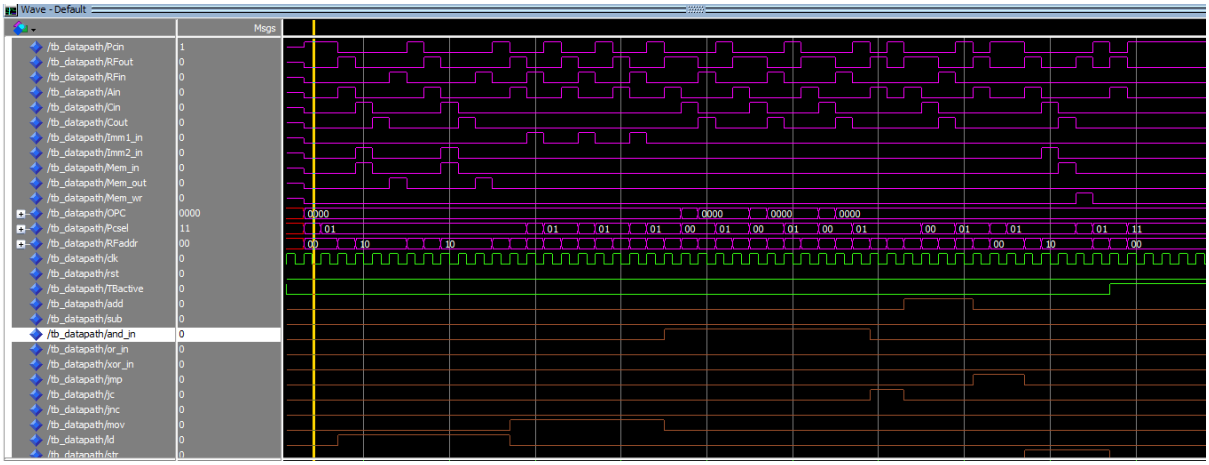
Brief explanation about the top entity:

The top entity describes system of a multi-cycle processor, focusing on the structural organization and interaction between its main components: the control unit, datapath, and two types of memory (ITCM and DTCM). Here's an overview of the structure and relationships:

1. **Control Unit and Datapath**: The core of the system is divided into two main components, the control unit and the datapath. The control unit responsible on the operation of the system by generating control signals based on the current state and inputs. These control signals dictate the behavior of the datapath, which performs the actual data processing tasks such as arithmetic operations, data movement, and memory access. The control unit and datapath communicate through a series of signals that represent control instructions, data to be processed, and status flags.
2. **ITCM (Instruction Tightly Coupled Memory)**: This memory is designed for storing and providing fast access to the instructions that the system executes. The ITCM is tightly coupled to the datapath, allowing for efficient instruction fetch cycles. This is critical for achieving high performance in systems where instruction fetch speed is a bottleneck.
3. **DTCM (Data Tightly Coupled Memory)**: Similar to the ITCM, the DTCM is optimized for data storage and access. It is tightly coupled to the datapath, enabling fast read and write operations for the data being processed. This is essential for systems that require quick access to data for real-time processing tasks.
4. **Interactions**:
    - The **control unit** generates signals that control datapath's. It interprets the current instruction and system state to produce control signals that guide the datapath's execution of operations and memory interactions.
    - The **datapath** interacts with both the ITCM and DTCM based on the control signals. It fetches instructions from the ITCM for decoding and execution and accesses data from the DTCM as required by the instruction set. The datapath is responsible for executing the instructions, performing computations, and managing data flow between registers, ALU, and memories.
    - **ITCM and DTCM** are specialized for their respective roles but share a common purpose: to provide fast, efficient access to the resources needed by the datapath to execute instructions and process data. Their design and integration into the system are critical for minimizing latency and maximizing performance.



Wave diagrams:



Magenta – Control signals, Green – clock and TB signals, Brown – Status signals

Orange – The data that comes from DataMem (DTCM).