

## Scenario 3:

a): Venus setup for Scenario 2 showing Program parameters, Cache parameters etc

```
Active File: null Save Close
9 # /* Step through the selected array segment with the given step size. */
10 # for (index = 0; index < arraysize; index += stepsize) {
11 #     if(option==0)
12 #         array[index] = 0; // Option 0: One cache access - write
13 #     else
14 #         array[index] = array[index] + 1; // Option 1: Two cache accesses - read AND write
15 # }
16 # }
17
18 .data
19 array: .word 2048 # max array size specified in BYTES (DO NOT CHANGE)
20
21 .text
22 #####
23 main: li a0, 128 # array size in BYTES (power of 2 < array size)
24     li a1, 1 # step size (power of 2 > 0)
25     li a2, 1 # rep count (int > 0)
26     li a3, 0 # 0 - option 0, 1 - option 1
27 # You MAY change the code above this section
28 #####
```

Level 1 cache parameters are:

Registers Memory Cache VDB	
Cache Levels	2
Block Size (Bytes)	8
Number of Blocks	8
Associativity	1
Cache Size (Bytes)	64
<span>Enable?</span>	Enables current selected level of the cache.
Direct Mapped	<span>▼</span>
LRU <span>▼</span>	L1 <span>▼</span>
Hit Count	0
Accesses	0
Hit Rate	???
<div>0) EMPTY</div> <div>1) EMPTY</div> <div>2) EMPTY</div> <div>3) EMPTY</div> <div>4) EMPTY</div> <div>5) EMPTY</div> <div>6) EMPTY</div> <div>7) EMPTY</div>	
NOTE: This is a write through, write allocate cache.	
Seed	6799548270239674178
Display Settings	Hex <span>▼</span>

Level 2 cache parameters are:

Registers

Memory

Cache

VDB

Cache Levels

2

Block Size (Bytes)

8

Number of Blocks

16

Associativity

1

Cache Size (Bytes)

128

Enable?

Enables current selected level of the cache.

Direct Mapped

▼

LRU

▼

L2

▼

Hit Count

0

Accesses

0

Hit Rate

???

0) EMPTY

1) EMPTY

2) EMPTY

3) EMPTY

4) EMPTY

5) EMPTY

6) EMPTY

7) EMPTY

8) EMPTY

9) EMPTY

10) EMPTY

11) EMPTY

12) EMPTY

13) EMPTY

14) EMPTY

15) EMPTY

NOTE: This is a write through, write allocate cache.

Seed

-6476401429875973288

Display Settings

Hex

▼

b): Answers to tasks 1, 2, 3, 4, 5

1): What is the hit rate of the L1 cache? The L2 cache? Overall? Each hit rate is a decimal rounded to two places.

hit rate of L1: 0.50

hit rate of L2: 0.00

Overall hit rate:  $(0+16)/32 = 0.50$

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**2): How many accesses do we have to the L1 cache total? How many of them are misses?**

Accesses of L1 cache: 32

Misses Count: 16

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**3): How many accesses do we have to the L2 cache total? HINT: Think about what the L1 cache has to do in order to make us access the L2 cache.**

Accesses of L2 cache: 16

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**4): What program parameter would allow us to increase the L2 hit rate, but keep the L1 hit rate the same?**

Rep Count (a2) is the parameter. Because in next iteration L2 cache is already filled with the data which was not available in first iteration and thus hit rate of L2 increases.

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**5): Do our L1 and L2 hit rates decrease (-), stay the same (=), or increase (+) as we (1) increase the number of blocks in L1, or (2) increase the L1 block size?**

**Increasing the number of blocks in L1:**

L1 = ; L2 =

If we increase number of blocks as the block size is same so there will be no effect on hit rate.

**Increasing block size in L1:**

L1+ ; L2 =

L1 will increase because more no. of words are fetched from the memory as a result of a miss.

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