ABV- Indian Institute of Information Technology & Management, Gwalior

Computer Organisation and Architecture (IT202)

Minor Semester Examination (Session 2023–24)

Maximum Time: 1.5 Hours **Max Marks: 30**

Note: All questions carry equal marks. Section A is compulsory. In Section B, attempt any 2 questions.

Section A ($5 \times 2 = 10$ Marks)
Answer all questions briefly. Each question carries 2 marks.

1. Differentiate between Computer Organisation and Computer Architecture.
2. What do you mean by Application Binary Interface (ABI)?
3. Represent the decimal number -18 in 8-bit two's complement form.
4. Define instruction cycle. List its main phases.
5. State one advantage and one disadvantage of pipelining.

Section B ($2 \times 10 = 20$ Marks)
Attempt any two questions. Each question carries 10 marks.

6. (a) Explain the basic functional units of a computer with the help of a neat block diagram. (b) Differentiate between RISC and CISC instruction set architectures.
7. (a) Perform the subtraction $(101101)_2 - (11001)_2$ using 2's complement method. (b) Explain Booth's multiplication algorithm with an example.
8. (a) Design a hardwired control unit for a simple instruction set (assume 3 instructions). (b) Discuss the characteristics and differences between SRAM and DRAM.
9. (a) Explain the concept of instruction pipelining. How does it improve CPU performance? (b) A CPU executes 4 pipeline stages with individual times of 10 ns, 12 ns, 8 ns, and 10 ns. Calculate:
   - The pipeline cycle time
   - Speedup for executing 100 instructions compared to non-pipelined execution