Sr. No...003302.....

JANUARY- 2023 B.Tech.III SEMESTER

Digital Electronics (ESC-302/ESCH-302)

Time: 3 Hours

Max. Marks:75

Instructions:

- 1. It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.
- 2. Answer any four questions from Part -B in detail.
- 3. Different sub-parts of a question are to be attempted adjacent to each other.

PART -A

Q1	(a)	Define Volatile and Non-volatile memory.	(1.5)
•	. ,	Convert $(109.125)_{10} = ()_2$	(1.5)
		Give the definition of Decoder.	(1.5)
		What is Modulus Counter.	(1.5)
		What are the advantages of CMOS logic families used for implementing logic	050 P50
	(e)	gates?	()
			(1.5)
	(f)		(1.5)
	(g)	Enlist significant specifications of ADCs.	
	(h)	Draw only logic diagram of J-K flip-flop	(1.5)
	(i)	An 8-bit DAC has full- scale voltage range from 0 to 5.12V. What is the	(1.5)
		output change per bit.	(1.5)
	(j)	What is sequential memory?	
PART -B			
Q2	(a)	Minimize the following function using K-map.	(10)
	19	$F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$	
	(b)	Design half-adder and full-adder using only NAND-Gates.	(5)
03	(a)	Convert the RS flip-flop to D flip-flop.	(5)
ų٥	(b)	Explain Ripple counter with suitable digram.	(10)
Q4	(1)	Simplify Boolean expression using Demorgans theorem. (15)	5)
		$Y(A,B) = (\overline{A+B})(\overline{A+B})$	
	(II)	Implement Boolean expression using only universal gate.	

 $Y = (\overline{(A+B)C})$

(III) Convert Boolean function into standard SOP Y(A,B,C) = AB+AC+BC(IV) Interfacing CMOS and TTL Devices. (V) Convert $(762.231)_8 = ()_{10}$ Q5.(a) Explain programmable logic array(PLA) and give advantages of PLDs. (5)(b) Briefly explain the working of Dynamic RAM cell. Also explain MROM, PROM, EPROM, EEPROM. (10)Q6(a) Implement the following function using 8:1 MUX (10) $F(A,B,C,D) = \sum_{m} (0,1,3,4,7,8,9,11,14,15)$ (5)(b) Explain 4-bit SISO shift Register Q7. Explain 3-bit flash type or parallel comparator ADC.with suitable dig. And truth table. (15)And give its advantages and disadvantages.
