Degree: B.Tech. (CSE/CSAI/CSDS/MAC)

Semester: III

MID-SEMESTER EXAMINATION, September 2023

Max. Marks: 25
Duration: 1:30 Hours

Course Title: Computer Architecture and Organization
Course Code: COCSC07/CACSC07/CDCSC07/CMCSC07

Note: Attempt ALL questions in the GIVEN ORDER only. Missing data/information (if any), may be suitably assumed and mentioned in the answer. Diagrams should be drawn neatly.

Q. No.	Question	Marks	CO
1a	What is instruction cycle? How interrupts affect instruction cycle?	2	CO1
1b	A digital system has three registers of 5 bits each. Design a bus for the system using either multiplexers or three-state buffers. Also, provide its function table.	3	CO2
2a	Design a 4-bit shifter circuit that has a mode bit M. The circuit implements logical shift-left if M = 0 and circular shift-right if M = 1.	2	CO2
2b	Differentiate between: • Program and instruction set • Hardwired control and microprogrammed control • Program counter and instruction register	3	CO1
3a	Explain the working of the two passes of an assembler.	2	CO1
3b	Design a 4-bit ALU that can implement the following microoperations: Subtract, Subtract with borrow, Decrement and Transfer. Also, provide the detailed function table.	3	CO2
4a	What is an addressing mode? Why CPUs support so many addressing modes?	2	CO1
4b	If you are writing programs in assembly language, then when will you use instructions with the following addressing modes? • Register addressing mode • Immediate addressing mode • Relative addressing mode	3	CO3
5a	List the characteristic features of CISC processors. Which of these features are found in the 8085 microprocessor?	2	CO3
5b	What are the advantages of the following features of RISC processors? • Large number of registers • Fixed-length instruction format • Memory access limited to load and store instructions	3	CO3

Degree: B.Tech. (CSAI/CSDS/MAC/CSE) **Semester: III**

END-SEMESTER EXAMINATION, Nov-Dec 2023

Course Title: Computer Architecture and Organization
Course Code: CACSC07/CDCSC07/CMCSC07/COCSC07

Max. Marks: 50

Time: 3 Hours

Note: Attempt ALL the five questions. Missing data/information (if any), maybe suitably assumed and mentioned in the answer.

<table>
<tr><th>Q. No.</th><th>Question</th><th>Marks</th><th>CO</th></tr>
<tr><td>Q 1</td><td>Attempt any 2 parts of the following.</td><td></td><td></td></tr>
<tr><td>1a</td><td>Explain the important features of:
• Digital system
• Instruction cycle
• Stored program organization
• Assembly language
• Parallel processing</td><td>5</td><td>CO1</td></tr>
<tr><td>1b</td><td>Instructions of which addressing mode should be used in the following situations?
• When the operands are specified implicitly in the definition of the instruction
• To initialize a register to a constant value
• To perform arithmetic and logic operations in optimum time
• To access a table of data in the memory
• To jump to a fixed memory location
Provide specific reasons in support of your answers.</td><td>5</td><td>CO1</td></tr>
<tr><td>1c</td><td>Compare the instruction sets of CISC and RISC.</td><td>5</td><td>CO1</td></tr>
<tr><td>Q 2</td><td>Attempt any 2 parts of the following.</td><td></td><td></td></tr>
<tr><td>Common for all parts of Q 2</td><td>A computer has 64 words of memory, each word being 8 bits wide. The CPU accesses the memory by outputting a 6-bit address on its output pins A[5..0] and reading in the 8-bit value from memory on its data pins D[7..0]. The CPU contains an address register (AR), a program counter (PC), an accumulator (AC), a data register (DR) and an instruction register (IR). The CPU must realize the following instructions.
<table>
<tr><th>Mnemonic</th><th>Instruction</th><th>Opcode</th><th>Operation</th></tr>
<tr><td>RST</td><td>Reset (software interrupt)</td><td>00</td><td>PC ← 000000</td></tr>
<tr><td>JREL</td><td>Jump (relative addressing mode)</td><td>01</td><td>PC ← PC + AAAAAA</td></tr>
<tr><td>OR</td><td>Or</td><td>10</td><td>AC ← AC or M [AAAAAA]</td></tr>
<tr><td>SUB</td><td>Subtract</td><td>11</td><td>AC ← AC - M [AAAAAA]</td></tr>
</table></td><td></td><td></td></tr>
<tr><td>2a</td><td>Determine the size of the registers and draw a block diagram of the computer showing how the different components are connected by a common bus.</td><td>5</td><td>CO2</td></tr>
<tr><td>2b</td><td>Design the control unit and the ALU of the computer.</td><td>5</td><td>CO2</td></tr>
<tr><td>2c</td><td>What is a software interrupt? How is it different from an ordinary instruction?</td><td>5</td><td>CO2</td></tr>
</table>

Q 3	*Attempt any 2 parts of the following.*		
3a	What basis was used by Flynn to classify computers? Describe the different types of computers according to the classification.	5	CO5
3b	A 4-segment pipeline is used to solve 16 similar tasks. Determine the speedup.	5	CO5
3c	Use Booth's algorithm to multiply 1100 and 0011. Show all the steps.	5	CO4
Q 4	*Attempt any 2 parts of the following.*		
4a	Design a 3-bit by 2-bit array multiplier. Show the calculations.	5	CO4
4b	Explain with the help of suitable timing diagrams how asynchronous data transfer with handshaking occurs between the CPU and a peripheral device.	5	CO3
4c	Explain the concepts of priority interrupts and DMA.	5	CO3
Q 5	*Attempt any 2 parts of the following.*		
5a	Why a computer must have the following memory devices? • ROM • RAM • Hard disk	5	CO3
5b	What is locality of references? How the concept applies to both code and data?	5	CO5
5c	What do you mean by cache performance? Explain with suitable example.	5	CO4