विश्वजीवनामृतं ज्ञानम्

Atal Bihari Vajpayee Indian Institute of Information Technology & Management, Gwalior

EE404: Integrated Circuit Technology

Minor Examination (Session 2023–24)

Maximum Time: 1.5 Hours **Max Marks: 25**

Note: Attempt all questions. Clear circuit diagrams are expected wherever required.

1. Explain the process steps involved in silicon wafer preparation for IC fabrication. (5 Marks)
2. Discuss the differences between bipolar and CMOS technologies. Mention two applications for each. (5 Marks)
3. Derive the expression for threshold voltage in a MOS transistor. (5 Marks)
4. Explain lithography in IC fabrication. How does optical lithography differ from electron-beam lithography? (5 Marks)
5. Write short notes on: (a) Ion implantation (b) Oxidation process in IC technology (5 Marks)