ABV- Indian Institute of Information Technology & Management, Gwalior

Computer Organisation and Architecture (IT202)

Major Semester Examination (Session 2023–24)

Maximum Time: 3 Hours **Max Marks: 70**

Note: Section A is compulsory. Attempt any three questions from Section B and both questions from Section C.

Section A (10 × 2 = 20 Marks)
Answer all questions briefly.

1. Differentiate between Von Neumann and Harvard architectures.
2. Define instruction set architecture (ISA). Give two examples.
3. Represent the decimal number 45.625 in IEEE-754 single precision format.
4. Explain the concept of microprogrammed control.
5. Define locality of reference. Why is it important in memory systems?
6. What are hazards in pipelining? List the types.
7. Differentiate between direct and associative mapping in cache memory.
8. State the advantages of using multiple buses in CPU design.
9. What is endianness? Explain with an example.
10. Write short notes on Input/Output interface modules.

Section B (3 × 10 = 30 Marks)
Attempt any three questions.

11. (a) Draw and explain the functional block diagram of a computer. (b) Discuss the role of the control unit in instruction execution.
12. (a) Explain hardwired vs microprogrammed control unit design with suitable diagrams. (b) Discuss advantages and disadvantages of each.

13. (a) Perform the multiplication of $(-13)_{10} \times (11)_{10}$ using Booth's algorithm. (b) Explain the steps involved in restoring division with an example.

14. (a) Discuss the memory hierarchy in detail with access time, cost, and size trade-offs. (b) Explain cache write policies with suitable diagrams.

15. (a) Explain pipelining performance with speedup and efficiency formulas. (b) A non-pipelined processor takes 50 ns to execute an instruction. A 5-stage pipeline has stage times of 12, 10, 8, 10, and 9 ns. Compute the speedup for execution of 100 instructions.

Section C ($2 \times 10 = 20$ Marks)
Attempt both questions.

16. A system has 64 KB cache and 4 MB main memory with block size of 1 KB. (a) How many bits are required for the main memory address? (b) Show the address format for:

    - Direct mapping
    - 2-way set associative mapping

17. Consider a CPU with a 4-stage pipeline (IF, ID, EX, WB). The instruction mix consists of 40% ALU operations, 25% load, 15% store, and 20% branches. Assume branch penalty = 2 cycles, load-use hazard penalty = 1 cycle, and CPI of ideal pipeline = 1. Calculate:

    - Effective CPI
    - Speedup compared to a non-pipelined processor with CPI = 4