Atal Bihari Vajpayee Indian Institute of Information Technology & Management, Gwalior

EE404: Integrated Circuit Technology

Major Examination (Session 2023–24)

Maximum Time: 3 Hours **Max Marks: 70**

Note: Attempt all questions. Use neat diagrams wherever necessary. Internal choices are provided.

1. (a) Explain crystal growth and wafer preparation process in IC fabrication. (7 Marks) (b) Compare the Czochralski and Float Zone methods. (5 Marks)

2. (a) Discuss the principle of photolithography. Draw a neat sketch of the steps involved. (8 Marks) (b) What are the challenges in achieving sub-micron lithography? (6 Marks)

3. Attempt any two: (a) Explain thermal oxidation process. Distinguish between wet and dry oxidation. (6 Marks) (b) Describe diffusion and ion implantation processes with equations. (6 Marks) (c) Explain epitaxy and its role in IC fabrication. (6 Marks)

4. **Numerical (10 Marks):** A silicon wafer is oxidized at 1100°C. Given B/A = 0.05 μm/hr and B = 0.2 μm^2/hr, calculate the oxide thickness after 4 hours. Show steps.

5. **Case Study (12 Marks):** A fabrication lab wants to transition from 180nm to 45nm technology. - Identify major technological hurdles. - Suggest solutions related to lithography, doping, and heat management. - Highlight how Moore's law is challenged.

6. Write short notes on (any three, 4 marks each): (a) Metallization techniques (b) Cleanroom environment and contamination control (c) CMOS process integration (d) Reliability issues in ICs