विश्वजीवनामृतं ज्ञानम्

Atal Bihari Vajpayee Indian Institute of Information Technology & Management, Gwalior

EE404: Integrated Circuit Technology

Major Examination (Session 2024–25)

Maximum Time: 3 Hours **Max Marks: 70**

Note: All questions are compulsory. Answers should be precise and well supported with diagrams.

1. (a) Explain wafer cleaning and preparation methods. (b) Discuss the importance of crystal orientation in IC fabrication. (10 Marks)

2. (a) Compare diffusion and ion implantation techniques with neat diagrams. (b) Discuss advantages and limitations of each. (10 Marks)

3. (a) Derive the small-signal model of MOSFET. (b) Explain the short-channel effects observed in modern MOS devices. (12 Marks)

4. (a) Explain photolithography steps in detail. (b) Why is resolution enhancement critical for sub-10nm technology nodes? (12 Marks)

5. (a) Describe different metallization techniques used in ICs. (b) Compare aluminum interconnects with copper interconnects. (10 Marks)

6. Short Notes (any three): (i) Silicon-on-Insulator (SOI) (ii) Shallow Trench Isolation (STI) (iii) FinFET technology (iv) Role of Packaging in IC performance (12 Marks)

7. Case Study: A fabrication unit is shifting from 90nm to 28nm process technology. Highlight the fabrication challenges, device performance improvements, and reliability concerns. (4 Marks)