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015405

August/September 2022

B.Tech. (ENC) IV SEMESTER

Digital System Design & Applications (ECP-405)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART-A

1. (a) What is VHDL? (1.5)

(b) What are sequential and concurrent statements? (1.5)

(c) What are the RTL description processes? (1.5)

(d) What does hierarchy mean? (1.5)

(e) What is entity? (1.5)

(f) Define process in VHDL. (1.5)

(g) What are the signal declaration and signal assignment statements? (1.5)

(h) What are Verilog strings? (1.5)

(i) What is structured design methodology? (1.5)

(j) What is user defined primitives? (1.5)

PART-B

2. (a) State the features of VHDL in detail. (7)
   (b) Explain the concept of delta delay's in VHDL. (8)

3. (a) Write VHDL code for 8:3 encoder. (7)
   (b) Write the VHDL code to implement the 8:1 multiplexer logic. (8)

4. (a) Explain different types of operators in VHDL. (8)
   (b) Compare data flow, behavioural and structural modelling in VHDL. (7)

5. (a) Design 8-to-3 encoder using verilog code. (7)
   (b) Discuss various descriptive styles available for hardware modelling using verilog HDL. (8)

6. (a) Explain in detail about verilog data types with suitable examples. (8)
   (b) Write a VHDL program for full adder. (7)

7. (a) Explain Mealy and Moore model with neat block diagram. (8)
   (b) Compare VHDL and verilog. (7)
