Atal Bihari Vajpayee Indian Institute of Information Technology & Management, Gwalior

EE404: Integrated Circuit Technology

Major Examination (Session 2024–25)

Maximum Time: 3 Hours **Max Marks: 75**

Note: Attempt all questions. Internal choices are provided.

1. (a) Describe the complete **CMOS fabrication process** with neat diagrams. (10 Marks) (b) What are the main differences between n-well and p-well CMOS? (5 Marks)

2. (a) Discuss various **thin film deposition techniques** (CVD, PVD, sputtering). (7 Marks) (b) Explain why step coverage is an important factor in metallization. (5 Marks)

3. **Numerical (10 Marks):** A wafer undergoes wet oxidation at 1000°C. Given B/A = 0.03 m/hr and B = 0.12 m^2/hr. Calculate the oxide thickness after 6 hours.

4. Attempt any two: (a) Explain the working principle of photolithography and challenges at 7 nm node. (7 Marks) (b) What are the different types of etching techniques? Compare wet vs dry etching. (7 Marks) (c) Discuss scaling limits of MOSFETs in deep sub-micron technology. (7 Marks)

5. **Case Study (12 Marks):** A semiconductor foundry is shifting from 90 nm to 14 nm node. - What modifications are required in lithography? - Discuss issues with short-channel effects. - Suggest how FinFET technology can solve scaling issues.

6. Write short notes on any three (5 marks each): (a) Epitaxial growth and its importance (b) Reliability issues in IC packaging (c) Semiconductor yield and process control (d) Impact of Moore's law in IC design