Atal Bihari Vajpayee Indian Institute of Information Technology & Management, Gwalior

EE404: Integrated Circuit Technology

Major Examination (Session 2023–24)

Maximum Time: 3 Hours **Max Marks: 60**

Note: Answer all questions. Stepwise explanation will carry weightage.

1. (a) Discuss crystal growth techniques for IC fabrication. (b) What are the advantages of Czochralski method? (10 Marks)

2. (a) Explain diffusion and ion implantation as doping methods. (b) Compare their precision and limitations. (10 Marks)

3. (a) Derive the current-voltage characteristics of a MOSFET. (b) Discuss channel length modulation effect. (10 Marks)

4. (a) Explain the photolithography process with neat sketches. (b) What are the challenges in sub-micron lithography? (8 Marks)

5. (a) Discuss the steps involved in metallization. (b) Compare evaporation and sputtering techniques. (8 Marks)

6. Write short notes on any three: (i) LOCOS isolation (ii) Chemical Vapor Deposition (CVD) (iii) Packaging in IC technology (iv) VLSI scaling challenges (9 Marks)

7. Case Study: A semiconductor company plans to migrate from 180nm to 45nm CMOS technology. Discuss the major fabrication challenges and design implications. (5 Marks)