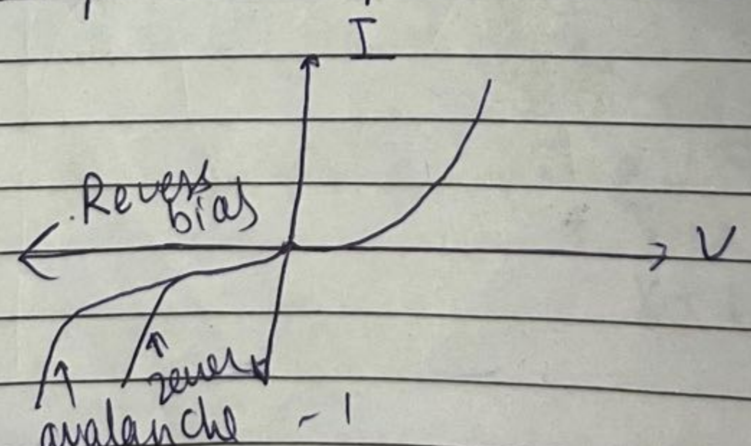
Ques Difference b/w zener and avalanche breakdown

Ans

Zener	avalanche
① Happens at the junction which are heavily doped and have narrow depletion region	① Happen at the junction which are lightly doped and have wide depletion region
② Has a very strong electric field in the depletion region	② Doesn't have as strong electric field
③ In this there is a rupture of ~~ete~~ covalent bonds due to which electron-hole pair are generated. (Tunneling)	③ In this minority carries collide with the semi conductor atoms and electron-hole pair are generated then accelerated by the electric field result in more collision
④ On Inc temp. the reverse voltage dec. breakdown	④ On Inc temp the reverse voltage inc.
⑤ Hard characterstics no knee point	⑤ Soft characterstic Knee point



$a = e^b \quad b = \ln a$

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Ques $I_s = 2.2 \times 10^{-6}$
$T = 300$
$I_D = 9 \times 10^{-3}$

$$I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right)$$

$$V_T = \frac{KT}{q} = \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}}$$
$$= \frac{1.38 \times 3 \times 10^{-23+2+19}}{1.6}$$

$K = 1.38 \times 10^{-23}$ J/K
T= in kelvin (300 in this)
$q = 1.6 \times 10^{-19}$C

$$= \frac{1.38 \times 3 \times 10^{-2}}{1.6}$$
$$= 2.58 \times 10^{-2}$$
$$= 0.258 \times 10^{-3}$$

$n=1$

$$\frac{I_D}{I_S} = e^{\frac{V_D}{nV_T}} - 1$$

$$= \frac{9 \times 10^{-3}}{2.2 \times 10^{-6}} = 4.09 \times 10^{3}$$
$$= 4090$$

$$4091 = e^{\frac{V_D}{0.258 \times 10^{-3}}}$$

$$\ln(4091) = \frac{V_D}{0.258 \times 10^{-3}}$$

$$8.3 = \frac{V_D}{0.258 \times 10^{-3}}$$

$8.3 \times 0.258 \times 10^{-3} = V_D$
$V_D = 2.1$ mV

Good Write

Si diode F·B (0.7V)
R·B (O·C)

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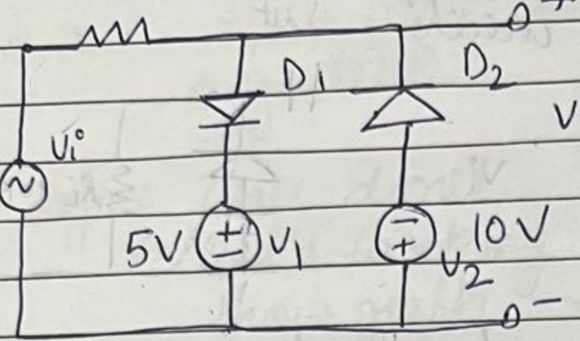
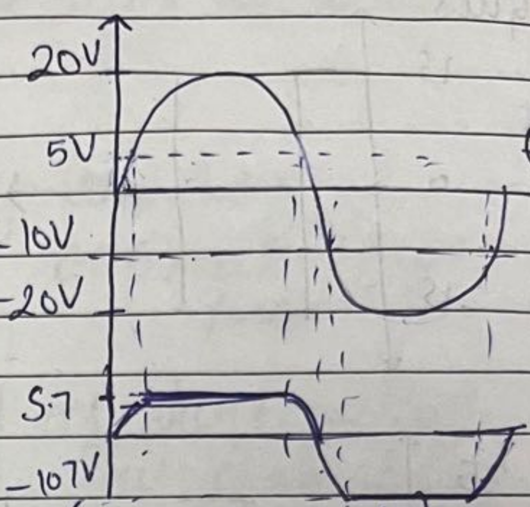
Sup

Ques





for +ve half cycle

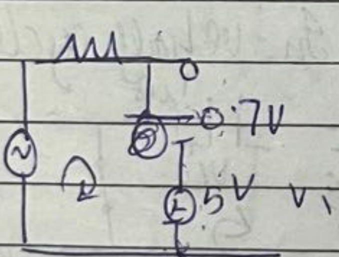
$D_2 \rightarrow$ R·B by V_i, V_2 (open circuit)

$V_i > 5V$

D_1 will be forward bias by V_i
replace D_i with 0.7V

$V_i < 5V$

D_1 will be reverse bias
D_i ≈ open circuit



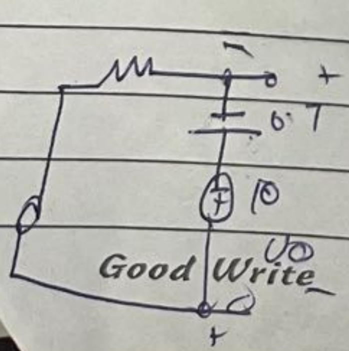
$5 + 0.7 - V_o = 0$
$V_o = 5 + 0.7$
$= 5.7V$

V_o follow V_i when $V_i < 5V$

for -ve half cycle

D_i will be reverse bias (O.C)

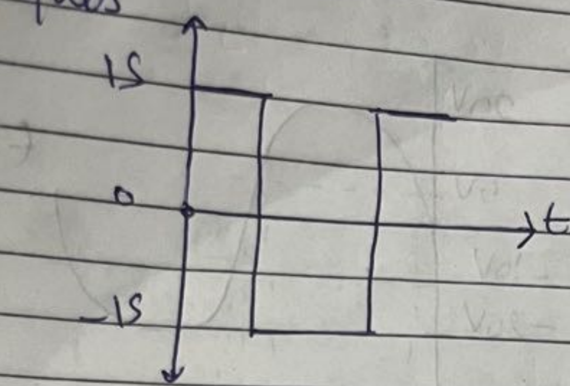
V_o follows V_i $V_i > -10$, D_2 in R·B due to V_2 (O·C)
$V_i < -10$, D_2 in F·B due V_2 (0.7V)



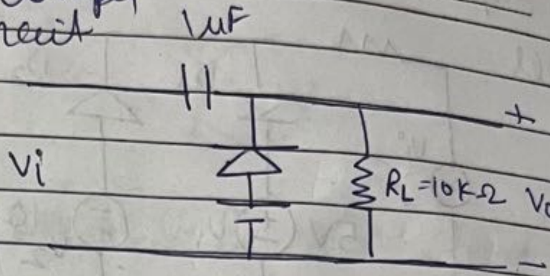
$V_o = -10 - 0.7 = -10.7$

Good Write

Ques



+ve clamper circuit



charging time const (diode)

$\tau = R_f C$

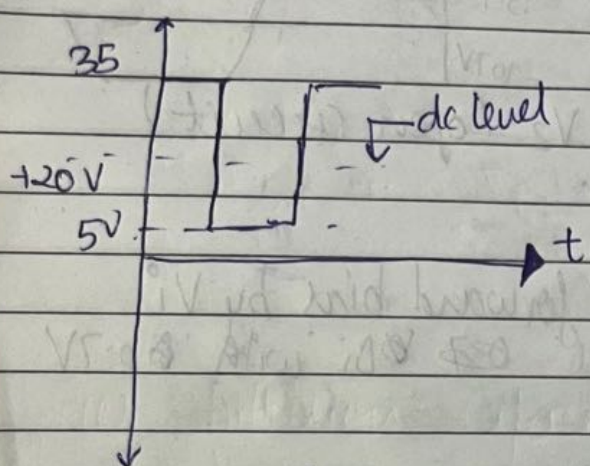
$= 0$

discharging time const, $\tau = R_L C$

$= 1 \times 10^{-6} \times 10 \times 10^{3}$

$= 10ms$

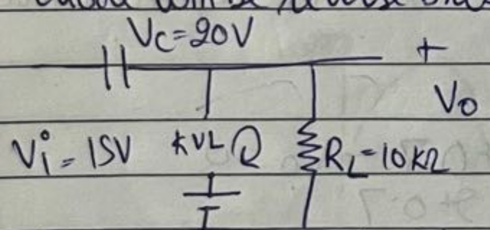
discharg tim $= \tau_D = 5R_L C = 50ms$



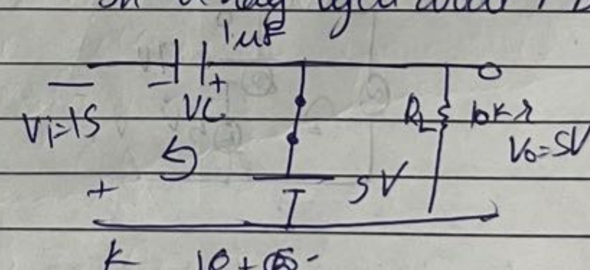
① analyse cycle which will put diode in F.B

+ve half cycle

diode will be reverse bias



In -ve half cycle diode = F.B



$15 + 20 - V_0 = 0$

$V_0 = 35V$

$-15 - 5 + V_C = 0$

$V_C = 20V$

(no explanation) $V_0 = 5V$

Good Write

quest

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Ques State and Prove De-Morgan Theorem

Ans $\overline{X+Y} = \overline{X} \cdot \overline{Y}$

$\overline{X \cdot Y} = \overline{X} + \overline{Y}$

X	Y	$\overline{X}$	$\overline{Y}$	$\overline{X+Y}$	$\overline{X} \cdot \overline{Y}$
0	0	1	1	1	1
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	0	0

equal

$\overline{X \cdot Y}$	$\overline{X} + \overline{Y}$
1	1
1	1
1	1
0	0

equal

de morgan law states that

$\overline{X+Y} = \overline{X} \cdot \overline{Y}$ —①

let us assume —① is true

now we try to prove compliment law

$A + \overline{A} = 1$

$A = \overline{X+Y}$

$\overline{X+Y} + X+Y$

$\overline{X+Y} + X + Y$

$\overline{X} \cdot \overline{Y} + X + Y$

$(\overline{X} + X)(\overline{Y} + X) + Y$

$\overline{Y} + X + Y$

$X + 1 = 1$

$\overline{X \cdot Y} + \overline{X \cdot Y} + \cancel{\overline{X}} + \overline{Y}$

how

$$\overline{X \cdot Y} = \overline{X} + \overline{Y}$$

$$A \cdot \overline{A} = 1 \qquad A = \overline{X \cdot Y}$$

$$\overline{X \cdot Y} \cdot \overline{\overline{X \cdot Y}}$$

$$= \overline{X \cdot Y} \cdot X \cdot Y$$

$$= (\overline{X} + \overline{Y}) X Y$$

$$\overline{X} + (X + \overline{Y})(\overline{Y} + \overline{Y})$$

$$\overline{X} + (X + \overline{Y}) \cdot 1$$

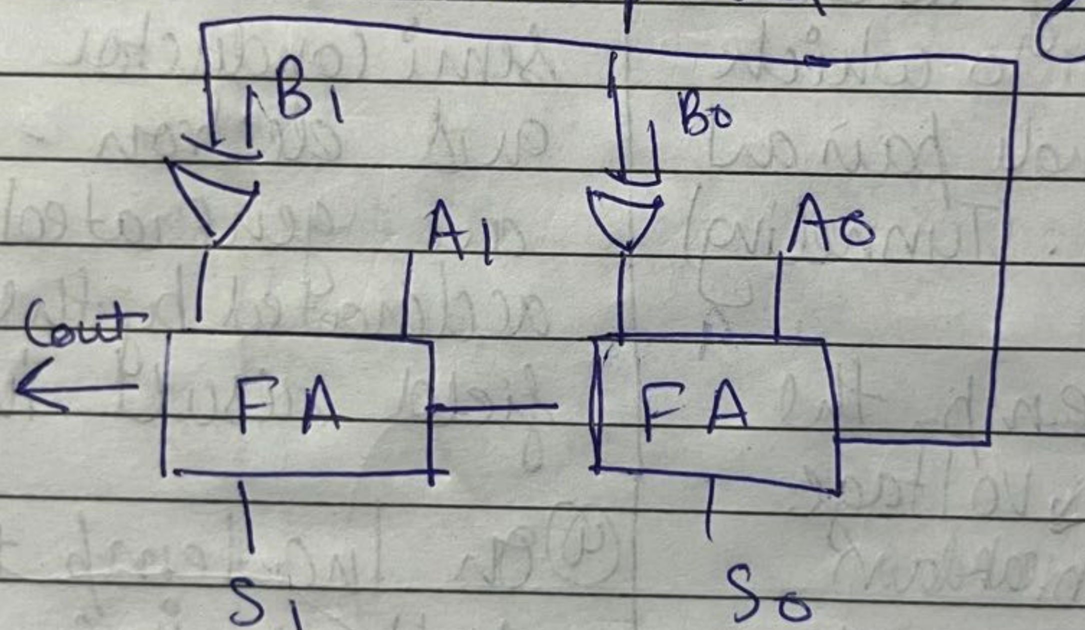
$$\overline{X} + X + \overline{Y}$$

$$1 + \overline{Y} = 1$$

Hence proved

$$= \overline{X\cdot Y}\cdot X\cdot Y$$
$$= (\overline{X}+\overline{Y})XY$$
$$\overline{X}+(X+\overline{Y})(\overline{Y}+\overline{Y})$$
$$\overline{X}+(X+\overline{Y})\cdot 1$$
$$\overline{X}+X+\overline{Y}$$
$$1+\overline{Y}=1$$

Hence proved



$C = 0$ add
$C = 1$ sub

as $I_C = \beta I_B$

Stabilization - process of making operatn pt independent of change in temp changes or variation

Thermal Runaway

Flow of collector current and also the collector leakage current cause heat dissipatn in unstabilized circuit which leads to self destruction

I_C inc

$P = I^2 V$

Stablizatn $\quad I_{CBO} \quad \beta_{dc} \quad V_{BE}$

<u>Voltage divider biasing</u>

3. β $\quad S(\beta) = \frac{\Delta I_C}{\Delta \beta}$ double for 10°C i
In

Ques what is thermal runaway

I_{CBO} , C

$I_C = \alpha I_E + I_{CBO}$

as temp in I_{CBO} inc

I_{CBO} inc I_C inc

$P = I^2 R$

so more power dissipation

To prevent → use heat sink

early effect is main limitation of BJT

disadv

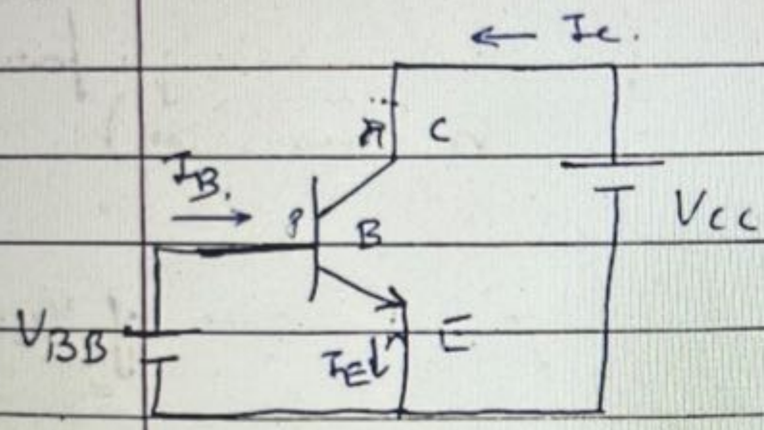
1. Bulky
2. Noisy
3. thermal runaway
4. leakage current at High freq.

adv

1. large gain bandwidth
2. low forward vol. drop
3. low o/p impedance high i/p impedance
4. long life

COMMON EMITTER

→ Most common Configuration.

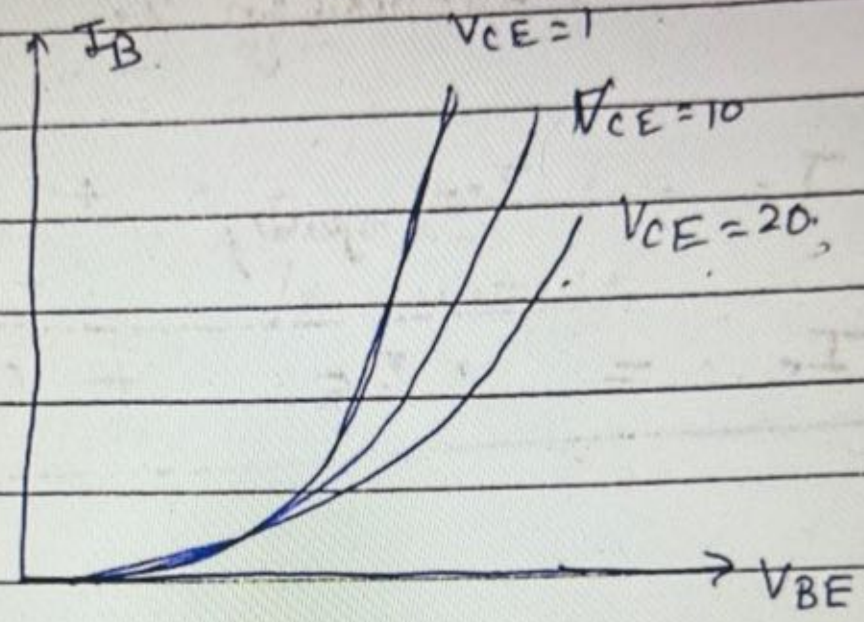


npn CE

For active region $V_{BB} < V_{CC}$

I/P Characteristics

I_B vs V_{BE} for diff values



→ i/p characteristic quite similar to F-B.

→ In comparison with CB, current less rapidly increases with increase in V_{BE}. This means i/p impedence is high for CE. (Details during h-parameter)

→ As the V_{CE} ↑

→ I/P characteristic quite similar to F-B.

→ In comparison with CB, current less rapidly increases with increase in V_{BE}. This means i/p impedence is high for CE. (Details during h-parameter)

→ As the $V_{CE} \uparrow$

I_B decreases for a value of V_{BE}.

→ Why? With increase in V_{CE}, the effective reverse ~~CB~~ voltage is increased b/w B & C, Depletion layer widen, Base width reduces, so less base current.

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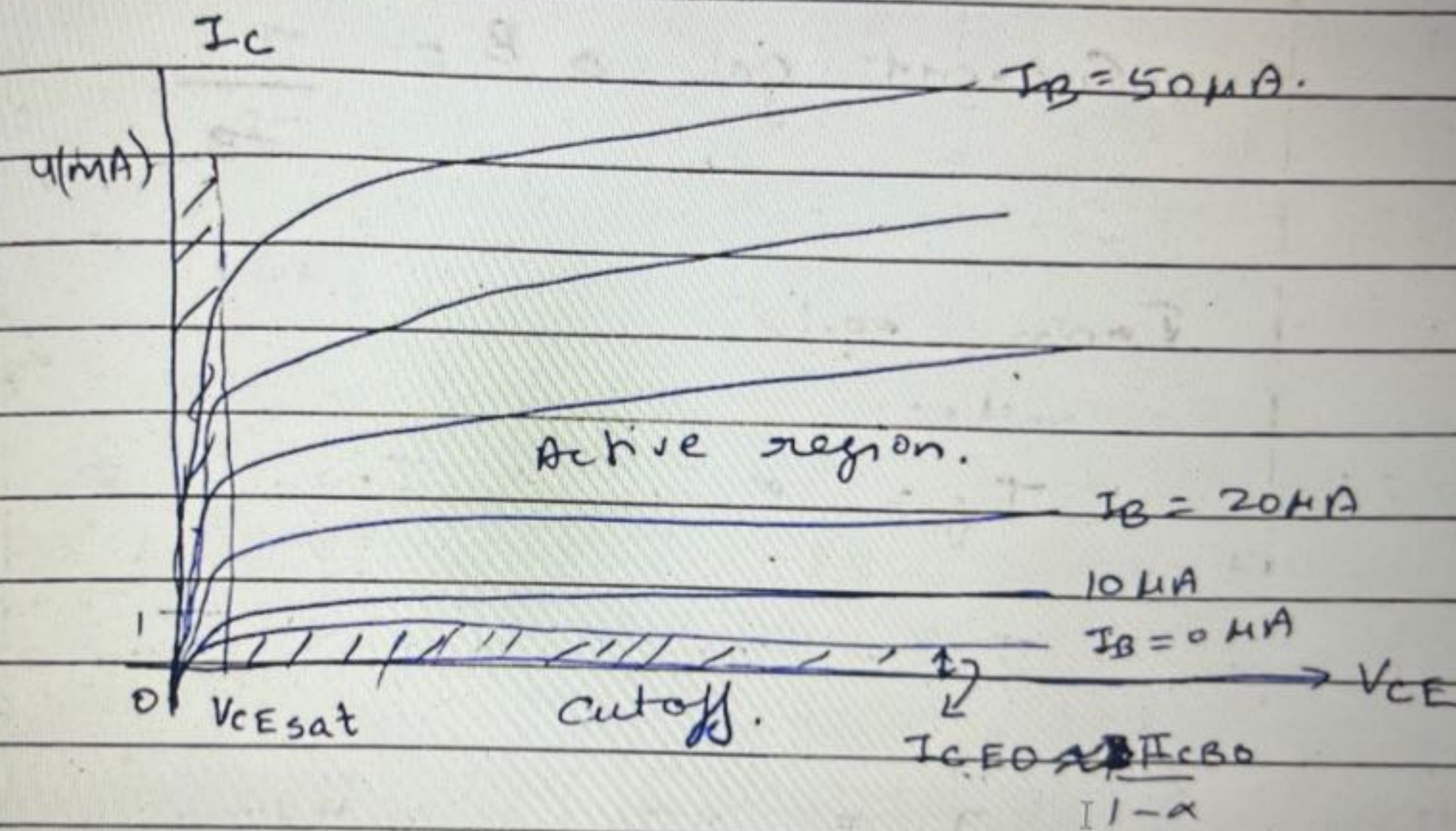
O/p Characterstics.



~~By eg~~ Comparision with CB O/p characteristics:

→ Slope is high.

why → It offer less o/p resistence.

$1-\alpha$

~~By ce~~ Comparision with CB o/p characteristics:

→ Slope is high.

why → It offer less o/p resistance.

I_{CEO} = current when i/p is open circuit, i.e $I_B = 0$.

here I_{CEO} is much higher that I_{CBO}.

(Details after β)

Definition: For ~~basic amplification purposes active region~~ cutoff region for CE,

the I_C current can be defined as.

From eq (2)

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$(1-\alpha) I_C = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

I_C at $I_B = 0$ is I_{CEO}

$$\boxed{I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\mu A}}$$

So it concludes that

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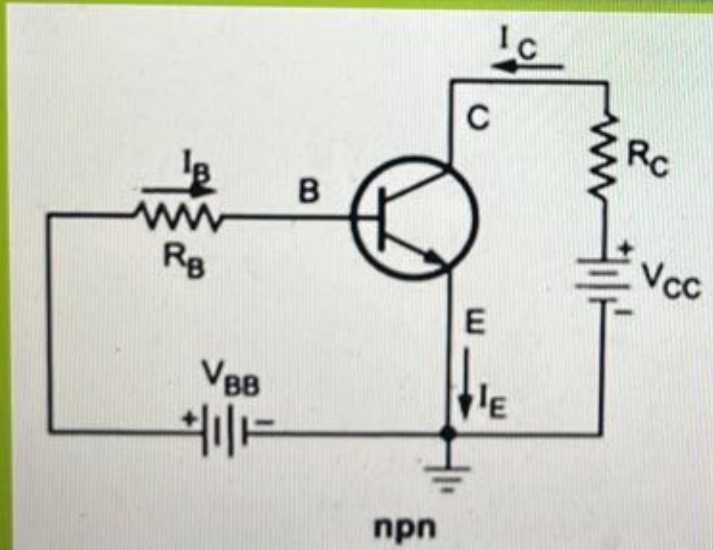
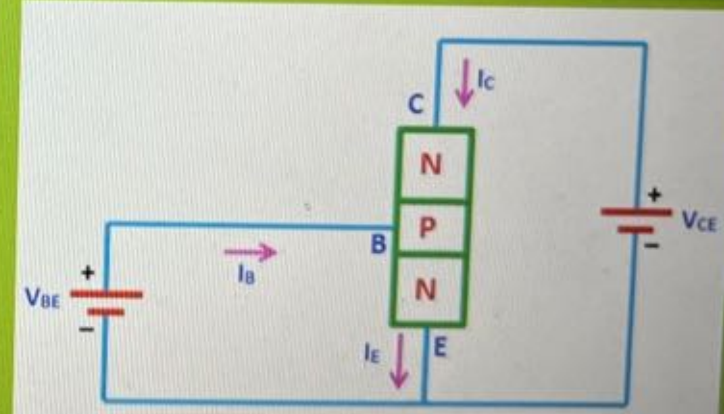
Common Emitter Configuration

ASET

In common emitter configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal for both input and output.

Thus the Emitter terminal of a transistor is common for both input and output terminals and hence it is named as **common emitter configuration.**





Common emitter configuration

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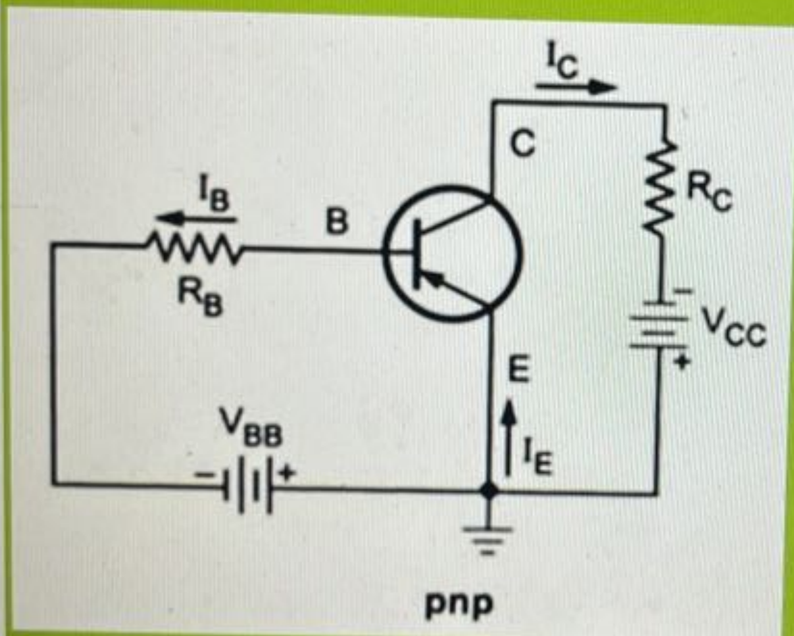

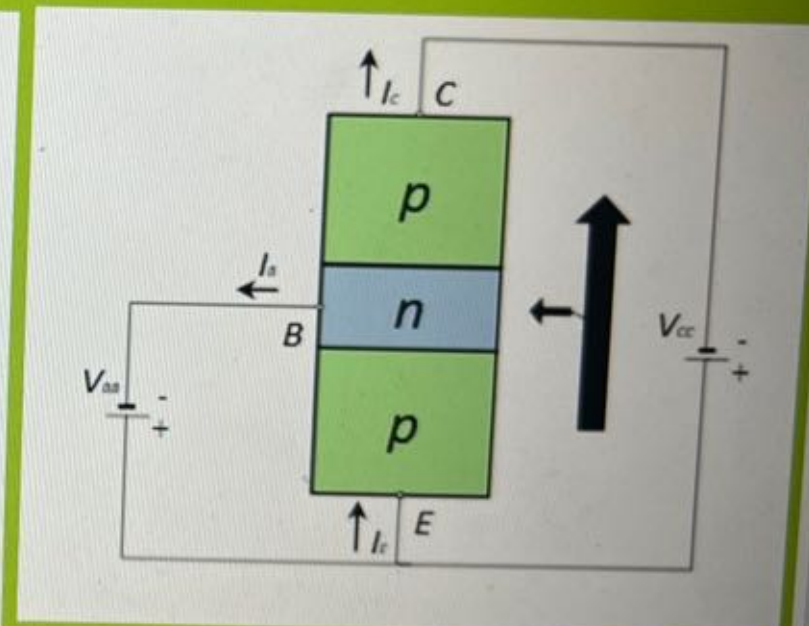

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Input characteristic

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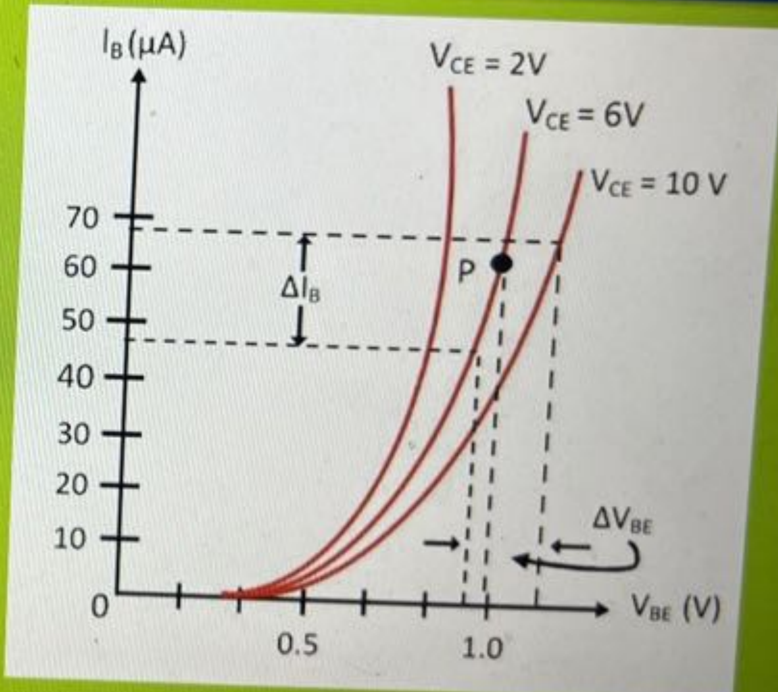
The curve plotted between input current and the input voltage by keeping the output voltage constant is called input characteristics.

Input current-Emitter current I_B
Input Voltage- Emitter-Base voltage V_{BE}
Output Voltage -V_{CE}

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$



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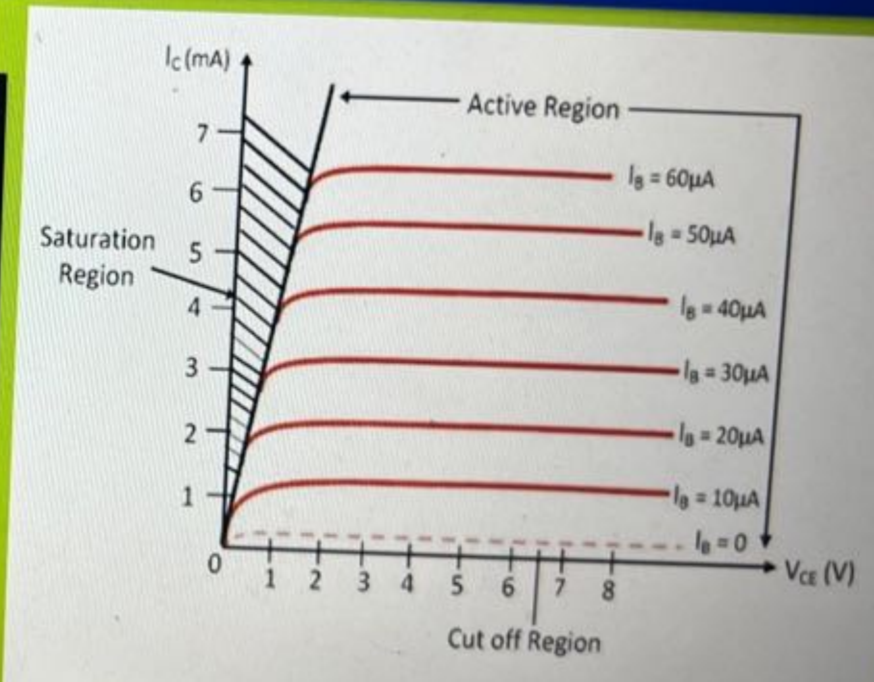
Output Characteristic

ASET

The characteristic curve which is plotted between output current and output voltage by keeping the input current constant is called output characteristic. Also called as collector characteristics.

Output current-collector current I_C
Output voltage- collector-Base voltage V_{CE}
Input current -I_B

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$



$$V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{cc} - I_c R_c - I_c R_E$$

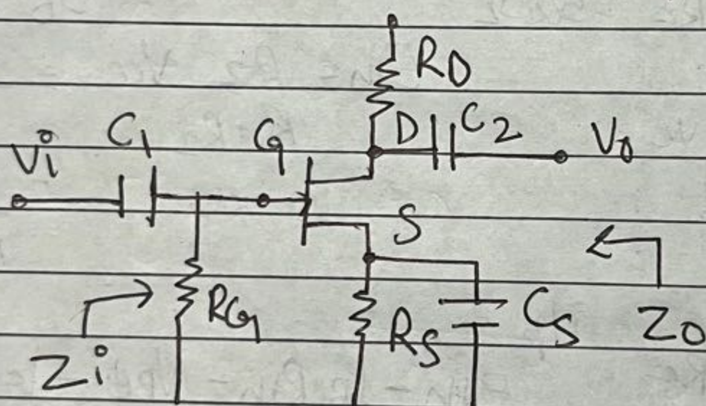
$$= 10 - I_c (R_c + R_E)$$

$$= 10 - 100 \times \left(\frac{3.58 - 0.7}{0.27 + 101 \times 0.56} \right) (1 + 0.56)$$

$\underline{A_v}$ =

Ques

Common source JFET amplifier



$$Z_i = R_G$$

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D \Big|_{r_d \geq 10 R_D}$$

$$A_v = -g_m (r_d \parallel R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \qquad r_d \geq 10 R_D$$

In the absence of r_d

$$\cancel{R_d} \frac{\cancel{g_m R_S}}{1 + \cancel{g_m R_S}}$$

$$A_v = \frac{g_m R_D}{1 + g_m R_S}$$

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Ques Prev year r_d not given

$$A_V = \frac{g_m r_D}{1 + g_m r_S} \quad - (1)$$

$$r_D = R_D \| R_L$$
$$= 6k \| 10k = 3.75\ k\Omega$$

$$r_S = R_S = 4000\ \Omega$$

$$\because A_V = \frac{4000 \times 10^{-6} \times 3.75 \times 10^{3}}{1 + 4000 \times 10^{-6} \times 400}$$

$$A_V = 5.7$$

if $r_S = 0$

$$A_V = g_m r_D = 400 \times 10^{-6} \times 3.35 \times 10^{3}$$
$$= 15$$

n-channel depletion region mosfet $\rightarrow$ working (3 mode) V_{GS}

S G D

Q-3

$$gain = \left(\frac{-400}{4}\right) = -100$$

$$v_o = (-100) \times \left(\frac{0.2}{10}\right) = (-2.0)\,V$$

$$R_i = \infty$$

$$R_o = 0$$

$$I_i = \left(\frac{0.2}{4 \times 10^3}\right) = 0.05\,mA$$

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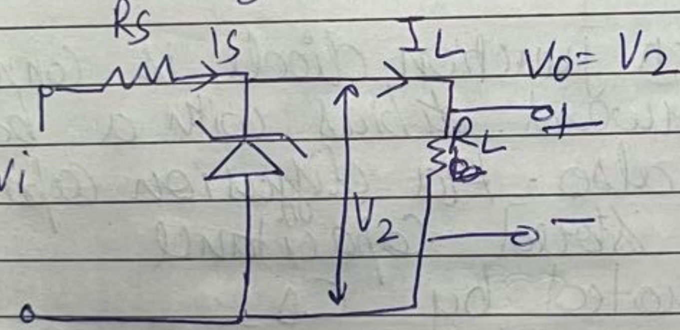
Ques show how zener diode can be used as voltage regulator.

Ans define zener diode
tell it's working
show graph
} if compulsory or 5 mark alone questn

zener diode are widely used as shunt voltage regulator for small load. This is done by attaching it parallely to the load. The Breakdown voltage remain const. for variety of current. We attach it such a way that it remains in reverse bias. When zener diode voltage exceed knee voltage voltage become const



Ques designing voltage regulator $V_0 = 30V$ $R_L = 1.2 K\Omega$
$V_i = 40V \sim 60V$

Rs, I_L and I_{ZM}

Ans $V_0 = V_L = 30$

using voltage divider rule on V_i 400

$$V_0 = \frac{R_L V_i}{R_L + R_S}$$

$1.2K \times R_S = 1200 \times 40$

$$30 = \frac{1.2K \times 40}{R_L + R_S}$$

$$R_S = \frac{\cancel{400}}{\cancel{1200}}$$

$1.6 - 1.2$
$= 0.4 K\Omega$

$1.2K + R_S = 400 \times 4$

$R_S = 3.33 K\Omega$

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for I_L

$$I_{R_S} = \frac{V_i - V_L}{R_S}$$

$$= \frac{60-30}{\cancel{333}\ 0.4} = \frac{30}{\cancel{333}\ 0.4\,k\Omega} = \frac{30 \times 10^{-3}}{0.4} = 75\,mA$$

$$I_L = \frac{V_L}{R_L} = \frac{3\cancel{0}}{\cancel{12}0\cancel{0}} = \frac{1}{4} \times 10^{-1} = 0.025\,A = 25\,mA$$

for I_{ZM}

$$I_{ZM} = I_{R_S} - I_L$$

$$= 75 - 25\,mA$$

$$= 50\,mA$$

Ques Diffusion capacitance

Ans when a p-n junction diode is connected in forward bias with a battery it is also k/a diffusion capacitance or stored capacitance denoted by C_D

It occurs due to stored charge of minority charge carrier ~~holes~~ in p-side & holes in n-side. It is very dense near the junction. The density decreases as distance increases. It is more than transition capacitance

$$C_D = \frac{i\tau}{nV_T}$$

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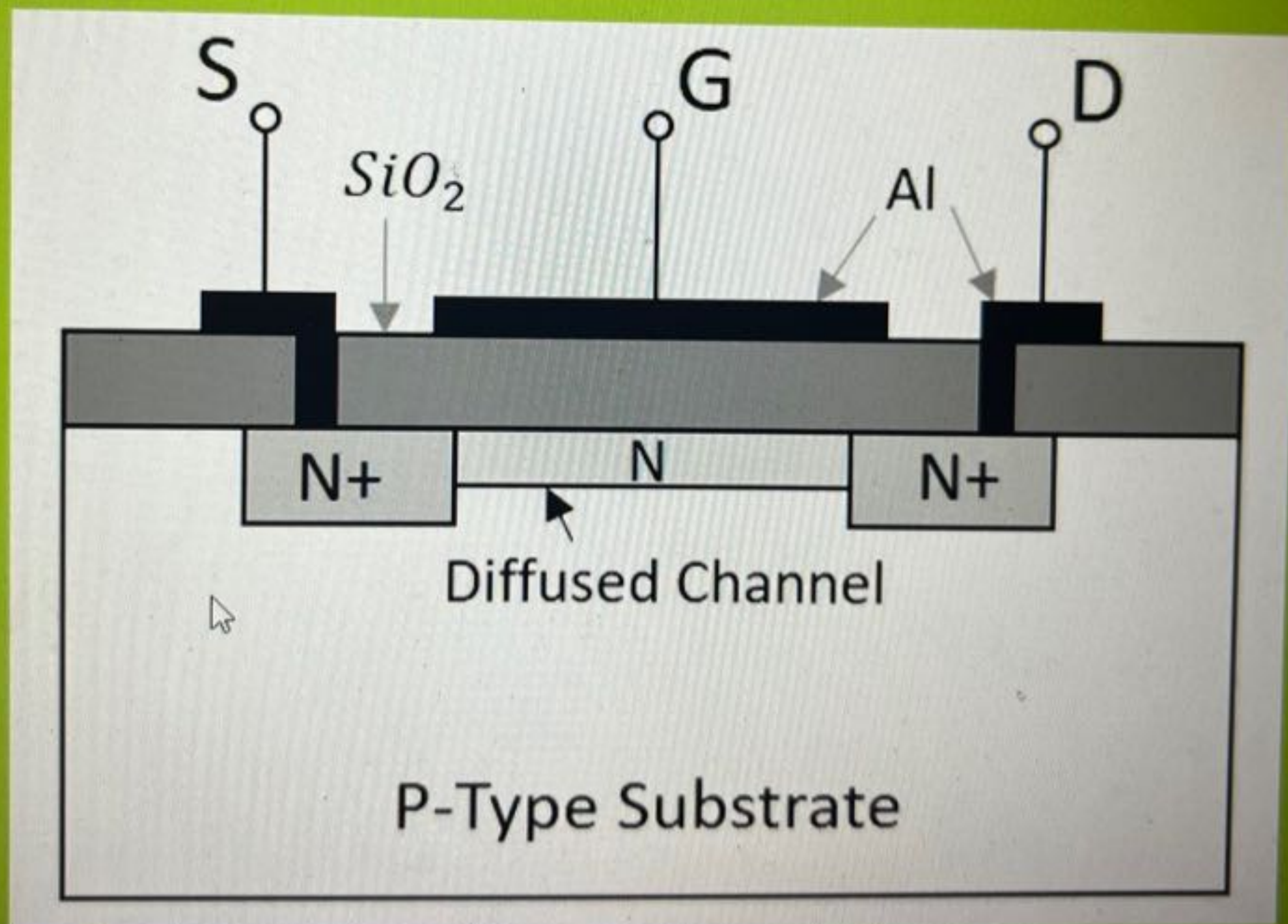
Depletion-Type MOSFET

ASET

Construction of N-channel Depletion MOSFET



P-type substrate is taken into which two heavily doped N-type regions are diffused, which ac

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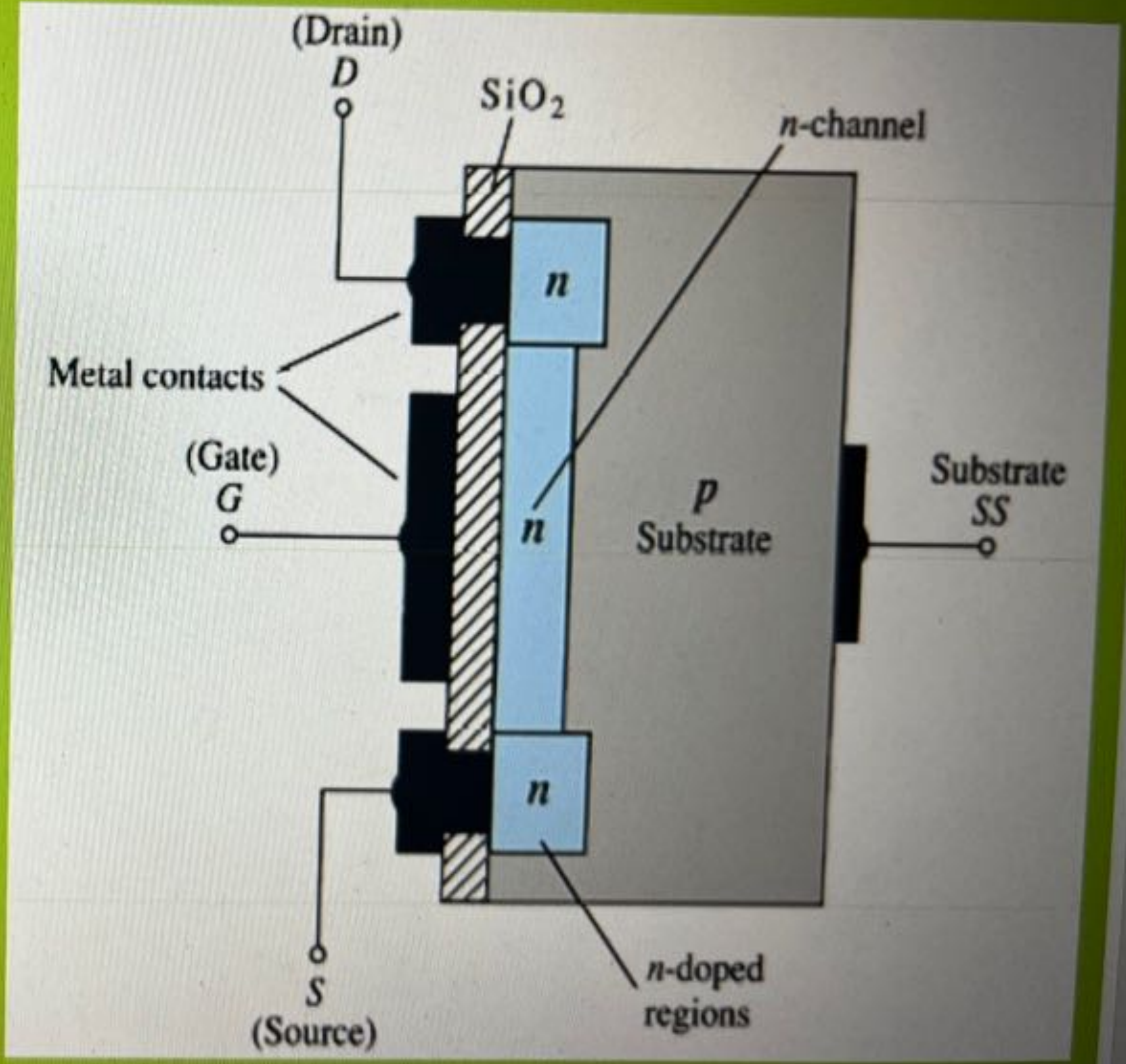
Depletion-Type MOSFET Construction

ASET

DE-MOSFET

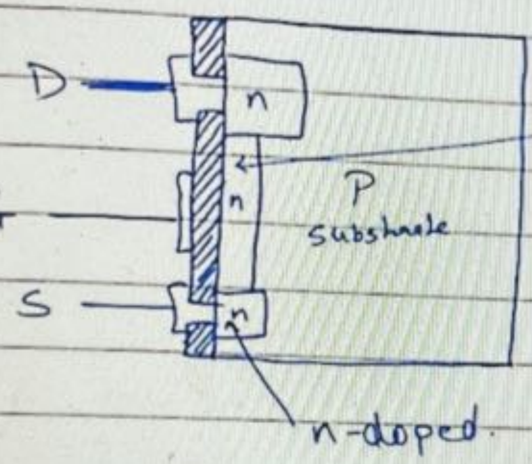
The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of SiO_2.



can be operated with either a positive or a negative gate. When gate is positive with respect to th

Depletion Type MOSFET.

→ Same structure with one ~~extra~~ addition.
n-channel adjacent to SiO_2



n channel. (Type of impurity is same as that of S& D.)

Operation

→ Like JFET.

$V_{GS} = 0$ $V_{DS} = +ve$ Current flow.

$V_{DS} = \uparrow$ current reach

Operation

→ Like JFET.

$V_{GS} = 0$ $V_{DS} = +ve$ current flow.

$V_{DS} = \uparrow$ current reach saturation because of pinch-off

→ As $V_{GS} \uparrow$ pinch-occur on higher value of V_{DS}.

→ $V_{GS} \downarrow$ pinch-off occur at lower values of V_{DS}.

→ $V_{GS} < 0$, For -ve value, e^- get repeled and at $V_{GS} = V_P$ (a negative value)

classmate

Date

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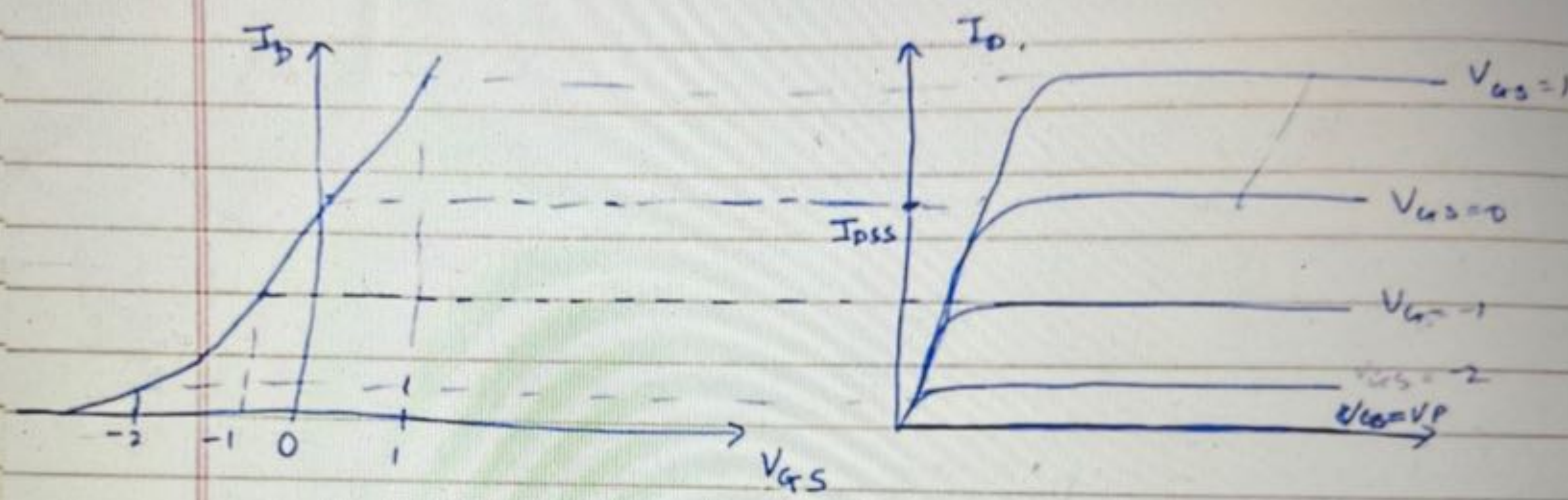
Characteristic Curve.



Equation: Same as that of JFET

Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2.$$

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