

Computer organization and architecture (PCC-CS-402) PYQs analysis

Based on: May 2019, Oct 2020, May 2024

- **Module 1:**

- Functional blocks of a computer (CPU, memory, input–output subsystems, control unit)
- Instruction set architecture (registers, instruction execution cycle, RTL interpretation, addressing modes, instruction set)
- Data representation (signed numbers, fixed/floating-point, character representation)
- Computer arithmetic (integer addition/subtraction, ripple carry adder, carry look-ahead adder, multiplication: shift-and-add, Booth multiplier, carry save multiplier, division: restoring/non-restoring, floating-point arithmetic)

- **Module 2:**

- Introduction to x86 architecture
- CPU control unit design (hardwired, micro-programmed, hypothetical CPU case study)
- Memory system design (semiconductor memory technologies, memory organization)
- Peripheral devices and I/O (I/O subsystems, device interfaces, program-controlled I/O, interrupt-driven I/O, DMA, privileged/non-privileged instructions, software interrupts, exceptions, SCII, USB)

- **Module 3:**

- Pipelining (basic concepts, throughput, speedup, pipeline hazards)
- Parallel processors (introduction, concurrent memory access, cache coherency)

- **Module 4:**

- Memory organization (memory interleaving, hierarchical memory, cache memory, cache size vs. block size, mapping functions, replacement algorithms, write policies)

- **Repeated Questions** (identical wording, topic, approach):

1. **Effective address calculation** (Module 1, Instruction set architecture):

- **2019**

- ***Q3(c)***: “An instruction is stored at location 300 with address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) immediate (iii) relative, and (iv) indirect.” *3 marks*
- ***2020***
 - ***Q2(a)***: “An instruction is stored at location 800 with address field at location 801. The address field has the value 900. A processor register Rx contains the number 800. Evaluate the effective address if the addressing mode of instruction is (i) direct (ii) immediate (iii) relative (iv) register indirect.” *4 marks*
- ***2024***
 - ***Q1(i)***: “An instruction is stored at location 200 with address field located at 201. The value of address field is 320. A processor register R1 contains the value 500. Calculate the effective address if the addressing mode is: (i) Direct (ii) Relative (iii) Register indirect.” *1.5 marks*
 - **Deviation:** 2024 omits “immediate” mode and uses different numerical values, but the structure and approach are identical.

2. Booth algorithm multiplication (Module 1, Computer arithmetic):

- ***2019***
 - ***Q2(c)***: “Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 4-bit registers for holding signed numbers. Multiplicand is +5: (i) $(+5) \times (+3)$ (ii) $(+5) \times (-3)$.” *4.5 marks*
- ***2020***
 - ***Q3(b)***: “Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 4-bit registers for holding signed numbers: (i) $(+5) \times (+3)$ (ii) $(-5) \times (-3)$.” *4 marks*
- ***2024***
 - ***Q3(b)***: “Obtain the result of multiplying (-6) and (-9) using Booth’s multiplier. Draw the flowchart to justify the steps used in obtaining the result.” *5 marks*
 - **Deviation:** Different numbers and inclusion of flowchart in 2024, but same algorithm and approach.
- **Similar Questions** (same topic, minor deviations):

1. Programmed vs. interrupt-driven I/O (Module 2, Peripheral devices and I/O):

- **2019**
 - **Q7(a):** "Differentiate between programmed I/O and interrupt-driven I/O. What is basic advantage of using interrupt-initiated data transfer over transfer under program control without interrupt?" *7 marks*
- **2020**
 - **Q5(c):** "Explain program controlled and interrupt initiated data transfer." *5 marks*
- **2024**
 - **Q7(a,d):** "Priority interrupts" *3 marks* and "Hardware interrupts" *3 marks*
 - **Deviation:** 2024 focuses on specific interrupt types, but all relate to interrupt-driven I/O concepts.

2. Division process (Module 1, Computer arithmetic):

- **2019**
 - **Q2(d):** "Show the contents of registers E, A, Q and SC during the process of division of (i) 10100011 by 1011 (ii) 11110000 by 0011." *7.5 marks*
- **2020**
 - **Q3(c):** "Show the contents of registers E, A, Q and SC during the process of division of (i) 10110011 by 1001 (ii) 11110000 by 0011." *5 marks*
- **2024**
 - **Q1(e):** "Draw the flowchart explaining the process of non-restoring division algorithm." *1.5 marks*
 - **Deviation:** 2024 focuses on the flowchart for non-restoring division, but all address division algorithms.

3. Flynn's classification (Module 3, Parallel processors):

- **2019**
 - **Q7(b):** "Give Flynn's Classifications of parallel processors." *4 marks*
- **2024**
 - **Q2(a):** "Explain Flynn's classification of parallel processors." *5 marks*
- **Deviation:** 2024 requires more detailed explanation, but same topic.

4. DMA controller (Module 2, Peripheral devices and I/O):

- **2019**
 - **Q6(b):** "Discuss different modes of DMA data transfer." *7 marks*
- **2020**
 - **Q5(b):** "Explain DMA. Discuss DMA controller using block diagrams." *5 marks*
- **2024**
 - **Q6(b):** "Explain the working of a DMA controller with the help of block diagram. What are the various modes of transfer used by DMA?" *10 marks*
- **Deviation:** 2024 combines explanation and modes with higher weightage, but same core concept.

5. Microprogrammed control unit (Module 2, CPU control unit design):

- **2020**
 - **Q4(a):** "What is meant by Micro programmed Control? Draw and explain the design of such a control unit." *10 marks*
- **2024**
 - **Q4(b):** "What is micro-programmed control unit? How to obtain address sequencing?" *10 marks*
- **Deviation:** 2024 emphasizes address sequencing, but both focus on microprogrammed control design.

6. RISC vs. CISC (Module 1, Instruction set architecture):

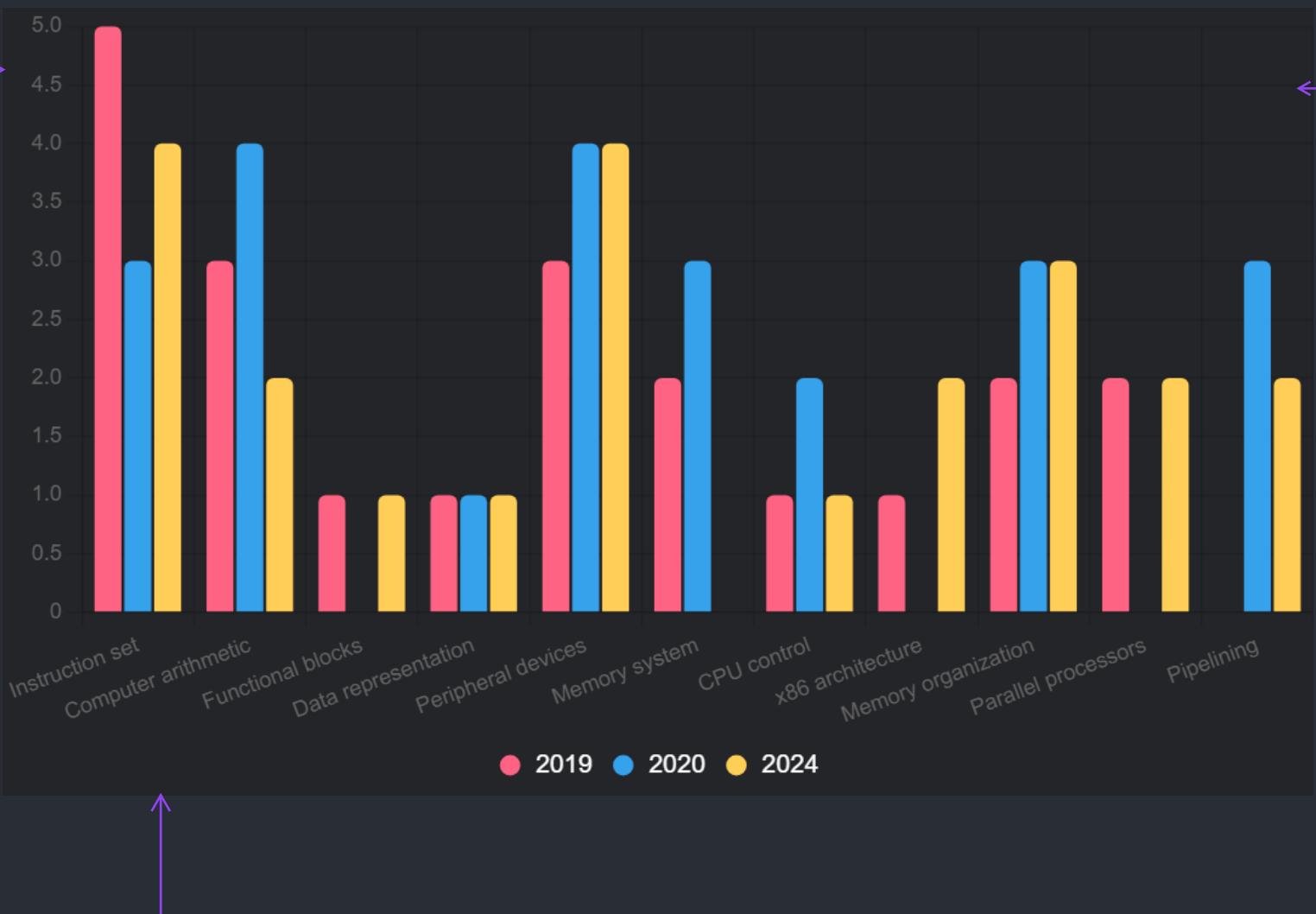
- **2019**
 - **Q5(c):** "Differentiate between RISC and CISC instruction sets." *3 marks*
- **2024**
 - **Q7(c):** "RISC vs. CISC instruction sets." *3 marks*
- **Deviation:** Identical phrasing, minor format difference (short note in 2024).
- **Latest Questions (unique to 2024):**
 1. **Stored program control** (Module 1, Instruction set architecture):
 - **Q1(a):** "What do you mean by stored program control concept?" *1.5 marks*

2. **Program status word** (Module 1, Instruction set architecture):
 - ***Q1(b)***: "What is program status word?" ***1.5 marks***
3. **8085 vs. 8086** (Module 2, x86 architecture):
 - ***Q1(f)***: "Bring out the differences between 8085 and 8086 microprocessors." ***1.5 marks***
4. **Stack-based CPU organization** (Module 1, Instruction set architecture):
 - ***Q3(a)***: "Explain stack based CPU organization. Use a suitable example to demonstrate the types of instruction formats used in this type of organization." ***10 marks***
5. **8086 status/flag register** (Module 2, x86 architecture):
 - ***Q5(a)***: "Explain the 16-bit status/flag register in 8086 microprocessor. If an addition operation is performed on two values -81 and FE (hexadecimal), what is the resultant value of this register?" ***5 marks***

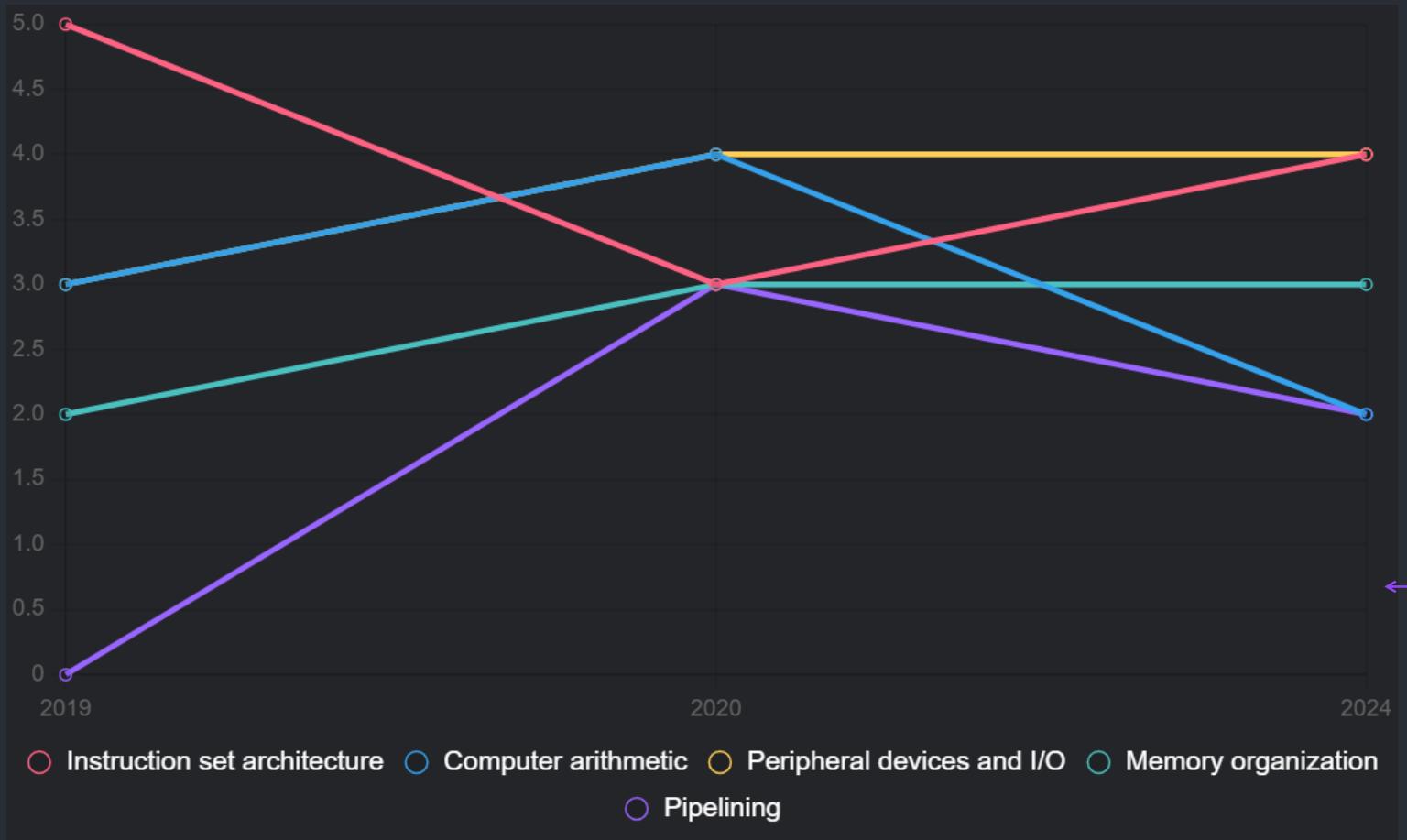
PYQFort by Praxian :)

PYQ means "PYQFort"

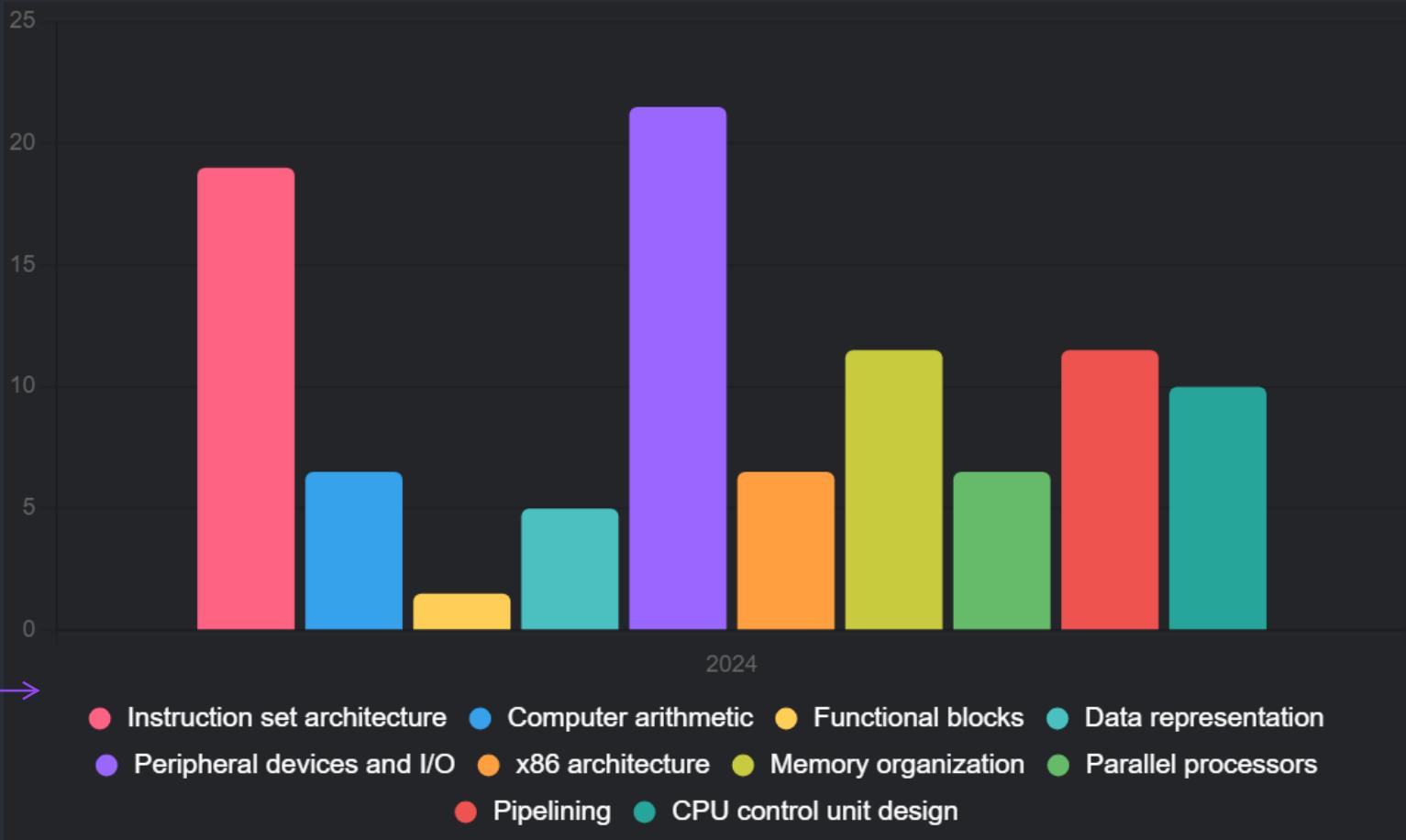
Visual Data Insights



Bar Chart: Number of questions per topic



Line Graph: Frequency trends of top 5 topics



→ **Stacked Bar Chart: Marks distribution across topics for 2024**

Original Data



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May, 2019

B.Tech. - IV SEMESTER

Computer Organization & Architecture (PCC-CS-402)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART-A

1. (a) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two address instructions, how many one-address instructions can be formulated? (1.5)
(b) Execute and share the result when Logical X-OR operation is applied to $(4AC0)_{16}$ & $(B53F)_{16}$. (1.5)
(c) Differentiate between decoder and demultiplexer. (1.5)
(d) Why are addressing modes necessary in computer architecture? (1.5)
(e) Represent (-18) in signed 1's complement and signed 2's complement representation. (1.5)

- (f) An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in the address and memory spaces? (1.5)
- (g) Represent the following conditional statement by two register transfer statement with control functions.
If ($P=1$) then ($R_1 \rightarrow R_2$) else if ($Q=1$) then ($R_1 \leftarrow R_3$). (1.5)
- (h) What does CMA, ISZ, SNA, SKI, ION signifies? (1.5)
- (i) Explain the terms : seek time, rotational latency, and transfer time. (1.5)
- (j) A bus has 16 data lines and requires 4 cycles of 250 ns each to transfer data. The bandwidth of the bus is 2 MBps. If the cycle time of the bus is reduced to 125 ns what would be the bandwidth of the bus? (1.5)

PART-B

2. (a) Design 4-bit by 4-bit array multiplier. Use AND gates and Binary adder. (4)
- (b) Give a flowchart for add and subtract operations. (3)
- (c) Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 4-bit registers for holding signed numbers. Multiplicand is +5:
- (i) $(+5) \times (+3)$
- (ii) $(+5) \times (-3)$. (4)

- (d) Show the contents of registers E, A, Q and SC during the process of division of
(i) 10100011 by 1011
(ii) 11110000 by 0011.
(use a dividend of 8bits). (4)

3. (a) Draw the timing diagram assuming that SC = 0 at the time T3 if control signal C7 is active C7T3 : SC-->0. C7 is activated with the positive clock transition associated with T1. (5)
(b) Discuss the different addressing modes. Also highlight the difference between indexed addressing and base register addressing modes? (6)
(c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) immediate (iii) relative, and (iv) indirect. (4)

4. (a) Explain the three types of mapping procedures used in the organization of cache memory. (10)
(b) A computer uses RAM chips of 1024×1 capacity.
(i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes.
(ii) How many chips are needed to provide a memory capacity of 16K Bytes ?
Show the connection diagram for the same. (3)

(c) What is miss rate and miss penalty? (2)

5. (a) Give a brief architecture of 8086 microprocessor. (5)
- (b) Discuss the different types of instructions that are commonly incorporated in computer systems. Also explain three instructions of each type for Berkeley RISC I. (7)
- (c) Differentiate between RISC and CISC instruction sets. (3)
6. (a) What is asynchronous data transfer? Discuss asynchronous data transfer using (i) strobe control and (ii) handshaking with timing and block diagram. (8)
- (b) Discuss different modes of DMA data transfer. (7)
7. (a) Differentiate between programmed I/O and interrupt-driven I/O. What is basic advantage of using interrupt-initiated data transfer over transfer under program control without interrupt? (7)
- (b) Give Flynn's Classifications of parallel processors. (4)
- (c) What do you mean by memory and cache coherence? (4)

May 2024**B. Tech. (CE/CE(HINDI)/IT/CSE(AIML))****(Fourth Semester)****Computer Organization and Architecture****(PCC-CS-402)****Time : 3 Hours]****[Maximum Marks : 75**

Note : It is compulsory to answer all the questions (1.5 marks each) of Part A in short. Answer any four questions from Part B in detail. Different sub-parts of a question are to be attempted adjacent to each other.

Part A

1. (a) What do you mean by stored program control concept ? 1.5
- (b) What is program status word ? 1.5
- (c) Explain the concept of Cache Coherence. 1.5
- (d) Differentiate between computer architecture and computer organization. 1.5
- (e) Draw the flowchart explaining the process of non-restoring division algorithm. 1.5

- (f) Bring out the differences between 8085 and 8086 microprocessors. 1.5
- (g) Briefly explain the different I/O interfaces - PCI, SCSI, USB. 1.5
- (h) How can we calculate the speedup and throughput of a system ? 1.5
- (i) An instruction is stored at location 200 with address field located at 201. The value of address field is 320. A processor register R1 contains the value 500. Calculate the effective address if the addressing mode is : 1.5
- (i) Direct
 - (ii) Relative
 - (iii) Register indirect
- (j) What is memory interleaving ? How is it useful ? 1.5

Part B

2. (a) Explain Flynn's classification of parallel processors. 5
- (b) Represent the decimal number $(-262.125)_{10}$ in single precision floating point format. 5
- (c) Explain the ripple carry adder/subtractor using the circuit diagram. 5

3. (a) Explain stack based CPU organization. Use a suitable example to demonstrate the types of instruction formats used in this type of organization ? 10
- (b) Obtain the result of multiplying $(-6)_{10}$ and $(-9)_{10}$ using booth's multiplier. Draw the flowchart to justify the steps used in obtaining the result. 5
4. (a) What is asynchronous data transfer ? Explain any *one* method used in asynchronous data transfer in detail. 5
- (b) What is micro-programmed control unit ? How to obtain address sequencing ? 10
5. (a) Explain the 16-bit status/flag register in 8086 microprocessor. If an addition operation is performed on two values – 81 and FE (hexadecimal), what is the resultant value of this register ? 5
- (b) What are the various pipeline hazards that are likely to occur in computer architecture ? 10
6. (a) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit

words. Calculate how many bits are required for addressing the main memory ? Also, how many bits are needed to represent the TAG, SET and WORD fields ? 5

(b) Explain the working of a DMA controller with the help of block diagram. What are the various modes of transfer used by DMA ? 10

7. Write short notes on the following : 15

- (a) Priority Interrupts
- (b) Write-back and Write-through policies
- (c) RISC vs. CISC instruction sets
- (d) Hardware interrupts
- (e) Hierarchical memory organization

Time: 3 hours

Max. Marks: 75

PART A (1.5 marks each)

- Q1** (a) Define Memory Address Register.
(b) What do you understand by bus arbitration?
(c) Perform $(12)_{10} - (14)_{10}$ using 2's complement notation.
(d) What is the difference between a subroutine and an Interrupt Service Routine (ISR) ?
(e) Under what situations the microprogram counter is not incremented after a new instruction is fetched from microprogram memory?
(f) Determine the four pages that are resident in the memory after each page reference change, if the replacement algorithm used is FIFO page if the following references to pages are made: 4 2 0 1 2 6 1 4 0 1 0 2 3 5 7.
(g) Differentiate between SRAM and DRAM.
(h) How many memory chips are needed to construct a $2M \times 16$ memory system using $512k \times 8$ memory chips?
(i) What are the major characteristics of a Pipeline?
(j) Draw a space time diagram for a 4-segment pipeline showing the time to process six tasks.

PART B

- Q2** (a) What are addressing modes? An instruction is stored at location 860 with address field at location 801. The address field has the value 960. A process or register Rx contains the number 800. Evaluate the effective address if the addressing mode of instruction is (i) direct (ii) immediate (iii) relative (iv) register indirect (4)
(b) What are different types of instruction in a basic CPU? Name a few of each type. (4)
(c) Design a 4-bit carry look-ahead adder. (4)
(d) What is RTL? Write RTL representation and interpretation for loading a register. (3)
- Q3** (a) Represent 52.21875 in 32-bit binary floating point format. (3)

- (b) Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 4-bit registers for holding signed numbers: (i) (+5) x (+3) (ii) (-5) x (-3) (2)
- (c) Show the contents of registers E, A, Q and SC during the process of division of (i) 10110011 by 1001 (ii) 11110000 by 0011. [use a dividend of 8 bits.] (5)
- (d) Starting from an initial value of R=11110110, determine the sequence of binary values of R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. (5)

Q4 (a) What is meant by Micro programmed Control? Draw and explain the design of such a control unit. (10)
 (b) What are static and dynamic memories? Explain. (5)

Q5 (a) With the help of a diagram, describe USB architecture. (5)
 (b) Explain DMA. Discuss DMA controller using block diagrams. (5)
 (c) Explain program controlled and interrupt initiated data transfer. (5)

Q6 (a) Draw and explain the flowchart for the interrupt cycle. (5)
 (b) Explain set associative cache organization with a suitable example. (5)
 (c) Explain the different write policies. (5)
 (d) What is meant by memory interleaving? Explain. (5)

Q7 Write short notes on:
 (i) Pipelining and its hazards. (8)
 (ii) Booth's multiplication. (7)



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