Study and Design of Phase Frequency Detector(PFD) for PLL on TSMC 65nm Technology

Report submitted for partial fulfilment of
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Bachelor of Technology / UG 3rd Year

By

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DECLARATION

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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Date : 05/05/24

ABSTRACT

A phase locked loop is used in synchronization of frequency synthesis of clocks and data recovery circuits. It is comprised of PFD, charge pump, loop filter, oscillator, divider. The phase frequency detector(PFD) in PLL compares two input clocks to produces output whose duty cycle is proportional to input phase/frequency difference. Main issues in PFD are dead zone and blind zone. This design aimed at resolving those issues on TSMC 65nm technology. Also, the effect of different parameters on the PFD design and the issues were studies through simulations and presented

CONTENTS

List of Figures

1. Introduction

The PLLs serve as crucial components in generating stable, high-frequency signals essential for various wireless communication functionalities. To meet the escalating demands of future wireless networks, the focus lies on enhancing the performance of PLLs to ensure efficient and reliable operation at millimetre-wave frequencies. Achieving wider bandwidths and lower spurious tones while minimizing noise is paramount for enabling seamless transmission of large volumes of data across the network.

Moreover, advancements in PLL design are pivotal for supporting emerging applications that heavily rely on high-speed data transfer, such as 5G and beyond, Internet of Things (IoT), and autonomous vehicles. By pushing the boundaries of PLL technology, researchers and engineers aim to unlock the full potential of mm-wave frequencies, paving the way for next-generation wireless networks capable of handling the immense data traffic expected in the foreseeable future. This concerted effort towards developing robust and efficient mm-wave circuits and systems underscores the relentless pursuit of innovation in the field of wireless communication.

Phase locked-loop (PLL) circuit consist of phase-frequency detector (PFD), charge pump (CP), loop filter, voltage-controlled oscillator (VCO) and programmable frequency divider blocks as in the Fig(a) below.

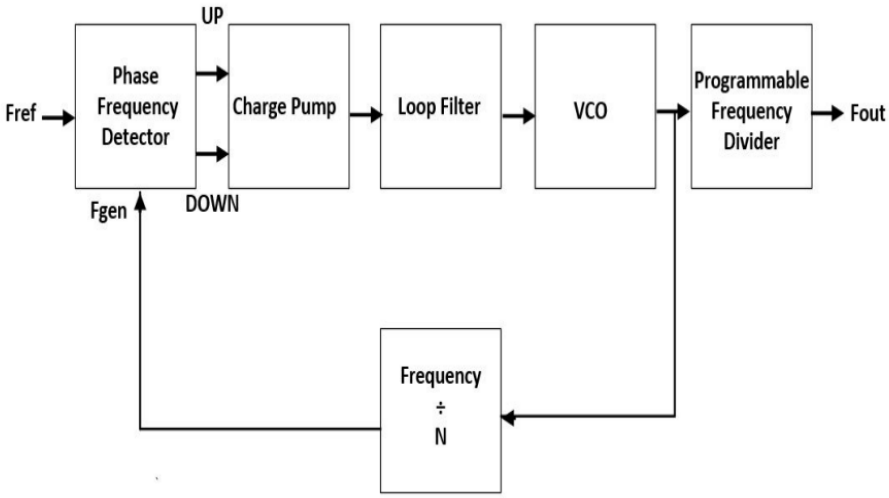

Fig 1(a) : CP based Phase Locked Loop (PLL)

At its core, a Phase-Locked Loop (PLL) functions by aligning the Voltage-Controlled Oscillator (VCO) output, which is fed back through a loop, with the output of a reference clock. This synchronization process is orchestrated through a series of precise steps.

Initially, the Phase Frequency Detector (PFD) detects any phase discrepancy between the feedback and reference signals, generating UP and DOWN pulses whose durations correspond to the phase offset. These pulses serve as triggers, initiating the flow of charge pump currents through the loop filter. When the UP pulse is generated, the charge pump drives current into the loop filter, resulting in its charging. Conversely, during the DOWN pulse, the charge pump discharges current, facilitating the filter's discharge. Consequently, a voltage signal proportional to the phase or frequency difference between the reference and feedback signals emerges at the output of the loop filter.

This voltage signal plays a pivotal role as the control voltage for the VCO, influencing its oscillation frequency. By adjusting the VCO's frequency in response to this control voltage, the PLL ensures that its output is synchronized with the reference clock, multiplied by a factor denoted as 'N'. This multiplication factor enables the PLL to adapt to various frequency requirements, providing flexibility in its application across diverse scenarios.

The better working of PLLs is analysed in terms of faster frequency acquisition, low output jitter and phase noise, low power consumption, wide bandwidth and more. These performance metrics in turn depends upon the individual component performances of PFD, charge pump, loop filter, VCO and frequency divider. Out of the performance metrics of the PFD, the dead zone and blind zone are very important as they are directly related to output phase noise, higher frequency acquisition range etc.

For very small phase offsets between the reference and feedback signals, the phase frequency detector would be unresponsive is called the ‘dead zone’ in a PFD. Also, for very large phase offsets in range of $[-2\pi, -2\pi + \theta]$ and $[2\pi, 2\pi - \theta]$, the PFD detects the lagging signal edge first and fails to detect the rising edge of leading phase signal which results in reversed phase information. This is the ‘blind zone’ in a PFD.

So, the main objective of my project is to address these two issues in the phase frequency detector(PFD) design of a PLL.

2. Literature Survey

- The Literature survey is done through researching and analysing different research papers published in IEEE transactions, journals and conferences by researchers all over the globe.
- The literature discussed in this section gave an idea to different design issues, parametric dependences of those issues and methods used to resolve them.

2.1 Conventional PFD :

- Firstly, I studied the conventional PFD from [1], which is designed using the sequential flip-flops along with a AND or NAND gate used to generate the reset pulse.

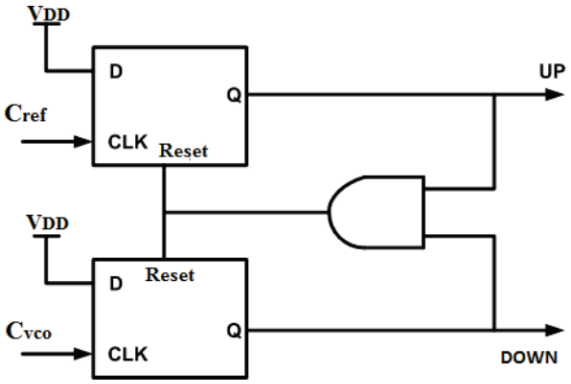

Fig 2.1(a). Flip-Flop level implementation

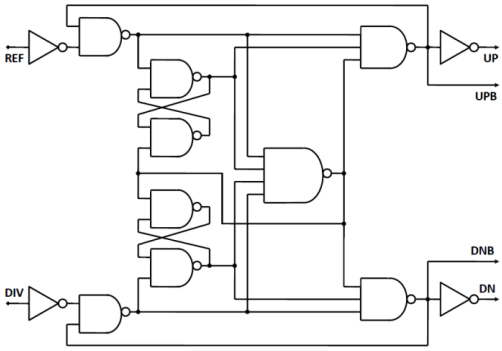

Fig 2.1(b). Gate level implementation

- This PFD compares the reference signal, Cref with the VCO output, Cvco to provide a phase difference in terms of UP and DOWN signals.
- Initially, both the outputs are assumed to be at zero level. On the onset of positive edge of one of the input signals, the corresponding output will go to high level.
- The PFD remains in the present state unless the positive edge of the second input reaches. As soon as the positive edge of the second input arrives, the second output will also go to high level. Now when both the outputs are high, the output of the AND gate will be high, and the circuit will be reset.
- The drawbacks of this circuit are that there is a large dead zone in the circuit and the operating frequency is also lower.

2.2 TSPC Based Sequential PFD :

- This design of PFD [2] is based on the TSPC logic for high frequency applications and to reduce the power consumption and uses transistor level implementation of D Flip-Flop and NOR gate is used as the reset logic.
- The variable delay elements are used to reduce the dead zone and blind zone areas of the PFD.

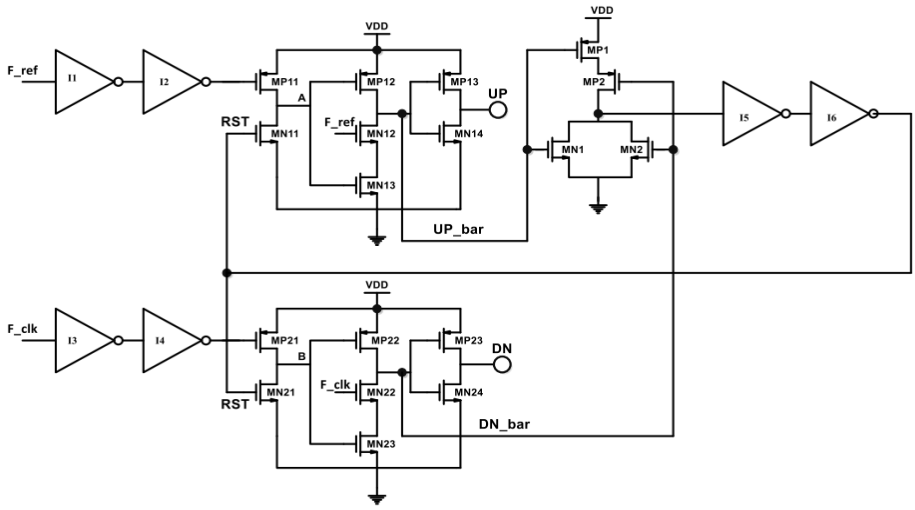

Fig 2.2(a) Circuit level implementation of TSPC based sequential PFD

- Initially, when signals F_ref, F_clk, and RST are LOW, transistors MP11/MP21 are turned ON, while MN11/MN21 and MN12/MN22 are turned OFF. In this situation nodes A and B will be fully charged if connected to VDD.
- When F_ref or F_clk goes high the UP_bar or DN_bar signals go zero, which further makes the UP and DN signals high by making use of inverters made by transistors MP13-MN14 and MP23-MN24 in the path.
- To carry out the reset operation, a two-input NOR gate with inputs UP_bar and DN_bar has been used.
- To address the blind zone issue, inverters I1 & I2 and I3 & I4 are added, while s I5 and I6 are added to the reset loop to fix the dead-zone issue.

2.3 Pass Transistor based PFD :

- This design using the pass transistor logic [3] to reduce the transistor count and also to reduce the static power.
- This uses master-slave configuration to implement flip-flop logic and uses the NAND gate as the reset
- This uses master-slave configuration to implement flip-flop logic and uses the NAND gate as the reset logic for the flip-flops.

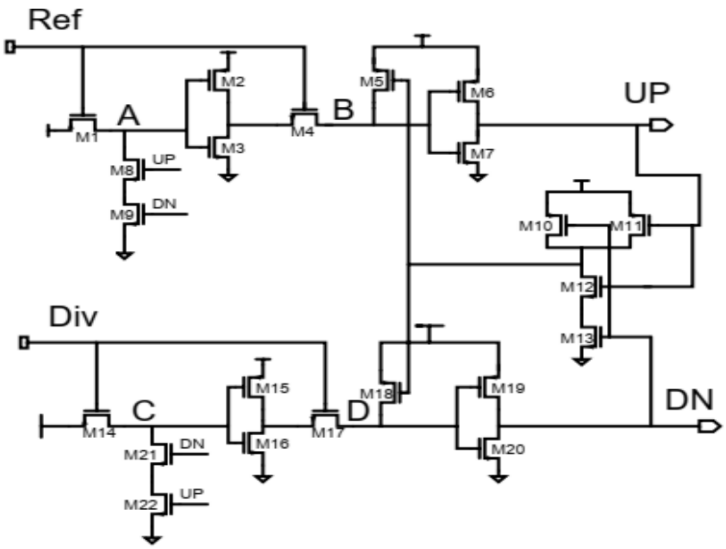

Fig 2.3(a) Circuit level implementation of pass-transistor based PFD

- Similarly, many other designs were explored like the [4], where quadrature sampling PFD is used to reduce the reference spur and jitter rejection.
- Also, some designs like [5], in which a stochastic PFD is designed specifically for the clock and data recovery circuits with no reference clock.
- At, the end it is understood that the different designs are targeted at different aims, some are aimed to reduce the dead & blind zones, some are concentrated high frequency applications, some in the low power applications.
- Some of the aims could be contradicting, like if we try to go for higher frequencies the power consumed will increase and if we try to reduce the dead zone by increasing the delay frequency will be lowered & blind zone will come into picture.

2.4 Design Topologies in PFD Design :

- The main way by which dead zone issue is resolved is through increasing the reset pulse width such that enough time would be there for charge pump currents though there is very small phase difference.
- There are different topologies in which the reset pulse is employed in the design. They are as explained through state diagrams and timing diagrams below :

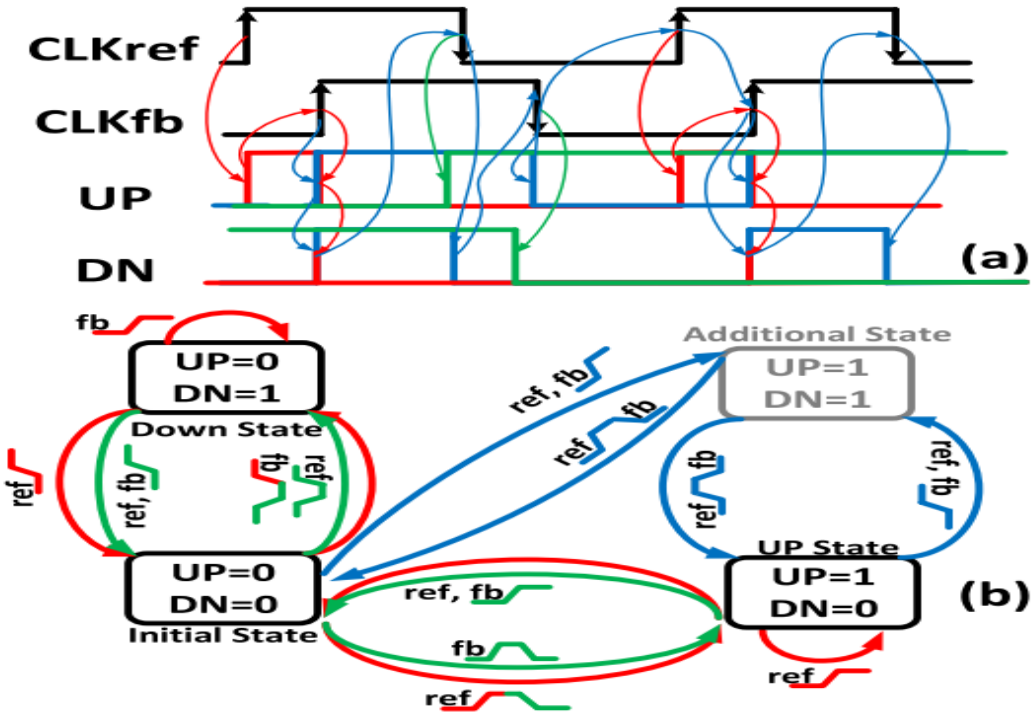

Fig 2.4(a) Timing and state diagrams of different PFD topologies

- The red path in the state diagram and the timing diagram represents the PFD with explicit reset pulse with dead zone.
- The blue path in the state diagram and the timing diagram represents the PFD with explicit reset pulse and dead zone free.
- The green path in the state diagram and the timing diagram represents the PFD with implicit reset pulse and dead zone free.
- In my design I employed the third type, provided the benefit of not needed to use a separate reset circuitry and dead zone free.

3. Circuit Explanation

- The design implemented by me is an explicit reset path, dead zone and blind zone free phase frequency detector.
- The design is taken from the research paper [4] and proper changes were made to design along with parametric analysis to decide the parameters of design.
- The circuit implemented is as shown in the below circuit diagram :

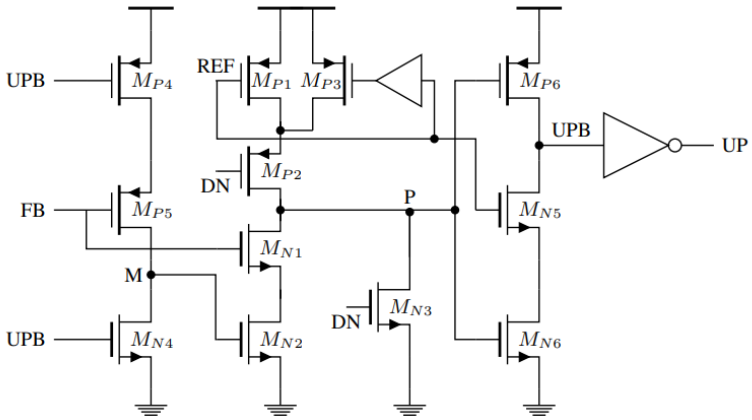

Fig 3(a). Pull-up part of the circuit

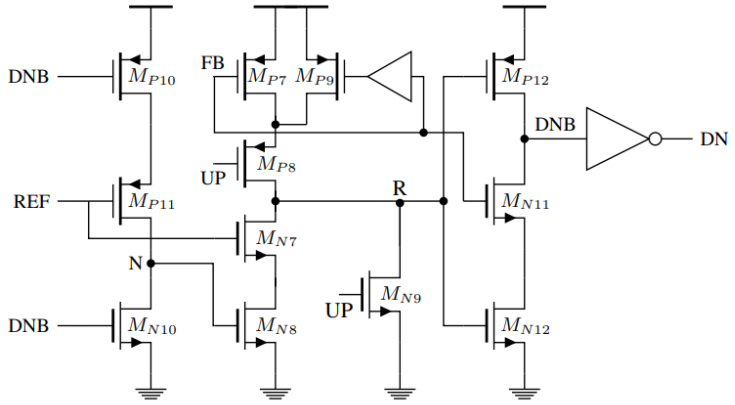

Fig 3(b). Pull-down part of the circuit

- Initially the inputs (REF and FB) are at logic low and PFD is in the state where UP and DN are at logic low. The nodes P and R were pre-charged to VDD through their corresponding pull up networks. A transition in REF signal from low to high will pull down the node UP through

MN5, MN6 and UP signal goes to logic high. Thus, the state machine has made a transition to state UP=1 and DN=0.

- Following this, the node R gets discharged through MN9 as soon as UP is driven to logic high and the pull up network MP7, MP8 is disabled as gate of MP 8 is driven high. Further, the node M is charged to VDD through MP4, MP5.
- Currently, the PFD is in the state UP=1 and DN=0. Any transition in the REF signal will not change the state of the PFD.
- Currently, the PFD is in the state UP=1 and DN=0. Any transition in the REF signal will not change the state of the PFD.
- Thus, the state machine makes a direct transition from state UP=1, DN=0 to UP=0, DN=0 unlike conventional designs.
- A similar working explanation can be provided transition to state UP=0, DN=1 by transition in signal FB followed by signal REF.

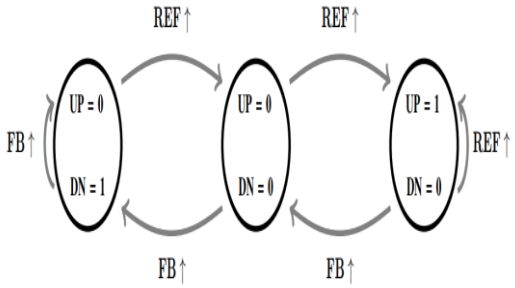

Fig 3(c). State Diagram

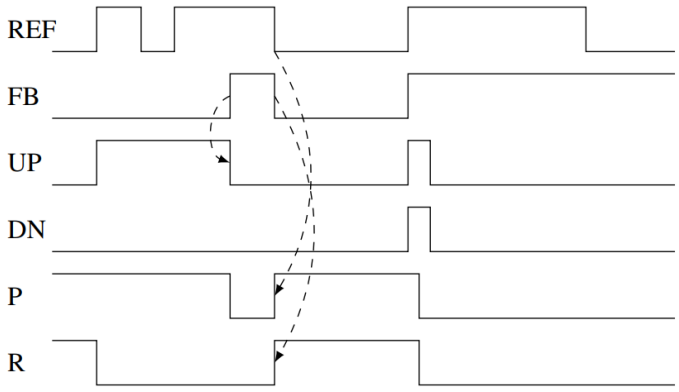

Fig 3(d). Timing Diagram

- In the case of delay between the two signals is very small that the phase difference is within the dead zone, P and R being pre-charged to high will pull up both UP and DN signals very quickly. As soon as UP and DN make a transition to logic high, the nodes P and R will be pulled down through MN3.
- Thus, we get a minimal width Reset pulse without the need for an explicit reset pulse generation circuit. With suitable scaling of MN3 and MN9, the width of reset pulse can be modified. The two transistors MP3 and MP9 driven by delayed input signals to turn on the pull up paths at the rising transition of the inputs. The delay added should be equal to the pre-charge time (T_{pch}), this completely eliminates the blind zone.

4. Simulation Results

- The simulations were performed on the Cadence Virtuoso EDA with devices from TSMC 65nm technology.
- The simulations included, transient analysis, parametric analysis and layout .

4.1 Timing Diagrams :

- To compare the design performance with the standard PFD design, initially a conventional PFD is designed with explicit reset path.
  - The circuit implementation of the conventional PFD is a below :

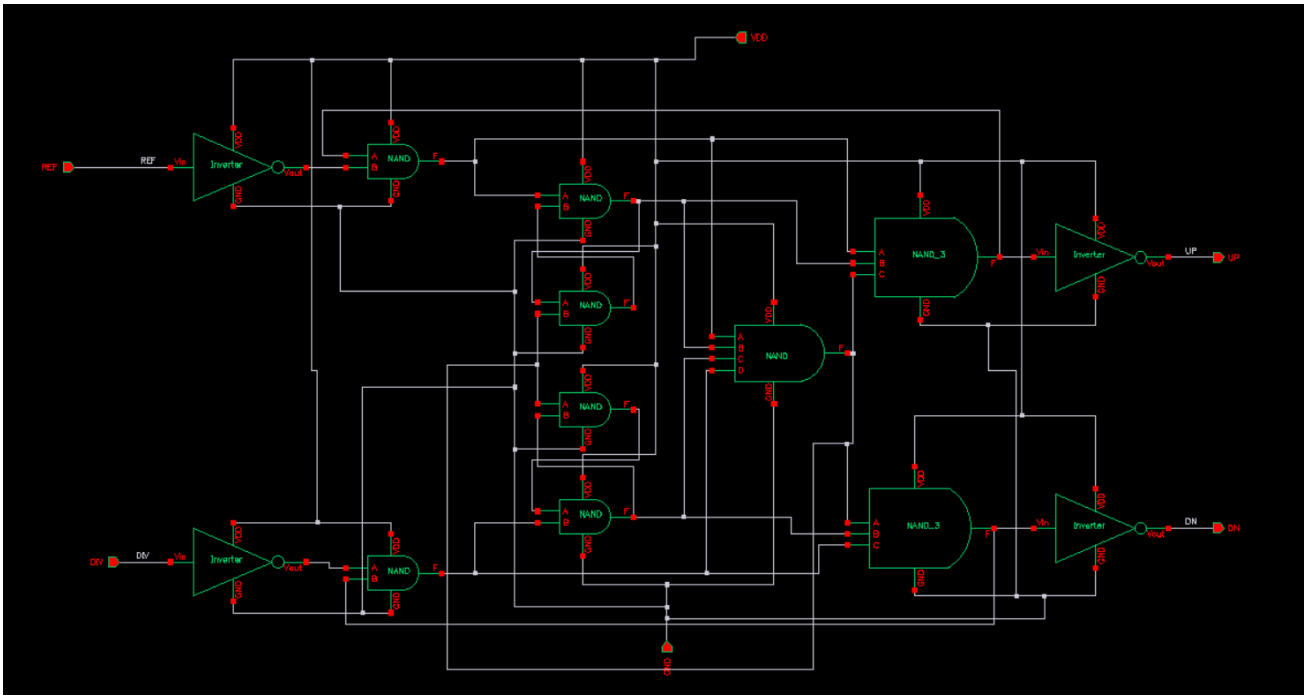

Fig 4.1(a). Conventional PFD Circuit implementation

  - The output characteristics of the PFD designed above is as follows :

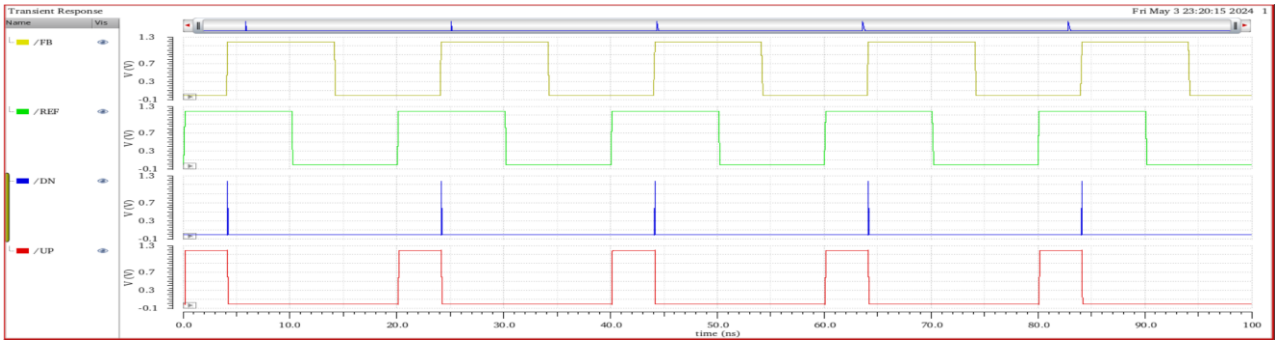

Fig 4.1(b). Conventional PFD timing diagram

- This design has been chosen as a reference to check the performance of my design for various parameters like power consumption, maximum frequency of operation, dead zone and blind zone.
- The implementation of the implicit reset path, dead zone and blind zone free PFD in Cadence Virtuoso is as shown below :

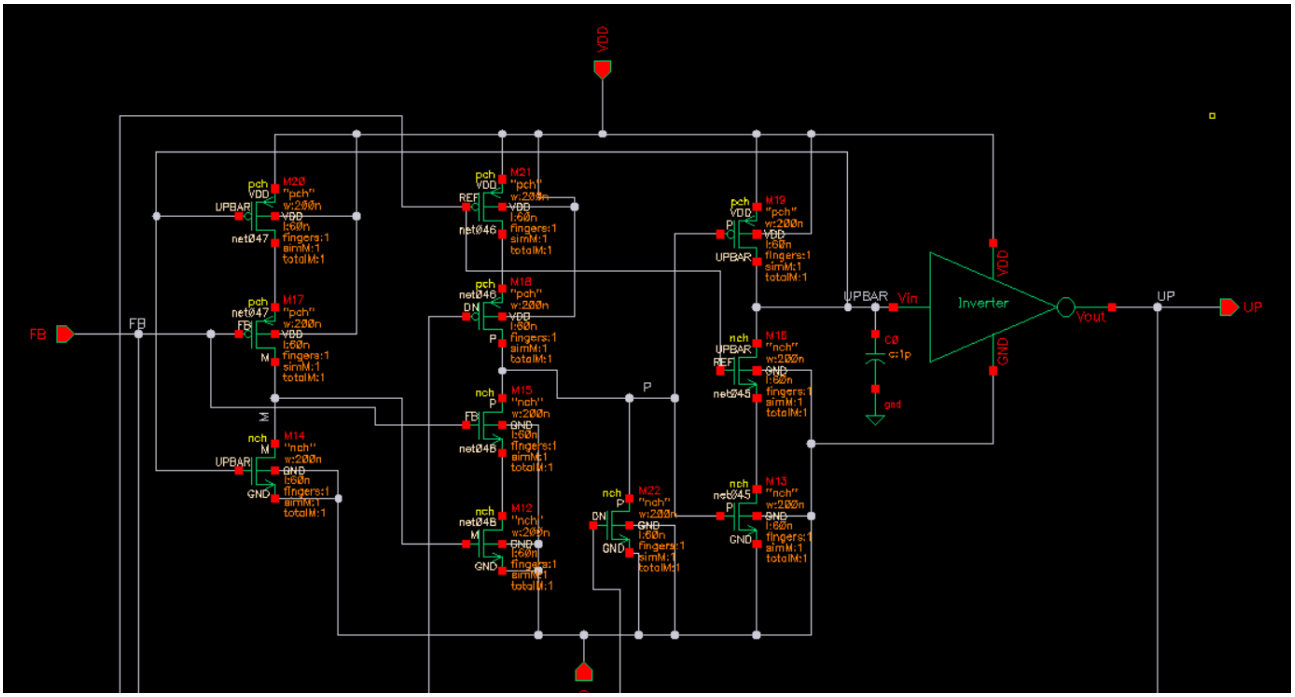

Fig 4.1(c). Pull-up network of PFD

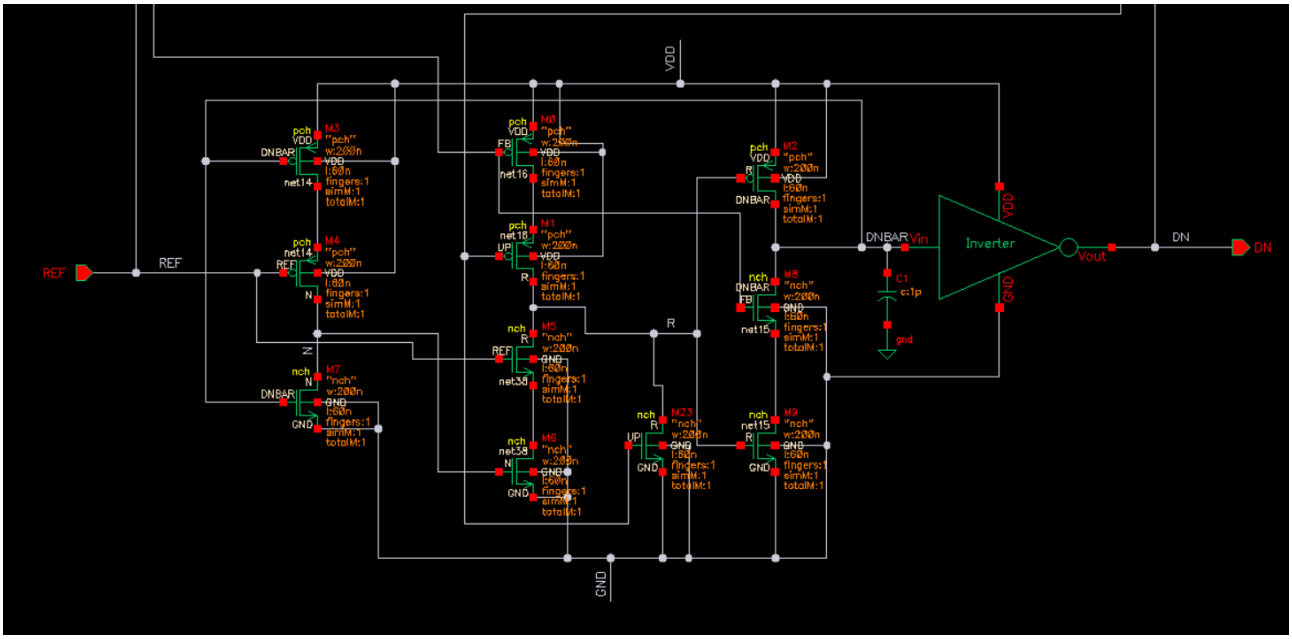

Fig 4.1(d). Pull-down network of the PFD

- The output characteristics for different combinations of reference and feedback clocks is as shown below :

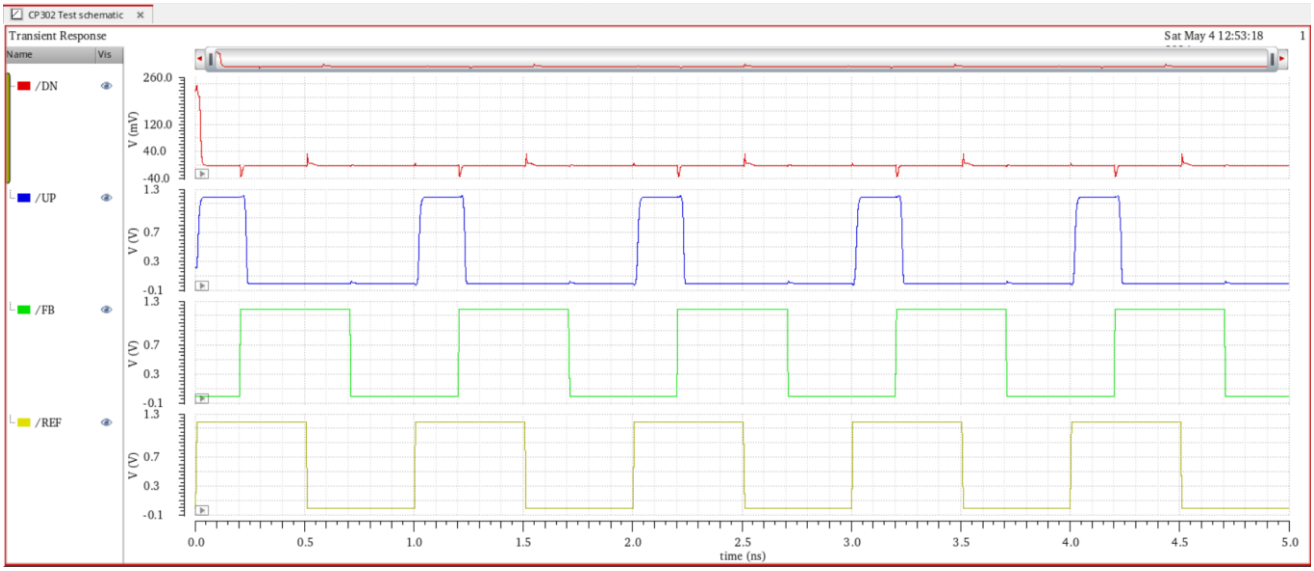

Fig 4.1(e). Timing diagram for FB clock lagging behind the reference clock

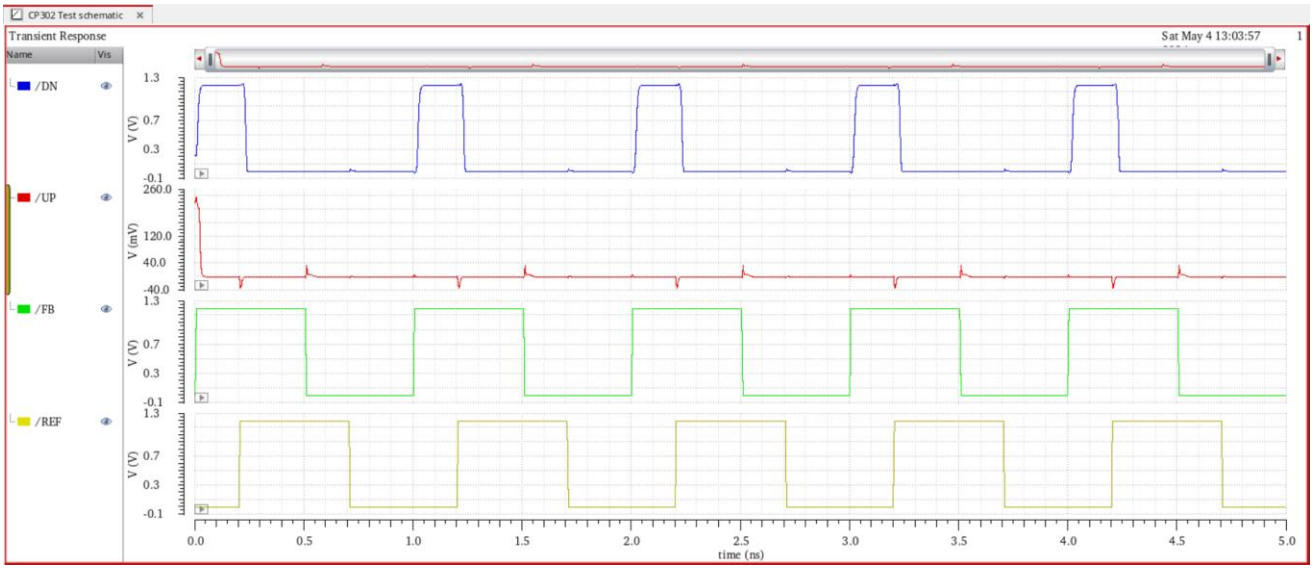

Fig 4.1(f). Timing diagram for FB clock leading the reference clock

4.2 Parametric Analysis :

- The reset delay used in the design in **T_{RES} = 19.2ps**, which means that nearly the maximum frequency over which the circuit can work is **f_{max} = 5GHz**.
- Since, we are using the TSMC 65nm technology for building the circuits, the node voltages supported would be 0.9V to 1.26V.
- Given these limits on the frequency and the supply voltage, simulations were performed on the power consumed when these two parameters were varied to get to know the optimal frequency of operation and supply voltage.
- The frequency is varied from 1GHz to 5GHz to observe the pattern of power consumption on both 'Dead zone and Blind zone free PFD' and the 'Conventional PFD', to compare the performance.

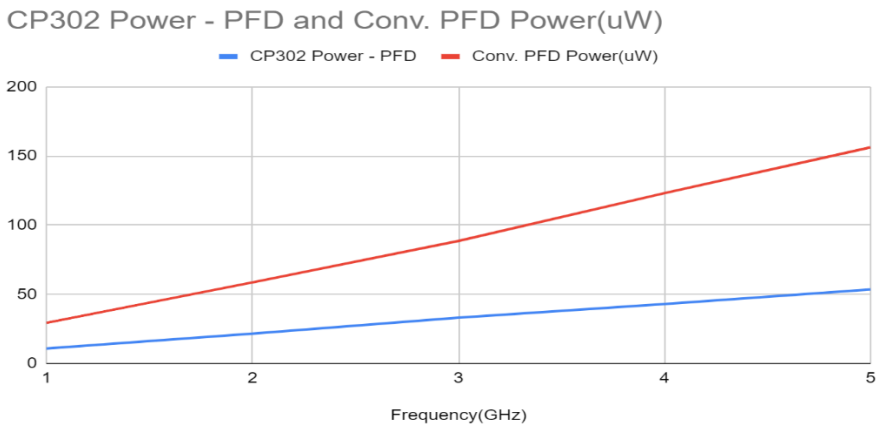

Fig 4.2(a). Power vs Frequency of Operation

- The UP-DN voltage when the input phase difference is varied is shown below :

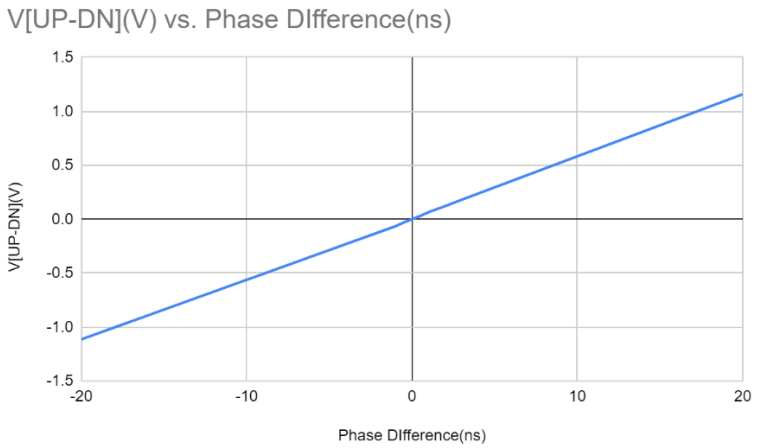

Fig 4.2(b). V(UP-DN) vs Phase Difference

- The supply voltage is varied from 0.9V to 1.26V to observe the power consumption patterns in both the 'Dead zone and Blind zone free PFD' and the 'Conventional PFD', to compare the performance.

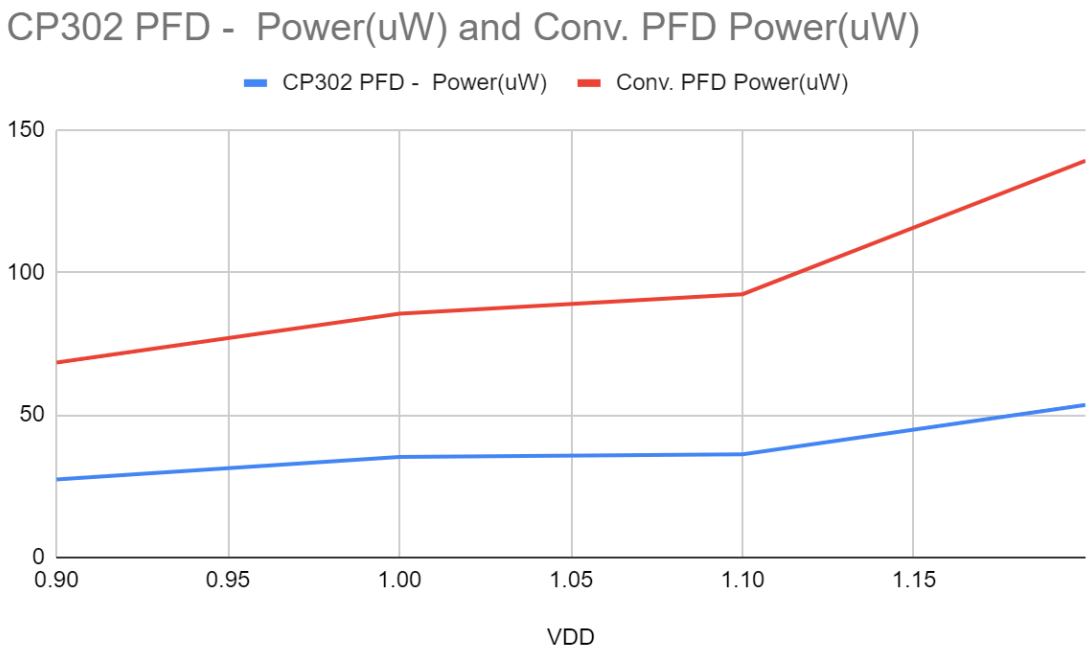

Fig 4.2(c) Power vs Supply Voltage

- The maximum frequency of the PFD is analysed as the supply voltage is varied from 0.9V to 1.2V :

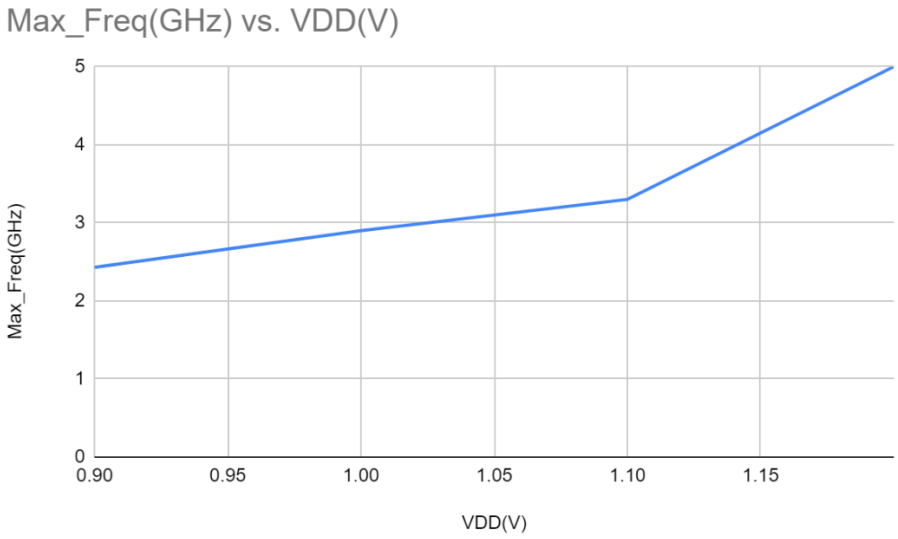

Fig 4.2(d). Maximum Operating Frequency vs Supply Voltage

4.2 Design Layout :

- The layout design is done on Assura layout tool in accordance with the schematic design.
- The layouts are as shown below :

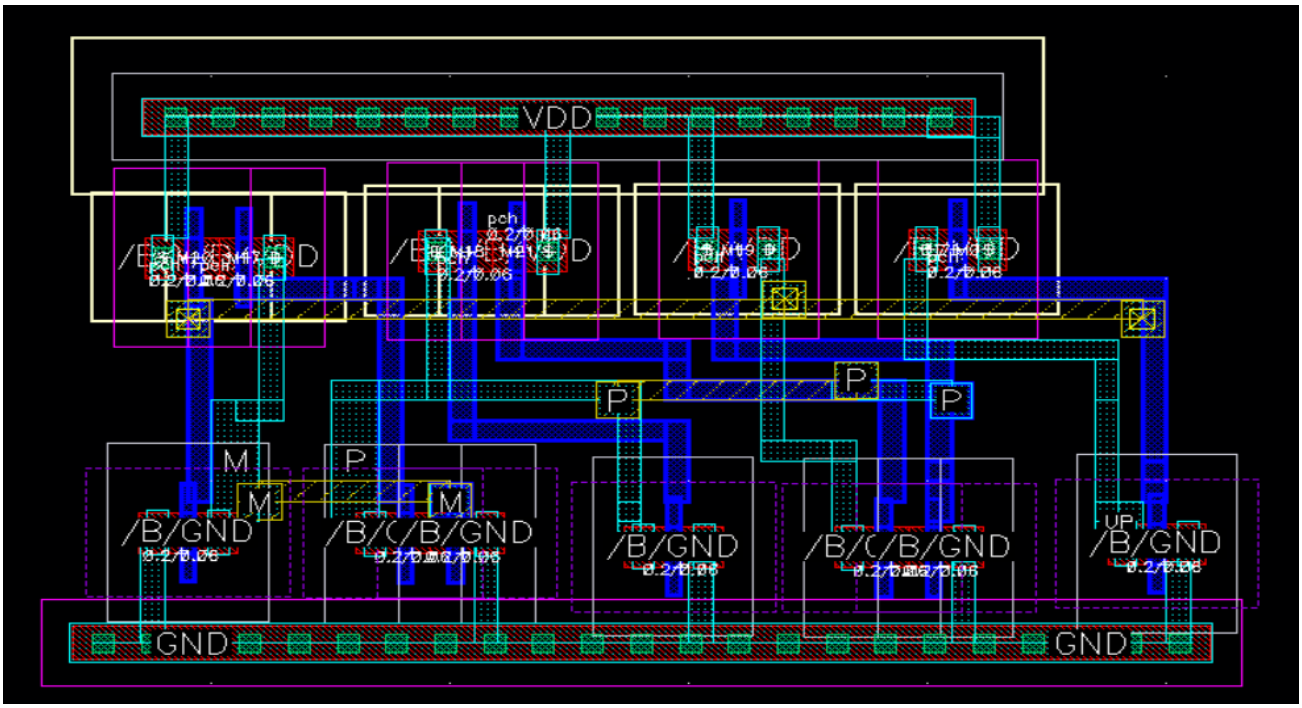

Fig 4.3(a). Pull-Up Network Layout

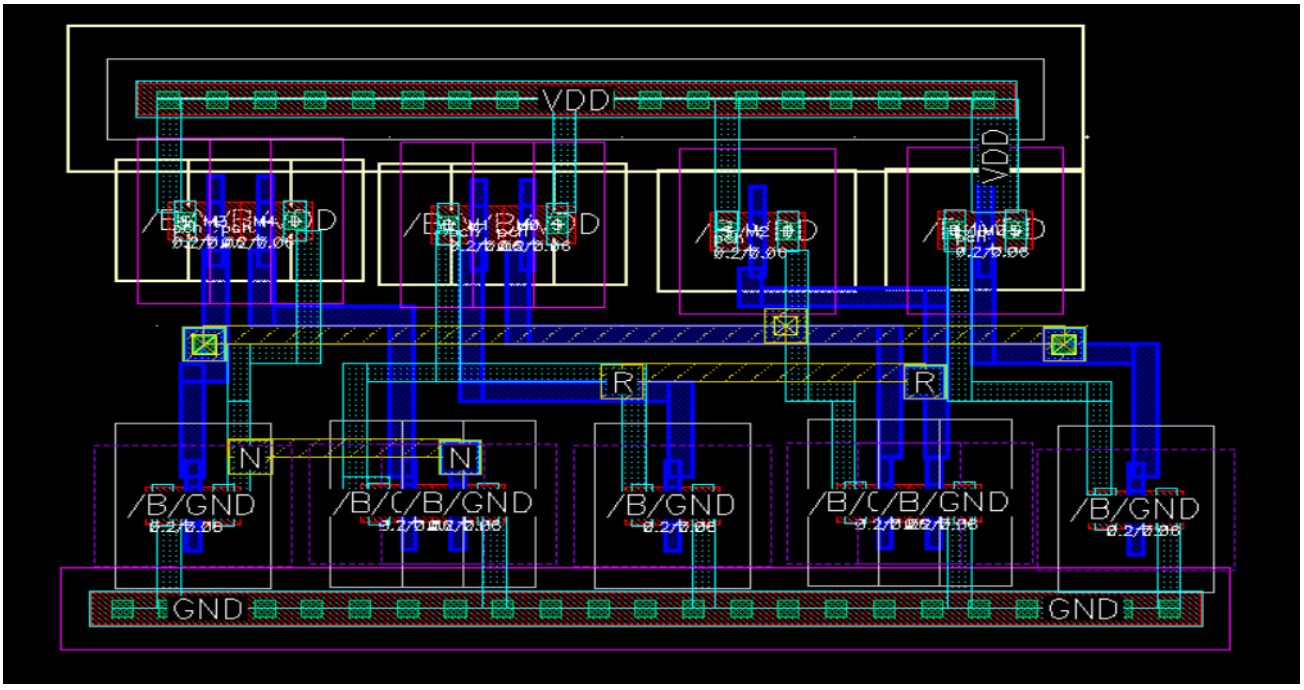

Fig 4.3(b). Pull-Down Network Layout

5. Results and Inferences

- Through the parametric analysis it is observed that the power consumption of the circuit increases with increase in the frequency of operation. But as compared to the conventional PFD the power consumption is way less.
- Though the power is increasing the higher frequency operation is required with the ever-evolving technologies especially the 5G and beyond as the higher spectrum are used for communication.
- The next simulation shows the UP – DN voltage as the input phase difference varies. The simulation results showed that there is no dead zone.
- The next simulation is power supply voltage, which showed that the power consumption increases with increase in supply voltage. But the power consumed is again way less than the conventional PFD.
- The next simulation was on the maximum possible operating frequency vs the supply voltage for the case of zero dead zone. This shown that the maximum operating frequency increases as the supply voltage increases. This is due to the fact that the current increases which leads to faster charging and discharging of transistors in the circuit.
- The above two simulations showed that the power consumption and maximum operating frequency are inversely related and hence if we want one factor we need to compromise on the other.
- Finally, the layout of the design is also performed in accordance with the circuit designed.
- At the end the design used explicit reset topology and design is dead zone and blind zone free with maximum operating frequency of 5GHz with supply voltage of 1.2V with TSMC 65nm device technology.
- This design of PFD could be incorporated in any PLL design to get better characteristics in terms of jitter or phase noise and power consumption at higher frequencies below the limit of 5GHz.

Acknowledgment

I would like to first acknowledge Dr. Mahendra Sakare sir for provided me with this opportunity to work on this design in the field of RF design under his valuable guidance. Secondly, I would acknowledge the guidance of Upendra sir, he helped me to resolve the design issues at many points in the cycle of design through his experience. That had helped me a lot in achieving this final design. I would also acknowledge Gaurav sir for helping with Cadence tool knowledge as Iam new to use the tool. I would acknowledge all the researcher whoever are mentioned in the references section for their valuable literature being published.

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