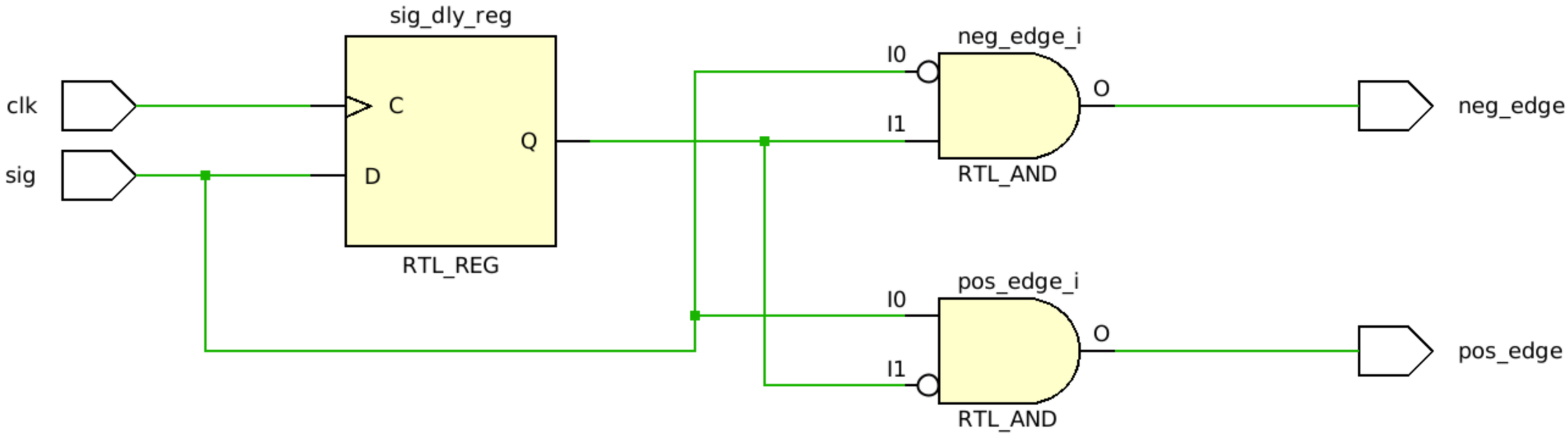
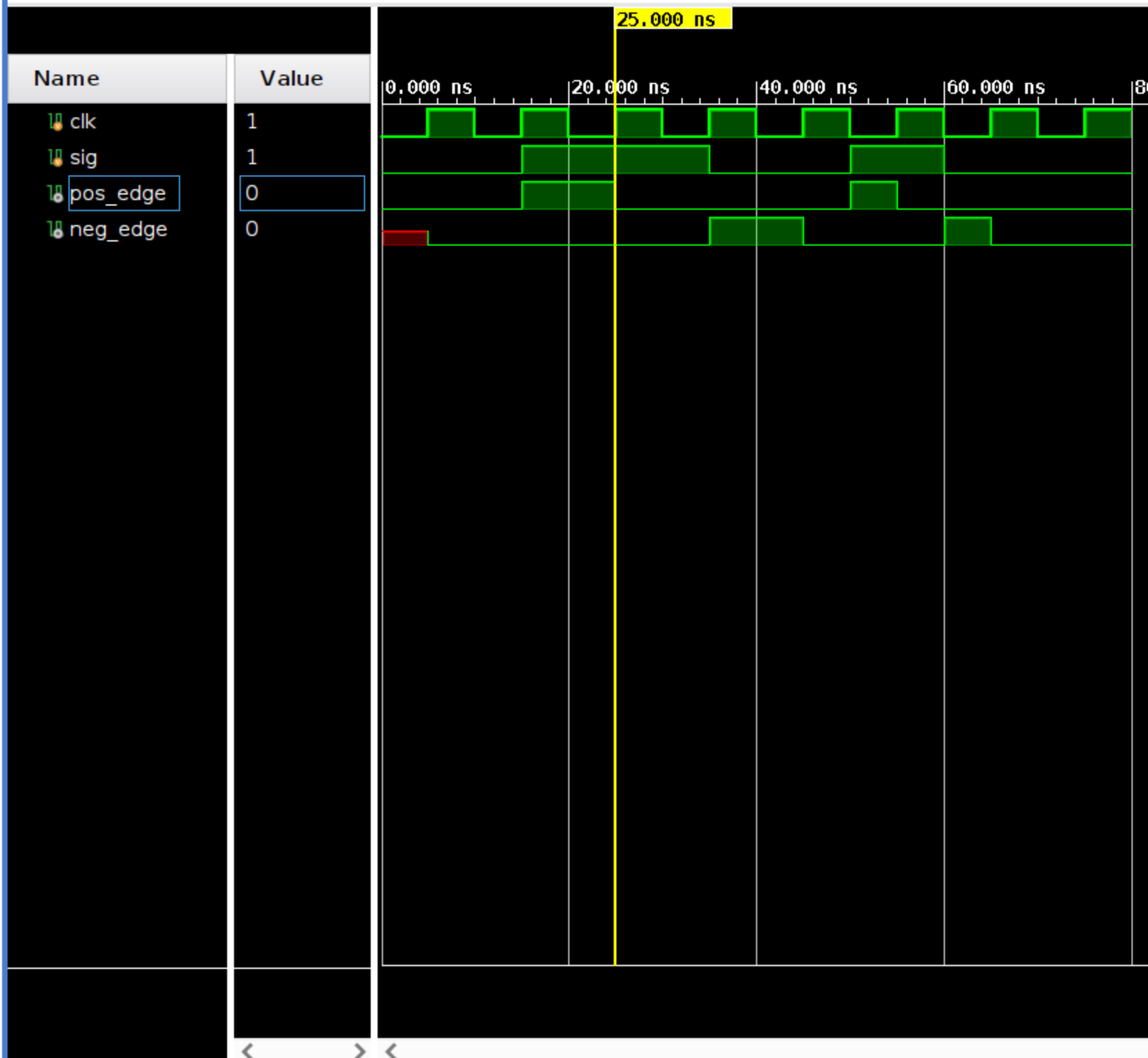
Summary | clk_edge_detector.v | clock_edge_tb.v | Schematic

3 Cells | 4 I/O Ports | 5 Nets



Messages | Log | Reports | Design Runs

clk_edge_detector.v | clock_edge_tb.v | Untitled 8*



Tcl Console | Messages | Log

clk_edge_detector.v | clock_edge_tb.v | Untitled 8*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_070/project_1/project_1.srcs/sources_1/new/clk_edge_detector

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/30/2024 04:56:26 AM
5  // Module Name: clk_edge_detector
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module clk_edge_detector(
10     input sig,
11     input clk,
12     output pos_edge,
13     output neg_edge);
14
15     reg   sig_dly;
16
17     always @ (posedge clk) begin
18         sig_dly <= sig;
19     end
20
21     assign pos_edge =  sig & ~sig_dly;
22     assign neg_edge = ~sig &  sig_dly;
23 endmodule
```

Tcl Console | Messages | Log

clk_edge_detector.v | clock_edge_tb.v | Untitled 8*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_070/project_1/project_1.srcs/sim_1/new/clock_edge_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/30/2024 05:02:55 AM
5   // Module Name: clock_edge_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module clock_edge_tb;
10      reg sig;
11      reg clk;
12      wire neg_edge,pos_edge;
13
14      clk_edge_detector DUT (   .sig(sig),
15                                .clk(clk),
16                                .pos_edge(pos_edge),
17                                .neg_edge(neg_edge)
18                                );
19
20      always #5 clk = ~clk;
21
22      initial begin
23          clk <= 0;
24          sig <= 0;
25          #15 sig <= 1;
26          #20 sig <= 0;
27          #15 sig <= 1;
28          #10 sig <= 0;
29          #20 $finish;
30      end
31  endmodule
32
```

Tcl Console | Messages | Log