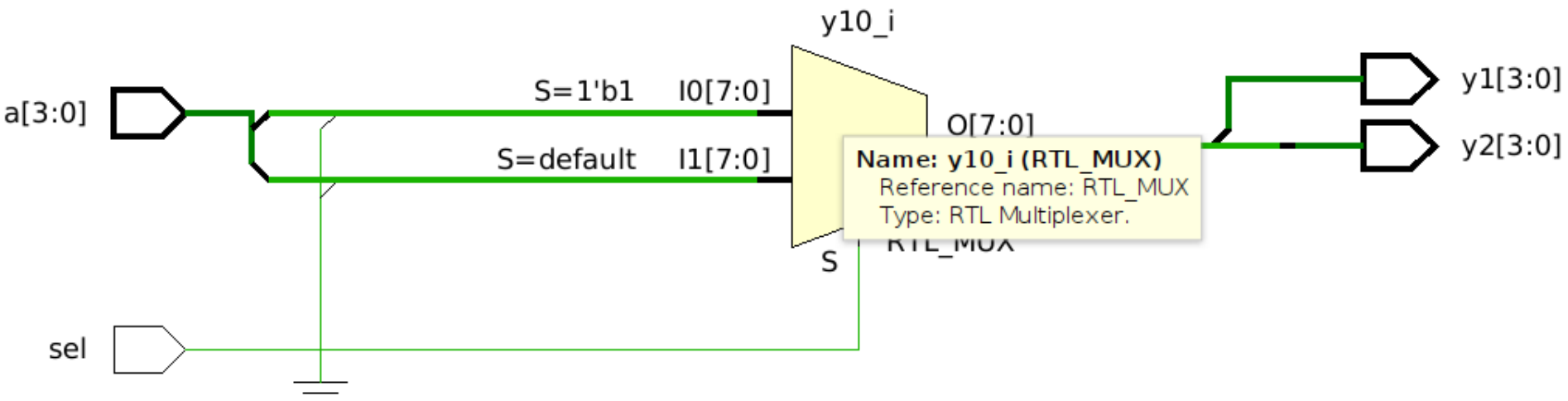
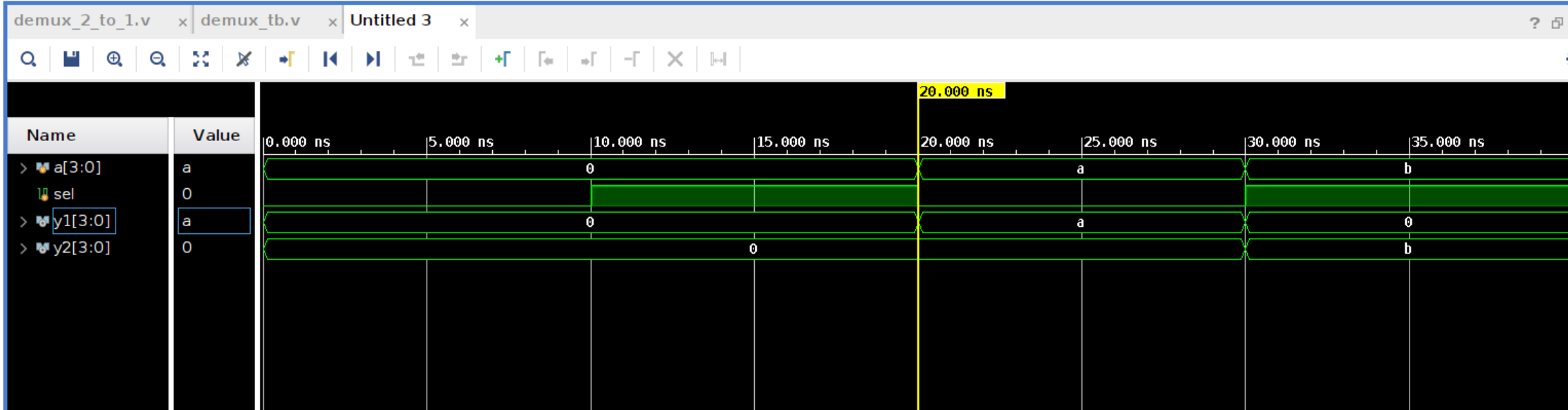
demux_2_to_1.v | Schematic | demux_tb.v | Schematic (2)

1 Cell | 13 I/O Ports | 14 Nets




demux_2_to_1.v
demux_tb.v
Untitled 3
Name
Value
a[3:0]
a
sel
0
y1[3:0]
a
y2[3:0]
0
20.000 ns
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
0
a
b
0
a
0
0
b

demux_2_to_1.v × demux_tb.v × Untitled 3 ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_028/project_1/project_1.srcs/sources_1/new/demux_2_to_1.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/19/2024 05:52:38 AM
5  // Module Name: demux_2_to_1
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module demux_2_to_1(
10 input [3:0] a,
11 input sel,
12 output [3:0] y1,y2
13   );
14 //  assign y1 = a &  sel;
15 //  assign y2 = a & ~sel;
16  assign {y1,y2} = sel?{4'b0,a}: {a,4'b0};
17 endmodule
18
```

demux_2_to_1.v | demux_tb.v | Untitled 3

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_028/project_1/project_1.srcs/sim_1/new/demux_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/19/2024 05:59:44 AM
5  // Module Name: demux_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module demux_tb;
10
11 reg [3:0]a;
12 reg sel;
13 wire [3:0] y1, y2;
14 demux_2_to_1 DUT(a,sel,y1,y2);
15
16 initial begin
17 a = 0; sel = 0; #10;
18 a = 0; sel = 1; #10;
19 a = 4'ha; sel = 0; #10;
20 a = 4'hb; sel = 1; #10;
21 $finish;
22 end
23 endmodule
24
```