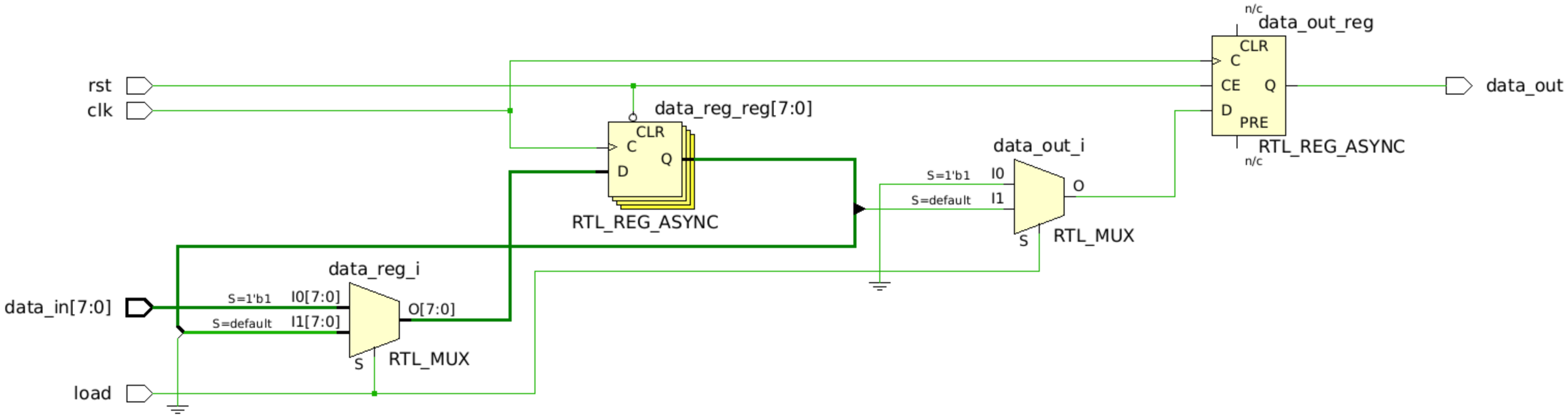
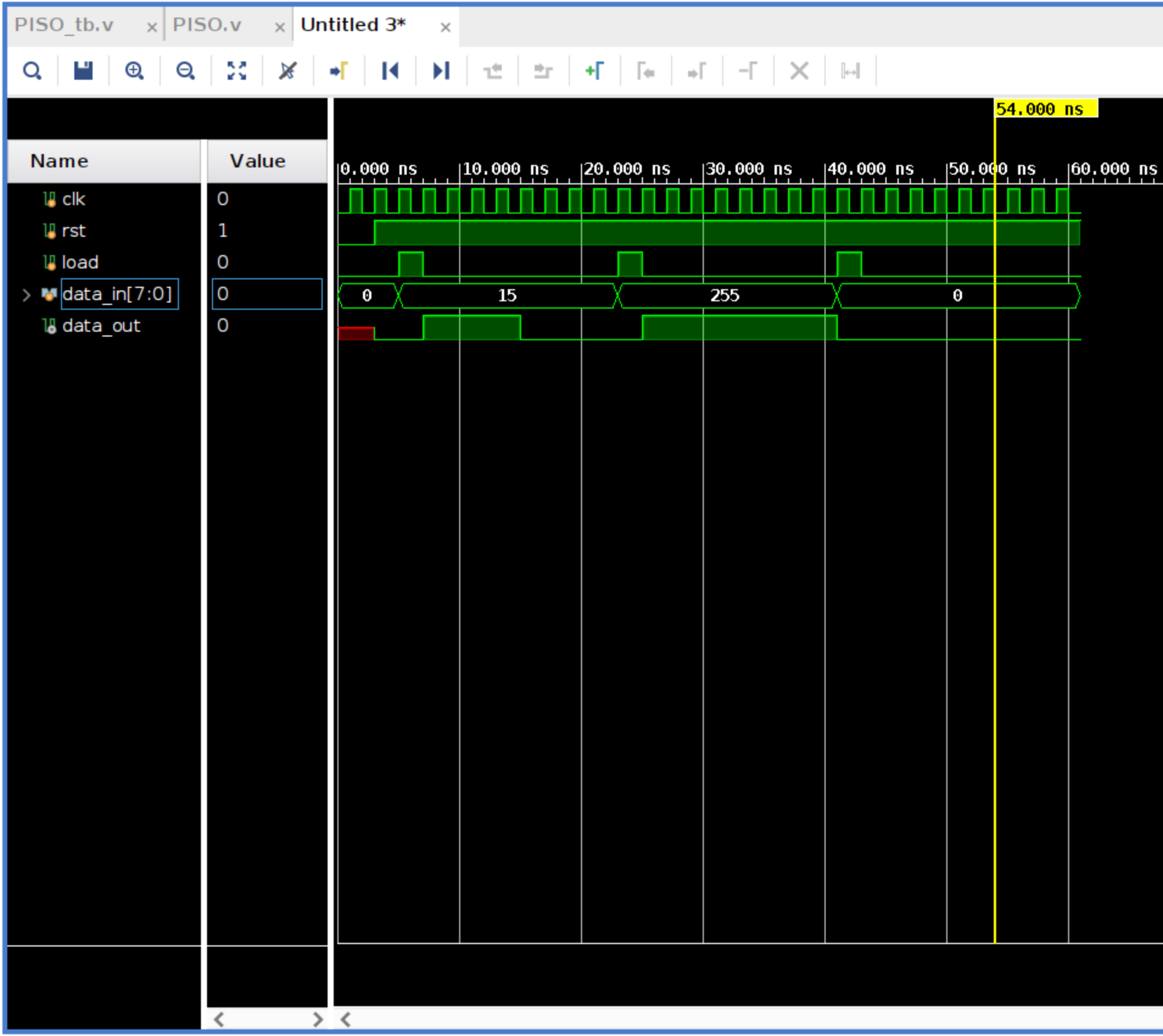
PISO_tb.v | PISO.v | Schematic | Schematic (2)

11 Cells 12 I/O Ports 30 Nets




PISO_tb.v
PISO.v
Untitled 3*
Name
Value
clk
0
rst
1
load
0
data_in[7:0]
0
data_out
0
54.000 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
0
15
255
0

PISO_tb.v | PISO.v | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_057/project_1/project_1.srcs/sources_1/new/PISO.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/17/2024 11:12:24 AM
5  // Module Name: PISO
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module PISO (input load, clk, rst,
9               input [7:0] data_in,
10              output reg data_out);
11
12   // PISO register array to load and shift data
13   reg [7:0] data_reg;
14
15   always @ (posedge clk or negedge rst) begin
16     if (~rst)
17       data_reg <= 8'h00; // Reset PISO register array on reset
18     else begin
19
20       // Load the data to the PISO register array and reset the serial data out register
21       if (load)
22         {data_reg, data_out} <= {data_in, 1'b0};
23       // Shift the loaded data 1 bit right; into the serial data out register
24       else
25         {data_reg, data_out} <= {1'b0, data_reg[7:0]};
26     end
27   end
28
29 endmodule
30
31
32
33
34
35
36
37
38
39
```

PISO_tb.v | PISO.v | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_057/project_1/project_1.srcs/sim_1/new/PISO_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/17/2024 02:04:10 AM
5  // Module Name: PISO_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module PISO_tb;
10
11   reg clk, rst, load;
12   reg [7:0] data_in;
13
14   wire data_out;
15
16   PISO DUT (load, clk, rst, data_in, data_out);
17
18   always #1 clk = ~clk;
19
20
21   initial begin
22     clk = 0; rst = 0; load = 0; data_in = 8'h00;
23     #3 rst = 1;
24     #2 load = 1; data_in = 8'd15;
25     #2 load = 0;
26     #16 load = 1; data_in = 8'd255;
27     #2 load = 0;
28     #16 load = 1; data_in = 8'd0;
29     #2 load = 0;
30     #18 $stop;
31
32   end
33
34 endmodule
35
36
37
38
39
```