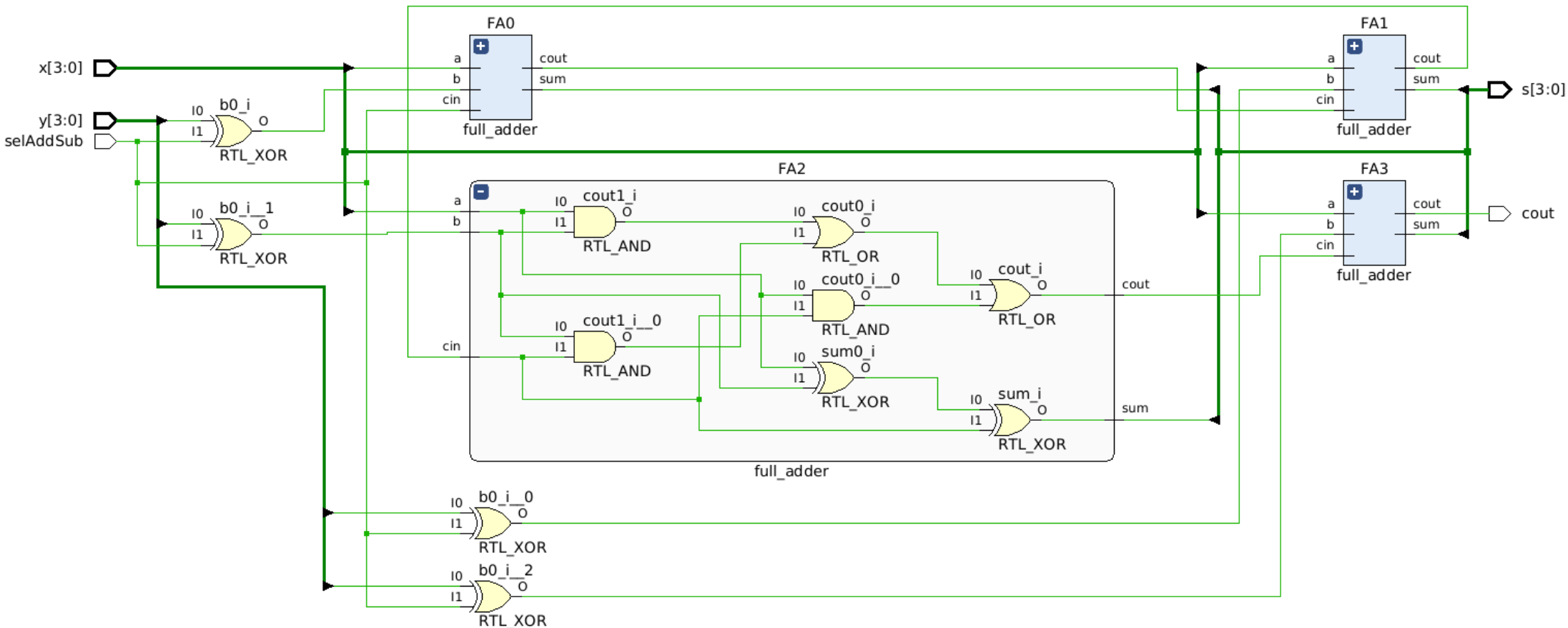
15 Cells 14 I/O Ports 31 Nets



Project Summary | parallel_adder_4b.v | parallel_adder_4b_tb.v | full_adder.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_008/project_1/project_1.srcs/sources_1/new/parallel_adder_4b.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/29/2024 08:27:49 PM
5  // Module Name: parallel_adder_4b
6  //////////////////////////////////////////////////////////////////////////////////
7
8  /* 4 Bit parallel Adder/Substractor */
9  module parallel_adder_4b(
10
11   input selAddSub,
12   input [3:0] x,y,
13   output [3:0] s,
14   output cout);
15   wire [2:0] c;
16  full_adder FA0(.a(x[0]),.b(y[0]^selAddSub),.cin(selAddSub),.sum(s[0]),.cout(c[0]));
17  full_adder FA1(.a(x[1]),.b(y[1]^selAddSub),.cin(c[0]),.sum(s[1]),.cout(c[1]));
18  full_adder FA2(.a(x[2]),.b(y[2]^selAddSub),.cin(c[1]),.sum(s[2]),.cout(c[2]));
19  full_adder FA3(.a(x[3]),.b(y[3]^selAddSub),.cin(c[2]),.sum(s[3]),.cout(cout));
20  endmodule
21
22
```

Project Summary | parallel_adder_4b.v | parallel_adder_4b_tb.v | full_adder.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_008/project_1/project_1.srcs/sim_1/new/parallel_adder_4b_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/29/2024 08:27:49 PM
5  // Module Name: parallel_adder_4b_tb
6  //////////////////////////////////////////////////////////////////////////////////
7  module parallel_adder_4b_tb;
8
9      reg [3:0] x, y;
10     reg selAddSub;
11     wire [3:0] s;
12     wire cout;
13     parallel_adder_4b dut (
14         .x(x),
15         .y(y),
16         .selAddSub(selAddSub),
17         .s(s),
18         .cout(cout)
19     );
20     initial begin
21
22         $display("x    y    selAddSub | s    cout");
23         $monitor("%d %d %b | %d %b", x, y, selAddSub, s, cout);
24
25         // Generate random values for addition (selAddSub = 0) and subtraction (selAddSub = 1)
26         repeat (10) begin
27             selAddSub = 1'b0;  // Test addition
28             x = $random % 16;
29             y = $random % 16;
30             #10;
31             selAddSub = 1'b1;  // Test subtraction
32             x = $random % 16;
33             y = $random % 16;
34             #10;
35         end
36         $finish;
37     end
38
39 endmodule
```

Project Summary | parallel_adder_4b.v | parallel_adder_4b_tb.v | **full_adder.v**

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_008/project_1/project_1.srcs/sources_1/new/full_adder.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/29/2024 08:30:36 PM
5  // Module Name: full_adder
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module full_adder (
10 input a,
11 input b,
12 input cin,
13 output sum,
14 output cout);
15 assign sum = (a^b^cin);
16 assign cout = (a&&b)||(b&&cin)||(a&&cin);
17 endmodule
```

Messages | Log | Tcl Console ×

```
# run 1000ns
x    y    selAddSub | s    cout
 4  1 0 |  5 0
 9  3 1 |  6 1
13 13 0 | 10 1
 5  2 1 |  3 1
 1 13 0 | 14 0
 6 13 1 |  9 0
13 12 0 |  9 1
 9  6 1 |  3 1
 5 10 0 | 15 0
 5  7 1 | 14 0
 2 15 0 |  1 1
 2 14 1 |  4 0
 8  5 0 | 13 0
12 13 1 | 15 0
13  5 0 |  2 1
 3 10 1 |  9 0
 0  0 0 |  0 0
10 13 1 | 13 0
 6  3 0 |  9 0
13  3 1 | 10 1
$finish called at time : 200 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_008/project_1/proje
INFO: [USF-XSim-96] XSim completed. Design snapshot 'parallel_adder_4b_tb_behav' loaded
```

Type a Tcl command here

parallel_adder_4b.v | full_adder.v | parallel_adder_4b_tb.v | Untitled 5