



```
carry_save_adder.v x carry_save_adder_tb.v x Untitled 1
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 018/project 1/project 1.srcs/sources 1/new/carry save adder.v
    2 🖨
       3 ¦
       // Engineer: Anjan Prasad
       // Create Date: 10/09/2024 09:59:34 AM
5
       '// Module Name: carry save adder
6 🖒
       7
8 ¦
       module carry save adder(
       input [3:0] a,b,c,
10
11
       output [5:0] sum,
12
       output cout
13
           );
14
           wire [3:0] s,c1,c2;
15
16
17
       full adder FA1(a[0],b[0],c[0],s[0],c1[0]);
18
         full adder FA2(a[1],b[1],c[1],s[1],c1[1]);
19
         full adder FA3(a[2],b[2],c[2],s[2],c1[2]);
20
         full adder FA4(a[3],b[3],c[3],s[3],c1[3]);
21
22
23
    \bigcirc assign sum[0] = s[0];
     o | assign sum[5] = cout;
24
25
       // assign c2 = {s[1],s[2],s[3],0};
26
       '// ripple carry adder 4bit RCA (c1,c2,0,sum[4:1],cout);
27
28
         full_adder FA5( c1[0], s[1], 0, sum[1], c2[0]);
29
         full adder FA6( c1[1], s[2], c2[0], sum[2], c2[1]);
30
         full adder FA7( c1[2], s[3], c2[1], sum[3], c2[2]);
31
         full adder FA8( c1[3], 0, c2[2], sum[4], cout);
32
33
           endmodule
2/
```

```
carry save adder.v
                   x carry save adder tb.v x Untitled 1
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 018/project 1/project 1.srcs/sim 1/new/carry save adder tb.v
     1
         timescale 1ns / 1ps
 2 🖨
 3 ¦
         1// Engineer: Anjan Prasad
 4
         // Create Date: 10/09/2024 10:29:12 AM
 5 ¦
         '// Module Name: carry save adder tb
 6 🖒
 7 T
 8 🖨
         module carry save adder tb;
 9 ¦
             reg [3:0] a, b, c;
10
             wire [5:0] sum;
11
             wire cout;
12
13
             carry save adder DUT (.a(a), .b(b), .c(c), .sum(sum), .cout(cout));
14
15 🖨
             initial begin
                  monitor("Time = \%0t | a = \%d, b = \%d, c = \%d | sum = \%d, cout = \%b", <math>time, a, b, c, sum, cout);
16
17
      \circ
               a = 4'b0001; b = 4'b0010; c = 4'b0100;
      \circ
18
                 #10;
19
      \circ
                 a = 4'b1010; b = 4'b0111; c = 4'b0011;
20
                 #10:
21
      \circ
                 a = 4'b1111; b = 4'b1111; c = 4'b1111;
22
                 #10:
23
      \circ
                 a = 4'b0000; b = 4'b0000; c = 4'b0001;
24
                 #10:
25
      \circ
                 a = 4'b1001; b = 4'b0110; c = 4'b0010;
26
      0
                 #10;
27
      \circ
                 a = 4'b00000; b = 4'b1111; c = 4'b1111;
28
                 #10;
      \circ
29
                 a = 4'b1111; b = 4'b0000; c = 4'b1111;
30
      \circ
                 #10;
31
      \circ
                 a = 4'b1111; b = 4'b1111; c = 4'b0000;
32
      \circ
                 #10;
33
      \bigcirc
                 $finish;
34 🖒
             end
35 🖒
         endmodule
36
```

