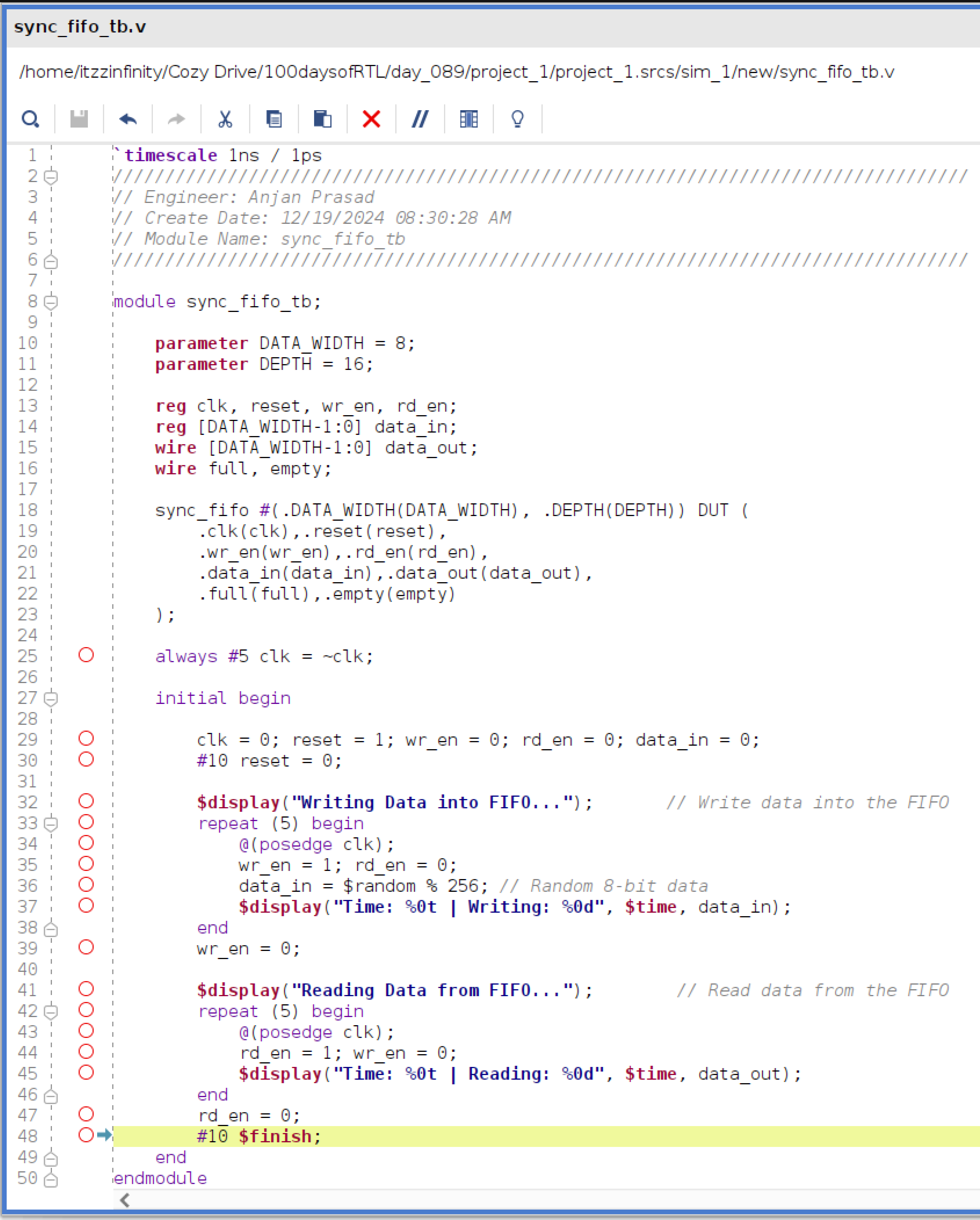
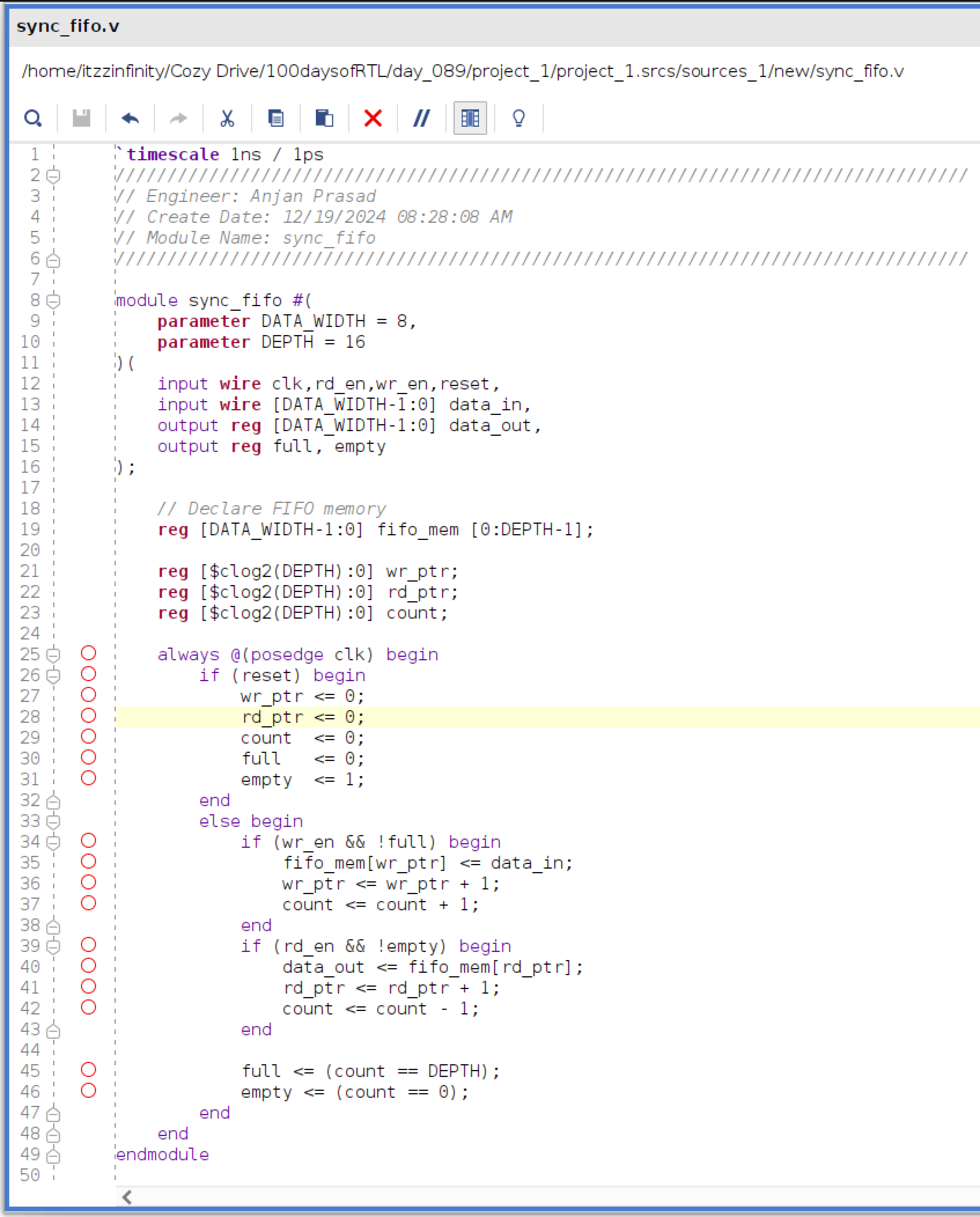

sync_fifo_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_089/project_1/project_1.srcs/sim_1/new/sync_fifo_tb.v

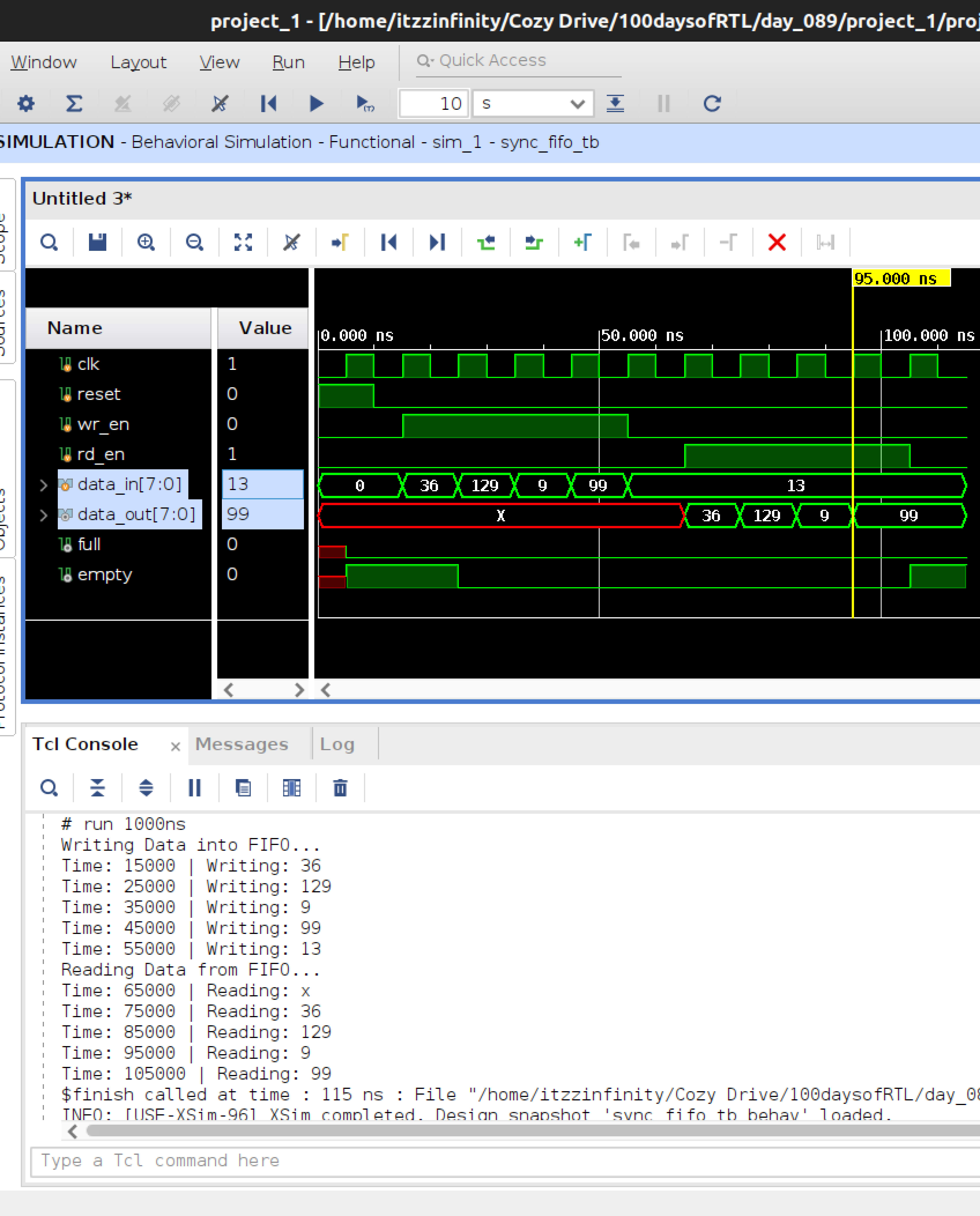
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/19/2024 08:30:28 AM
// Module Name: sync_fifo_tb
//////////////////////////////////////////////////////////////////////////////////

module sync_fifo_tb;

    parameter DATA_WIDTH = 8;
    parameter DEPTH = 16;

    reg clk, reset, wr_en, rd_en;
    reg [DATA_WIDTH-1:0] data_in;
    wire [DATA_WIDTH-1:0] data_out;
    wire full, empty;

    sync_fifo #(.DATA_WIDTH(DATA_WIDTH), .DEPTH(DEPTH)) DUT (
        .clk(clk),.reset(reset),
        .wr_en(wr_en),.rd_en(rd_en),
        .data_in(data_in),.data_out(data_out),
        .full(full),.empty(empty)
    );

    always #5 clk = ~clk;

    initial begin

        clk = 0; reset = 1; wr_en = 0; rd_en = 0; data_in = 0;
        #10 reset = 0;

        $display("Writing Data into FIFO...");       // Write data into the FIFO
        repeat (5) begin
            @(posedge clk);
            wr_en = 1; rd_en = 0;
            data_in = $random % 256; // Random 8-bit data
            $display("Time: %0t | Writing: %0d", $time, data_in);
        end
        wr_en = 0;

        $display("Reading Data from FIFO...");       // Read data from the FIFO
        repeat (5) begin
            @(posedge clk);
            rd_en = 1; wr_en = 0;
            $display("Time: %0t | Reading: %0d", $time, data_out);
        end
        rd_en = 0;
        #10 $finish;
    end
endmodule
```



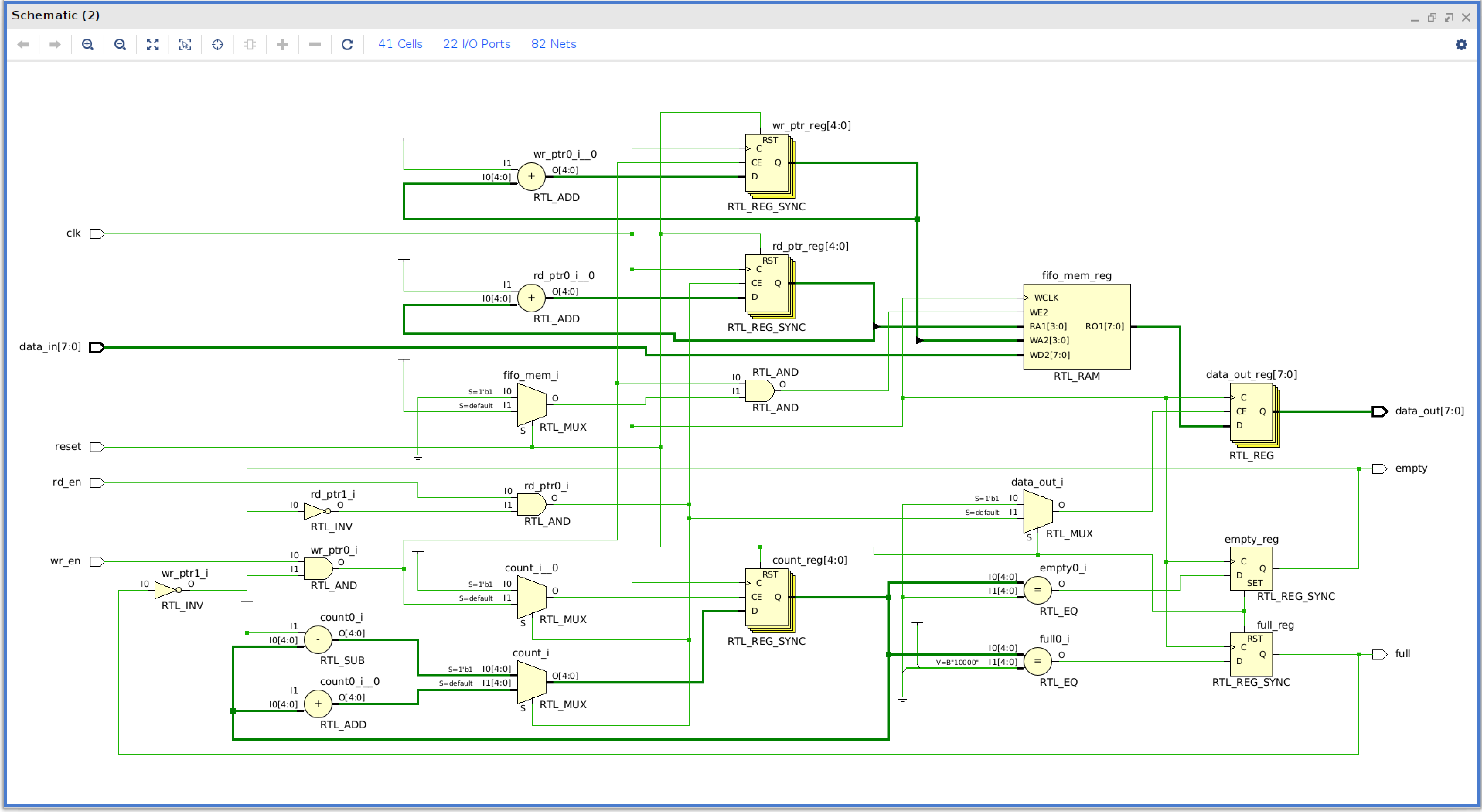
sync_fifo.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_089/project_1/project_1.srcs/sources_1/new/sync_fifo.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/19/2024 08:28:08 AM
// Module Name: sync_fifo
//////////////////////////////////////////////////////////////////////////////////

module sync_fifo #(
    parameter DATA_WIDTH = 8,
    parameter DEPTH = 16
)(
    input wire clk,rd_en,wr_en,reset,
    input wire [DATA_WIDTH-1:0] data_in,
    output reg [DATA_WIDTH-1:0] data_out,
    output reg full, empty
);

    // Declare FIFO memory
    reg [DATA_WIDTH-1:0] fifo_mem [0:DEPTH-1];

    reg [$clog2(DEPTH):0] wr_ptr;
    reg [$clog2(DEPTH):0] rd_ptr;
    reg [$clog2(DEPTH):0] count;

    always @(posedge clk) begin
        if (reset) begin
            wr_ptr <= 0;
            rd_ptr <= 0;
            count  <= 0;
            full   <= 0;
            empty  <= 1;
        end
        else begin
            if (wr_en && !full) begin
                fifo_mem[wr_ptr] <= data_in;
                wr_ptr <= wr_ptr + 1;
                count <= count + 1;
            end
            if (rd_en && !empty) begin
                data_out <= fifo_mem[rd_ptr];
                rd_ptr <= rd_ptr + 1;
                count <= count - 1;
            end

            full <= (count == DEPTH);
            empty <= (count == 0);
        end
    end
endmodule

```



```
# run 1000ns
Writing Data into FIFO...
Time: 15000 | Writing: 36
Time: 25000 | Writing: 129
Time: 35000 | Writing: 9
Time: 45000 | Writing: 99
Time: 55000 | Writing: 13
Reading Data from FIFO...
Time: 65000 | Reading: x
Time: 75000 | Reading: 36
Time: 85000 | Reading: 129
Time: 95000 | Reading: 9
Time: 105000 | Reading: 99
$finish called at time : 115 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_08
INFO: [USF-XSim-96] XSim completed. Design snapshot 'sync_fifo_tb_behav' loaded.
```



Schematic (2)
41 Cells
22 I/O Ports
82 Nets
clk
data_in[7:0]
reset
rd_en
wr_en
wr_ptr_reg[4:0]
wr_ptr0_i__0
RTL_ADD
RTL_REG_SYNC
rd_ptr_reg[4:0]
rd_ptr0_i__0
fifo_mem_reg
WCLK
WE2
RA1[3:0]
WA2[3:0]
WD2[7:0]
RO1[7:0]
RTL_RAM
fifo_mem_i
RTL_MUX
RTL_AND
data_out_reg[7:0]
RTL_REG
data_out[7:0]
empty
rd_ptr1_i
RTL_INV
rd_ptr0_i
data_out_i
wr_ptr0_i
wr_ptr1_i
count_i__0
count_reg[4:0]
empty0_i
RTL_EQ
empty_reg
full_reg
full
count0_i
RTL_SUB
count0_i__0
count_i
full0_i
V=B"10000"
S=1'b1
S=default