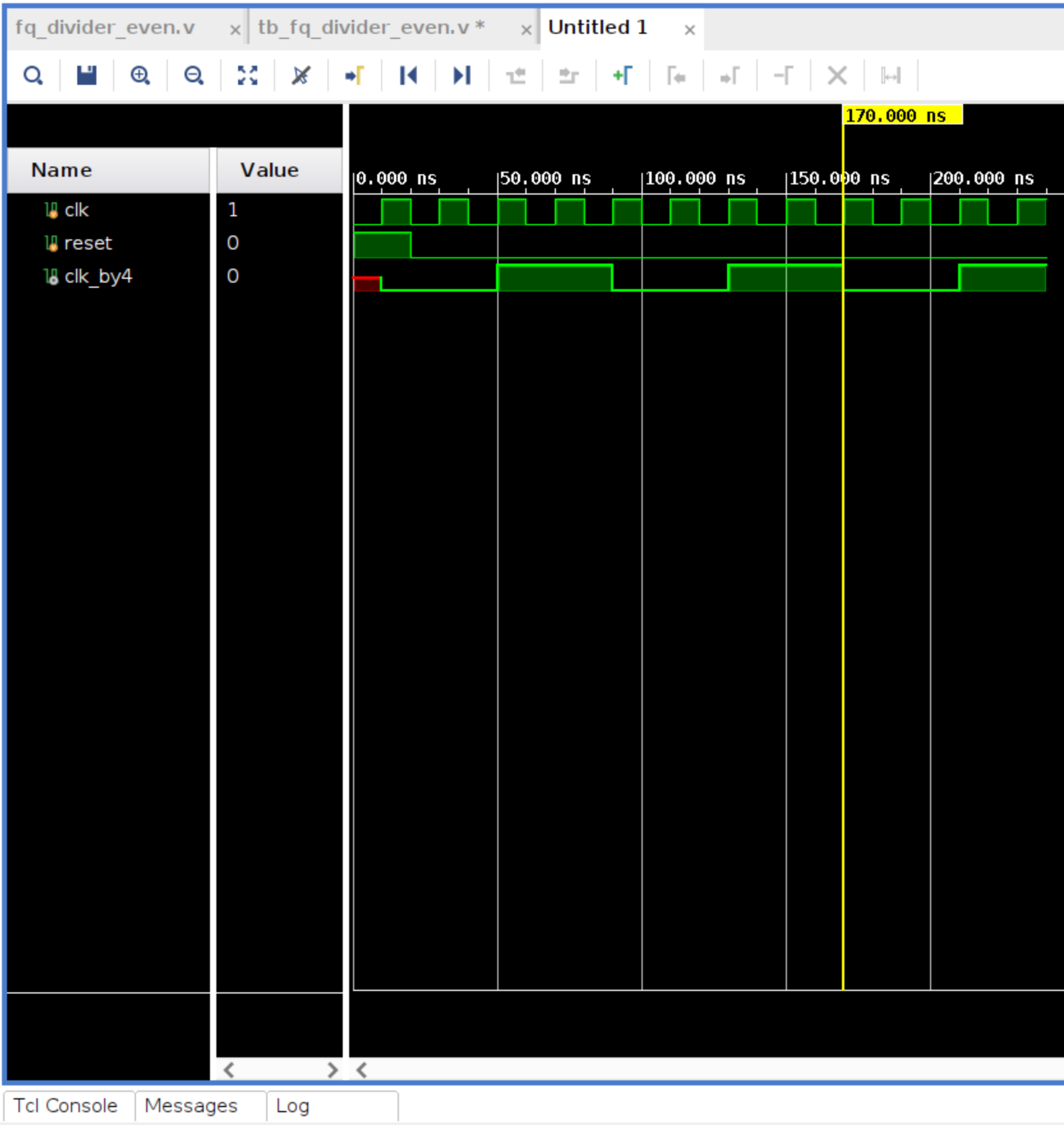
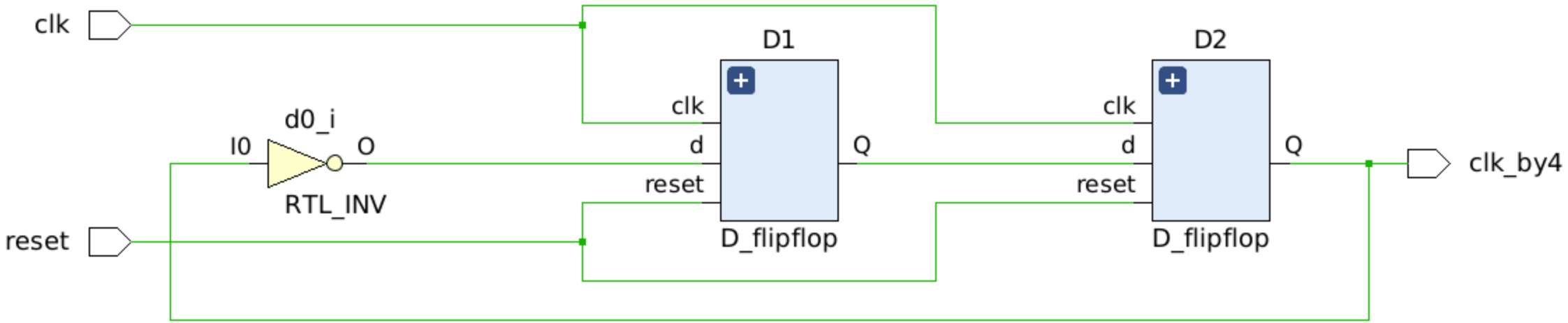

fq_divider_even.v
tb_fq_divider_even.v *
Untitled 1
Name
Value
clk
1
reset
0
clk_by4
0
170.000 ns
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
Tcl Console
Messages
Log

Project Summary | fq_divider_even.v | tb_fq_divider_even.v | Schematic

5 Cells 3 I/O Ports 13 Nets



fq_divider_even.v × | tb_fq_divider_even.v * × | Untitled 1 ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_071/project_1/project_1.srcs/sources_1/new/fq_divider_even.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 12/01/2024 06:26:38 AM
5  // Module Name: fq_divider_even
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9
10 module fq_divider_even(
11     input clk, reset,
12     output clk_by4
13     );
14     wire clk_by2;
15
16     D_flipflop D1(clk, reset, ~clk_by4, clk_by2);
17     D_flipflop D2(clk, reset, clk_by2, clk_by4);
18
19 endmodule
20
21
22
23
24
25
26
27
28
29
30
31
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34
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36
37
38
39
```

Tcl Console | Messages | Log

fq_divider_even.v | tb_fq_divider_even.v * | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_071/project_1/project_1.srcs/sim_1/new/tb_fq_divider_even.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 12/01/2024 06:42:06 AM
5  // Module Name: tb_fq_divider_even
6  //////////////////////////////////////////////////////////////////////////////////
7
8  `timescale 1ns / 1ps
9
10 module tb_fq_divider_even;
11
12 reg clk, reset;
13 wire clk_by4;
14
15 fq_divider_even DUT(clk, reset, clk_by4);
16
17 initial begin
18 clk= 1'b0;
19 forever #10 clk= ~clk;
20 end
21 initial begin
22 reset= 1'b1;
23 #20
24 reset= 1'b0;
25 #220 $finish;
26 end
27 endmodule
28
29
30
31
32
33
34
35
36
37
38
39
```

Tcl Console | Messages | Log