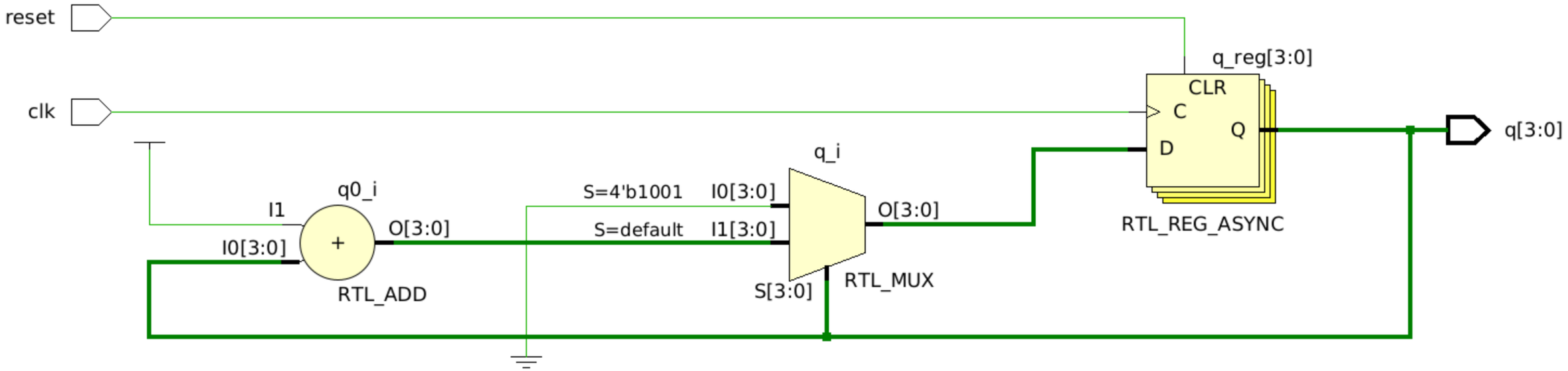
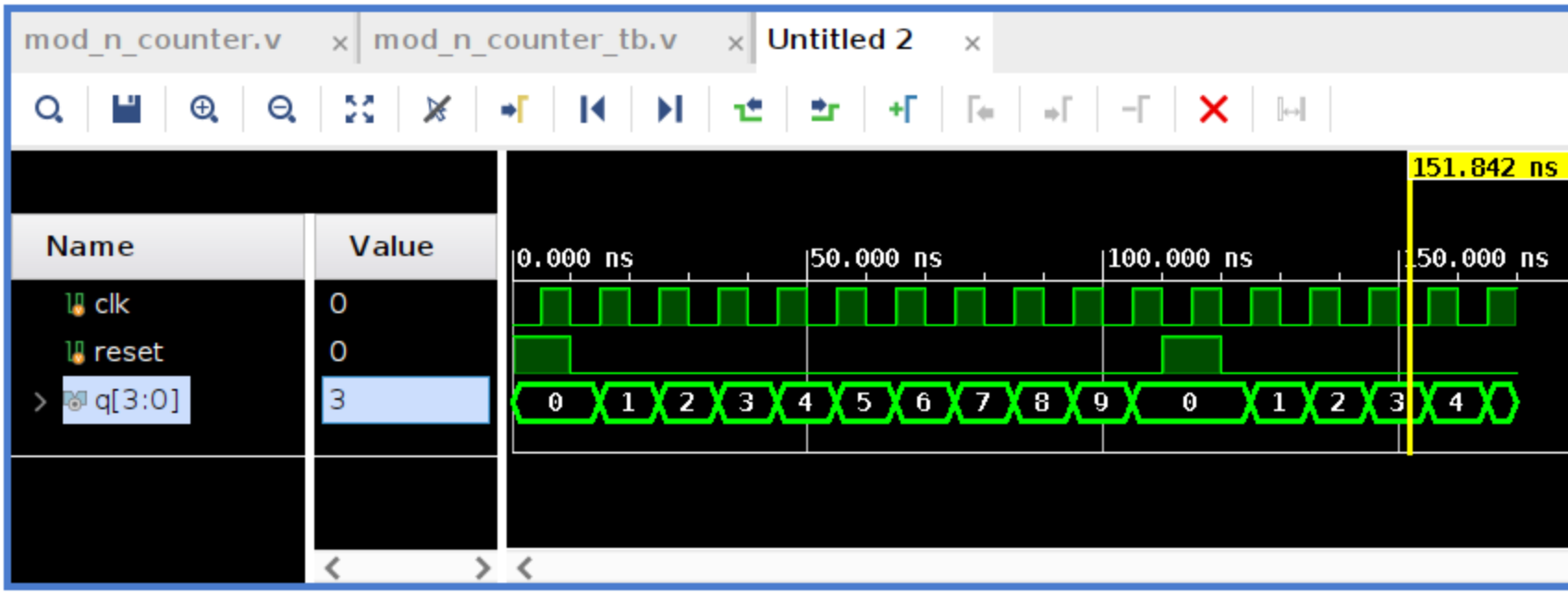

reset
clk
q_reg[3:0]
CLR
C
D
Q
RTL_REG_ASYNC
q[3:0]
q_i
S=4'b1001
I0[3:0]
O[3:0]
S=default
I1[3:0]
RTL_MUX
S[3:0]
q0_i
I1
I0[3:0]
+
O[3:0]
RTL_ADD



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```
# }
# run 1000ns
Time = 0 | Reset = 1 | Count =  0
Time = 10000 | Reset = 0 | Count =  0
Time = 15000 | Reset = 0 | Count =  1
Time = 25000 | Reset = 0 | Count =  2
Time = 35000 | Reset = 0 | Count =  3
Time = 45000 | Reset = 0 | Count =  4
Time = 55000 | Reset = 0 | Count =  5
Time = 65000 | Reset = 0 | Count =  6
Time = 75000 | Reset = 0 | Count =  7
Time = 85000 | Reset = 0 | Count =  8
Time = 95000 | Reset = 0 | Count =  9
Time = 105000 | Reset = 0 | Count =  0
Time = 110000 | Reset = 1 | Count =  0
Time = 120000 | Reset = 0 | Count =  0
Time = 125000 | Reset = 0 | Count =  1
Time = 135000 | Reset = 0 | Count =  2
Time = 145000 | Reset = 0 | Count =  3
Time = 155000 | Reset = 0 | Count =  4
Time = 165000 | Reset = 0 | Count =  5
$stop called at time : 170 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_065/p
```

Type a Tcl command here

mod_n_counter.v × | mod_n_counter_tb.v × | Untitled 2 ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_065/project_1/project_1.srcs/sources_1/new/mod_n_counter.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/25/2024 08:30:40 AM
5   // Module Name: mod_n_counter
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module mod_n_counter #(parameter n = 10)(
9       input clk,          // Clock signal
10      input reset,        // Active high reset
11      output reg [$clog2(n)-1:0] q // Dynamically calculate bit-width
12  );
13
14      always @(posedge clk or posedge reset) begin
15          if (reset)
16              q <= 0;                 // Reset counter to 0
17          else if (q == n-1)
18              q <= 0;                 // Reset to 0 after reaching n-1
19          else
20              q <= q + 1;             // Increment counter
21      end
22
23  endmodule
24
25
26
```

Scope
Sources
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mod_n_counter.v × | mod_n_counter_tb.v × | Untitled 2 ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_065/project_1/project_1.srcs/sim_1/new/mod_n_counter_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/25/2024 08:42:16 AM
5   // Module Name: mod_n_counter_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module mod_n_counter_tb;
9
10      reg clk, reset;
11      wire [3:0] q;  // Assuming n=10, q is 4 bits wide
12
13      mod_n_counter #(10) DUT (
14          .clk(clk),
15          .reset(reset),
16          .q(q)
17      );
18
19      initial begin
20          clk = 0;
21          forever #5 clk = ~clk;
22      end
23
24
25      initial begin
26          reset = 1;
27          #10 reset = 0;
28
29          #100;
30          reset = 1;
31          #10 reset = 0;
32
33          #50 $stop;
34      end
35
36      initial begin
37          $monitor("Time = %0t | Reset = %b | Count = %d", $time, reset, q);
38      end
39
```

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