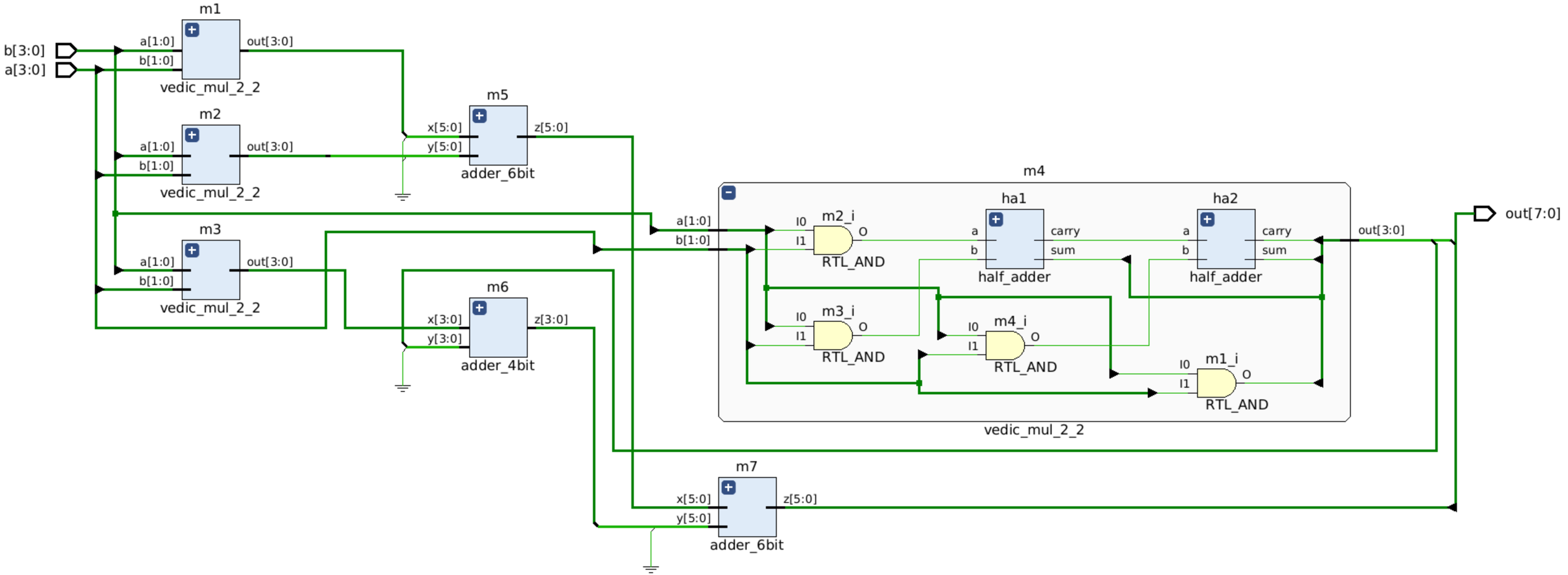

b[3:0]
a[3:0]
m1
a[1:0]
b[1:0]
out[3:0]
vedic_mul_2_2
m2
a[1:0]
b[1:0]
out[3:0]
vedic_mul_2_2
m3
a[1:0]
b[1:0]
out[3:0]
vedic_mul_2_2
m5
x[5:0]
y[5:0]
z[5:0]
adder_6bit
m6
x[3:0]
y[3:0]
z[3:0]
adder_4bit
m7
x[5:0]
y[5:0]
z[5:0]
adder_6bit
m4
a[1:0]
b[1:0]
m2_i
I0
I1
O
RTL_AND
m3_i
I0
I1
O
RTL_AND
m4_i
I0
I1
O
RTL_AND
m1_i
I0
I1
O
RTL_AND
ha1
a
b
carry
sum
half_adder
ha2
a
b
carry
sum
half_adder
out[3:0]
vedic_mul_2_2
out[7:0]

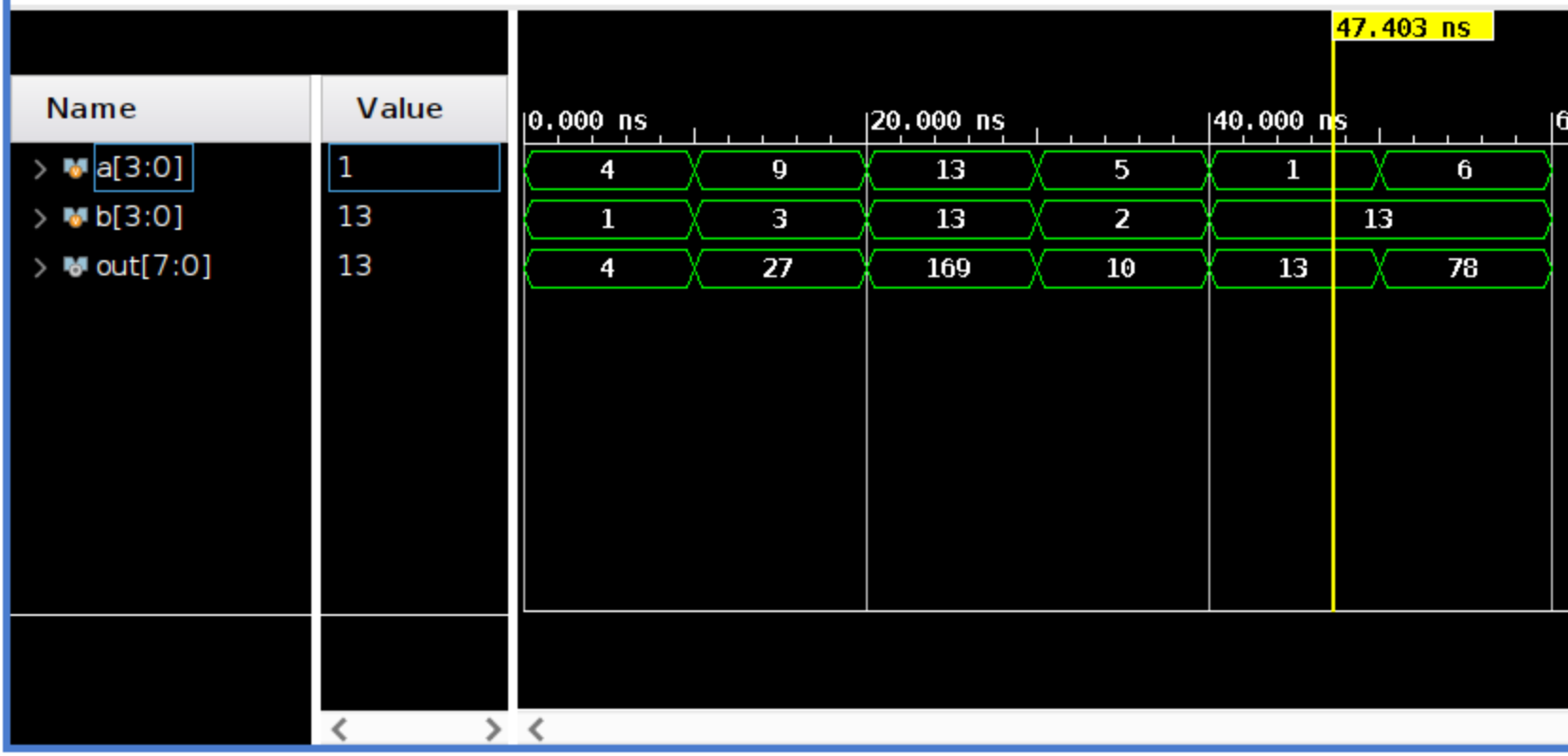
project_1 - [/home/itzzinfinity/Cozy Drive/100daysofRTL/day_064/project_1/pro

Window Layout View Run Help Quick Access

100 ms

SIMULATION - Behavioral Simulation - Functional - sim_1 - test_bench

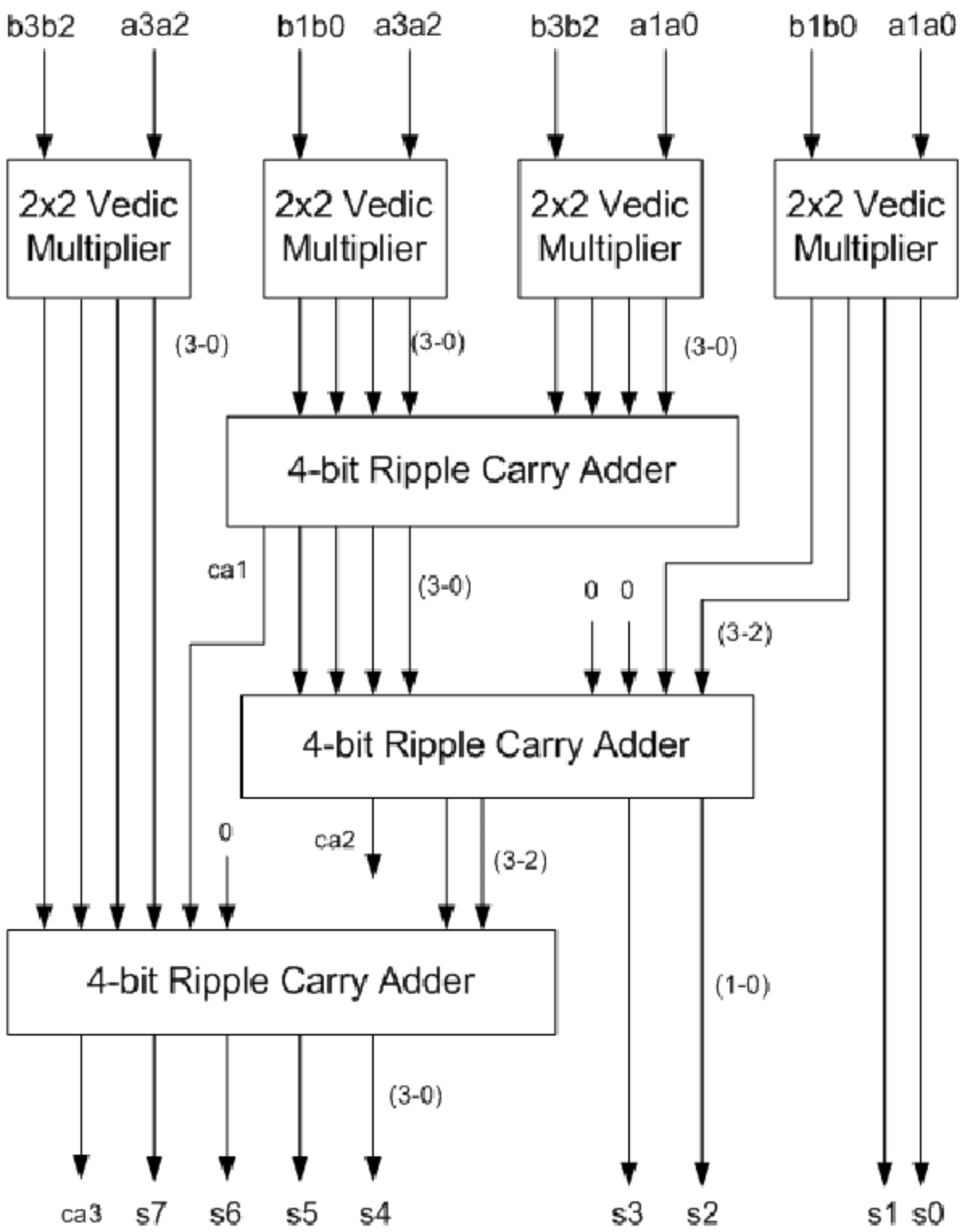
Untitled 2* test_bench.v



Tcl Console Messages Log

```
#   }
# }
# run 1000ns
 4 *  1 =   4
 9 *  3 =  27
13 * 13 = 169
 5 *  2 =  10
 1 * 13 =  13
 6 * 13 =  78
$finish called at time : 60 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_06
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_bench_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory (MB): peak = 9
```

Type a Tcl command here


b3b2
a3a2
b1b0
a3a2
b3b2
a1a0
b1b0
a1a0
2x2 Vedic Multiplier
2x2 Vedic Multiplier
2x2 Vedic Multiplier
2x2 Vedic Multiplier
(3-0)
(3-0)
(3-0)
4-bit Ripple Carry Adder
ca1
(3-0)
0 0
(3-2)
4-bit Ripple Carry Adder
0
ca2
(3-2)
4-bit Ripple Carry Adder
(1-0)
(3-0)
ca3
s7
s6
s5
s4
s3
s2
s1
s0

vedic_mul_4_4.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_064/project_1/project_1.srcs/sources_1/new/vedic_mul_4_4.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/24/2024 05:19:14 AM
// Module Name: vedic_mul_4_4
//////////////////////////////////////////////////////////////////////////////////

module vedic_mul_4_4(
    input [3:0] a,b,
    output [7:0] out
    );

    wire [3:0] w3,w2,w1,w0,w;
    wire [5:0] w4;

    vedic_mul_2_2 m1(b[3:2],a[3:2],w3[3:0]);
    vedic_mul_2_2 m2(b[3:2],a[1:0],w2[3:0]);
    vedic_mul_2_2 m3(b[1:0],a[3:2],w1[3:0]);
    vedic_mul_2_2 m4(b[1:0],a[1:0],w0[3:0]);

    adder_6bit m5({w3[3:0],2'b00},{2'b00,w2[3:0]},w4);

    adder_4bit m6(w1[3:0],{2'b00,w0[3:2]},w);

    adder_6bit m7(w4,{2'b00,w[3:0]},out[7:2]);

    assign out[1:0]=w0[1:0];

endmodule
```

half_adder.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_064/project_1/project_1.srcs/sources_1/new/half_adder.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/24/2024 05:19:14 AM
5  // Module Name: half_adder
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module half_adder(
9      input a,b,
10     output sum,carry
11     );
12     assign sum=a^b;
13     assign carry=a&b;
14 endmodule
```

adder_4bit.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_064/project_1/project_1.srcs/sources_1/new/adder_4bit.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/24/2024 05:19:14 AM
5  // Module Name: adder_4bit
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module adder_4bit(
9          input [3:0] x,y,
10         output [3:0] z
11         );
12     assign z=x+y;
13 endmodule
14
```

adder_6bit.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_064/project_1/project_1.srcs/sources_1/new/adder_6bit.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/24/2024 05:19:14 AM
5  // Module Name: adder_6bit
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module adder_6bit(
9          input [5:0] x,y,
10         output [5:0] z
11         );
12     assign z=x+y;
13 endmodule
```

vedic_mul_2_2.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_064/project_1/project_1.srcs/sources_1/new/vedic_mul_2_

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/24/2024 05:19:14 AM
5  // Module Name: vedic_mul_2_2
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module vedic_mul_2_2(
9      input [1:0] a,b,
10     output [3:0] out
11      );
12 wire [3:0] w;
13
14     and m1(out[0],a[0],b[0]);
15     and m2(w[0],a[0],b[1]);
16     and m3(w[1],a[1],b[0]);
17     and m4(w[2],a[1],b[1]);
18
19     half_adder ha1(w[0],w[1],out[1],w[3]);
20     half_adder ha2(w[3],w[2],out[2],out[3]);
21
22 endmodule
23
```

test_bench.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_064/project_1/project_1.srcs/sim_1/new/test_bench.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/24/2024 05:33:14 AM
5  // Module Name: test_bench
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module test_bench;
9  reg [3:0] a,b;
10 wire [7:0] out;
11
12 vedic_mul_4_4 DUT(a,b,out);
13
14 always begin
15 a=$random;
16 b=$random;
17 #10;
18 end
19
20 initial begin
21 $monitor("%d * %d = %d", a,b,out);
22 #60 $finish;
23 end
24 endmodule
```