

```
timescale 1ns / 1ps
             module alu 8bit (
                 input wire [7:0] A,
                 input wire [7:0] B,
input wire [3:0] opcode,
                output reg [7:0] result,
                output reg carry,
                 output reg zero,
                 output reg overflow,
                 output reg sign
                 reg [15:0] temp;
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                localparam ADD
                 localparam AND
                                   = 4'b0010;
•
                 localparam OR
                 localparam XOR
                                 = 4'b0100;
                 localparam NOT
                                  = 4'b0101;
                 localparam LSHIFT = 4'b0110;
                 localparam RSHIFT = 4'b0111;
                 localparam LT
                 localparam EQ localparam INC
                 localparam DEC
                 localparam MUL
                 localparam DIV
                 always @(*) begin
                     carry = 0;
                    overflow = 0;
                     zero = 0;
                     sign = 0;
                     case (opcode)
                         ADD: begin
                             temp = A + B;
                             result = temp[7:0];
                             carry = temp[8]; // Capture carry
                             overflow = (~A[7] & ~B[7] & result[7]) | (A[7] & B[7] & ~result[7]); // Overflow check
                         end
                         SUB: begin
                             temp = A - B;
                             result = temp[7:0];
                             carry = (A < B);
                             overflow = (A[7] & ~B[7] & ~result[7]) | (~A[7] & B[7] & result[7]); // Overflow check
                         AND: result = A & B;
                         OR: result = A | B;
                         XOR: result = A ^ B;
                         NOT: result = ~A;
                         LSHIFT: result = A << 1;
                         RSHIFT: result = A >>
                         LT: result = (A < B);
                         EQ: result = (A == B);
                         INC: begin
                             temp = A + 1;
                             result = temp[7:0];
                             carry = temp[8];
                         DEC: begin
                             temp = A - 1;
                            result = temp[7:0];
                            carry = (A == 0);
                         MUL: begin
                             temp = A * B;
                             result = temp[7:0];
                             carry = temp[15:8] != 0;
                         end
                         DIV: begin
                            if (B != 0) begin
                               result = A / B;
                                carry = 0;
                                result = 8'b00000000;
                                carry = 1;
                             end
                         default: result = 8'b000000000;
                     zero = (result == 8'b000000000);
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                     sign = result[7];
             endmodule
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4 // Create Date: 11/10/2024 05:24:45 AM
     `timescale 1ns / 1ps
     module tb alu 8bit;
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         reg [7:0] A;
         reg [7:0] B;
         reg [3:0] opcode;
         wire [7:0] result;
         wire carry;
         wire zero;
         wire overflow;
         wire sign;
             .A(A),.B(B),.opcode(opcode),.result(result),.carry(carry),.zero(zero),.overflow(overflow),.sign(sign)
         );
         task display results;
            input [7:0] A;
             input [7:0] B;
            input [3:0] opcode;
             input [7:0] expected result;
            input expected carry;
             input expected zero;
             input expected overflow;
             input expected sign;
                 $display("A = %b, B = %b, Opcode = %b | Result = %b, Carry = %b, Zero = %b, Overflow = %b, Sign = %b",
                          A, B, opcode, result, carry, zero, overflow, sign);
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                 if (result !== expected result)
                     $display("Error: Expected Result = %b", expected result);
                 if (carry !== expected carry)
                     $display("Error: Expected Carry = %b", expected carry);
                 if (zero !== expected zero)
                     $display("Error: Expected Zero = %b", expected zero);
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task display results;
                 if (zero !== expected zero)
                 if (overflow !== expected overflow)
                     $display("Error: Expected Overflow = %b", expected overflow);
                 if (sign !== expected sign)
                     $display("Error: Expected Sign = %b", expected sign);
             end
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         initial begin
             A = 8'b00001111; B = 8'b00000001; opcode = 4'b0000;
             #10 display results (A, B, opcode, 8'b00010000, 1'b0, 1'b0, 1'b0, 1'b0);
             A = 8'b011111111; B = 8'b00000001; opcode = 4'b0000;
             #10 display results (A, B, opcode, 8'b10000000, 1'b0, 1'b0, 1'b1, 1'b1);
             A = 8'b00001000; B = 8'b00000100; opcode = 4'b0001;
             #10 display results (A, B, opcode, 8'b00000100, 1'b0, 1'b0, 1'b0, 1'b0);
             A = 8'b00001000; B = 8'b00001000; opcode = 4'b0001;
             #10 display_results(A, B, opcode, 8'b000000000, 1'b0, 1'b1, 1'b0, 1'b0);
             A = 8'b000000000; B = 8'b00000001; opcode = 4'b0001;
             #10 display results (A, B, opcode, 8'b11111111, 1'b1, 1'b0, 1'b0, 1'b1);
             A = 8'b11001100; B = 8'b10101010; opcode = 4'b0010;
             #10 display results(A, B, opcode, 8'b10001000, 1'b0, 1'b0, 1'b0, 1'b0);
             A = 8'b11001100; B = 8'b10101010; opcode = 4'b0011;
             #10 display results (A, B, opcode, 8'b11101110, 1'b0, 1'b0, 1'b0, 1'b0);
             A = 8'b11001100; B = 8'b10101010; opcode = 4'b0100;
             #10 display results (A, B, opcode, 8'b01100110, 1'b0, 1'b0, 1'b0, 1'b0);
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             A = 8'b00001111; opcode = 4'b0101;
             #10 display results (A, B, opcode, 8'b11110000, 1'b0, 1'b0, 1'b0, 1'b1);
             A = 8'b00001111; opcode = 4'b0110;
             #10 display results (A, B, opcode, 8'b00011110, 1'b0, 1'b0, 1'b0, 1'b0);
             A = 8'b00001111; opcode = 4'b0111;
                                                                                                                          // A RSHIFT
             #10 display results (A, B, opcode, 8'b00000111, 1'b0, 1'b0, 1'b0, 1'b0);
                     polapiay( Error: Expected Zero - wp , expected Zero);
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module tb alu 8bit;

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initial begin
    A - o booodilli; opcode - a bolli;
   #10 display_results(A, B, opcode, 8'b00000111, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b00001000; B = 8'b00000100; opcode = 4'b1000;
   #10 display results(A, B, opcode, 8'b00000000, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b00000100; B = 8'b00001000; opcode = 4'b1000;
    #10 display results(A, B, opcode, 8'b00000001, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b00001000; B = 8'b00001000; opcode = 4'b1001;
   #10 display results (A, B, opcode, 8'b00000001, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b00001111; opcode = 4'b1010;
   #10 display results(A, B, opcode, 8'b00010000, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b000000001; opcode = 4'b1011;
    #10 display results(A, B, opcode, 8'b00000000, 1'b0, 1'b1, 1'b0, 1'b0);
   A = 8'b000000000; opcode = 4'b1011;
   #10 display results (A, B, opcode, 8'b111111111, 1'b1, 1'b0, 1'b0, 1'b1);
   A = 8'b00000010; B = 8'b00000010; opcode = 4'b1100;
   #10 display results (A, B, opcode, 8'b00000100, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b00001000; B = 8'b00000010; opcode = 4'b1100;
   #10 display results (A, B, opcode, 8'b00010000, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b00001000; B = 8'b00000010; opcode = 4'b1101;
    #10 display results(A, B, opcode, 8'b00000100, 1'b0, 1'b0, 1'b0, 1'b0);
   A = 8'b00000000; B = 8'b00000001; opcode = 4'b1101;
   #10 display results (A, B, opcode, 8'b00000000, 1'b0, 1'b1, 1'b0, 1'b0);
   A = 8'b00001000; B = 8'b00000000; opcode = 4'b1101;
   #10 display results (A, B, opcode, 8'b00000000, 1'b1, 1'b0, 1'b0, 1'b0);
   $finish;
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135 endmod

end

module tb alu 8bit;

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