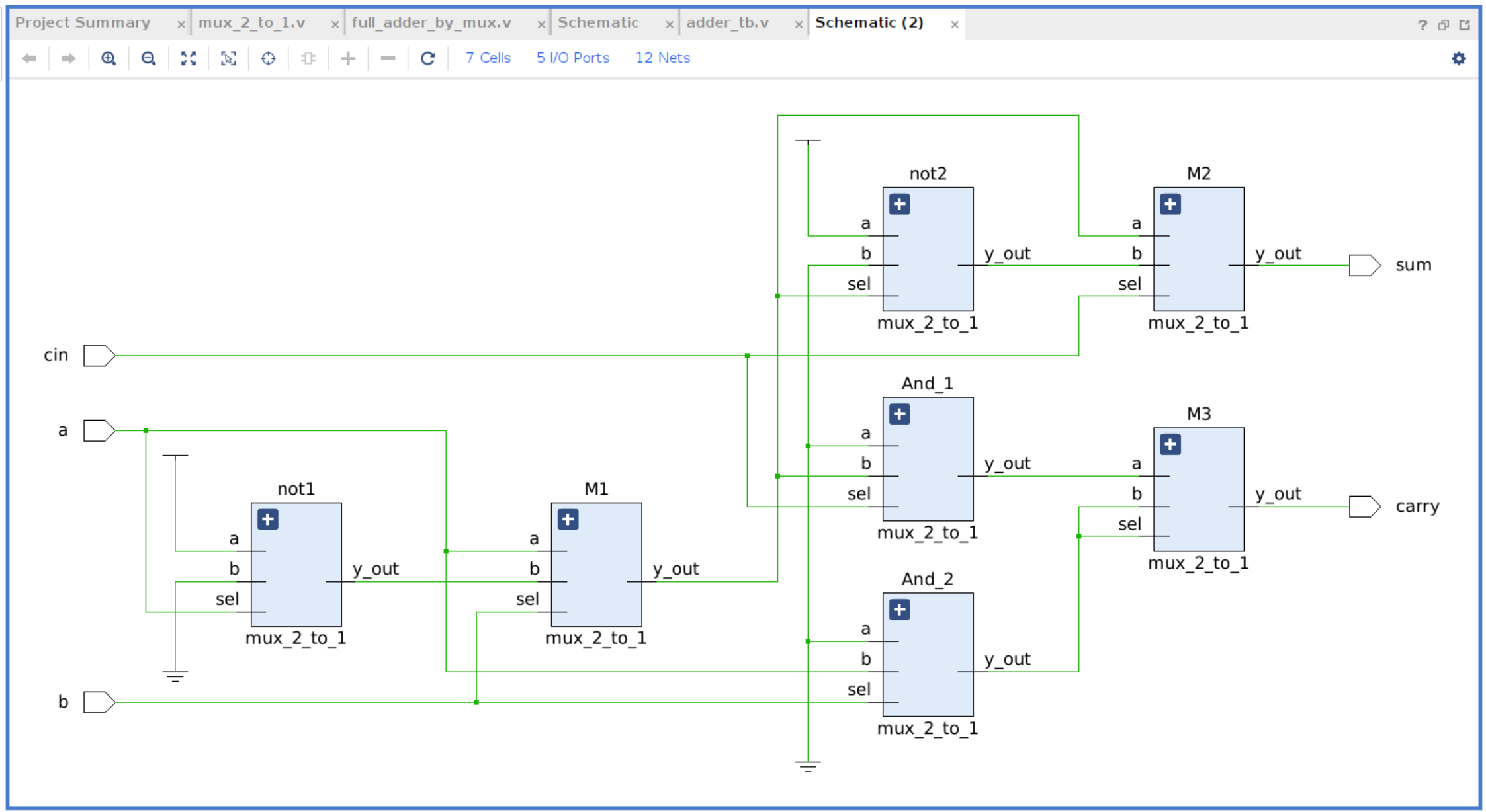
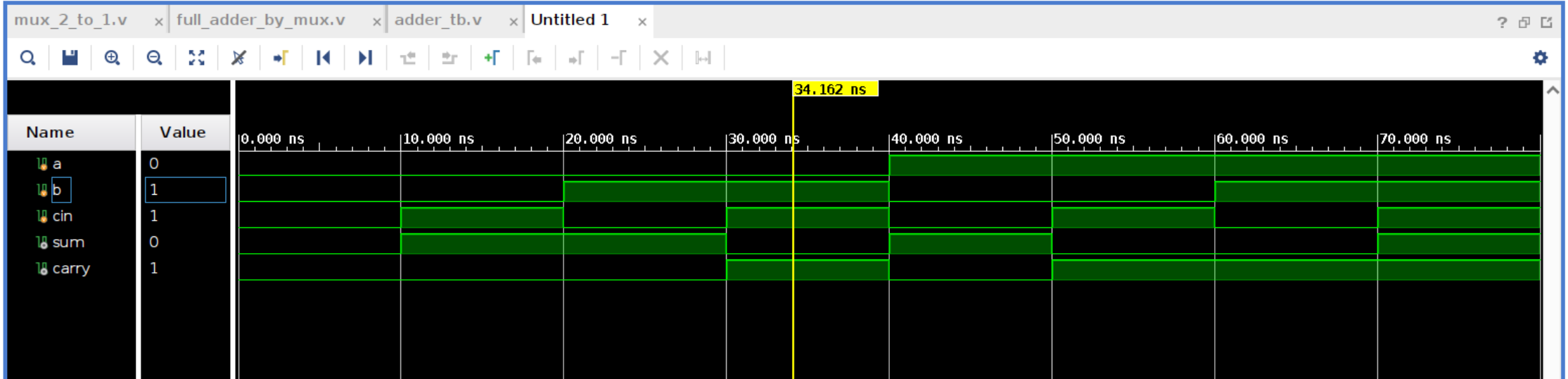

Project Summary
mux_2_to_1.v
full_adder_by_mux.v
Schematic
adder_tb.v
Schematic (2)
7 Cells
5 I/O Ports
12 Nets
not2
M2
a
b
sel
y_out
mux_2_to_1
sum
cin
And_1
M3
carry
a
b
not1
M1
And_2
sel
y_out
mux_2_to_1


mux_2_to_1.v
full_adder_by_mux.v
adder_tb.v
Untitled 1
34.162 ns
Name
Value
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
a
0
b
1
cin
1
sum
0
carry
1

mux_2_to_1.v | full_adder_by_mux.v | adder_tb.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_027/project_1/project_1.srcs/sources_1/new/full_adder_by_mux.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/18/2024 08:38:25 AM
5  // Module Name: full_adder_by_mux
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module full_adder_by_mux(
10     input a,b,cin,
11     output sum, carry
12     );
13     wire [4:0]w;
14
15     mux_2_to_1 not1(1'b1, 1'b0, a, w[0]);
16     mux_2_to_1 M1(a, w[0], b, w[1]);
17     mux_2_to_1 not2(1'b1, 1'b0, w[1], w[2]);
18     mux_2_to_1 M2(w[1], w[2], cin, sum);
19
20     mux_2_to_1 And_1(1'b0, w[1], cin, w[3]);
21     mux_2_to_1 And_2(1'b0, a, b, w[4]);
22     mux_2_to_1 M3(w[3], w[4], w[4], carry);
23
24 endmodule
```

mux_2_to_1.v | full_adder_by_mux.v | adder_tb.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_027/project_1/project_1.srcs/sim_1/new/adder_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/18/2024 08:47:52 AM
5  //////////////////////////////////////////////////////////////////////////////////
6
7
8  module adder_tb;
9    reg a, b, cin;
10   wire sum, carry;
11
12   full_adder_by_mux DUT(a, b, cin, sum, carry);
13
14   initial begin
15
16     a = 0; b = 0; cin = 0;
17     #10;
18     a = 0; b = 0; cin = 1;
19     #10;
20     a = 0; b = 1; cin = 0;
21     #10;
22     a = 0; b = 1; cin = 1;
23     #10;
24     a = 1; b = 0; cin = 0;
25     #10;
26     a = 1; b = 0; cin = 1;
27     #10;
28     a = 1; b = 1; cin = 0;
29     #10;
30     a = 1; b = 1; cin = 1;
31     #10;
32   end
33
34     initial begin
35     $monitor("a = %b, b = %b, cin = %b, sum = %b, carry = %b", a, b, cin, sum, carry);
36     #80 $finish;
37   end
38 endmodule
```

mux_2_to_1.v | full_adder_by_mux.v | adder_tb.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_027/project_1/project_1.srcs/sources_1/new/mux_2_to_1.v

```
1   module mux_2_to_1(
2       input a,b,
3       input sel,
4       output y_out
5       );
6       assign y_out= sel ? b : a;
7   endmodule
```