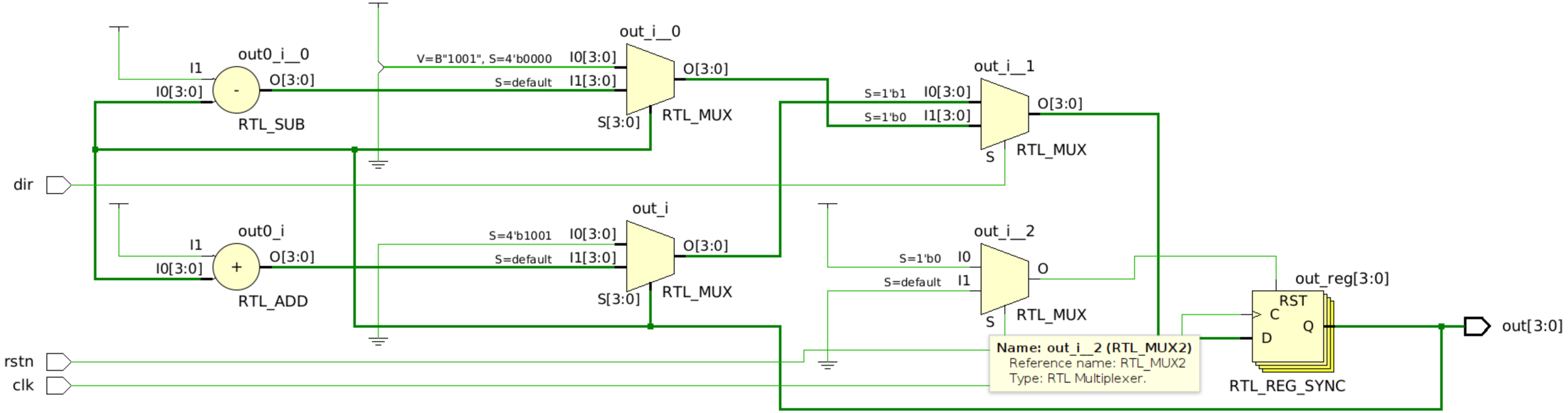
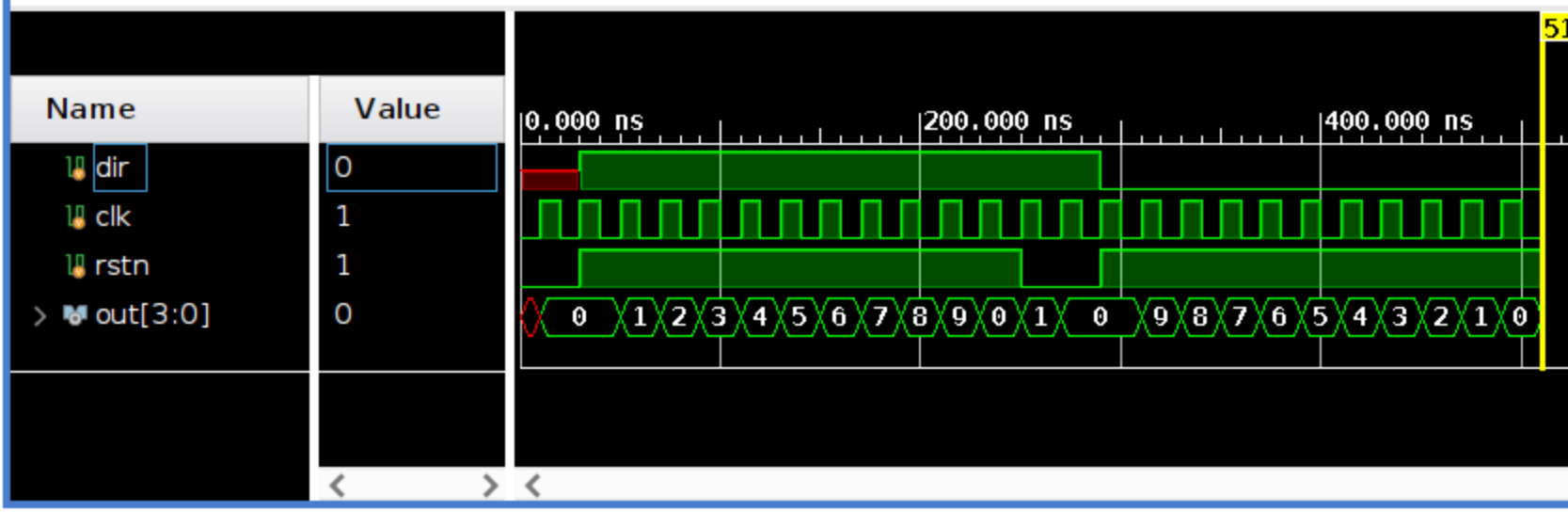

out0_i__0
I1
I0[3:0]
-
O[3:0]
RTL_SUB
out_i__0
V=B"1001", S=4'b0000
S=default
I0[3:0]
I1[3:0]
O[3:0]
S[3:0]
RTL_MUX
out_i__1
S=1'b1
S=1'b0
I0[3:0]
I1[3:0]
O[3:0]
S
RTL_MUX
dir
out0_i
I1
I0[3:0]
+
O[3:0]
RTL_ADD
out_i
S=4'b1001
S=default
I0[3:0]
I1[3:0]
O[3:0]
S[3:0]
RTL_MUX
out_i__2
S=1'b0
S=default
I0
I1
O
S
RTL_MUX
out_reg[3:0]
RST
C
D
Q
RTL_REG_SYNC
out[3:0]
rstn
clk
Name: out_i__2 (RTL_MUX2)
Reference name: RTL_MUX2
Type: RTL Multiplexer.

Up_Down_Counter.v | Up_Down_Counter_tb.v | Untitled 4*



Tcl Console | Messages | Log

```
T=210000 rstn=1 out=0x9
T=230000 rstn=1 out=0x0
T=250000 rstn=0 out=0x1
T=250000 rstn=0 out=0x1
T=270000 rstn=0 out=0x0
T=270000 rstn=0 out=0x0
T=290000 rstn=1 out=0x0
T=290000 rstn=1 out=0x0
T=310000 rstn=1 out=0x9
T=310000 rstn=1 out=0x9
T=330000 rstn=1 out=0x8
T=330000 rstn=1 out=0x8
T=350000 rstn=1 out=0x7
T=350000 rstn=1 out=0x7
T=370000 rstn=1 out=0x6
T=370000 rstn=1 out=0x6
T=390000 rstn=1 out=0x5
T=390000 rstn=1 out=0x5
T=410000 rstn=1 out=0x4
T=410000 rstn=1 out=0x4
T=430000 rstn=1 out=0x3
```

Type a Tcl command here

Up_Down_Counter.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_067/project_1/project_1.srcs/sources_1/new/Up_Down_Counter.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/27/2024 06:20:37 AM
5  // Module Name: Up_Down_Counter
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module Up_Down_Counter #(parameter N = 10,
10     parameter WIDTH = 4)
11
12   ( input   clk,
13     input   rstn,
14     input   dir,
15     output  reg [WIDTH-1:0] out);
16
17   always @ (posedge clk) begin
18     if (!rstn) begin
19       out <= 0;
20     end else begin
21     case(dir)
22     1'b1: begin
23       if (out == N-1)
24         out <= 0;
25       else
26         out <= out + 1;
27         end
28      1'b0: begin
29         if (out == 0)
30         out <= 9;
31       else
32         out <= out - 1;
33         end
34     endcase
35
36      end
37    end
38 endmodule
39
```

Up_Down_Counter_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_067/project_1/project_1.srcs/sim_1/new/Up_Down_Counter_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/24/2024 06:22:12 AM
5  // Module Name: Up_Down_Counter_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module Up_Down_Counter_tb;
10 parameter N = 10;
11   parameter WIDTH = 4;
12   reg dir;
13   reg clk;
14   reg rstn;
15   wire [WIDTH-1:0] out;
16
17   Up_Down_Counter DUT(  .clk(clk),
18                         .rstn(rstn),
19                         .out(out),
20                         .dir(dir));
21
22   always #10 clk = ~clk;
23
24   initial begin
25     {clk, rstn} <= 0;
26     // up count
27     $monitor ("T=%0t rstn=%0b out=0x%0h", $time, rstn, out);
28     repeat(2) @ (posedge clk);
29     rstn <= 1;
30     dir <=1;
31     repeat(11) @ (posedge clk);
32      // down time
33     rstn <= 0;
34
35     $monitor ("T=%0t rstn=%0b out=0x%0h", $time, rstn, out);
36     repeat(2) @ (posedge clk);
37     rstn <= 1;
38     dir <=0;
39     repeat(11) @ (posedge clk);
40     $finish;
41   end
42 endmodule
43
```