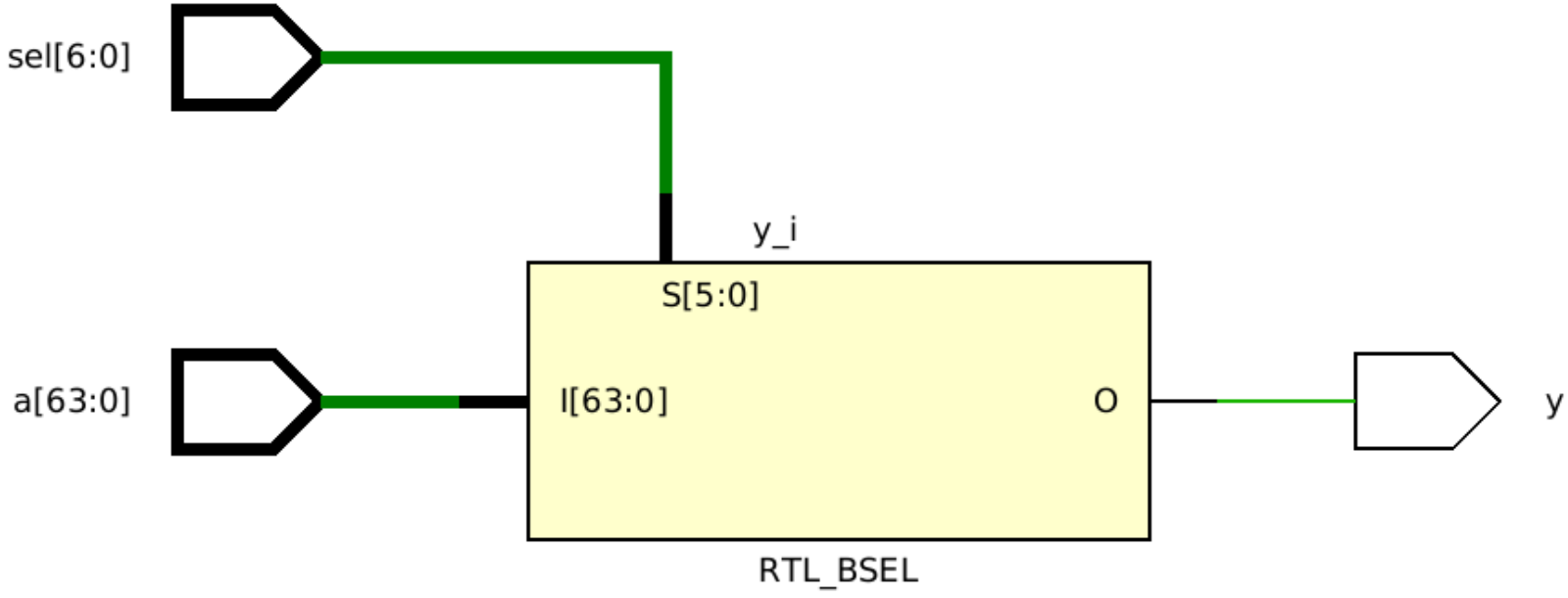
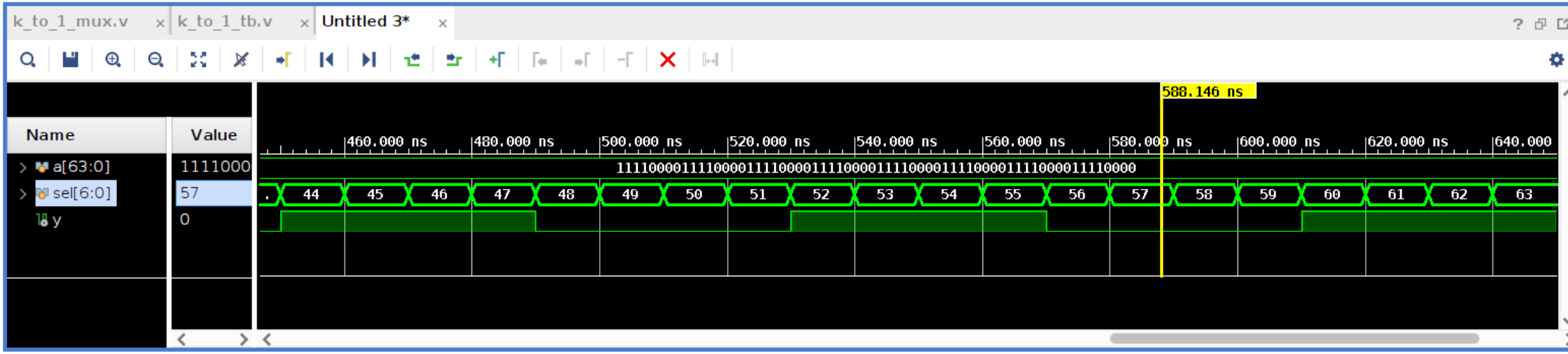

sel[6:0]
y_i
S[5:0]
a[63:0]
I[63:0]
O
y
RTL_BSEL



Tcl Console | Messages | Log

```
sel =  43, y = 0
sel =  44, y = 1
sel =  45, y = 1
sel =  46, y = 1
sel =  47, y = 1
sel =  48, y = 0
sel =  49, y = 0
sel =  50, y = 0
sel =  51, y = 0
sel =  52, y = 1
sel =  53, y = 1
sel =  54, y = 1
sel =  55, y = 1
sel =  56, y = 0
sel =  57, y = 0
sel =  58, y = 0
sel =  59, y = 0
sel =  60, y = 1
sel =  61, y = 1
sel =  62, y = 1
sel =  63, y = 1
```

Type a Tcl command here

k_to_1_mux.v | k_to_1_tb.v | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_025/project_1/project_1.srcs/sources_1/new/k_to_1_mux.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/16/2024 07:00:13 AM
5   // Module Name: k_to_1_mux
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module k_to_1_mux
10  #(parameter N = 64)(
11  input [N-1:0]a,
12  input [6:0] sel,
13  output y
14      );
15      assign y = a[sel];
16  endmodule
17
```

Project Summary | k_to_1_mux.v | **k_to_1_tb.v**

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_025/project_1/project_1.srcs/sim_1/new/k_to_1_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/16/2024 07:00:13 AM
5  // Module Name: k_to_1_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module k_to_1_tb;
9    reg [63:0] a;
10   reg [6:0] sel;
11   wire y;
12   k_to_1_mux #(64) uut (
13     .a(a),
14     .sel(sel),
15     .y(y)
16   );
17
18   initial begin
19     a = 64'h0;
20     #10;
21     a = 64'hF0F0F0F0F0F0F0F0;  // Sample input pattern
22     for (sel = 0; sel < 64; sel = sel + 1) begin
23       #10;
24       $display("sel = %d, y = %b", sel, y);
25     end
26     $finish;
27   end
28 endmodule
```