Project Summary | Schematic | **basic_gates.v** | basic_gates_tb.v

/home/itzzinfinity/Xilinx/study/100daysofRTL/day_001/Basic_Gates_Behavioral.srcs/sources_1/new/basic_gates.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/22/2024 08:57:06 PM
5  // Module Name: basic_gates
6  // Project Name: 100DaysofRTL
7  //////////////////////////////////////////////////////////////////////////////////
8
9  module basic_gates(
10 input a,b,
11 output reg out_and, out_or, out_nand, out_nor, out_xor, out_xnor);
12
13 always @(*) begin
14     out_and = a&b;
15     out_or = a|b;
16     out_nand =  ~(a&b);
17     out_nor = ~(a|b);
18     out_xor = a^b;
19     out_xnor = ~(a^b);
20 end
21 endmodule
22
```

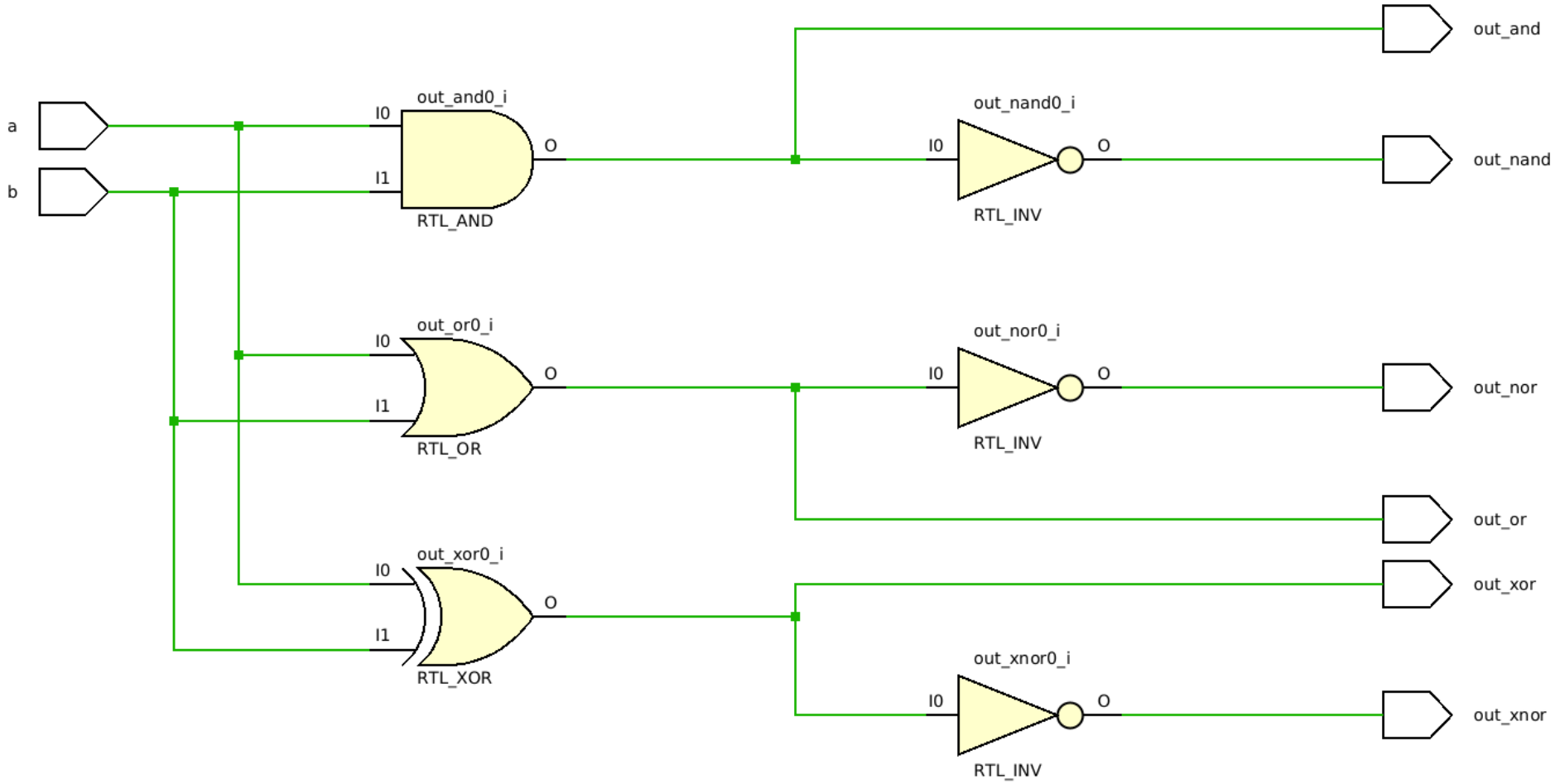
Project Summary | Schematic | basic_gates.v | **basic_gates_tb.v**

/home/itzzinfinity/Xilinx/study/100daysofRTL/day_001/Basic_Gates_Behavioral.srcs/sim_1/new/basic_gates_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/22/2024 08:57:06 PM
5  // Module Name: basic_gates
6  // Project Name: 100DaysofRTL
7  //////////////////////////////////////////////////////////////////////////////////
8
9
10 module basic_gates_tb;
11     reg a,b;
12     wire out_and, out_or, out_nand, out_nor, out_xor, out_xnor;
13     basic_gates DUT (a,b, out_and, out_or, out_nand, out_nor, out_xor, out_xnor);
14  initial begin
15  #10 a = 1'b0; b = 1'b0;
16  #10 a = 1'b0; b = 1'b1;
17  #10 a = 1'b1; b = 1'b0;
18  #10 a = 1'b1; b = 1'b1;
19 end
20 endmodule
21
```

Project Summary | Schematic | basic_gates.v | basic_gates_tb.v

6 Cells 8 I/O Ports 8 Nets



basic_gates.v | basic_gates_tb.v | Untitled 1*

Name	Value
a	1
b	0
out_and	0
out_or	1
out_nand	1
out_nor	0
out_xor	1
out_xnor	0