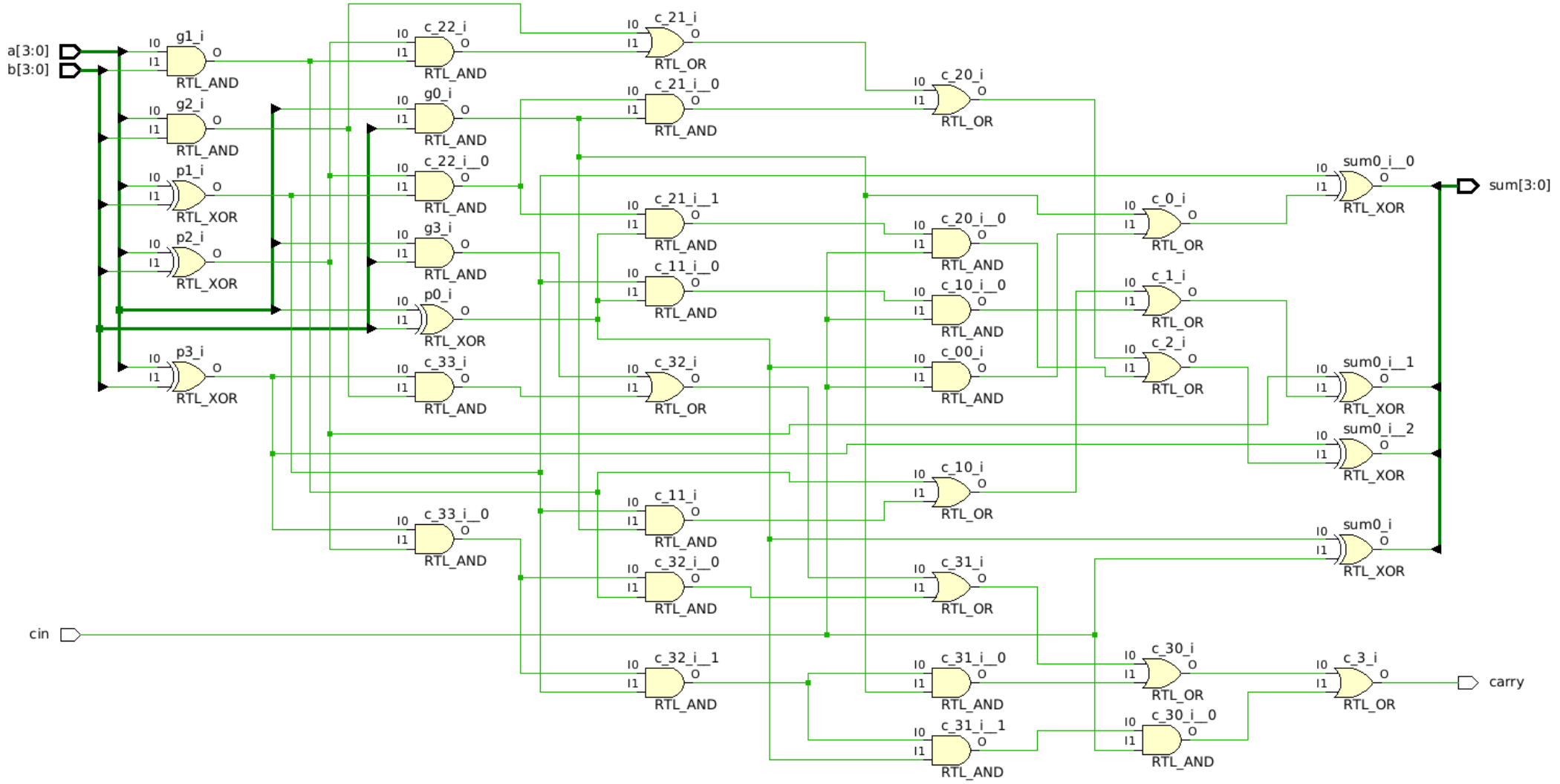
ELABORATED DESIGN - xc7a12ticsg325-1L

Sources

Project Summary | carry_look_ahead_adder.v | cla_tb.v | Schematic

38 Cells 14 I/O Ports 47 Nets



SIMULATION - Behavioral Simulation - Functional - sim_1 - cla_tb

carry_look_ahead_adder.v | cla_tb.v | Untitled 14*

8.077 ns

Name	Value
a[3:0]	1000
b[3:0]	0011
cin	0
sum[3:0]	1011
carry	0
add[4:0]	01011

	0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns	60.000 ns
a[3:0]	1000	0011	0110	0111	1011	1001	1110
b[3:0]	0011	1010	0110	1110	0110	0100	1110
cin							
sum[3:0]	1011	1110	1100	0101	0010	1101	
carry							
add[4:0]	01011	01110	01100	10101	10010	01101	11101

carry_look_ahead_adder.v | cla_tb.v | Untitled 14

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_016/project_1/project_1.srcs/sources_1/new/carry_look_ahead_adder.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/07/2024 06:43:35 AM
5   // Module Name: carry_look_ahead_adder
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module carry_look_ahead_adder(
10      input [3:0] a, b,
11      input cin,
12      output [3:0] sum,
13      output carry
14      );
15  wire p0, g0, p1, g1, p2, g2, p3, g3;
16  wire [3:0]c;
17
18  and (g0, a[0], b[0]),
19      (g1, a[1], b[1]),
20      (g2, a[2], b[2]),
21      (g3, a[3], b[3]);
22
23  xor (p0, a[0], b[0]),
24      (p1, a[1], b[1]),
25      (p2, a[2], b[2]),
26      (p3, a[3], b[3]);
27
28  xor (sum[0], p0, cin),
29      (sum[1], p1, c[0]),
30      (sum[2], p2, c[1]),
31      (sum[3], p3, c[2]);
32
33  assign  c[0] = g0 | (p0 & cin),
34          c[1] = g1 | (p1 & g0) | (p1 & p0 & cin),
35          c[2] = g2 | (p2 & g1) | (p2 & p1 & g0) | (p2 & p1 & p0 & cin),
36          c[3] = g3 | (p3 & g2) | (p3 & p2 & g1) | (p3 & p2 & p1 & g0) |(p3 & p2 & p1 & p0 & cin);
37
38  assign carry = c[3];
39  endmodule
```

carry_look_ahead_adder.v | cla_tb.v | Untitled 14

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_016/project_1/project_1.srcs/sim_1/new/cla_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/07/2024 06:43:35 AM
5   // Module Name: cla_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module cla_tb;
10      reg [3:0] a, b;
11      reg cin;
12      wire [3:0] sum;
13      wire carry;
14      wire [4:0] add;
15      carry_look_ahead_adder dut(a, b, cin, sum, carry);
16      assign add = {carry, sum};
17      initial
18          begin
19              a = 4'b1000; b = 4'b0011; cin = 1'b0;
20          #10 a = 4'b0011; b = 4'b1010; cin = 1'b1;
21          #10 a = 4'b0110; b = 4'b0110; cin = 1'b0;
22          #10 a = 4'b0111; b = 4'b1110; cin = 1'b0;
23          #10 a = 4'b1011; b = 4'b0110; cin = 1'b1;
24          #10 a = 4'b1001; b = 4'b0100; cin = 1'b0;
25          #10 a = 4'b1110; b = 4'b1110; cin = 1'b1;
26      end
27      initial
28      begin
29          $display("a  +  b , Cin = add | sum  cout");
30          $monitor("%d + %d , %b  = %d  | %d   %b", a, b,cin, add, sum, carry);
31
32      #70 $finish;
33      end
34  endmodule
```

Tcl Console | Messages | Log

```
# run 1000ns
a  +  b , Cin = add | sum  cout
 8 +  3 , 0  = 11  | 11   0
 3 + 10 , 1  = 14  | 14   0
 6 +  6 , 0  = 12  | 12   0
 7 + 14 , 0  = 21  |  5   1
11 +  6 , 1  = 18  |  2   1
 9 +  4 , 0  = 13  | 13   0
14 + 14 , 1  = 29  | 13   1
$finish called at time : 70 ns : File "/home/itzzinfinity/Cozy Drive/100day
INFO: [USF-XSim-96] XSim completed. Design snapshot 'cla_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 . Memory (
```

Type a Tcl command here