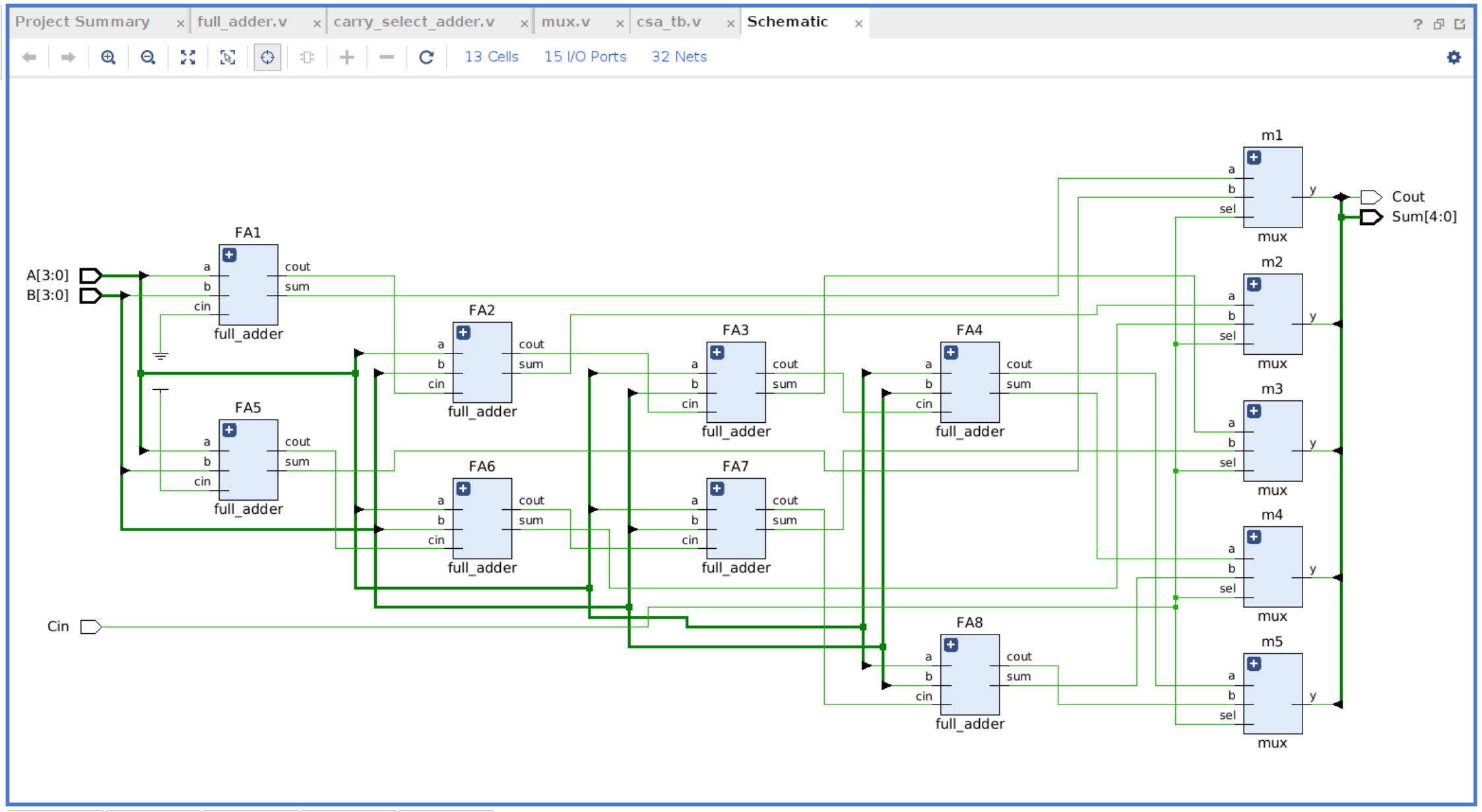
Project Summary
full_adder.v
carry_select_adder.v
mux.v
csa_tb.v
Schematic
13 Cells
15 I/O Ports
32 Nets
A[3:0]
B[3:0]
Cin
Cout
Sum[4:0]
FA1
FA2
FA3
FA4
FA5
FA6
FA7
FA8
full_adder
a
b
cin
cout
sum
m1
m2
m3
m4
m5
mux
sel
y

SIMULATION - Behavioral Simulation - Functional - sim_1 - csa_tb

full_adder.v | carry_select_adder.v | mux.v | csa_tb.v | Untitled 16

Scope | Sources | Objects | Protocol Instances

Name	Value
a[3:0]	3
b[3:0]	a
cin	1
sum[3:0	e
carry	0
add[4:0]	0e

18.793 ns

	0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns	60.000 ns
a[3:0]	8	3	6	7	b	9	e
b[3:0]	3	a	6	e	6	4	e
cin							
sum[3:0	b	e	c	5	2	d	
carry							
add[4:0]	0b	0e	0c	15	12	0d	1d

Project Summary | full_adder.v | carry_select_adder.v | mux.v | csa_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_017/project_1/project_1.srcs/sources_1/new/carry_select_adder.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Engineer: Anjan Prasad
3  // Create Date: 10/08/2024 08:36:17 AM
4  // Module Name: carry_select_adder
5  //////////////////////////////////////////////////////////////////////////////////
6
7
8  module carry_select_adder(
9  input [3:0] A,B,
10 input Cin,
11 output [4:0] Sum,
12 output Cout);
13 wire [3:0] w0,w1,c0,c1;
14 ///FOR CARRY=0;
15 full_adder FA1(.a(A[0]),.b(B[0]),.cin(0),.sum(w0[0]),.cout(c0[0]));
16 full_adder FA2(.a(A[1]),.b(B[1]),.cin(c0[0]),.sum(w0[1]),.cout(c0[1]));
17 full_adder FA3(.a(A[2]),.b(B[2]),.cin(c0[1]),.sum(w0[2]),.cout(c0[2]));
18 full_adder FA4(.a(A[3]),.b(B[3]),.cin(c0[2]),.sum(w0[3]),.cout(c0[3]));
19 ///FOR CARRY=1;
20 full_adder FA5(.a(A[0]),.b(B[0]),.cin(1),.sum(w1[0]),.cout(c1[0]));
21 full_adder FA6(.a(A[1]),.b(B[1]),.cin(c1[0]),.sum(w1[1]),.cout(c1[1]));
22 full_adder FA7(.a(A[2]),.b(B[2]),.cin(c1[1]),.sum(w1[2]),.cout(c1[2]));
23 full_adder FA8(.a(A[3]),.b(B[3]),.cin(c1[2]),.sum(w1[3]),.cout(c1[3]));
24
25 ///To select the carry
26
27 mux m1(.a(w0[0]),.b(w1[0]),.sel(Cin),.y(Sum[0]));
28 mux m2(.a(w0[1]),.b(w1[1]),.sel(Cin),.y(Sum[1]));
29 mux m3(.a(w0[2]),.b(w1[2]),.sel(Cin),.y(Sum[2]));
30 mux m4(.a(w0[3]),.b(w1[3]),.sel(Cin),.y(Sum[3]));
31 mux m5(.a(c0[3]),.b(c1[3]),.sel(Cin),.y(Cout));
32
33 assign Sum[4]=Cout;
34 endmodule
35
```

Tcl Console | Messages | Log | Reports | Design Runs

Project Summary | full_adder.v | carry_select_adder.v | mux.v | csa_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_017/project_1/project_1.srcs/sim_1/new/csa_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/08/2024 08:36:17 AM
5  // Module Name: csa_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module csa_tb;
10     reg [3:0] a, b;
11     reg cin;
12     wire [3:0] sum;
13     wire carry;
14     wire [4:0] add;
15     carry_select_adder DUT(a, b, cin, sum, carry);
16     assign add = {carry, sum};
17     initial
18         begin
19             a = 4'b1000; b = 4'b0011; cin = 1'b0;
20         #10 a = 4'b0011; b = 4'b1010; cin = 1'b1;
21         #10 a = 4'b0110; b = 4'b0110; cin = 1'b0;
22         #10 a = 4'b0111; b = 4'b1110; cin = 1'b0;
23         #10 a = 4'b1011; b = 4'b0110; cin = 1'b1;
24         #10 a = 4'b1001; b = 4'b0100; cin = 1'b0;
25         #10 a = 4'b1110; b = 4'b1110; cin = 1'b1;
26     end
27     initial
28     begin
29         $display("a  +  b , Cin = add | sum  cout");
30         $monitor("%d + %d , %b  = %d  | %d   %b", a, b,cin, add, sum, carry);
31
32     #70 $finish;
33     end
34 endmodule
```

Tcl Console | Messages | Log | Reports | Design Runs

Project Summary | full_adder.v | carry_select_adder.v | **mux.v** | csa_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_017/project_1/project_1.srcs/sources_1/new/mux.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Engineer: Anjan Prasad
3  // Create Date: 10/08/2024 08:36:17 AM
4  // Module Name: mux
5  //////////////////////////////////////////////////////////////////////////////////
6
7
8  module mux(
9  input a,b,
10 input sel,
11 output y);
12
13 assign y = (~sel)?a:b;
14
15
16 endmodule
```

Tcl Console × Messages | Log | Reports | Design Runs

```
# run 1000ns
a  +  b , Cin = add | sum  cout
 8 +  3 , 0  = 11  | 11   0
 3 + 10 , 1  = 14  | 14   0
 6 +  6 , 0  = 12  | 12   0
 7 + 14 , 0  = 21  |  5   1
11 +  6 , 1  = 18  |  2   1
 9 +  4 , 0  = 13  | 13   0
14 + 14 , 1  = 29  | 13   1
$finish called at time : 70 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_017/project_
```