







```
Project Summary x mux 4to1.v
                             x mux 2 to 1.v x mux tb.v
/home/itzzinfinity/Cozy\ Drive/100 days of RTL/day\_023/project\_1/project\_1.srcs/sim\_1/new/mux\_tb.v
                    `timescale 1ns / 1ps
 3 : // Engineer: Anjan Prasad
 4 // Create Date: 10/14/2024 06:16:57 AM
    // Module Name: mux tb
    8
    module mux tb;
    reg [3:0] a,b,c,d;
10
11
    reg [1:0] sel;
12
    wire [3:0] y;
13
14
    mux 4to1 DUT (a,b,c,d,sel,y);
15 initial begin
           $display("Select line is Sel so now the output is y , where a , b , a , b are:");
16
           $monitor("
17
                                 %b
                                                      %d,
                                                                     %d
                                                                        %d %d", sel,y,a,b,c,d);
                                                                 %d
18 : //repeat(10) begin
19 #10
20 🖨 //
             a= $random %16 ;
21
    //
             b = \$ random \% 16 ;
22
  1//
             c = \$random \%16;
23 : //
            d= $random %16 :
24 🖒 //
             sel = \$random;
25
26
27
           a= 4'd15 ;b= 4'd10 ;c= 4'd5 ;d= 4'd3 ;sel = 2'b00 ;
28
           #10
29
           a = 4'd3; b = 4'd7; c = 4'd5; d = 4'd8; sel = 2'b01;
30
           #10
31
           a = 4'd5; b = 4'd11; c = 4'd6; d = 4'd1; sel = 2'b10;
32
           #10
33
           a = 4'd7; b = 4'd13; c = 4'd15; d = 4'd6; sel = 2'b11;
34
           #10
35
           a = 4'd8; b = 4'd6; c = 4'd1; d = 4'd10; sel = 2'b11;
36
    //end
37
    $finish;
38 🛆 end
    endmodule
```

