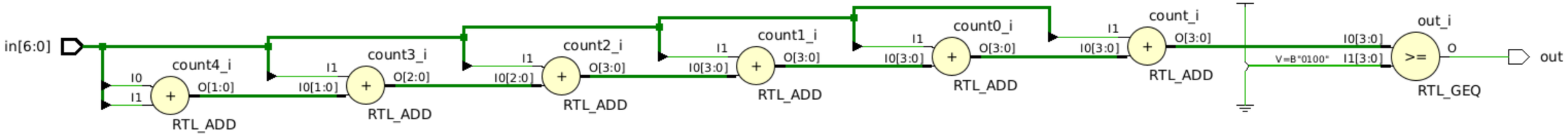
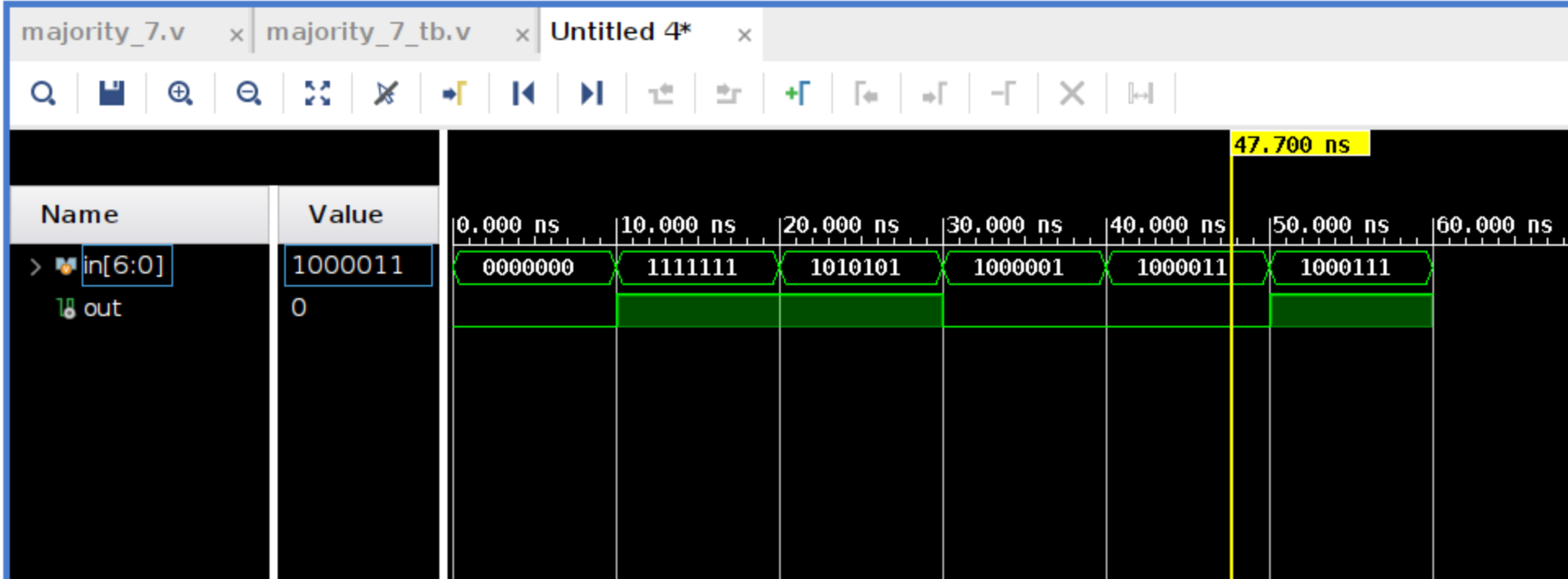
Project Summary | majority_7.v | majority_7_tb.v | Schematic | Schematic (2)

7 Cells 8 I/O Ports 31 Nets




majority_7.v
majority_7_tb.v
Untitled 4*
47.700 ns
Name
Value
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
in[6:0]
1000011
0000000
1111111
1010101
1000001
1000011
1000111
out
0

majority_7.v | majority_7_tb.v | Untitled 4*

/home/itzzinfinity/Cozy Drive/100daysofRTL.day_041/project_1/project_1.srcs/sources_1/new/majority_7.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/01/2024 12:55:59 AM
5   // Module Name: majority_7
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module majority_7 (
10      input [6:0] in,  // 7 input lines
11      output out       // Majority output
12  );
13
14
15      wire [3:0] count;
16
17      // Count how many inputs are high using a simple adder
18      assign count = in[0] + in[1] + in[2] + in[3] + in[4] + in[5] + in[6];
19
20      // Output is high if count is greater than or equal to 4
21      assign out = (count >= 4) ? 1'b1 : 1'b0;
22
23  endmodule
24
```

majority_7.v | majority_7_tb.v | Untitled 4*

/home/itzzinfinity/Cozy Drive/100daysofRTL.day_041/project_1/project_1.srcs/sim_1/new/majority_7_tb.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/01/2024 01:03:20 AM
5   // Module Name: majority_7_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module majority_7_tb;
10      reg [6:0] in;
11      wire out;
12      majority_7 dut (.in(in),.out(out));
13
14      initial begin
15          in = 7'b0000000;  // Test case 1: Majority of 0s
16          #10;
17          in = 7'b1111111;  // Test case 2: Majority of 1s
18          #10;
19          in = 7'b1010101;
20          #10;
21          in = 7'b1000001;
22          #10;
23          in = 7'b1000011;
24          #10;
25          in = 7'b1000111;
26          #10;
27          $finish;
28      end
29
30  endmodule
```