```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 09/25/2024 09:54:11 AM
// Module Name: mos_inv_tb
//////////////////////////////////////////////////////////////////////////////////


module mos_inv(
    input in,
    output out
    );

    supply0 gnd;
    supply1 vdd;

    pmos(out, vdd, in);
    nmos(out, gnd, in);

endmodule
```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_004/project_1/project_1.srcs/sim_1/new/mos_inv_tb.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 09/25/2024 09:54:11 AM
// Module Name: mos_inv_tb
//////////////////////////////////////////////////////////////////////////////


module mos_inv_tb;

    reg in;
    wire out;
    mos_inv dut(in, out);
    initial in= 1'b0;
    initial forever #50 in = ~in;
    initial #600 $finish;
endmodule
```

Name	Value	599,993 ps	599,994 ps	599,995 ps	599,996 ps	599,997 ps
in	1					
out	0					

599,997 ps