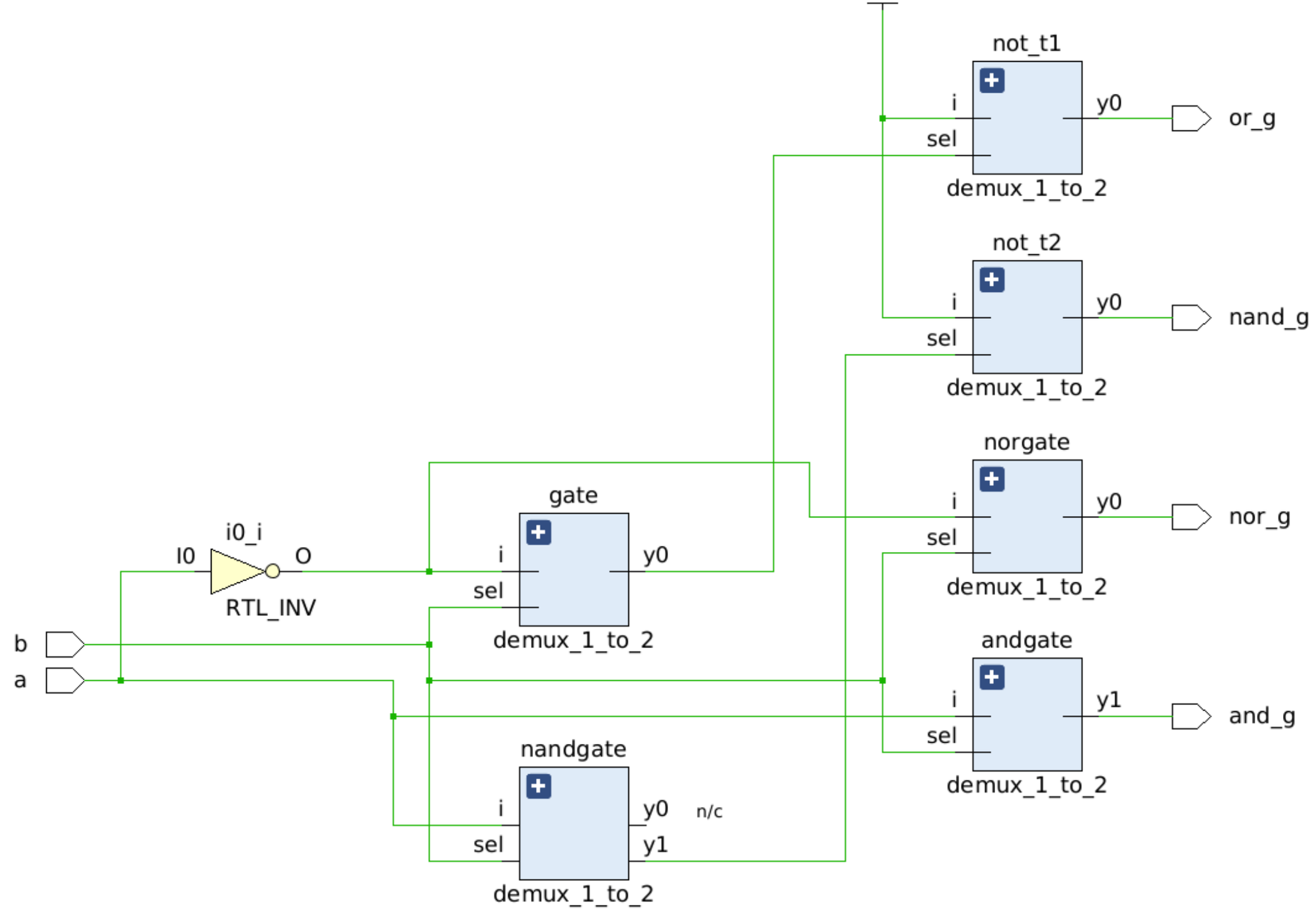
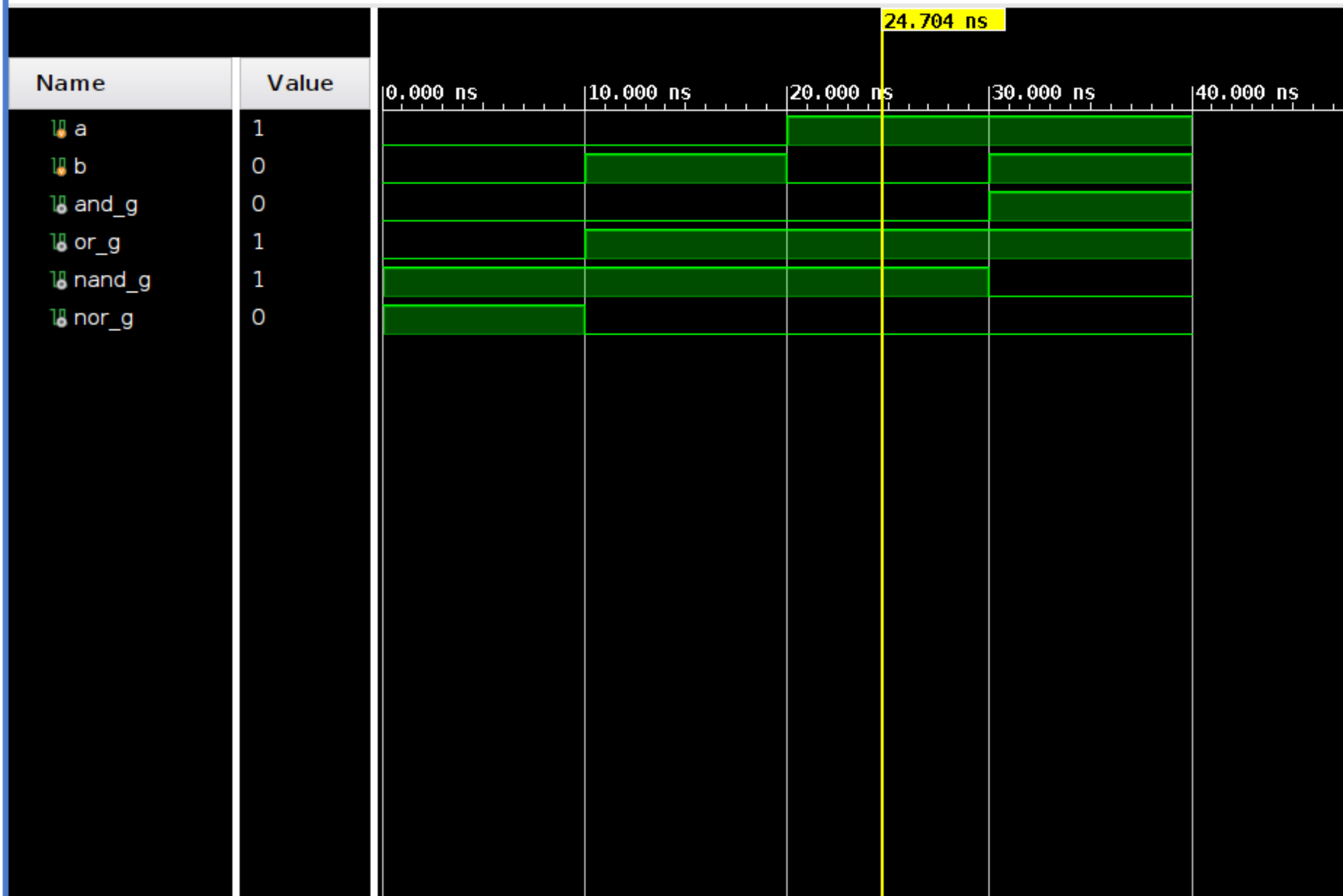
ux_to_gates.v × Schematic ×

8 Cells 6 I/O Ports 15 Nets



demux_to_gates.v | Untitled 1 | demux_gates_tb.v



Project Summary | demux_to_gates.v | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_031/project_1/project_1.srcs/sources_1/new/demux_to_gates.v

```
1
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/22/2024 06:19:32 AM
5  // Module Name: demux_to_gates
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module demux_to_gates(
10     input a, b,
11     output and_g,or_g,nand_g,nor_g
12     );
13     wire w0,w1, w2, w3,w4,w5,w6,w7,w8,w9,w10,w11;
14
15     demux_1_to_2 andgate(b, a, w0, and_g);
16
17
18     demux_1_to_2 gate(b, ~a, w1, w2);
19     demux_1_to_2 not_t1(w1, 1'b1, or_g, w3);
20
21
22     demux_1_to_2 nandgate(b, a, w4, w5);
23     demux_1_to_2 not_t2(w5, 1'b1, nand_g, w6);
24
25
26     demux_1_to_2 norgate(b, ~a, nor_g, w7);
27
28
29 endmodule
30
31
```

demux_to_gates.v | Untitled 1 | **demux_gates_tb.v**

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_031/project_1/project_1.srcs/sim_1/new/demux_gates_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/22/2024 06:32:58 PM
5   // Module Name: demux_gates_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module demux_gates_tb;
10
11      reg a,b;
12      wire and_g,or_g,nand_g,nor_g;
13      demux_to_gates DUT (a,b, and_g,or_g,nand_g,nor_g);
14   initial begin
15    a = 1'b0; b = 1'b0;
16   #10;
17   a = 1'b0; b = 1'b1;
18   #10;
19   a = 1'b1; b = 1'b0;
20   #10;
21   a = 1'b1; b = 1'b1;
22   #10;
23   $finish;
24  end
25  endmodule
26
```