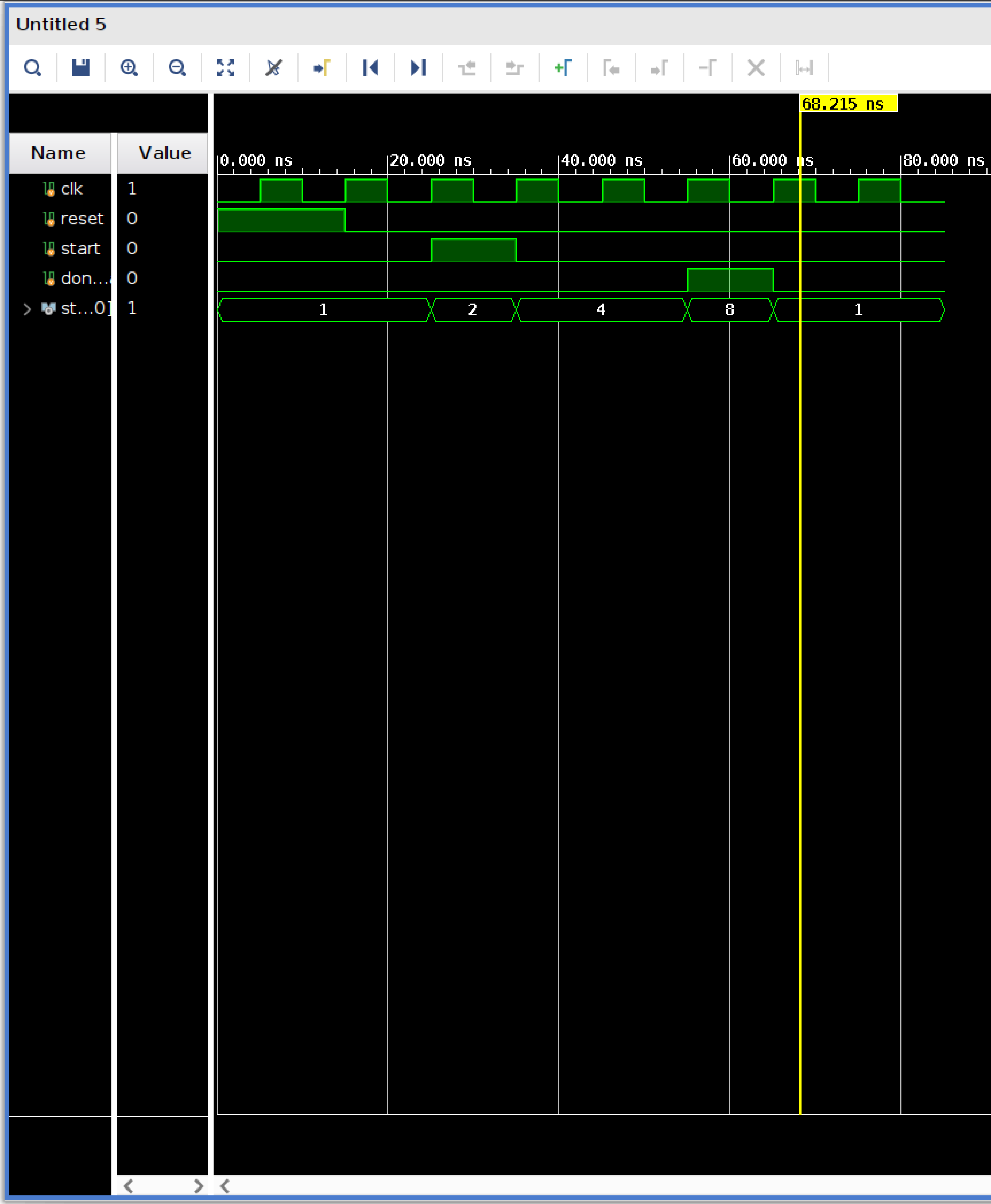
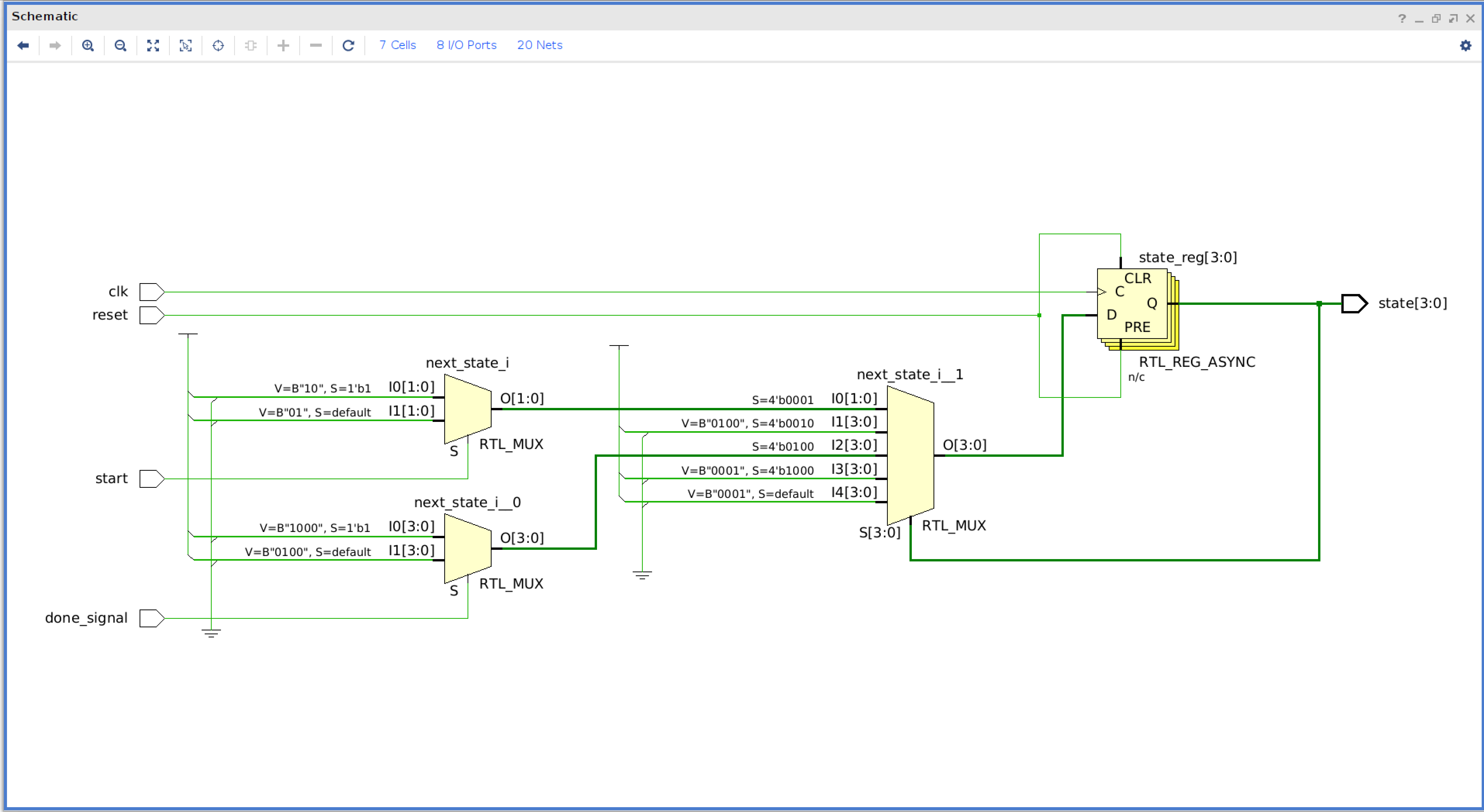
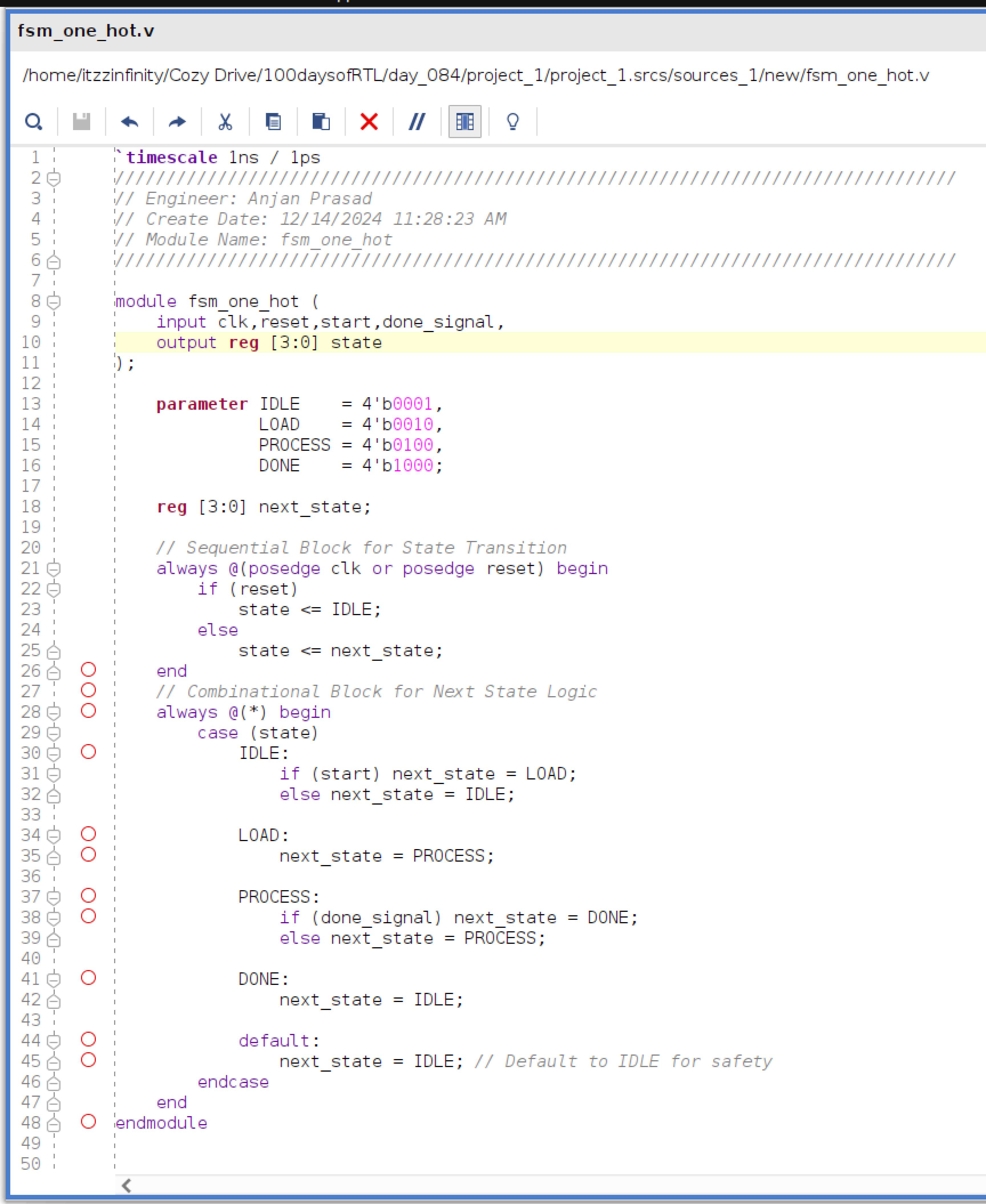


Untitled 5

Name	Value
clk	1
reset	0
start	0
don…	0
st…0]	1

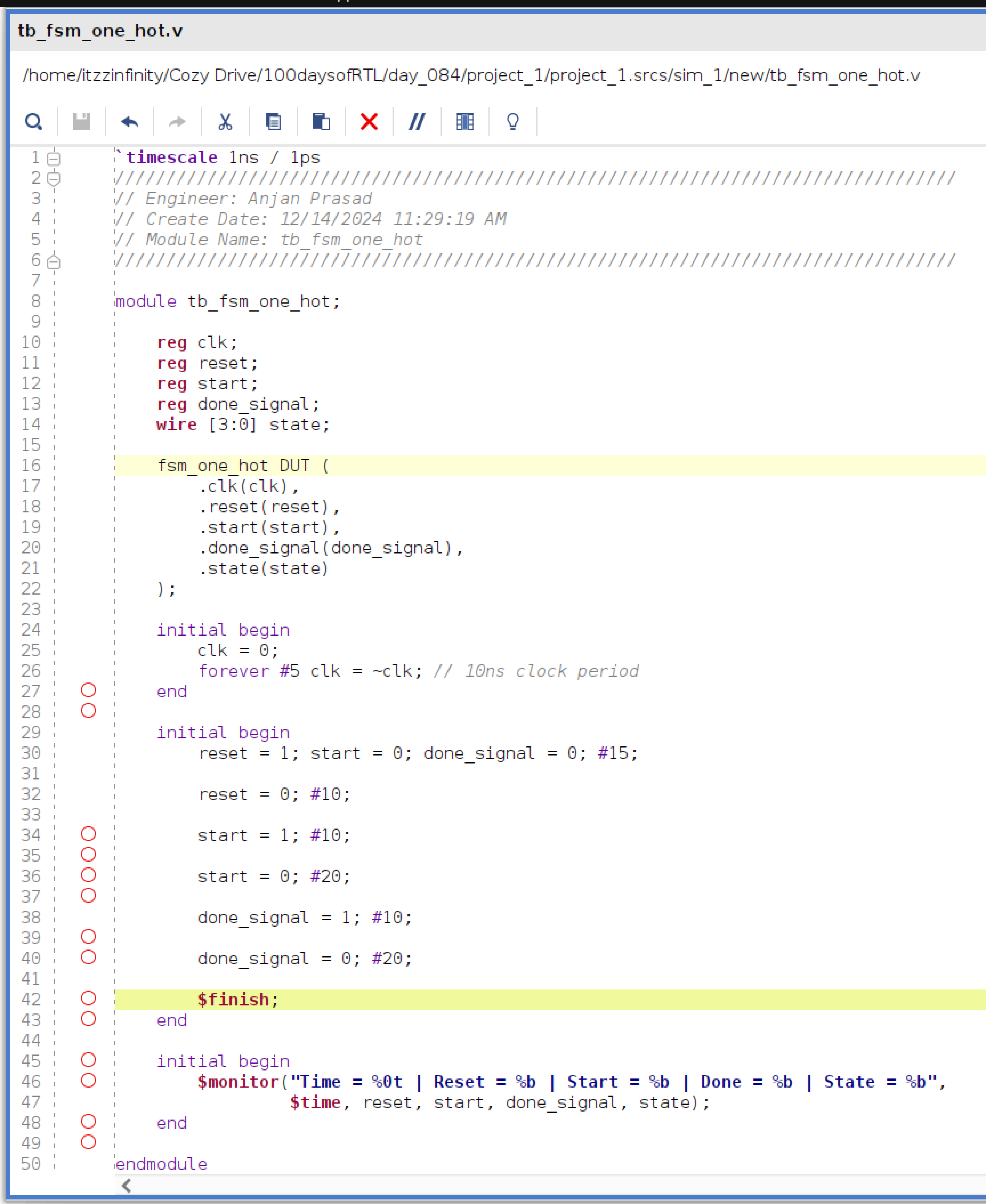

Schematic
7 Cells
8 I/O Ports
20 Nets
clk
reset
start
done_signal
state_reg[3:0]
CLR
C
Q
D
PRE
RTL_REG_ASYNC
n/c
state[3:0]
next_state_i
V=B"10", S=1'b1
I0[1:0]
V=B"01", S=default
I1[1:0]
O[1:0]
S
RTL_MUX
next_state_i__0
V=B"1000", S=1'b1
I0[3:0]
V=B"0100", S=default
I1[3:0]
O[3:0]
S
RTL_MUX
next_state_i__1
S=4'b0001
I0[1:0]
V=B"0100", S=4'b0010
I1[3:0]
S=4'b0100
I2[3:0]
V=B"0001", S=4'b1000
I3[3:0]
V=B"0001", S=default
I4[3:0]
O[3:0]
S[3:0]
RTL_MUX



fsm_one_hot.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_084/project_1/project_1.srcs/sources_1/new/fsm_one_hot.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/14/2024 11:28:23 AM
// Module Name: fsm_one_hot
//////////////////////////////////////////////////////////////////////////////////

module fsm_one_hot (
    input clk,reset,start,done_signal,
    output reg [3:0] state
);

    parameter IDLE    = 4'b0001,
              LOAD    = 4'b0010,
              PROCESS = 4'b0100,
              DONE    = 4'b1000;

    reg [3:0] next_state;

    // Sequential Block for State Transition
    always @(posedge clk or posedge reset) begin
        if (reset)
            state <= IDLE;
        else
            state <= next_state;
    end
    // Combinational Block for Next State Logic
    always @(*) begin
        case (state)
            IDLE:
                if (start) next_state = LOAD;
                else next_state = IDLE;

            LOAD:
                next_state = PROCESS;

            PROCESS:
                if (done_signal) next_state = DONE;
                else next_state = PROCESS;

            DONE:
                next_state = IDLE;

            default:
                next_state = IDLE; // Default to IDLE for safety
        endcase
    end
endmodule
```


tb_fsm_one_hot.v
/home/itzzinfinity/Cozy Drive/100daysofRTL/day_084/project_1/project_1.srcs/sim_1/new/tb_fsm_one_hot.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/14/2024 11:29:19 AM
// Module Name: tb_fsm_one_hot
//////////////////////////////////////////////////////////////////////////////////

module tb_fsm_one_hot;

    reg clk;
    reg reset;
    reg start;
    reg done_signal;
    wire [3:0] state;

    fsm_one_hot DUT (
        .clk(clk),
        .reset(reset),
        .start(start),
        .done_signal(done_signal),
        .state(state)
    );

    initial begin
        clk = 0;
        forever #5 clk = ~clk; // 10ns clock period
    end

    initial begin
        reset = 1; start = 0; done_signal = 0; #15;

        reset = 0; #10;

        start = 1; #10;

        start = 0; #20;

        done_signal = 1; #10;

        done_signal = 0; #20;

        $finish;
    end

    initial begin
        $monitor("Time = %0t | Reset = %b | Start = %b | Done = %b | State = %b",
                 $time, reset, start, done_signal, state);
    end

endmodule
```