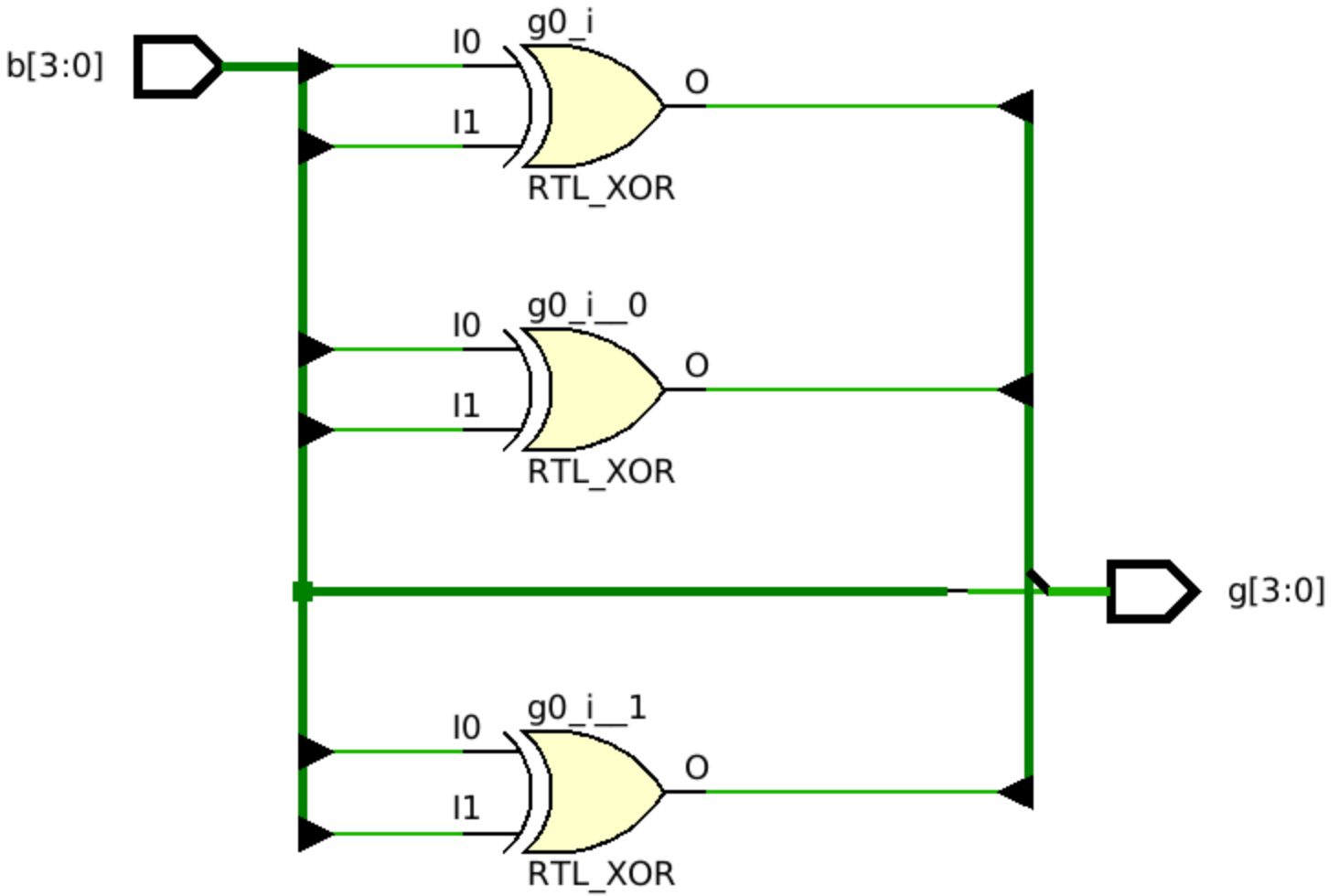
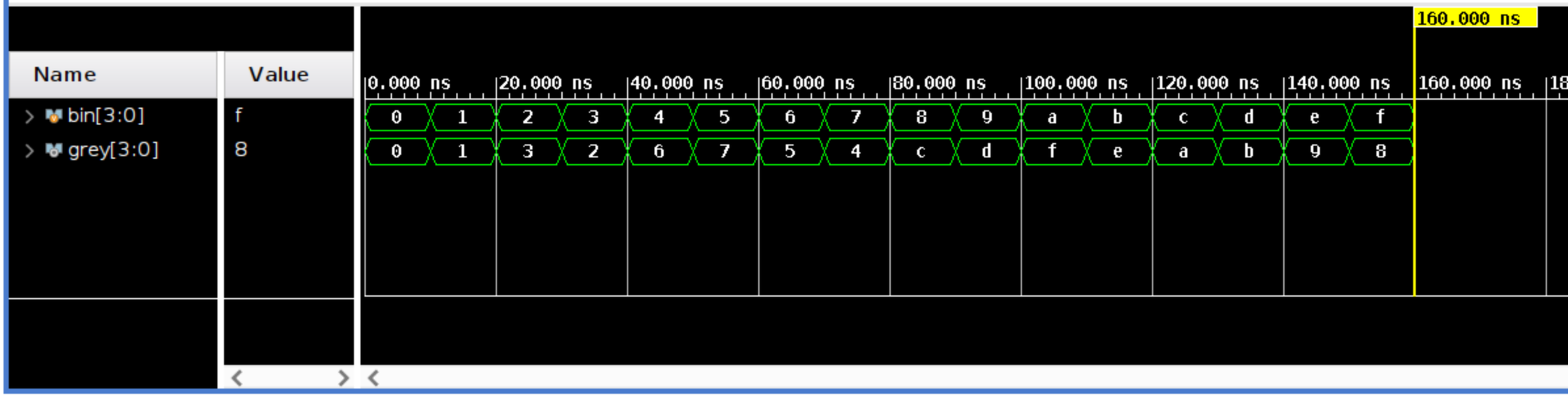
Bin_to_Grey.v | tb_Bin_to_Grey.v | Schematic | **Schematic (2)**

3 Cells 8 I/O Ports 7 Nets



Bin_to_Grey.v | tb_Bin_to_Grey.v | Untitled 1



Tcl Console | Messages | Log

```
# run 1000ns
Binary = 0000, Grey = 0000
Binary = 0001, Grey = 0001
Binary = 0010, Grey = 0011
Binary = 0011, Grey = 0010
Binary = 0100, Grey = 0110
Binary = 0101, Grey = 0111
Binary = 0110, Grey = 0101
Binary = 0111, Grey = 0100
Binary = 1000, Grey = 1100
Binary = 1001, Grey = 1101
Binary = 1010, Grey = 1111
Binary = 1011, Grey = 1110
Binary = 1100, Grey = 1010
Binary = 1101, Grey = 1011
Binary = 1110, Grey = 1001
Binary = 1111, Grey = 1000
$finish called at time : 160 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_042/project_1/project_1.srcs/sim_1/new/tb_
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_Bin_to_Grey_behav' loaded.
```

Type a Tcl command here

Bin_to_Grey.v × tb_Bin_to_Grey.v × Untitled 1 ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_042/project_1/project_1.srcs/sources_1/new/Bin_to_Grey.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/02/2024 04:31:54 AM
5   // Module Name: Bin_to_Grey
6   //////////////////////////////////////////////////////////////////////////////////
7
8   /* Binary to Grey Code Converters */
9   module Bin_to_Grey(
10  input [3:0] b,
11  output [3:0]g);
12  assign g[0] = b[0] ^ b[1];
13  assign g[1] = b[1] ^ b[2];
14  assign g[2] = b[2] ^ b[3];
15  assign g[3] = b[3];
16  endmodule
17
```

Bin_to_Grey.v | tb_Bin_to_Grey.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_042/project_1/project_1.srcs/sim_1/new/tb_Bin_to_Grey.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/02/2024 04:34:02 AM
5  // Module Name: tb_Bin_to_Grey
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module tb_Bin_to_Grey;
9      reg [3:0] bin;
10     wire [3:0] grey;
11     Bin_to_Grey uut (.b(bin),.g(grey));
12     initial begin
13         $monitor("Binary = %b, Grey = %b", bin, grey);
14         bin = 4'b0000; #10;
15         bin = 4'b0001; #10;
16         bin = 4'b0010; #10;
17         bin = 4'b0011; #10;
18         bin = 4'b0100; #10;
19         bin = 4'b0101; #10;
20         bin = 4'b0110; #10;
21         bin = 4'b0111; #10;
22         bin = 4'b1000; #10;
23         bin = 4'b1001; #10;
24         bin = 4'b1010; #10;
25         bin = 4'b1011; #10;
26         bin = 4'b1100; #10;
27         bin = 4'b1101; #10;
28         bin = 4'b1110; #10;
29         bin = 4'b1111; #10;
30
31         $finish;
32     end
33 endmodule
34
35
```

Tcl Console | Messages | Log