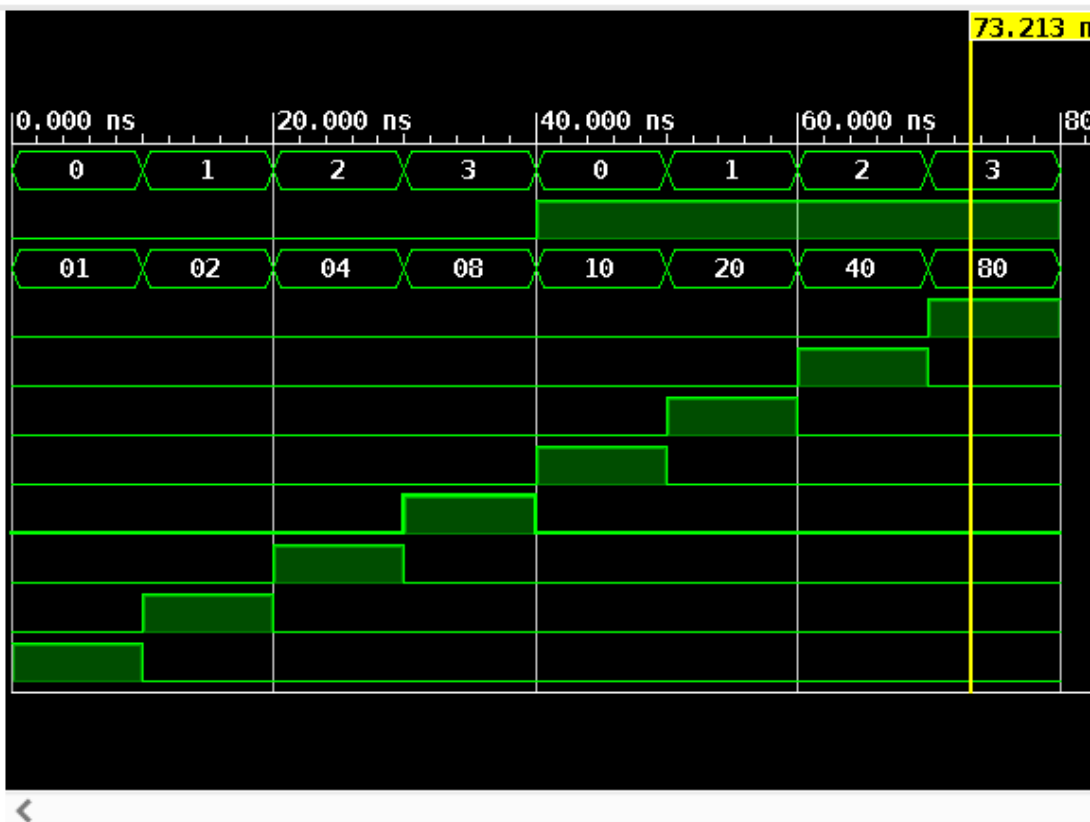




Name	Value
> s[1:0]	3
en	1
▼ y[7:0]	80
y[7]	1
y[6]	0
y[5]	0
y[4]	0
y[3]	0
y[2]	0
y[1]	0
y[0]	0



Tcl Console x Messages Log



```
# }
# run 1000ns
s = 00, so at the output y0 = 1,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 01, so at the output y0 = 0,y1 = 1,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 10, so at the output y0 = 0,y1 = 0,y2 = 1,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 11, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 1,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 00, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 1,y5 = 0,y6 = 0,y7 = 0
s = 01, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 1,y6 = 0,y7 = 0
s = 10, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 1,y7 = 0
s = 11, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 1
$finish called at time : 80 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_036
INFO: IUSE: VSim 061 VSim completed. Design snapshot 'three_to_eight_decoder_tb_behav' loc
```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day\_036/project\_1/project\_1.srscs/sources\_1/new/decoder\_2\_4.v



```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/27/2024 05:16:21 AM
5  // Module Name: decoder_2_4
6  //////////////////////////////////////
7
8
9  module decoder_2_4(EN, A0, A1, D);
10     input EN, A0, A1;
11     output [3:0] D;
12
13     assign D[0] =(EN & ~A1 & ~A0);
14     assign D[1] =(EN & ~A1 & A0);
15     assign D[2] =(EN & A1 & ~A0);
16     assign D[3] =(EN & A1 & A0);
17 endmodule
```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day\_036/project\_1/project\_1.srscs/sources\_1/new/three\_to\_eight\_decoder.v



```
1  `timescale 1ns / 1ps
2  ///////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/27/2024 07:17:51 AM
5  // Module Name: three_to_eight_decoder
6  ///////////////////////////////////////////////////////////////////
7
8
9  module three_to_eight_decoder(
10     input [1:0]a,
11     input en,
12     output [7:0]y
13 );
14     decoder_2_4 Decoder_1 (.EN(~en),.A0(a[0]),.A1(a[1]),.D(y[3:0]));
15     decoder_2_4 Decoder_2 (.EN(en),.A0(a[0]),.A1(a[1]),.D(y[7:4]));
16 endmodule
17
```

/home/itzinfinity/Cozy Drive/100daysofRTL/day\_036/project\_1/project\_1.srcs/sim\_1/new/three\_to\_eight\_decoder\_tb.v

x



```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/27/2024 07:28:24 AM
5  // Module Name: three_to_eight_decoder_tb
6  //////////////////////////////////////
7
8  module three_to_eight_decoder_tb;
9      reg [1:0]s;
10     reg en;
11     wire [7:0]y;
12
13     three_to_eight_decoder DUT (s,en,y);
14
15     initial begin
16         $monitor("s = %b, so at the output y0 = %b,y1 = %b,y2 = %b,y3 = %b,y4 = %b,y5 = %b,y6 = %b,y7 = %b ",s,y[0],y[1],y[2],y[3],y[4],y[5],y[6],y[7]);
17
18         {en,s} = 3'b000; #10;
19         {en,s} = 3'b001; #10;
20         {en,s} = 3'b010; #10;
21         {en,s} = 3'b011; #10;
22         {en,s} = 3'b100; #10;
23         {en,s} = 3'b101; #10;
24         {en,s} = 3'b110; #10;
25         {en,s} = 3'b111; #10;
26
27         $finish;
28     end
29
30 endmodule
```