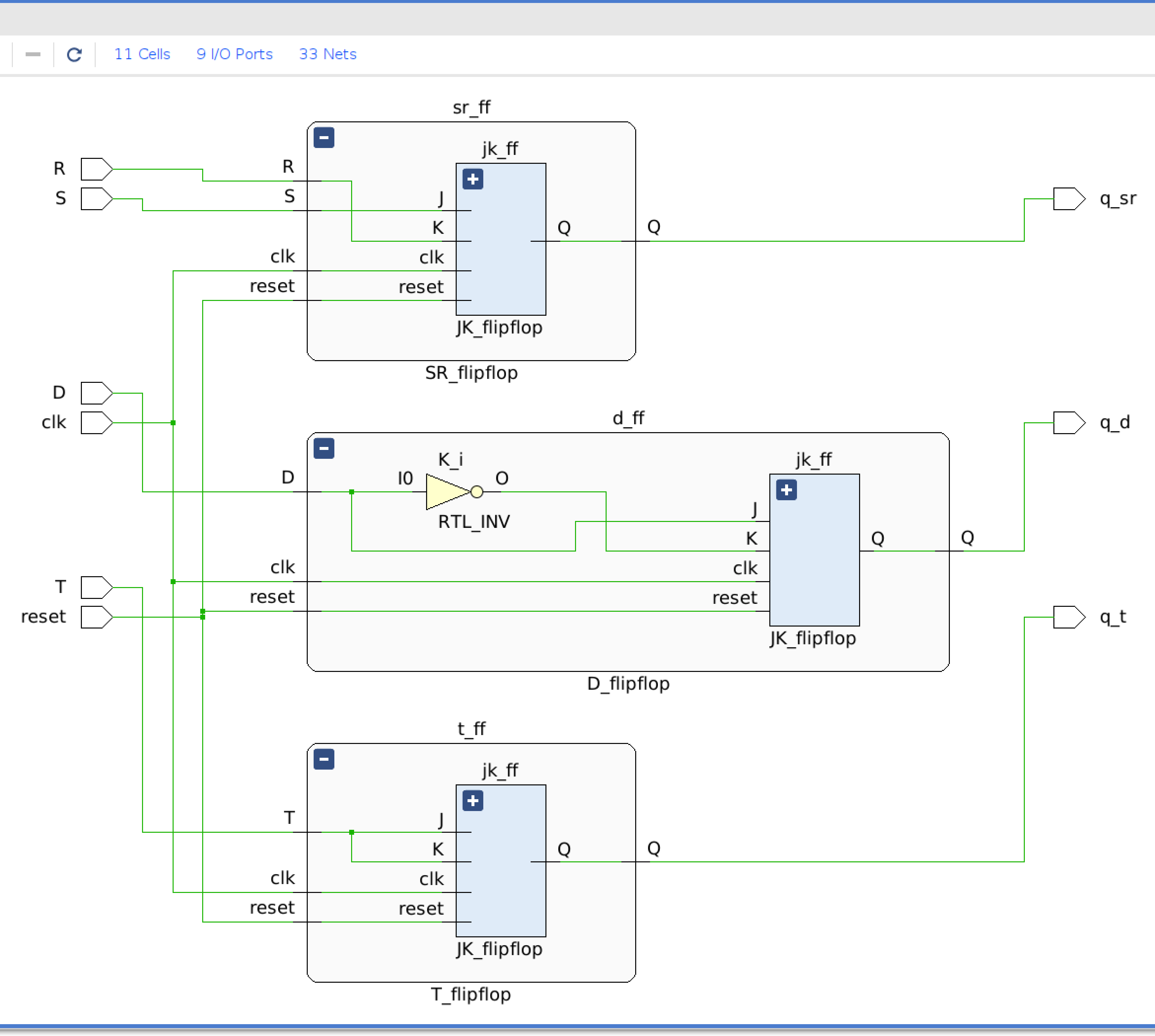
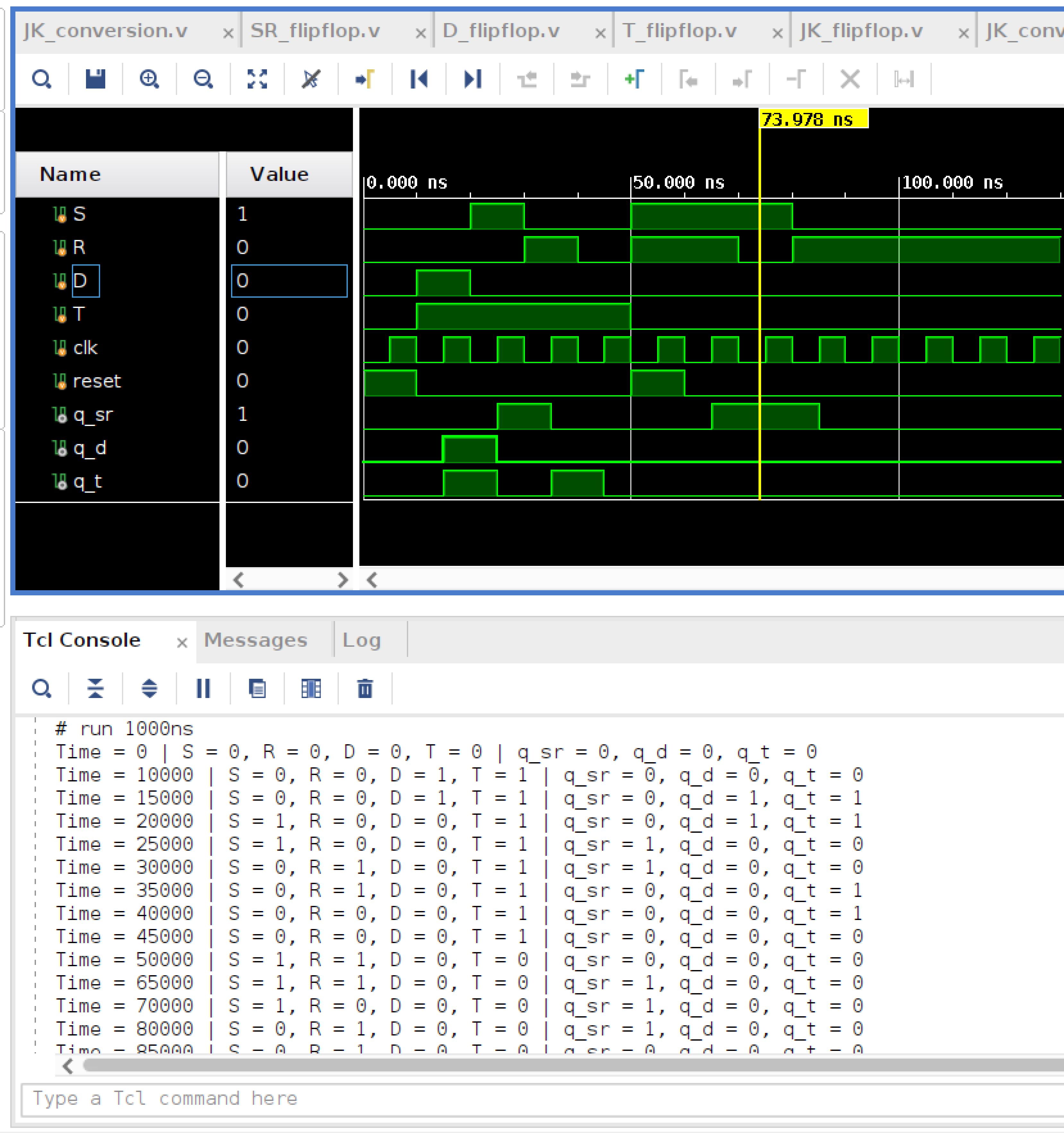
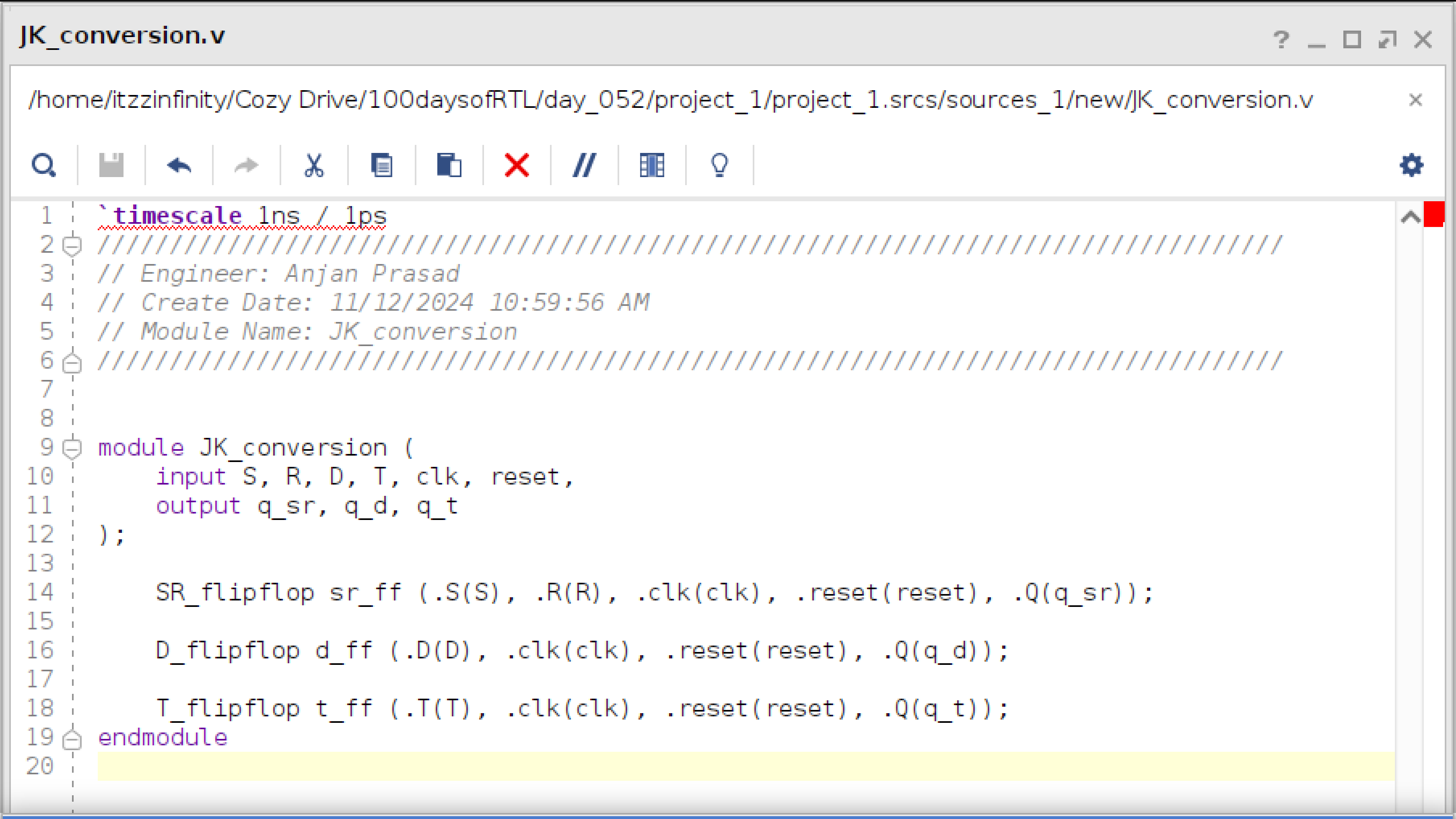

11 Cells
9 I/O Ports
33 Nets
R
S
D
clk
T
reset
sr_ff
jk_ff
R
S
J
K
clk
reset
Q
Q
clk
reset
JK_flipflop
SR_flipflop
d_ff
K_i
I0
O
RTL_INV
D
jk_ff
J
K
clk
reset
Q
Q
clk
reset
JK_flipflop
D_flipflop
t_ff
jk_ff
T
J
K
clk
reset
Q
Q
clk
reset
JK_flipflop
T_flipflop
q_sr
q_d
q_t



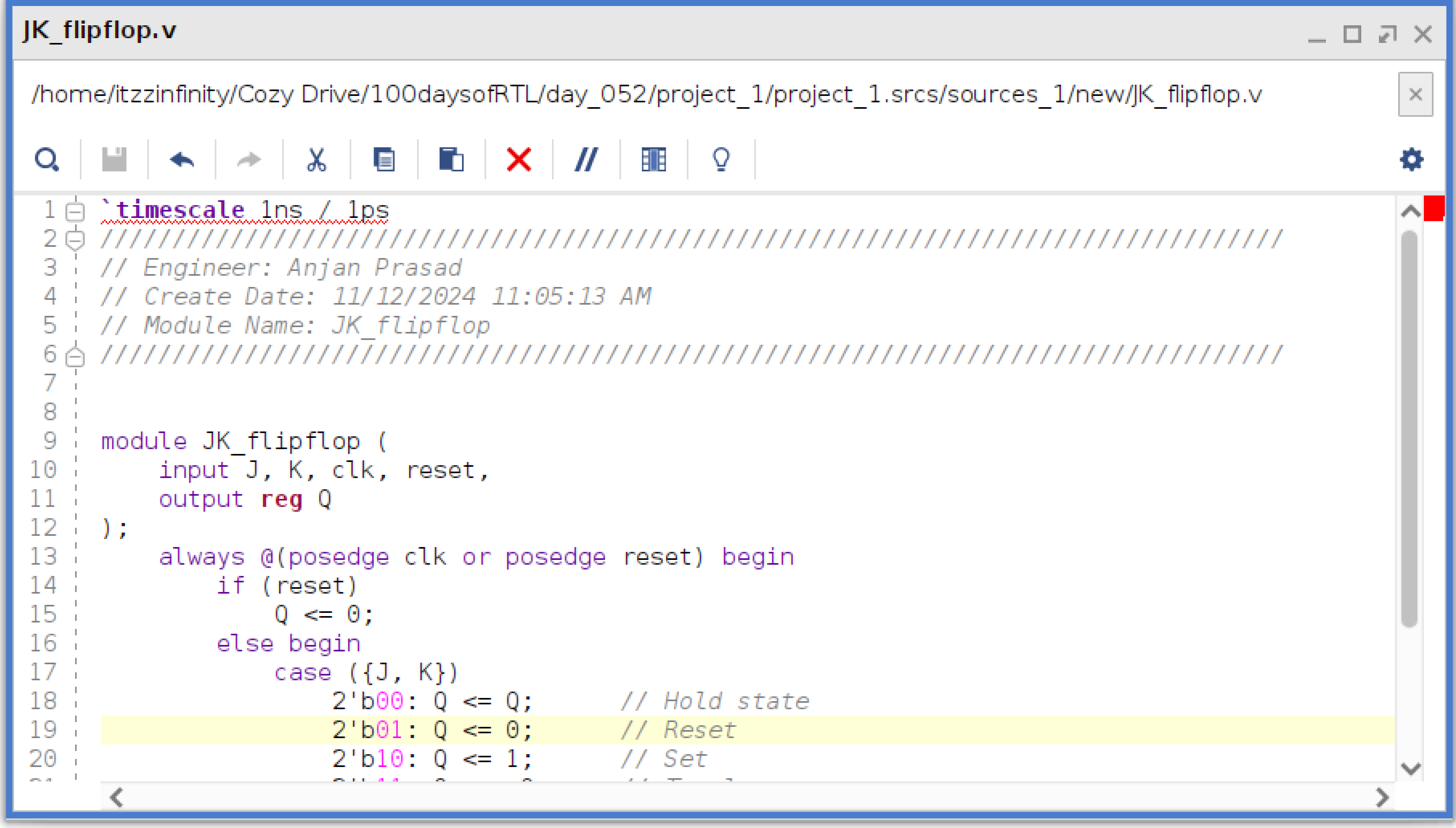
```
# run 1000ns
Time = 0 | S = 0, R = 0, D = 0, T = 0 | q_sr = 0, q_d = 0, q_t = 0
Time = 10000 | S = 0, R = 0, D = 1, T = 1 | q_sr = 0, q_d = 0, q_t = 0
Time = 15000 | S = 0, R = 0, D = 1, T = 1 | q_sr = 0, q_d = 1, q_t = 1
Time = 20000 | S = 1, R = 0, D = 0, T = 1 | q_sr = 0, q_d = 1, q_t = 1
Time = 25000 | S = 1, R = 0, D = 0, T = 1 | q_sr = 1, q_d = 0, q_t = 0
Time = 30000 | S = 0, R = 1, D = 0, T = 1 | q_sr = 1, q_d = 0, q_t = 0
Time = 35000 | S = 0, R = 1, D = 0, T = 1 | q_sr = 0, q_d = 0, q_t = 1
Time = 40000 | S = 0, R = 0, D = 0, T = 1 | q_sr = 0, q_d = 0, q_t = 1
Time = 45000 | S = 0, R = 0, D = 0, T = 1 | q_sr = 0, q_d = 0, q_t = 0
Time = 50000 | S = 1, R = 1, D = 0, T = 0 | q_sr = 0, q_d = 0, q_t = 0
Time = 65000 | S = 1, R = 1, D = 0, T = 0 | q_sr = 1, q_d = 0, q_t = 0
Time = 70000 | S = 1, R = 0, D = 0, T = 0 | q_sr = 1, q_d = 0, q_t = 0
Time = 80000 | S = 0, R = 1, D = 0, T = 0 | q_sr = 1, q_d = 0, q_t = 0
Time = 85000 | S = 0, R = 1, D = 0, T = 0 | q_sr = 0, q_d = 0, q_t = 0
```



JK_conversion.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_052/project_1/project_1.srcs/sources_1/new/JK_conversion.v

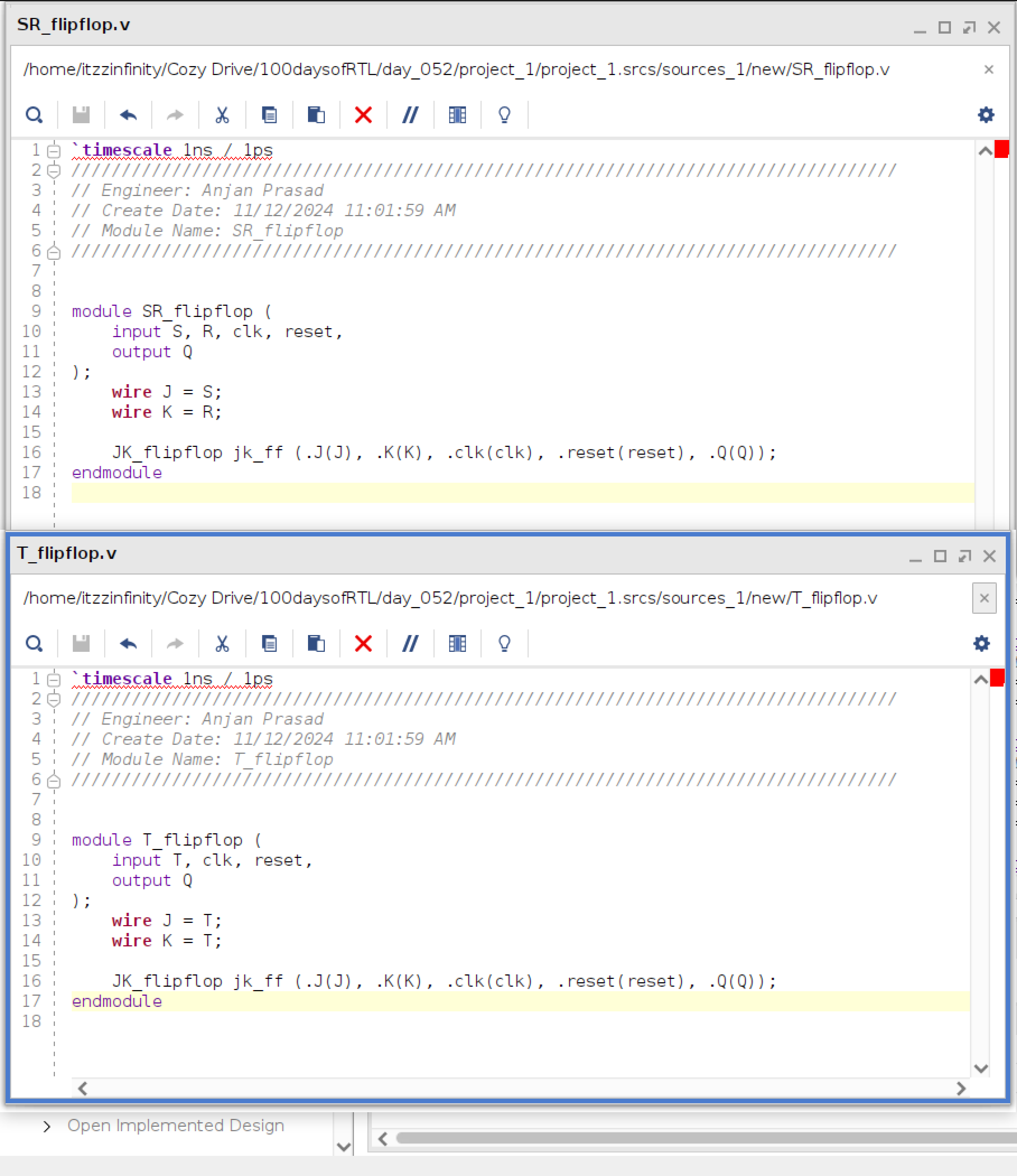
```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/12/2024 10:59:56 AM
// Module Name: JK_conversion
//////////////////////////////////////////////////////////////////////////////////


module JK_conversion (
    input S, R, D, T, clk, reset,
    output q_sr, q_d, q_t
);

    SR_flipflop sr_ff (.S(S), .R(R), .clk(clk), .reset(reset), .Q(q_sr));

    D_flipflop d_ff (.D(D), .clk(clk), .reset(reset), .Q(q_d));

    T_flipflop t_ff (.T(T), .clk(clk), .reset(reset), .Q(q_t));
endmodule

```



JK_flipflop.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_052/project_1/project_1.srcs/sources_1/new/JK_flipflop.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/12/2024 11:05:13 AM
// Module Name: JK_flipflop
//////////////////////////////////////////////////////////////////////////////////


module JK_flipflop (
    input J, K, clk, reset,
    output reg Q
);
    always @(posedge clk or posedge reset) begin
        if (reset)
            Q <= 0;
        else begin
            case ({J, K})
                2'b00: Q <= Q;      // Hold state
                2'b01: Q <= 0;      // Reset
                2'b10: Q <= 1;      // Set
```



SR_flipflop.v

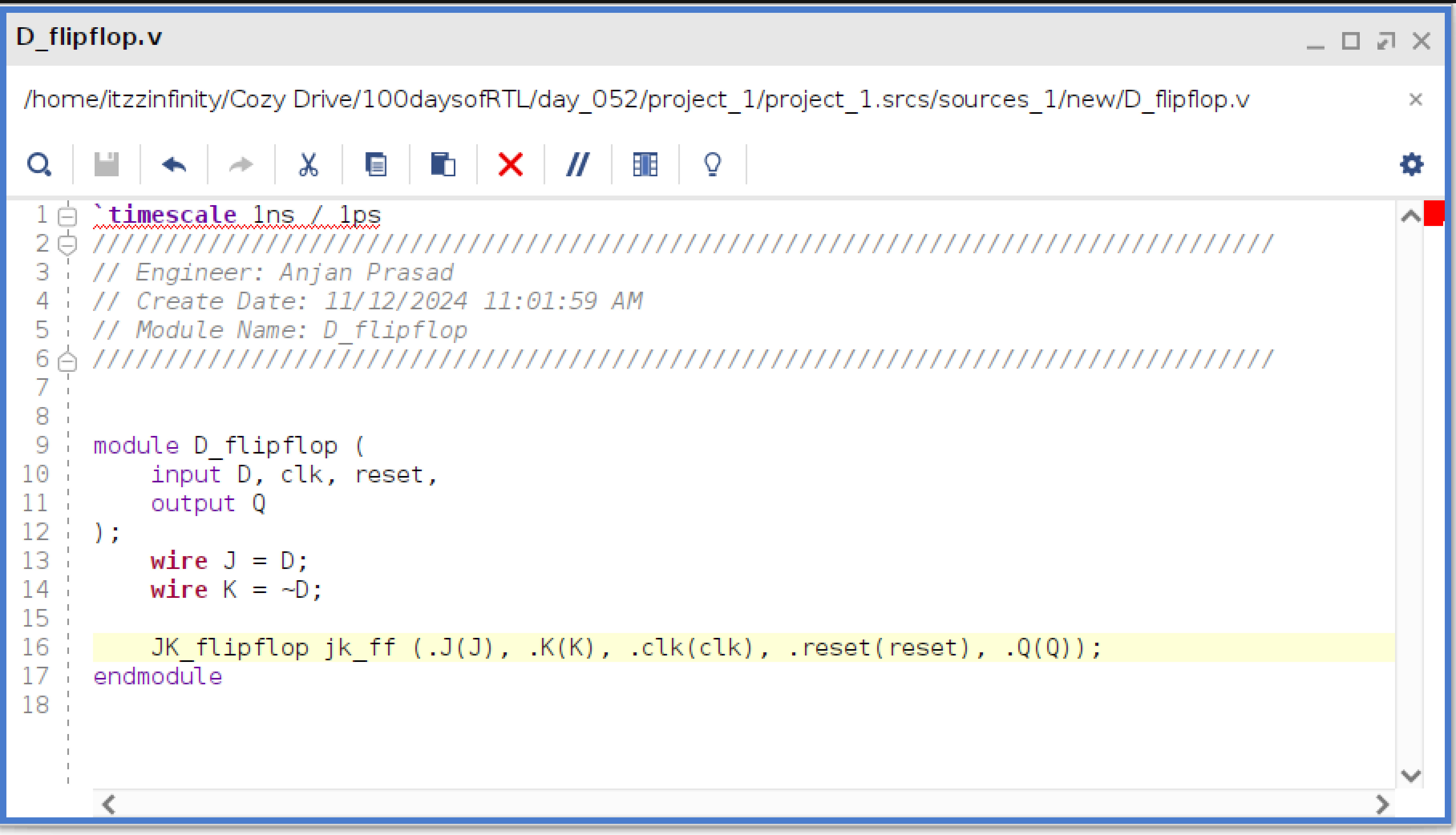
/home/itzzinfinity/Cozy Drive/100daysofRTL/day_052/project_1/project_1.srcs/sources_1/new/SR_flipflop.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/12/2024 11:01:59 AM
// Module Name: SR_flipflop
//////////////////////////////////////////////////////////////////////////////////


module SR_flipflop (
    input S, R, clk, reset,
    output Q
);
    wire J = S;
    wire K = R;

    JK_flipflop jk_ff (.J(J), .K(K), .clk(clk), .reset(reset), .Q(Q));
endmodule

```

T_flipflop.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_052/project_1/project_1.srcs/sources_1/new/T_flipflop.v

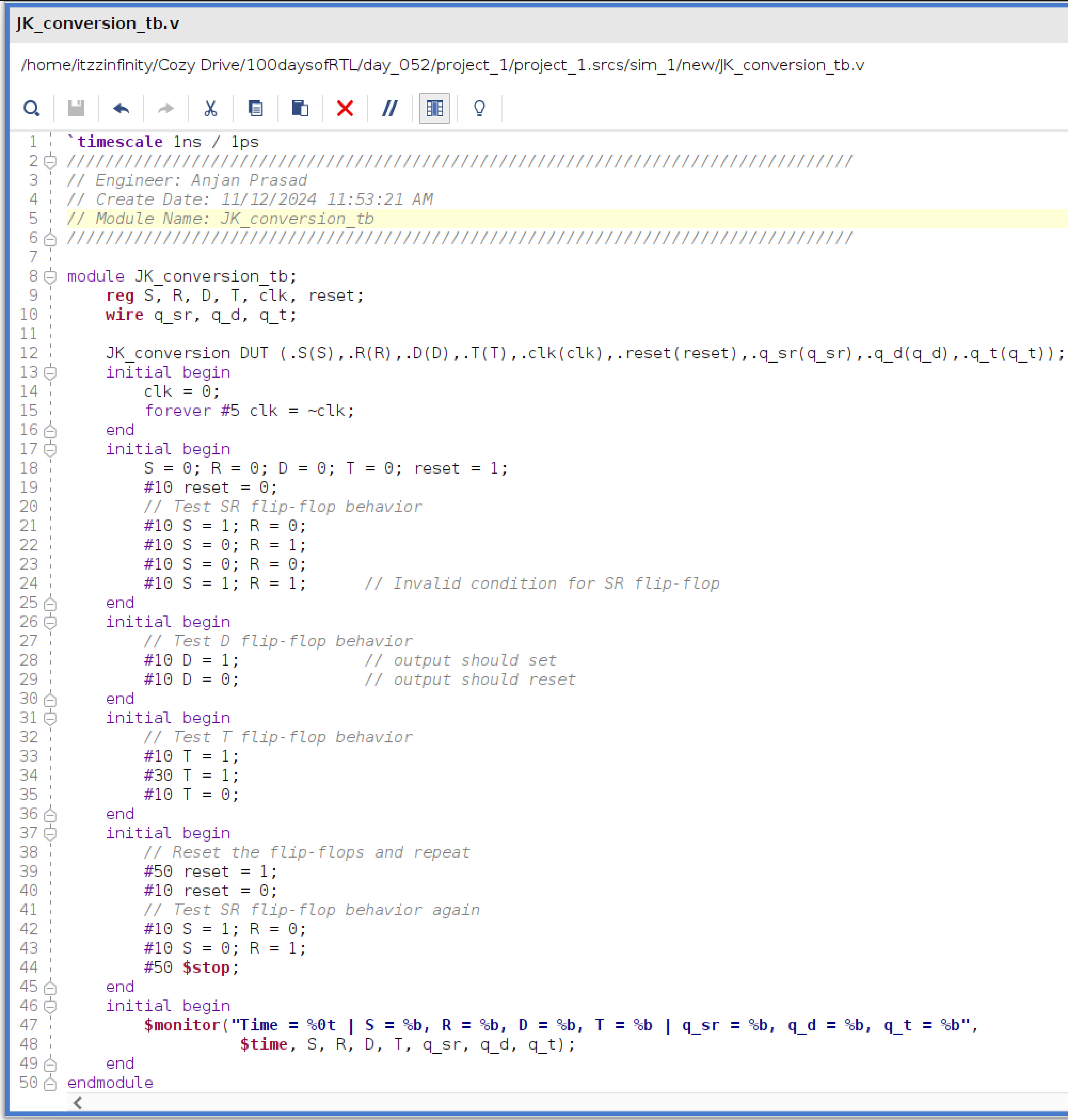
```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/12/2024 11:01:59 AM
// Module Name: T_flipflop
//////////////////////////////////////////////////////////////////////////////////


module T_flipflop (
    input T, clk, reset,
    output Q
);
    wire J = T;
    wire K = T;

    JK_flipflop jk_ff (.J(J), .K(K), .clk(clk), .reset(reset), .Q(Q));
endmodule

```



D_flipflop.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_052/project_1/project_1.srcs/sources_1/new/D_flipflop.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/12/2024 11:01:59 AM
// Module Name: D_flipflop
//////////////////////////////////////////////////////////////////////////////////


module D_flipflop (
    input D, clk, reset,
    output Q
);
    wire J = D;
    wire K = ~D;

    JK_flipflop jk_ff (.J(J), .K(K), .clk(clk), .reset(reset), .Q(Q));
endmodule

```


JK_conversion_tb.v
/home/itzzinfinity/Cozy Drive/100daysofRTL/day_052/project_1/project_1.srcs/sim_1/new/JK_conversion_tb.v

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/12/2024 11:53:21 AM
// Module Name: JK_conversion_tb
//////////////////////////////////////////////////////////////////////////////////

module JK_conversion_tb;
    reg S, R, D, T, clk, reset;
    wire q_sr, q_d, q_t;

    JK_conversion DUT (.S(S),.R(R),.D(D),.T(T),.clk(clk),.reset(reset),.q_sr(q_sr),.q_d(q_d),.q_t(q_t));
    initial begin
        clk = 0;
        forever #5 clk = ~clk;
    end
    initial begin
        S = 0; R = 0; D = 0; T = 0; reset = 1;
        #10 reset = 0;
        // Test SR flip-flop behavior
        #10 S = 1; R = 0;
        #10 S = 0; R = 1;
        #10 S = 0; R = 0;
        #10 S = 1; R = 1;      // Invalid condition for SR flip-flop
    end
    initial begin
        // Test D flip-flop behavior
        #10 D = 1;             // output should set
        #10 D = 0;             // output should reset
    end
    initial begin
        // Test T flip-flop behavior
        #10 T = 1;
        #30 T = 1;
        #10 T = 0;
    end
    initial begin
        // Reset the flip-flops and repeat
        #50 reset = 1;
        #10 reset = 0;
        // Test SR flip-flop behavior again
        #10 S = 1; R = 0;
        #10 S = 0; R = 1;
        #50 $stop;
    end
    initial begin
        $monitor("Time = %0t | S = %b, R = %b, D = %b, T = %b | q_sr = %b, q_d = %b, q_t = %b",
                  $time, S, R, D, T, q_sr, q_d, q_t);
    end
endmodule
```