Aim – Even Parity Generation and Check

1. Even Parity Generation

Project Summary | even_parity_gen.v | even_parity_gen_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_020/project_1/project_1.srcs/sources_1/new/even_parity_gen.v

```
1
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/11/2024 11:06:28 AM
5  // Module Name: even_parity_gen
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module even_parity_gen(input [7:0] a,
10 output p_even,
11 output [8:0]b
12 );
13
14 assign p_even = ^a;
15 assign b = {a,p_even};
16 endmodule
17
```

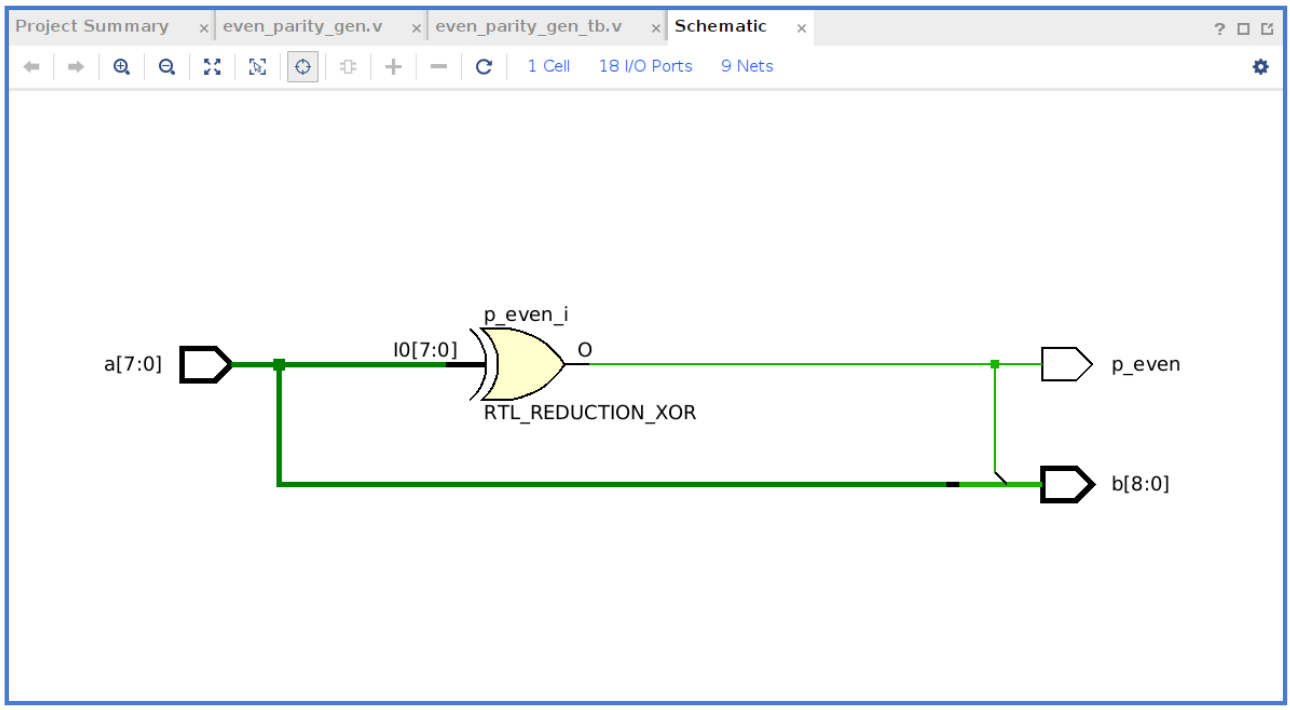
Main Code

Project Summary | even_parity_gen.v | even_parity_gen_tb.v

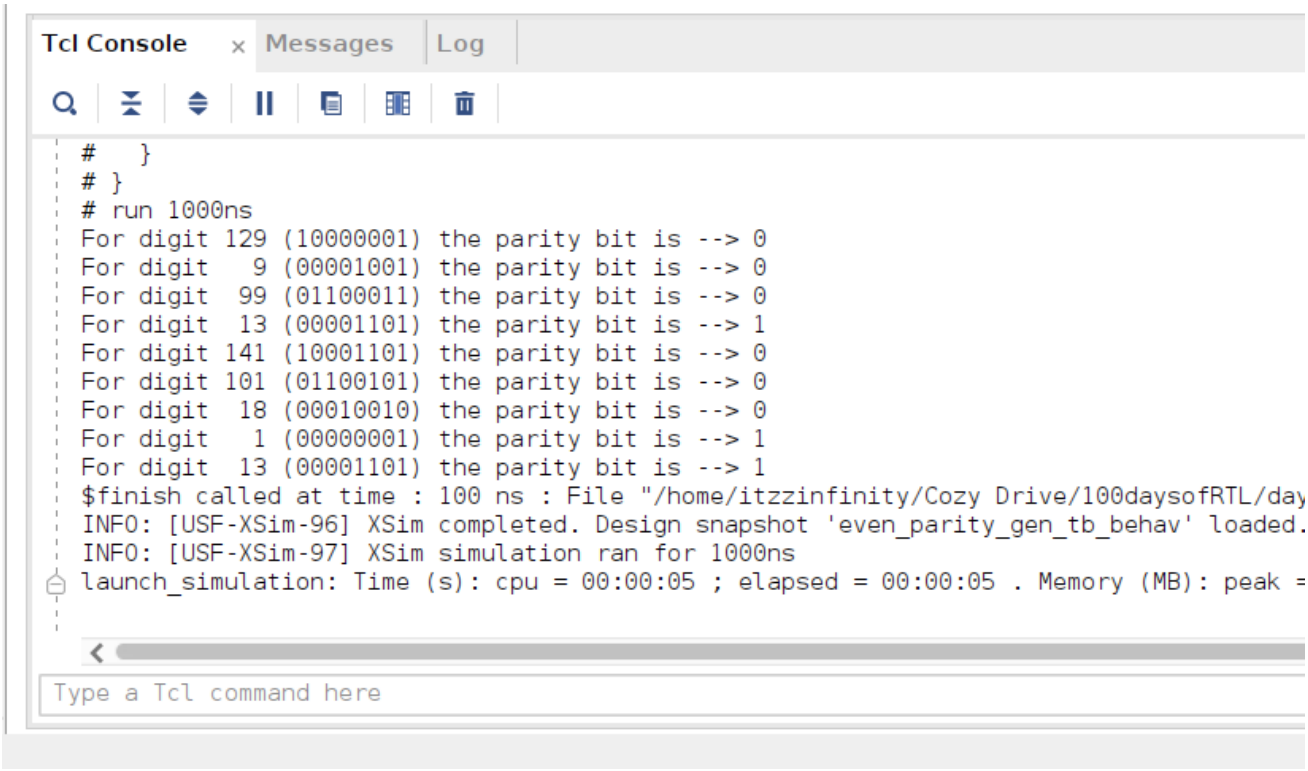
/home/itzzinfinity/Cozy Drive/100daysofRTL/day_020/project_1/project_1.srcs/sim_1/new/even_parity_gen_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/11/2024 11:07:15 AM
5  // Module Name: even_parity_gen_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module even_parity_gen_tb;
10   reg [7:0]a;
11   wire p_even;
12   wire [8:0] b;
13
14   even_parity_gen DUT(a,p_even,b);
15     initial begin
16         repeat(10) begin
17         a = $random(); #10;
18         $monitor("For digit %d (%b) the parity bit is --> %b",a,a,p_even);
19         end
20         $finish;
21     end
22 endmodule
23
```

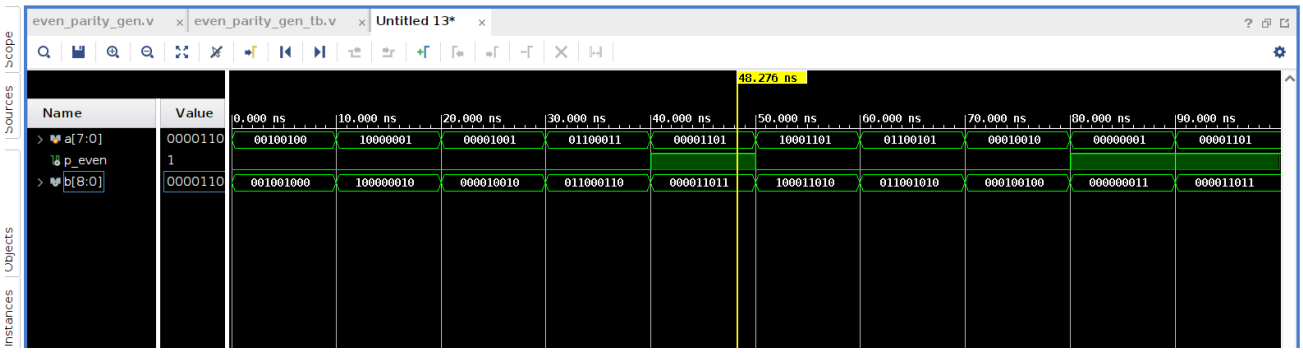
Testbench



RTL View

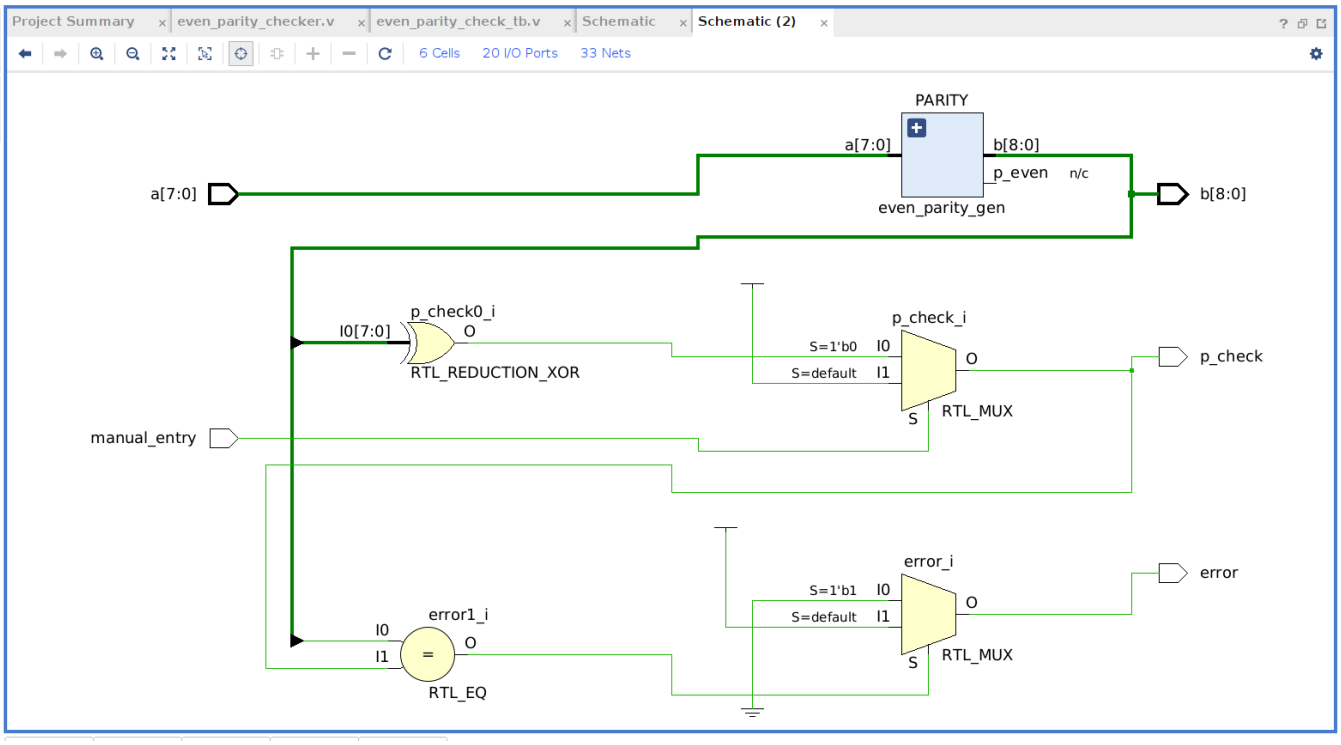


TCL Console

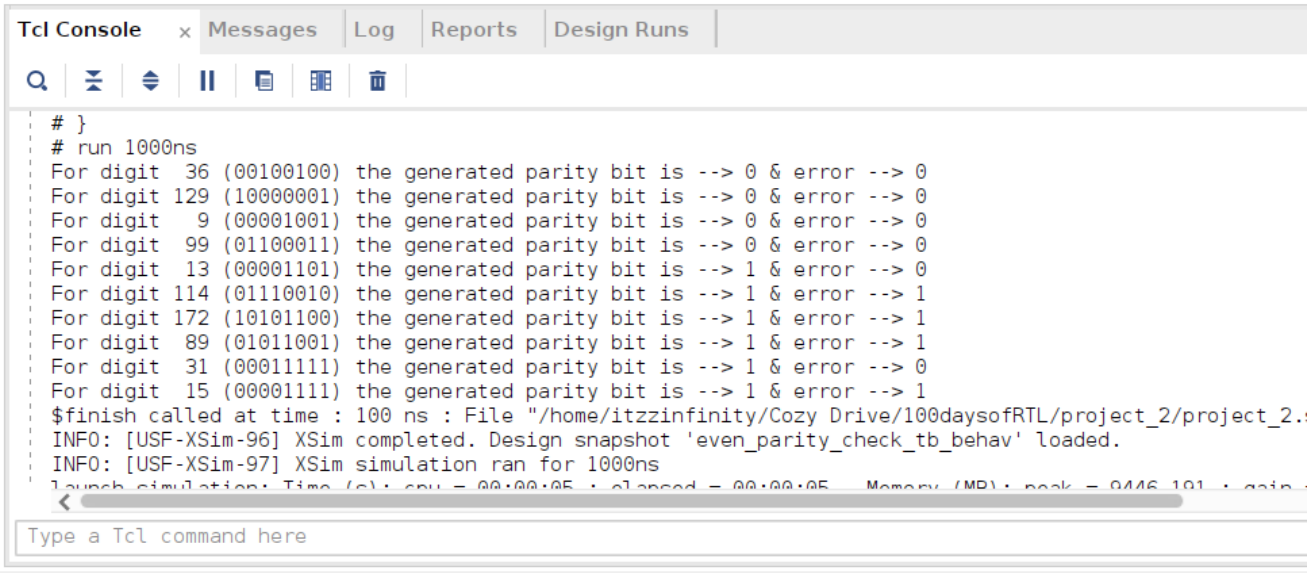


Waveforms

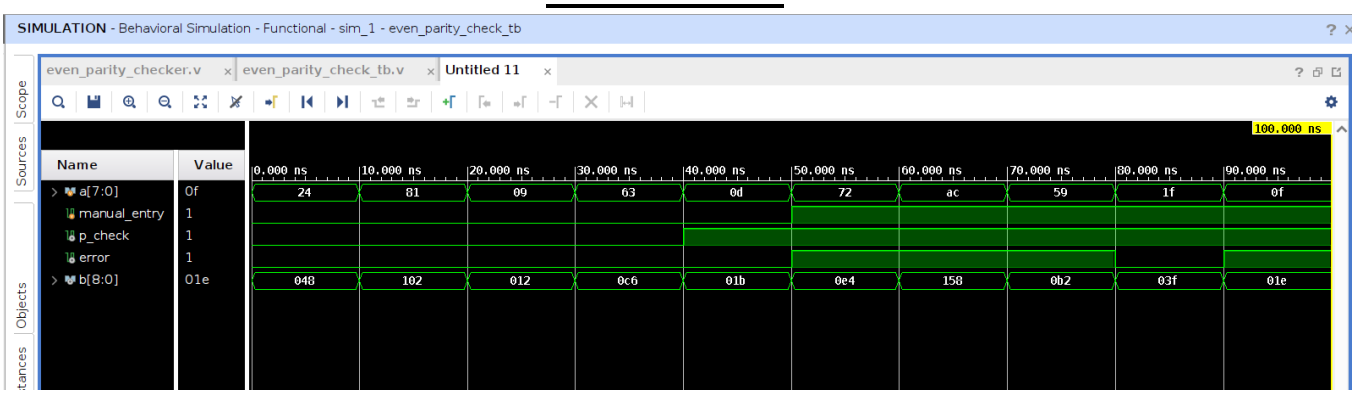
2. Even Parity Check



RTL View



TCL Console



Waveforms

even_parity_checker.v | even_parity_check_tb.v | Untitled 11

/home/itzzinfinity/Cozy Drive/100daysofRTL/project_2/project_2.srcs/sources_1/new/even_parity_checker.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/11/2024 11:55:12 AM
5   // Module Name: even_parity_checker
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module even_parity_checker(
10      input [7:0] a,
11      input manual_entry,
12      output p_check,error,
13      output [8:0]b
14  );
15
16      even_parity_gen PARITY(.a(a),.b(b)); //
17
18     assign p_check =(manual_entry==0)?^b[8:1]:1'b1; //created a 2 to 1 mux to enter parity bit and check
19     assign error = (b[0]==p_check)?1'b0:1'b1;
20
21  endmodule
22
```

Main Code

even_parity_checker.v | even_parity_check_tb.v | Untitled 11

/home/itzzinfinity/Cozy Drive/100daysofRTL/project_2/project_2.srcs/sim_1/new/even_parity_check_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/11/2024 11:56:23 AM
5   // Module Name: even_parity_check_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module even_parity_check_tb;
10      reg [7:0] a;
11      reg manual_entry;
12      wire p_check,error;
13      wire [8:0] b;
14
15      even_parity_checker DUT(a,manual_entry,p_check,error,b);
16
17          initial begin
18          repeat(5) begin
19          $monitor("For digit %d (%b) the generated parity bit is --> %b & error --> %b",a,a,p_check,error);
20          a = $random(); manual_entry=1'b0; #10;
21
22          end
23          begin
24                                              // Manually entering wrong parity bit
25          a = 8'd114; manual_entry=1'b1; #10;
26          a = 8'd172; manual_entry=1'b1; #10;
27          a = 8'd89; manual_entry=1'b1; #10;
28          a = 8'd31; manual_entry=1'b1; #10;
29          a = 8'd15; manual_entry=1'b1; #10;
30
31          $finish;
32          end
33      end
34  endmodule
35
```

Testbench