# **Aim - Even Parity Generation and Check**

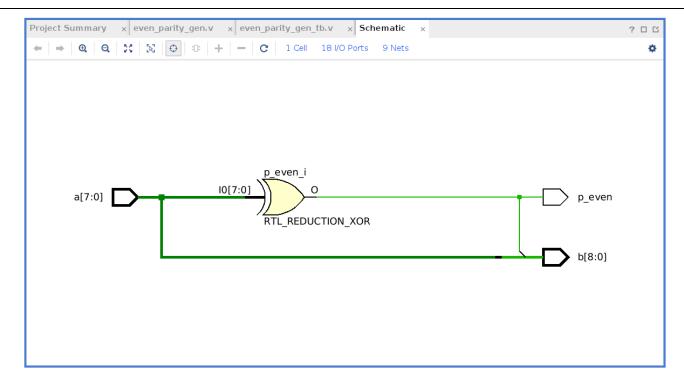
## 1. Even Parity Generation

```
Project Summary
            x even_parity_gen.v x even_parity_gen_tb.v
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 020/project 1/project 1.srcs/sources 1/new/even parity gen.v
  // Engineer: Anjan Prasad
  // Create Date: 10/11/2024 11:06:28 AM
  // Module Name: even_parity_gen
9 module even_parity_gen(input [7:0] a,
10
   output p_even,
11
   output [8:0]b
12
13
14
   assign p even = ^a;
15
   assign b = {a,p even};
16 🖒 endmodule
17
```

### **Main Code**

```
Project Summary
             x even_parity_gen.v
                             × even_parity_gen_tb.v
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 020/project 1/project 1.srcs/sim 1/new/even parity gen tb.v
  `timescale 1ns / 1ps
// Engineer: Anjan Prasad
   // Create Date: 10/11/2024 11:07:15 AM
8
9 module even parity gen tb;
10
    reg [7:0]a;
11
     wire p_even;
12
    wire [8:0] b;
13
     even_parity_gen DUT(a,p_even,b);
15 🖨
      initial begin
16 🖨
         repeat(10) begin
17
         a = \frac{n}{m} (); #10;
18
         $monitor("For digit %d (%b) the parity bit is --> %b",a,a,p_even);
19 🖒
         $finish;
20
21 🖒
      end
22 🖒 endmodule
23
```

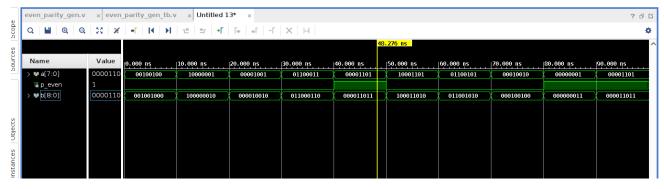
### **Testbench**



### **RTL View**

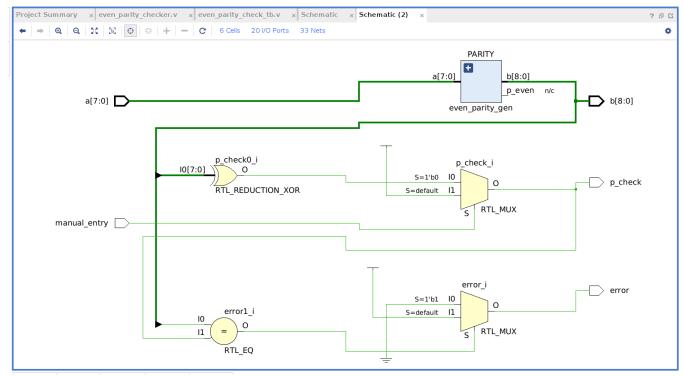
```
Tcl Console
                           Log
             x Messages
                   Û
  #
  # }
  # run 1000ns
  For digit 129 (10000001) the parity bit is --> 0
  For digit
              9 (00001001) the parity bit is --> 0
  For digit
             99 (01100011) the parity bit is --> 0
             13 (00001101) the parity bit is --> 1
  For digit
  For digit 141 (10001101) the parity bit is --> 0
  For digit 101 (01100101) the parity bit is --> 0
  For digit 18 (00010010) the parity bit is --> 0
             1 (00000001) the parity bit is --> 1
  For digit
  For digit 13 (00001101) the parity bit is --> 1
  $finish called at time : 100 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day
  INFO: [USF-XSim-96] XSim completed. Design snapshot 'even_parity_gen_tb_behav' loaded.
  INFO: [USF-XSim-97] XSim simulation ran for 1000ns
△ launch_simulation: Time (s): cpu = 00:00:05; elapsed = 00:00:05. Memory (MB): peak =
   < =
Type a Tcl command here
```

### **TCL Console**

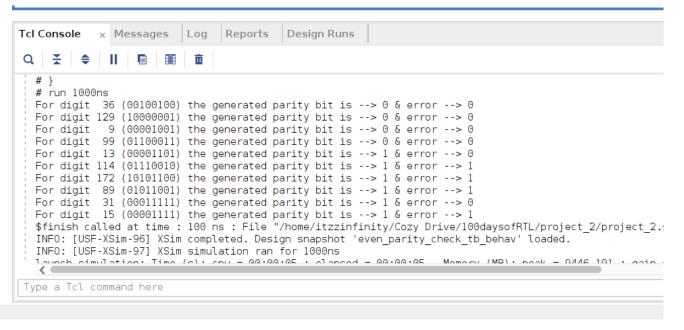


**Waveforms** 

# 2. Even Parity Check



### **RTL View**



### **TCL Console**



### **Waveforms**

```
even_parity_checker.v x even_parity_check_tb.v x Untitled 11
Scope
   /home/itzzinfinity/Cozy Drive/100daysofRTL/project_2/project_2.srcs/sources_1/new/even_parity_checker.v
   Sources
    2 🖕
           √/ Engineer: Anjan Prasad
           // Create Date: 10/11/2024 11:55:12 AM
           '// Module Name: even_parity_checker
    6 🖒
           8
          module even_parity_checker(
    9 🖨
Objects
   10
              input [\overline{7}:0] a,
              input manual entry,
              output p check, error,
              output [8:0]b
   13
Protocol Instances
   14
          );
   15
   16
              even_parity_gen PARITY(.a(a),.b(b)); //
   17
   18
             assign p check =(manual entry==0)?^b[8:1]:1'b1; //created a 2 to 1 mux to enter parity bit and check
   19
             assign error = (b[0]==p_check)?1'b0:1'b1;
   20
   21 🖒
           endmodule
   22
```

# Main Code

```
even_parity_checker.v x even_parity_check_tb.v x Untitled 11
Scope
    /home/itzzinfinity/Cozy Drive/100daysofRTL/project_2/project_2.srcs/sim_1/new/even_parity_check_tb.v
    Sources
     1 (=)
2 (=)
              timescale 1ns / 1ps
             √/ Engineer: Anjan Prasad
             // Create Date: 10/11/2024 11:56:23 AM
             5
     6 🖒
     9
             module even parity check tb;
Objects
    10
                reg [7:\overline{0}] a;
                 reg manual entry;
    12
                 wire p_check,error;
    13
                 wire [8:0] b;
Protocol Instances
    15
                 even_parity_checker DUT(a,manual_entry,p_check,error,b);
    16
                     initial begin
         000
    18
                     repeat(5) begin
    19
                     $monitor("For digit %d (%b) the generated parity bit is --> %b & error --> %b",a,a,p check,error);
    20
                     a = $random(); manual entry=1'b0; #10;
    21
    22
                     end
    23
                     beain
    24
                                                         // Manually entering wrong parity bit
                     a = 8'd114; manual_entry=1'b1; #10;
a = 8'd172; manual_entry=1'b1; #10;
    25
    26
         00000
                     a = 8'd89; manual_entry=1'b1; #10;
a = 8'd31; manual_entry=1'b1; #10;
a = 8'd15; manual_entry=1'b1; #10;
    27
    28
    29
    30
    31
                     $finish:
    32
                     end
    33
                 end
    34
             endmodule
    35
```

### **Testbench**