2 Cells   21 I/O Ports   34 Nets

Rst_n

bin[7:0]

Clk

BIN2BCD

Rst_n

bin[8:0]

clk

binary_to_bcd

hundreds[3:0]

ones[3:0]

tens[3:0]

sevDEC

Clk

hundreds[3:0]

ones[3:0]

tens[3:0]

seven_segment_decoder

digit[3:0]

seg[6:0]

digit[3:0]

seg[6:0]

Rst_n
bin[7:0]
Clk

bcd0_i__0
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bcd1_i__0
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

bcd0_i__1
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bcd1_i__1
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

Rst_n

bcd0_i
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bin[8:0]

bcd1_i
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

clk

bcd0_i__2
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bcd_i__0
S=1'b1 I0[3:0]
S=default I1[3:0]
O[3:0]
S
RTL_MUX

bcd_i__1
S=1'b1 I0[3:0]
S=default I1[3:0]
O[3:0]
S
RTL_MUX

bcd_i
S=1'b1 I0[3:0]
S=default I1[3:0]
O[3:0]
S
RTL_MUX

bcd1_i__2
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

bcd_i__2
S=1'b1 I0[14:0]
S=default I1[14:0]
O[14:0]
S
RTL_MUX

bcd0_i__3
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bcd1_i__3
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

bcd0_i__4
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bcd1_i__4
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

bcd0_i__5
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bcd1_i__5
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

bcd_i__3
S=1'b1 I0[3:0]
S=default I1[3:0]
O[3:0]
S
RTL_MUX

bcd0_i__6
I0[3:0]
I1[1:0]
+
O[3:0]
RTL_ADD

bcd_i__4
S=1'b1 I0[3:0]
S=default I1[3:0]
O[3:0]
S
RTL_MUX

bcd1_i__6
I0[3:0]
V=B"0101" I1[3:0]
>=
O
RTL_GEQ

bcd_i__5
S=1'b1 I0[3:0]
S=default I1[3:0]
O[3:0]
S
RTL_MUX

bcd_i__6
S=1'b1 I0[14:0]
S=default I1[14:0]
O[14:0]
S
RTL_MUX

143 Cells   21 I/O Ports   492 Nets

BIN2BCD

bcd0_i__7
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd1_i__7
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

bcd1_i__8
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

bcd0_i__8
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd0_i__9
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd1_i__9
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

bcd_i__7
S=1'b1
S=default
I0[3:0]
I1[3:0]
O[3:0]
S
RTL_MUX

bcd_i__8
S=1'b1
S=default
I0[3:0]
I1[3:0]
O[3:0]
S
RTL_MUX

bcd_i__9
S=1'b1
S=default
I0[3:0]
I1[3:0]
O[3:0]
S
RTL_MUX

bcd0_i__10
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd_i__10
S=1'b1
S=default
I0[14:0]
I1[14:0]
O[14:0]
S
RTL_MUX

bcd1_i__10
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

bcd0_i__11
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd1_i__11
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

bcd1_i__12
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

bcd0_i__12
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd0_i__13
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd1_i__13
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

bcd_i__11
S=1'b1
S=default
I0[3:0]
I1[3:0]
O[3:0]
S
RTL_MUX

bcd_i__12
S=1'b1
S=default
I0[3:0]
I1[3:0]
O[3:0]
S
RTL_MUX

bcd_i__13
S=1'b1
S=default
I0[3:0]
I1[3:0]
O[3:0]
S
RTL_MUX

bcd0_i__14
I0[3:0]
I1[1:0]
O[3:0]
+
RTL_ADD

bcd_i__14
S=1'b1
S=default
I0[14:0]
I1[14:0]
O[14:0]
S
RTL_MUX

bcd1_i__14
I0[3:0]
I1[3:0]
O
>=
V=B"0101"
RTL_GEQ

I0[3:0]
V=B"0101"
I1[3:0]

I0[3:0]
I1[3:0]

I0[3:0]
I1[1:0]

I0[3:0]
I1[1:0]

I0[3:0]
V=B"0101"
I1[3:0]

binary_to_bcd

143 Cells   21 I/O Ports   492 Nets

sevDEC

seven_segment_decoder

refresh_counter0_i
RTL_ADD
I1
I0[19:0]
O[19:0]

Clk

refresh_counter_i
RTL_MUX
S=20'b00000110100101111000
I0[19:0]
S=default
I1[19:0]
O[19:0]
S[19:0]

refresh_counter_reg[19:0]
RTL_REG
C
D
Q

digit_select_i
RTL_ROM
A[19:0]   O

digit_select0_i
RTL_ADD
I1
I0[1:0]
O[1:0]

digit_select_reg[1:0]
RTL_REG
C
CE
D
Q

hundreds[3:0]
ones[3:0]
n/c
tens[3:0]

current_digit_i
RTL_MUX
S=2'b00   I0[3:0]
S=2'b01   I1[3:0]
S=2'b10   I2[3:0]
S=2'b11   I3[3:0]
O[3:0]
S[1:0]

digit_i
RTL_MUX
V=B"0111", S=2'b00   I0[3:0]
V=B"1011", S=2'b01   I1[3:0]
V=B"1101", S=2'b10   I2[3:0]
V=B"1110", S=2'b11   I3[3:0]
O[3:0]
S[1:0]
digit[3:0]

seg_i
RTL_ROM
A[3:0]   O[6:0]
seg[6:0]

[3:0]