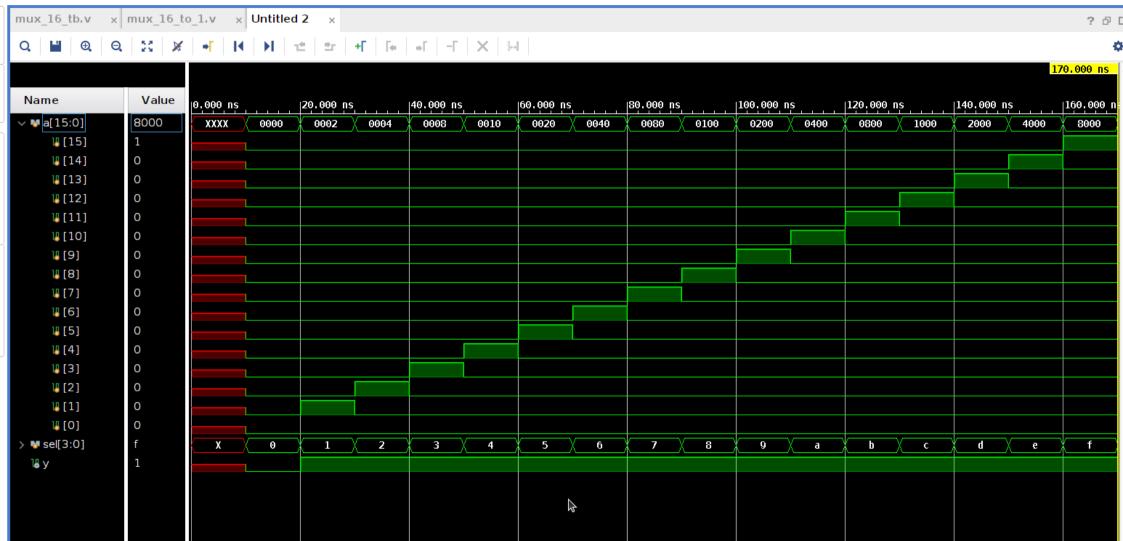
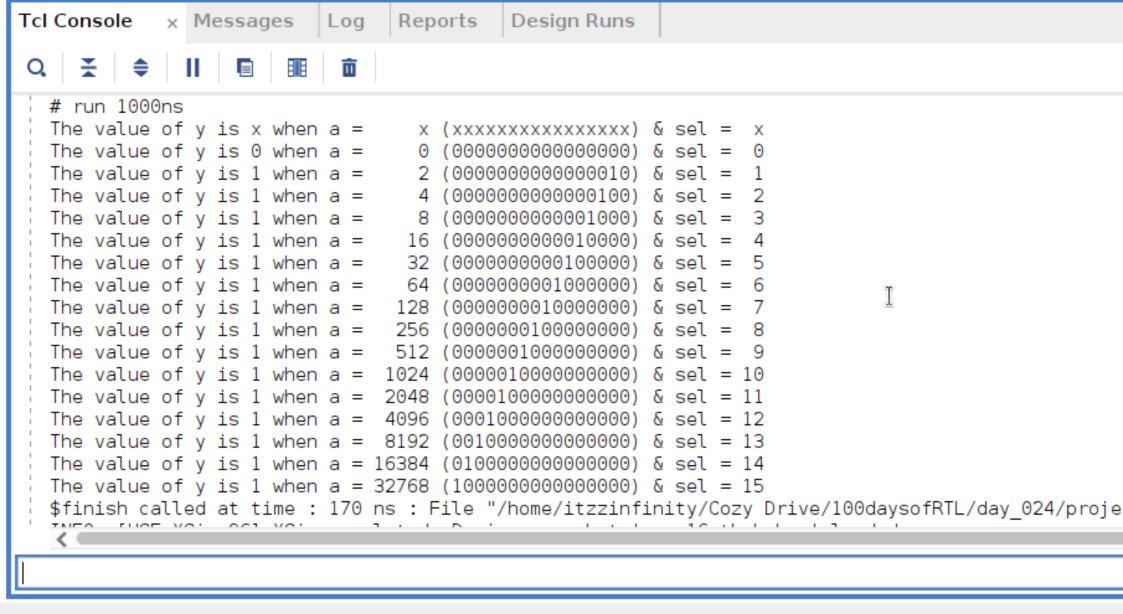
o.v x mux_16_to_1.v x Schematic x 16 Cells 21 I/O Ports 49 Nets mux_1 a[3:0] a[15:0] b[3:0] y[3:0] sel[3:0] mux_2_to_1 mux_2 y[3:0] b[3:0] mux_2_to_1 mux_3 mux_9 a[3:0] a[3:0] b[3:0] y[3:0] b[3:0] y[3:0] mux_2_to_1 mux_2_to_1 mux_4 mux_10 mux_13 a[3:0] a[3:0] a[3:0] b[3:0] y[3:0] b[3:0] y[3:0] b[3:0] y[3:0] mux_15 mux_2_to_1 mux_2_to_1 mux_2_to_1 a[3:0] S=1'b0 | 10[3:0] 0[3:0] y[3:0] mux_5 b[3:0] S=default |1[3:0] a[3:0] mux_11 RTL_MUX a[3:0] mux_14 sel b[3:0] y[3:0] a[3:0] b[3:0] y[3:0] mux_2_to_1 y[3:0] b[3:0] mux_2_to_1 mux_2_to_1 mux_6 mux_2_to_1 a[3:0] y[3:0] b[3:0] mux_12 sel a[3:0] mux_2_to_1 b[3:0] y[3:0] mux_7 mux_2_to_1 a[3:0] b[3:0] y[3:0] mux_2_to_1 mux_8 a[3:0] b[3:0] y[3:0] mux_2_to_1





```
Project Summary
                x mux 16 tb.v
                               x mux 16 to 1.v
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 024/project 1/project 1.srcs/sources 1/new/mux 16 to 1.v
                     `timescale 1ns / 1ps
 // Engineer: Anjan Prasad
  // Create Date: 10/15/2024 08:26:12 AM
    // Module Name: mux 16 to 1
 5
 7
8 🖨
    module mux 16 to 1(
       input [15:0] a,
9
       input [3:0] sel,
10
11
       output y);
12
13
       wire [7:0] w;
14
       //level 1
15
       mux 2 to 1 mux 1(a[0],a[1],sel[0],w[0]);
       mux 2 to 1 mux 2(a[2],a[3],sel[0],w[1]);
16
       mux 2 to 1 mux 3(a[4],a[5],sel[0],w[2]);
17
18
       mux 2 to 1 mux 4(a[6],a[7],sel[0],w[3]);
19
       mux 2 to 1 mux 5(a[8],a[9],sel[0],w[4]);
       mux 2 to 1 mux 6(a[10],a[11],sel[0],w[5]);
20
       mux 2 to 1 mux 7(a[12],a[13],sel[0],w[6]);
21
22
       mux 2 to 1 mux 8(a[14],a[15],sel[0],w[7]);
23
24
       //level 2
25
        wire [3:0] x;
26
       mux 2 to 1 mux 9(w[0], w[1], sel[1], x[0]);
27
       mux 2 to 1 mux 10(w[2], w[3], sel[1], x[1]);
28
       mux 2 to 1 mux 11(w[4], w[5], sel[1], x[2]);
29
       mux 2 to 1 mux 12(w[6], w[7], sel[1], x[3]);
30
31
       //level 3
32
       wire [1:0] z:
33
       mux 2 to 1 mux 13(x[0],x[1],sel[2],z[0]);
34
       \max 2 to 1 \max 14(x[2],x[3],sel[2],z[1]);
35
36
       //level 4
37
       mux 2 to 1 mux 15(z[0],z[1],sel[3],v);
    endmodule
38 🛆
39
```

```
x Schematic
               x mux 16 tb.v
                            x mux 16 to 1.v
Project Summary
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 024/project 1/project 1.srcs/sim 1/new/mux 16 tb.v
                  `timescale 1ns / 1ps
   // Engineer: Anjan Prasad
    // Create Date: 10/15/2024 08:27:52 AM
 4
    // Module Name: mux 16 tb
 5
    module mux 16 tb:
       req [15:0] a;
 8
9
       req [3:0] sel;
10
       wire v;
11
12
       mux 16 to 1 uut (
13
           .a(a), .sel(sel), .y(y)
14
       );
15
16 🖨
       initial begin
17
          $monitor("The value of y is %b when a = %d (%b) & sel = %d",y,a,a,sel);
18
          #10:
19
          a = 16'b00000000000000000; sel = 4'b0000; #10; // Select a[0]
20
          21
          22
          23
          a = 16'b00000000000010000; sel = 4'b0100; #10; // Select a[4]
24
          a = 16'b000000000001000000; sel = 4'b0101; #10; // Select a[5]
25
          a = 16'b00000000010000000; sel = 4'b0110; #10; // Select a[6]
          a = 16'b00000000100000000; sel = 4'b0111; #10; // Select a[7]
26
27
          a = 16'b00000001000000000; sel = 4'b1000; #10; // Select a[8]
28
          a = 16'b00000010000000000; sel = 4'b1001; #10; // Select a[9]
29
          a = 16'b00000100000000000; sel = 4'b1010; #10; // Select a[10]
30
          a = 16'b00001000000000000; sel = 4'b1011; #10; // Select a[11]
31
          a = 16'b00010000000000000; sel = 4'b1100; #10; // Select a[12]
32
          a = 16'b00100000000000000; sel = 4'b1101; #10; // Select a[13]
          a = 16'b01000000000000000; sel = 4'b1110; #10; // Select a[14]
33
          a = 16'b10000000000000000; sel = 4'b1111; #10; // Select a[15]
34
35
          $finish;
36
37 🛆
       end
38 点
    endmodule
39
```