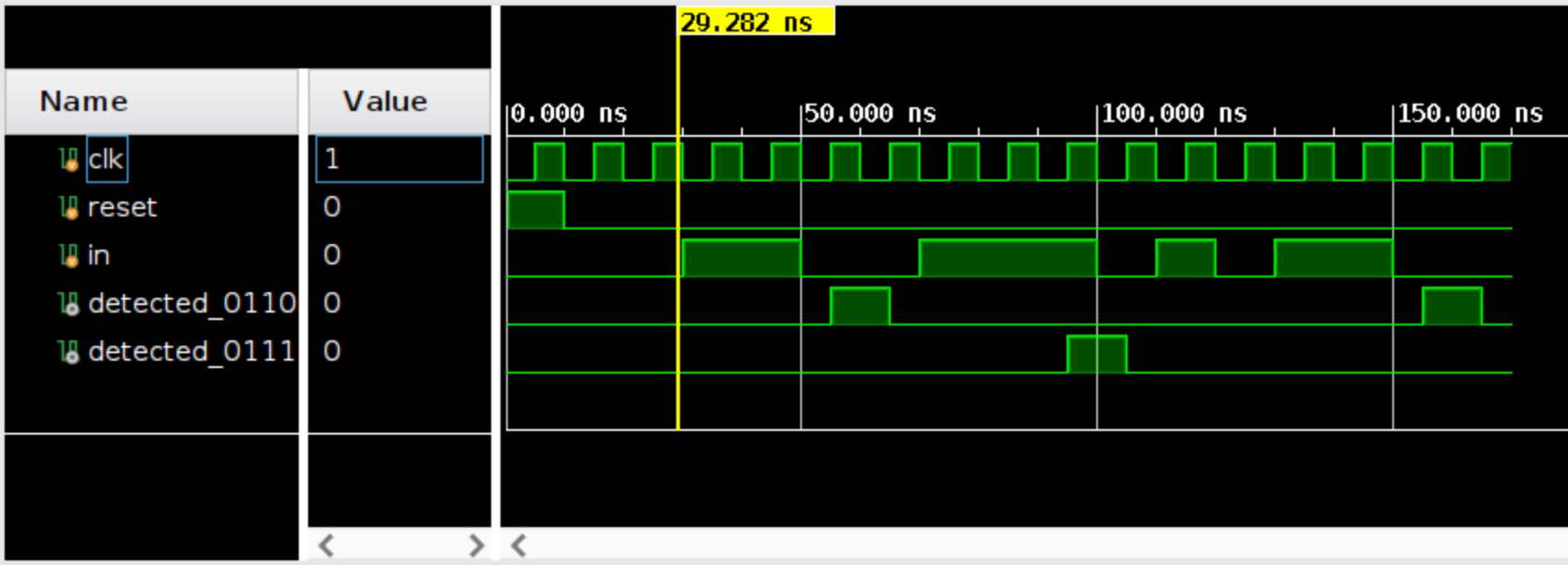
seq_detector.v | seq_detector_tb.v | Untitled 1*

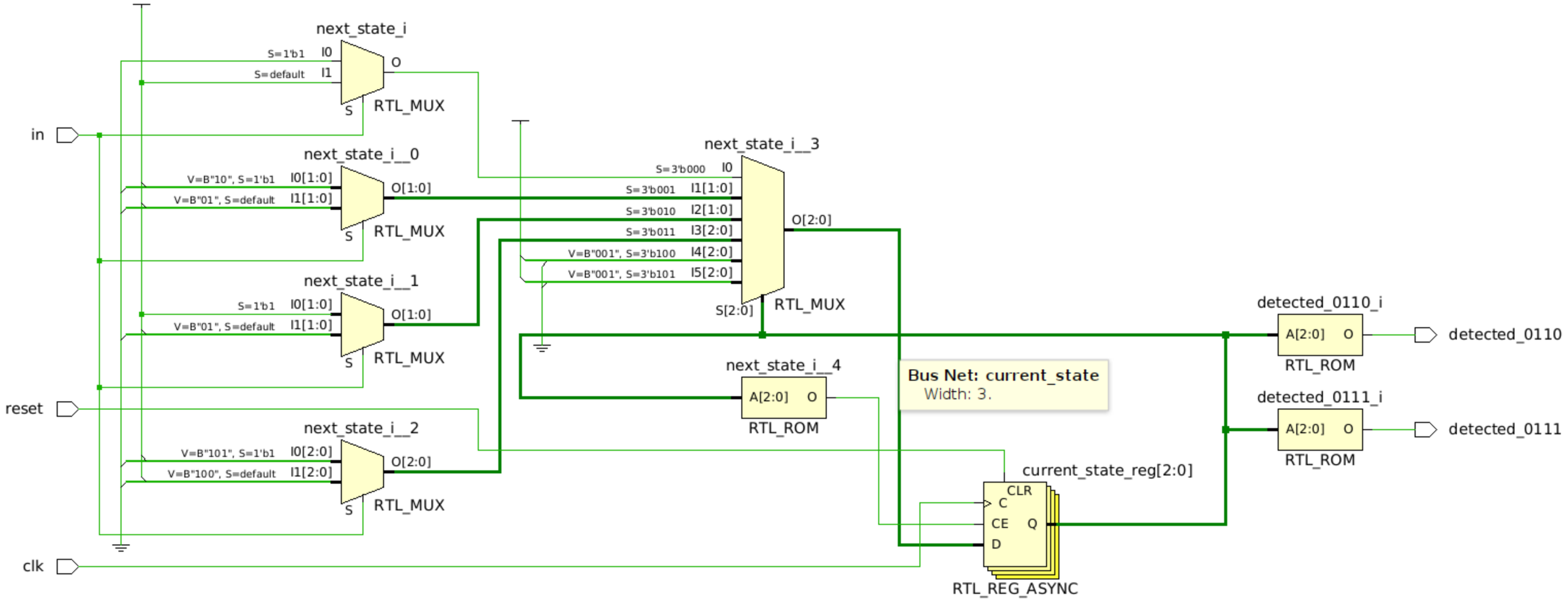


Tcl Console | Messages | Log

```
# run 1000ns
Time=0 | Reset=1 | In=0 | Det_0110=0 | Det_0111=0
Time=10000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=0
Time=30000 | Reset=0 | In=1 | Det_0110=0 | Det_0111=0
Time=50000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=0
Time=55000 | Reset=0 | In=0 | Det_0110=1 | Det_0111=0
Time=65000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=0
Time=70000 | Reset=0 | In=1 | Det_0110=0 | Det_0111=0
Time=95000 | Reset=0 | In=1 | Det_0110=0 | Det_0111=1
Time=100000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=1
Time=105000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=0
Time=110000 | Reset=0 | In=1 | Det_0110=0 | Det_0111=0
Time=120000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=0
Time=130000 | Reset=0 | In=1 | Det_0110=0 | Det_0111=0
Time=150000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=0
Time=155000 | Reset=0 | In=0 | Det_0110=1 | Det_0111=0
Time=165000 | Reset=0 | In=0 | Det_0110=0 | Det_0111=0
$finish called at time : 170 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_074/
INFO: [USF-XSim-96] XSim completed. Design snapshot 'seq_detector_tb_behav' loaded.
```

Project Summary | seq_detector.v | Schematic | seq_detector_tb.v | Schematic (2)

11 Cells 5 I/O Ports 22 Nets



Tcl Console | Messages | Log | Reports | Design Runs

seq_detector_tb.v | Untitled 1* | seq_detector.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_074/project_1/project_1.srcs/sources_1/new/seq_detector.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Engineer: Anjan Prasad
3  // Create Date: 12/04/2024 08:16:09 AM
4  // Module Name: seq_detector
5  //////////////////////////////////////////////////////////////////////////////////
6
7  module seq_detector(
8      input clk,reset,in,
9      output reg detected_0110,detected_0111
10 );
11     localparam
12         IDLE   = 3'b000,
13         S0     = 3'b001,  // Detected '0'
14         S01    = 3'b010,  // Detected '01'
15         S011   = 3'b011,  // Detected '011'
16         S0110  = 3'b100,  // Detected '0110'
17         S0111  = 3'b101;   // Detected '0111';
18
19 reg [2:0] current_state, next_state;
20
21     always @(posedge clk or posedge reset) begin
22         if (reset)
23             current_state <= IDLE;
24         else
25             current_state <= next_state;
26     end
27
28     always @(*) begin
29
30         next_state = current_state;
31         detected_0110 = 1'b0;
32         detected_0111 = 1'b0;
33
34         case (current_state)
35             IDLE: begin
36                 if (in)
37                     next_state = IDLE;  // Stay in IDLE if input is '1'
38                 else
39                     next_state = S0;    // Move to S0 if input is '0'
```

Tcl Console | Messages | Log

seq_detector_tb.v | Untitled 1* | seq_detector.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_074/project_1/project_1.srcs/sources_1/new/seq_detector.v

```
37                      next_state = IDLE;  // Stay in IDLE if input is '1'
38                  else
39                      next_state = S0;    // Move to S0 if input is '0'
40              end
41
42              S0: begin
43                  if (in)
44                      next_state = S01;  // Detected '01'
45                  else
46                      next_state = S0;   // Stay in S0 if input is '0'
47              end
48
49              S01: begin
50                  if (in)
51                      next_state = S011; // Detected '011'
52                  else
53                      next_state = S0;   // Reset to S0 if input is '0'
54              end
55
56              S011: begin
57                  if (in)
58                      next_state = S0111; // Detected '0111'
59                  else
60                      next_state = S0110; // Detected '0110'
61              end
62
63              S0110: begin
64                  detected_0110 = 1'b1;   // Sequence '0110' detected
65                  next_state = S0;        // Reset to S0
66              end
67
68              S0111: begin
69                  detected_0111 = 1'b1;   // Sequence '0111' detected
70                  next_state = S0;        // Reset to S0
71              end
72          endcase
73      end
74  endmodule
75
```

Tcl Console | Messages | Log

seq_detector_tb.v | Untitled 1* | seq_detector.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_074/project_1/project_1.srcs/sim_1/new/seq_detector_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer : Anjan Prasad
4  // Create Date: 12/04/2024 08:22:44 AM
5  // Module Name: seq_detector_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module seq_detector_tb;
9      reg clk;
10     reg reset;
11     reg in;
12
13     wire detected_0110;
14     wire detected_0111;
15
16     seq_detector DUT (
17         .clk(clk),
18         .reset(reset),
19         .in(in),
20         .detected_0110(detected_0110),
21         .detected_0111(detected_0111)
22     );
23
24     initial begin
25         clk = 0;
26         forever #5 clk = ~clk;
27     end
28
29     initial begin
30
31         reset = 1;
32         in = 0;
33
34         #10 reset = 0;
35
36         #10 in = 0;  // Starting with 0
37         #10 in = 1;  // 01
38         #10 in = 1;  // 011
39         #10 in = 0;  // 0110 (should detect sequence 0110)
```

Tcl Console | Messages | Log

seq_detector_tb.v | Untitled 1* | seq_detector.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_074/project_1/project_1.srcs/sim_1/new/seq_detector_tb.v

```
22      );
23
24      initial begin
25          clk = 0;
26          forever #5 clk = ~clk;
27      end
28
29      initial begin
30
31          reset = 1;
32          in = 0;
33
34          #10 reset = 0;
35
36          #10 in = 0;  // Starting with 0
37          #10 in = 1;  // 01
38          #10 in = 1;  // 011
39          #10 in = 0;  // 0110 (should detect sequence 0110)
40          #10 in = 0;
41          #10 in = 1;  // 01
42          #10 in = 1;  // 011
43          #10 in = 1;  // 0111 (should detect sequence 0111)
44          #10 in = 0;
45
46          #10 in = 1;  // Unmatched sequence
47          #10 in = 0;  // 0
48          #10 in = 1;  // 01
49          #10 in = 1;  // 011
50          #10 in = 0;  // 0110 (should detect again)
51          #20 $finish;
52      end
53
54      initial begin
55          $monitor("Time=%0t | Reset=%b | In=%b | Det_0110=%b | Det_0111=%b",
56                   $time, reset, in, detected_0110, detected_0111);
57      end
58  endmodule
59
60
```

Tcl Console | Messages | Log