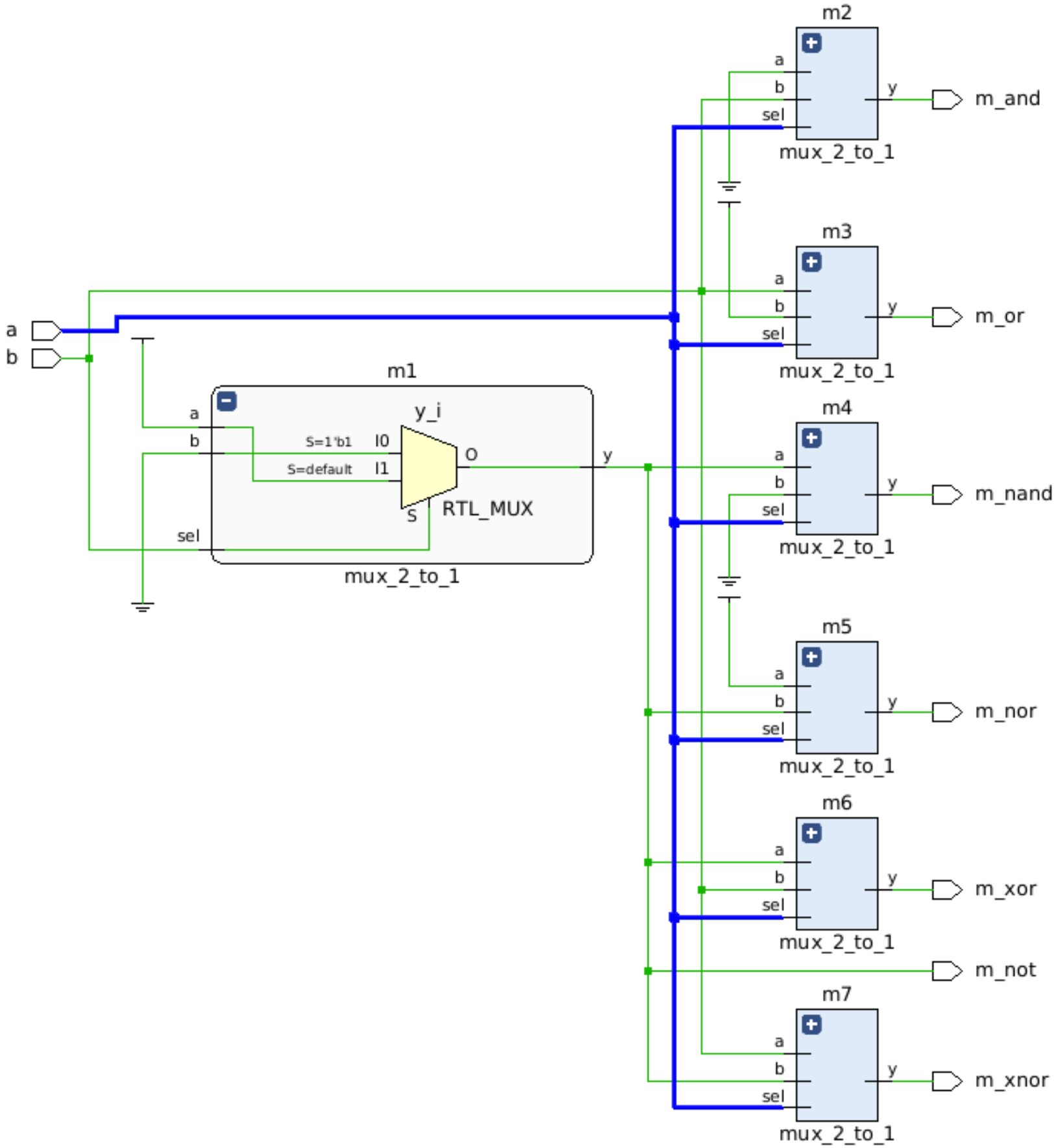
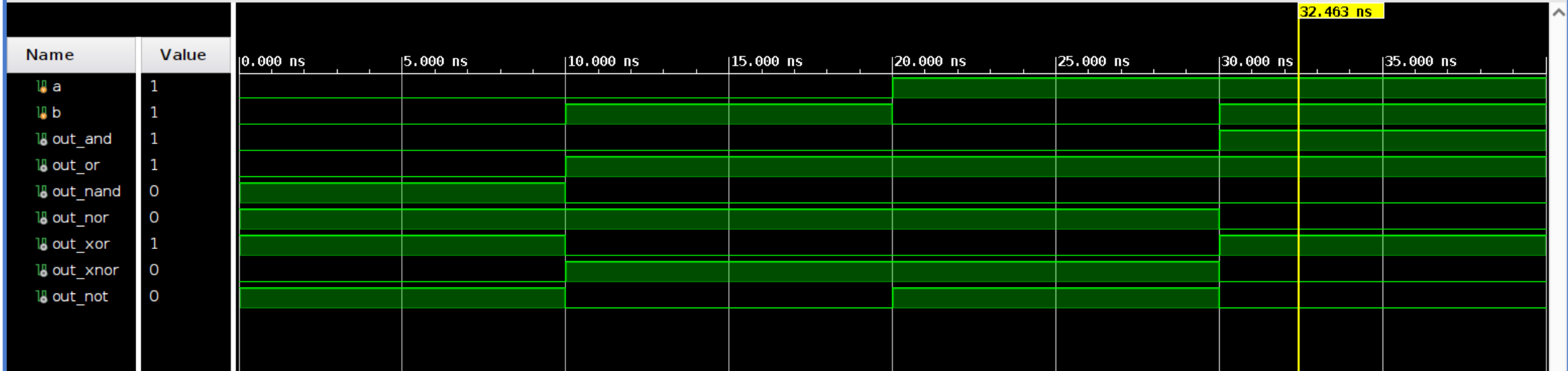
8 Cells 9 I/O Ports 15 Nets



mux_2_to_1.v | mux_to_gates.v | mux_gate_tb.v | Untitled 6



mux_2_to_1.v | **mux_to_gates.v** | mux_gate_tb.v | Untitled 6

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_026/project_1/project_1.srcs/sources_1/new/mux_to_gates.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/13/2024 06:16:57 AM
5  // Module Name: mux_to_gates
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module mux_to_gates(
10 input a,b,
11 output m_and,m_or,m_nand,m_nor,m_xor,m_xnor,m_not);
12
13 mux_2_to_1 m1 (1'b1,  1'b0,  b, m_not);
14 mux_2_to_1 m2 (1'b0,  b,     a, m_and);
15 mux_2_to_1 m3 (b,     1'b1,  a, m_or);
16 mux_2_to_1 m4 (m_not, 1'b0,  a, m_nand);
17 mux_2_to_1 m5 (1'b1,  m_not, a, m_nor);
18 mux_2_to_1 m6 (m_not, b,     a, m_xor);
19 mux_2_to_1 m7 (b,     m_not, a, m_xnor);
20
21
22 endmodule
23
```

mux_2_to_1.v | mux_to_gates.v | mux_gate_tb.v | Untitled 6

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_026/project_1/project_1.srcs/sources_1/new/mux_2_to_1.v

```
1  module mux_2_to_1(
2  input a,b,
3  input sel,
4  output y);
5
6  assign y = (sel)?b:a;
7
8  endmodule
9
```

mux_2_to_1.v | mux_to_gates.v | **mux_gate_tb.v** | Untitled 6

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_026/project_1/project_1.srcs/sim_1/new/mux_gate_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/13/2024 06:06:15 AM
5  // Module Name: mux_gate_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module mux_gate_tb;
10
11     reg a,b;
12     wire out_and, out_or, out_nand, out_nor, out_xor, out_xnor,out_not;
13     mux_to_gates DUT (a,b, out_and, out_or, out_nand, out_nor, out_xor, out_xnor,out_not);
14  initial begin
15   a = 1'b0; b = 1'b0;
16  #10;
17  a = 1'b0; b = 1'b1;
18  #10;
19  a = 1'b1; b = 1'b0;
20  #10;
21  a = 1'b1; b = 1'b1;
22  #10;
23  $finish;
24 end
25 endmodule
26
```