Name	Value
a[3:0]	c
b[3:0]	3
c	1
sum[3:0]	0
cout	1
total[4:0]	10

60.000 ns

| | 0.000 ns | 5.000 ns | 10.000 ns | 15.000 ns | 20.000 ns | 25.000 ns | 30.000 ns | 35.000 ns | 40.000 ns | 45.000 ns | 50.000 ns | 55.000 ns |

a[3:0]: 1   6   f   a   f   c

b[3:0]: 2   5   1   5   f   3

sum[3:0]: 3   b   1   0   e   0

total[4:0]: 03   0b   11   10   0e   10

```verilog
1
2  ////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/10/2024 09:12:03 AM
5  // Module Name: carry_skip_adder
6  ////////////////////////////////////////////////////////////////////////////
7
8
9  module carry_skip_adder(
10 input [3:0] a,b,
11 input c,
12 output [3:0] sum,
13 output cout);
14     wire [3:0] s,c1,p;
15
16
17   full_adder FA1(a[0],b[0],c,sum[0],c1[0]);
18   full_adder FA2(a[1],b[1],c1[0],sum[1],c1[1]);
19   full_adder FA3(a[2],b[2],c1[1],sum[2],c1[2]);
20   full_adder FA4(a[3],b[3],c1[2],sum[3],c1[3]);
21 assign p = a^b;
22 assign s = & (p [3:0]);
23 mux_2_to_1 M1 (c,c1[3],s,cout);
24 endmodule
25
26
27
28
29
```

```verilog
//////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 10/10/2024 09:12:03 AM
// Module Name: tb_carry_skip_adder
//////////////////////////////////////////////////////////////////////////////

module tb_carry_skip_adder;
    reg [3:0] a, b;
    reg c;
    wire [3:0] sum;
    wire cout;
    wire [4:0] total;

    carry_skip_adder uut (.a(a),.b(b),.c(c), .sum(sum), .cout(cout));
assign total = {cout,sum};

    initial begin

        $monitor("Time=%0t | a=%d, b=%d, c=%b | total=%d  | sum=%d, cout=%b", $time, a, b, c,total, sum, cout);
        a = 4'b0001; b = 4'b0010; c = 1'b0;
        #10;
        a = 4'b0110; b = 4'b0101; c = 1'b0;
        #10;
        a = 4'b1111; b = 4'b0001; c = 1'b1;
        #10;
        a = 4'b1010; b = 4'b0101; c = 1'b1;
        #10;
        a = 4'b1111; b = 4'b1111; c = 1'b0;
        #10;
        a = 4'b1100; b = 4'b0011; c = 1'b1;
        #10;

        $stop;
    end
endmodule
```

```
# }
# run 1000ns
Time=0    | a= 1, b= 2, c=0 | total= 3   | sum= 3, cout=0
Time=10000 | a= 6, b= 5, c=0 | total=11   | sum=11, cout=0
Time=20000 | a=15, b= 1, c=1 | total=17   | sum= 1, cout=1
Time=30000 | a=10, b= 5, c=1 | total=16   | sum= 0, cout=1
Time=40000 | a=15, b=15, c=0 | total=14   | sum=14, cout=0
Time=50000 | a=12, b= 3, c=1 | total=16   | sum= 0, cout=1
$stop called at time : 60 ns : File "/home/itzzinfinity/Cozy Drive/100day
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_carry_skip_adder_
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory
```

Type a Tcl command here