```verilog
1    `timescale 1ns / 1ps
2    //////////////////////////////////////////////////////////////////////
3    // Engineer: Anjan Prasad
4    // Create Date: 09/25/2024 11:40:15 AM
5    // Module Name: N_bit_comparator
6    //////////////////////////////////////////////////////////////////////
7
8
9    `timescale 1ns / 1ps
10
11   module N_bit_comparator(a, b, Lesser, Greater, Equal);
12       parameter N = 8;
13       input [N-1:0] a, b;
14       output reg Lesser, Greater, Equal;
15
16       always @(*) begin
17           Lesser  = (a < b);
18           Greater = (a > b);
19           Equal   = (a == b);
20       end
21
22   endmodule
23
```

```verilog
1    `timescale 1ns / 1ps
2    //////////////////////////////////////////////////////////////////////////////////
3    // Engineer: Anjan Prasad
4    // Create Date: 09/25/2024 11:40:15 AM
5    // Module Name: N_bit_comparator_tb
6    //////////////////////////////////////////////////////////////////////////////////
7
8
9    module N_bit_comp_tb;
10   reg [7:0] a,b;
11   wire Lesser,Greater,Equal;
12    N_bit_comparator DUT (a,b,Lesser,Greater,Equal);
13    initial begin
14        $display("in between  a   and  b     A_lessThan_B  A_greaterThan_B  A_equalTo_B ");
15        $monitor("            %d       %d    %b             %b                %b ", a, b,Lesser,Greater,Equal);
16   repeat(10) begin
17   #10
18        a= $random %8 ;
19        b= $random %8 ;
20
21   end
22   $finish;
23   end
24
25   endmodule
```

```
Tcl Console    x  Messages    Log

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# run 1000ns
in between   a    and   b    A_lessThan_B   A_greaterThan_B   A_equalTo_B
             x         x    x              x                 x
             4       249    1              0                 0
           249       251    1              0                 0
             5         5    0              0                 1
           253       250    0              1                 0
             1         5    1              0                 0
             6         5    0              1                 0
             5         4    0              1                 0
             1       254    1              0                 0
           253       250    0              1                 0
$finish called at time : 100 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_021/project_1/project_1.srcs/sim_1/new/N_bit_comp_tb.v" Line 36
INFO: [USF-XSim-96] XSim completed. Design snapshot 'N_bit_comp_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:09 ; elapsed = 00:00:06 . Memory (MB): peak = 9184.488 ; gain = 8.000 ; free physical = 205 ; free virtual = 1534

<

Type a Tcl command here
```