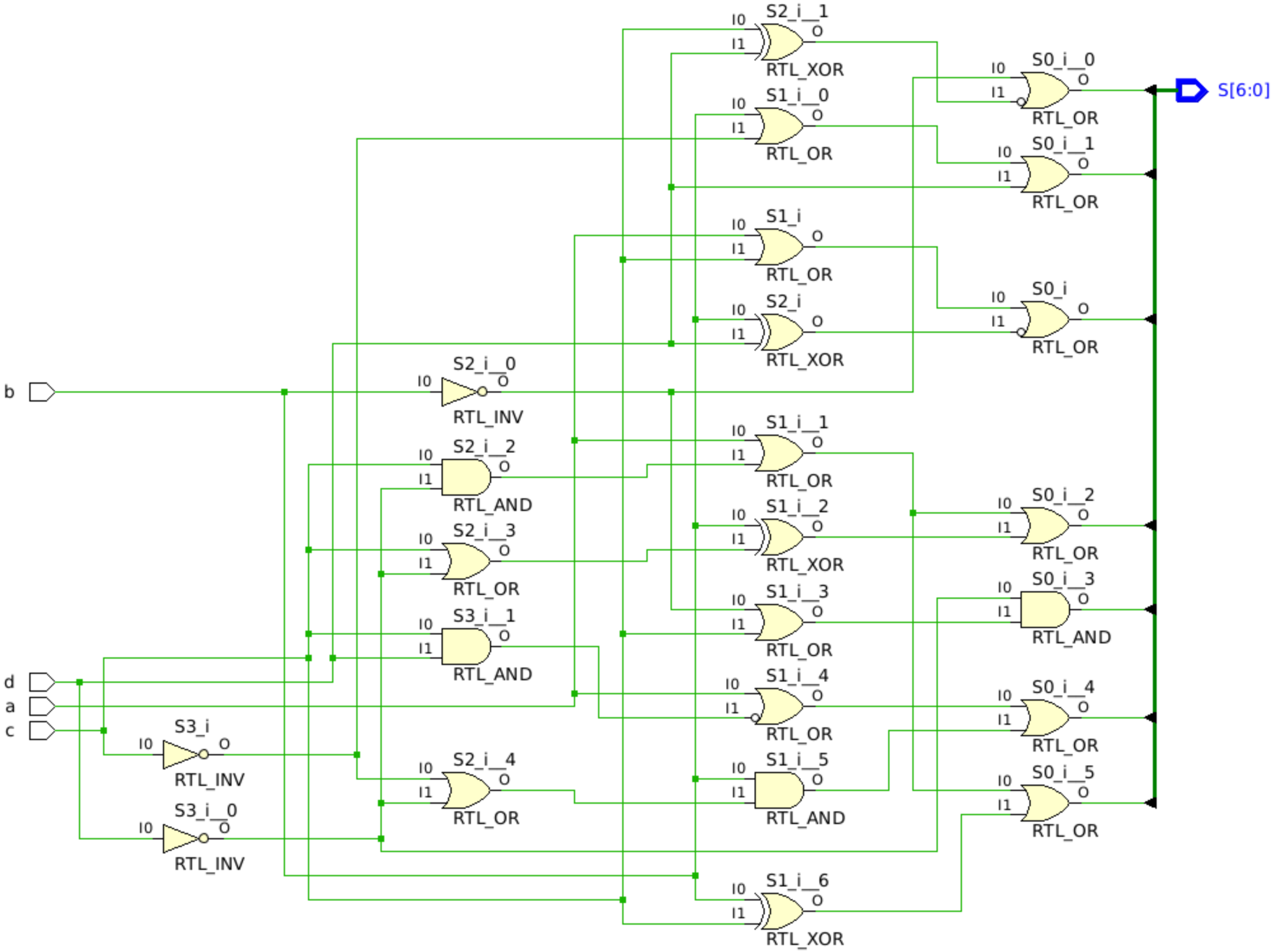
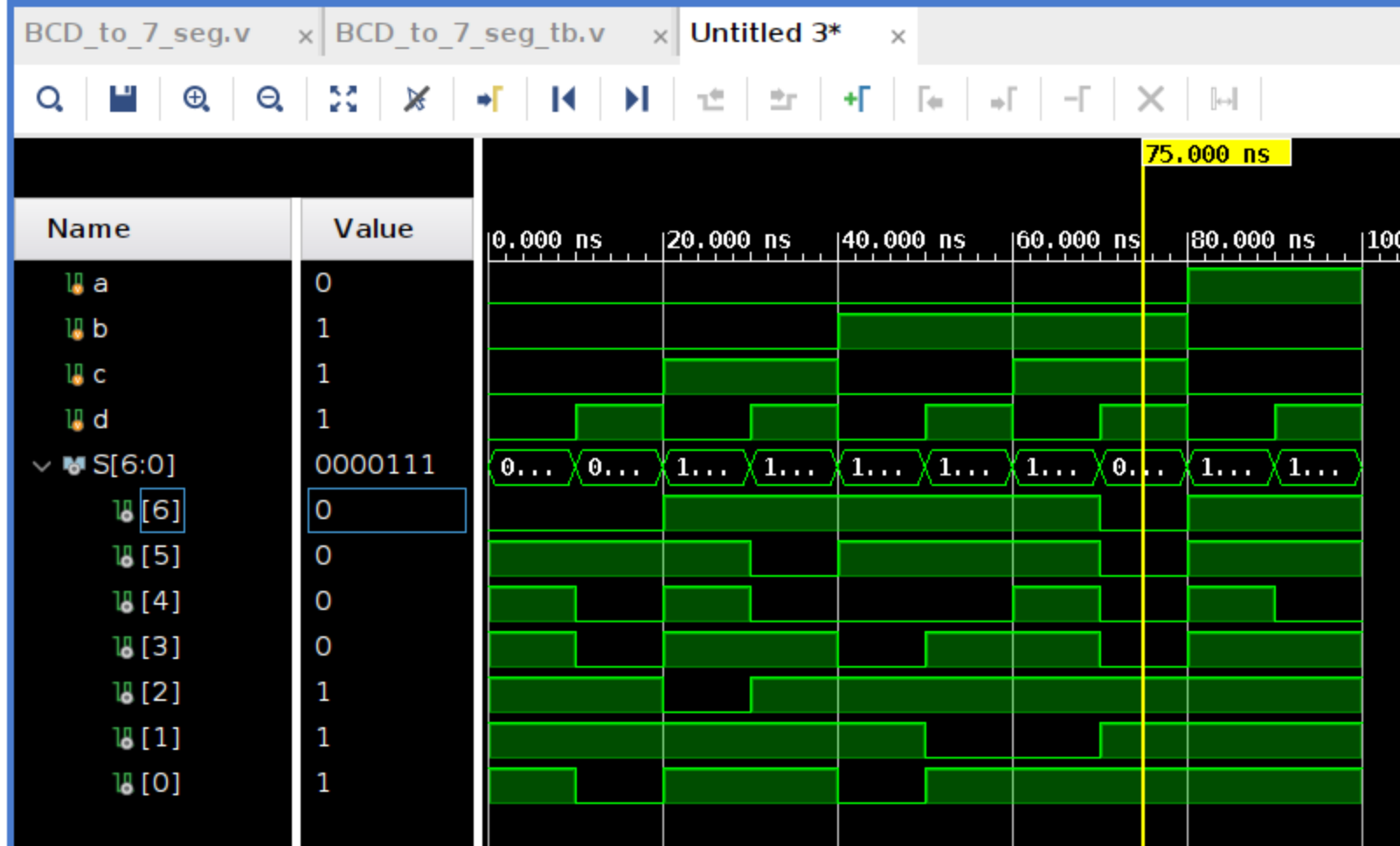

b
d
a
c
S2_i__0
RTL_INV
S2_i__2
RTL_AND
S2_i__3
RTL_OR
S3_i__1
RTL_AND
S3_i
RTL_INV
S3_i__0
RTL_INV
S2_i__4
RTL_OR
S2_i__1
RTL_XOR
S1_i__0
RTL_OR
S1_i
RTL_OR
S2_i
RTL_XOR
S1_i__1
RTL_OR
S1_i__2
RTL_XOR
S1_i__3
RTL_OR
S1_i__4
RTL_OR
S1_i__5
RTL_AND
S1_i__6
RTL_XOR
S0_i__0
RTL_OR
S0_i__1
RTL_OR
S0_i
RTL_OR
S0_i__2
RTL_OR
S0_i__3
RTL_AND
S0_i__4
RTL_OR
S0_i__5
RTL_OR
S[6:0]


BCD_to_7_seg.v
BCD_to_7_seg_tb.v
Untitled 3*
Name
Value
a
0
b
1
c
1
d
1
S[6:0]
0000111
[6]
0
[5]
0
[4]
0
[3]
0
[2]
1
[1]
1
[0]
1
75.000 ns
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
0...
0...
1...
1...
1...
1...
1...
0...
1...
1...

BCD_to_7_seg.v × BCD_to_7_seg_tb.v * × Untitled 3* ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_045/project_1/project_1.srcs/sources_1/new/BCD_to_7_seg.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/05/2024 05:54:37 AM
5  // Module Name: BCD_to_7_seg
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module BCD_to_7_seg(
9  input a,b,c,d,
10 output [6:0]S);
11 assign S[0] = a|c|(~(b^d));
12 assign S[1] = ~b|~(c^d);
13 assign S[2] = b|(~c)|d;
14 assign S[3] = a|(c&~d)|b^(c|~d);
15 assign S[4] = ~d&(~b|c);
16 assign S[5] = a|~(c&d)|b&(~c|~d);
17 assign S[6] = a|(c&~d)|(b^c);
18 endmodule
19
```

BCD_to_7_seg.v | BCD_to_7_seg_tb.v * | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_045/project_1/project_1.srcs/sim_1/new/BCD_to_7_seg_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/05/2024 06:01:21 AM
5   // Module Name: BCD_to_7_seg_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module BCD_to_7_seg_tb;
10  reg a,b,c,d;
11  wire [6:0]S;
12
13
14  BCD_to_7_seg DUT (a,b,c,d,S);
15
16  initial begin
17      {a,b,c,d}=4'd0;
18      #10  {a,b,c,d}=4'd1;
19      #10  {a,b,c,d}=4'd2;
20      #10  {a,b,c,d}=4'd3;
21      #10  {a,b,c,d}=4'd4;
22      #10  {a,b,c,d}=4'd5;
23      #10  {a,b,c,d}=4'd6;
24      #10  {a,b,c,d}=4'd7;
25      #10  {a,b,c,d}=4'd8;
26      #10  {a,b,c,d}=4'd9;
27      #10  $finish;
28
29  end
30
31  endmodule
```