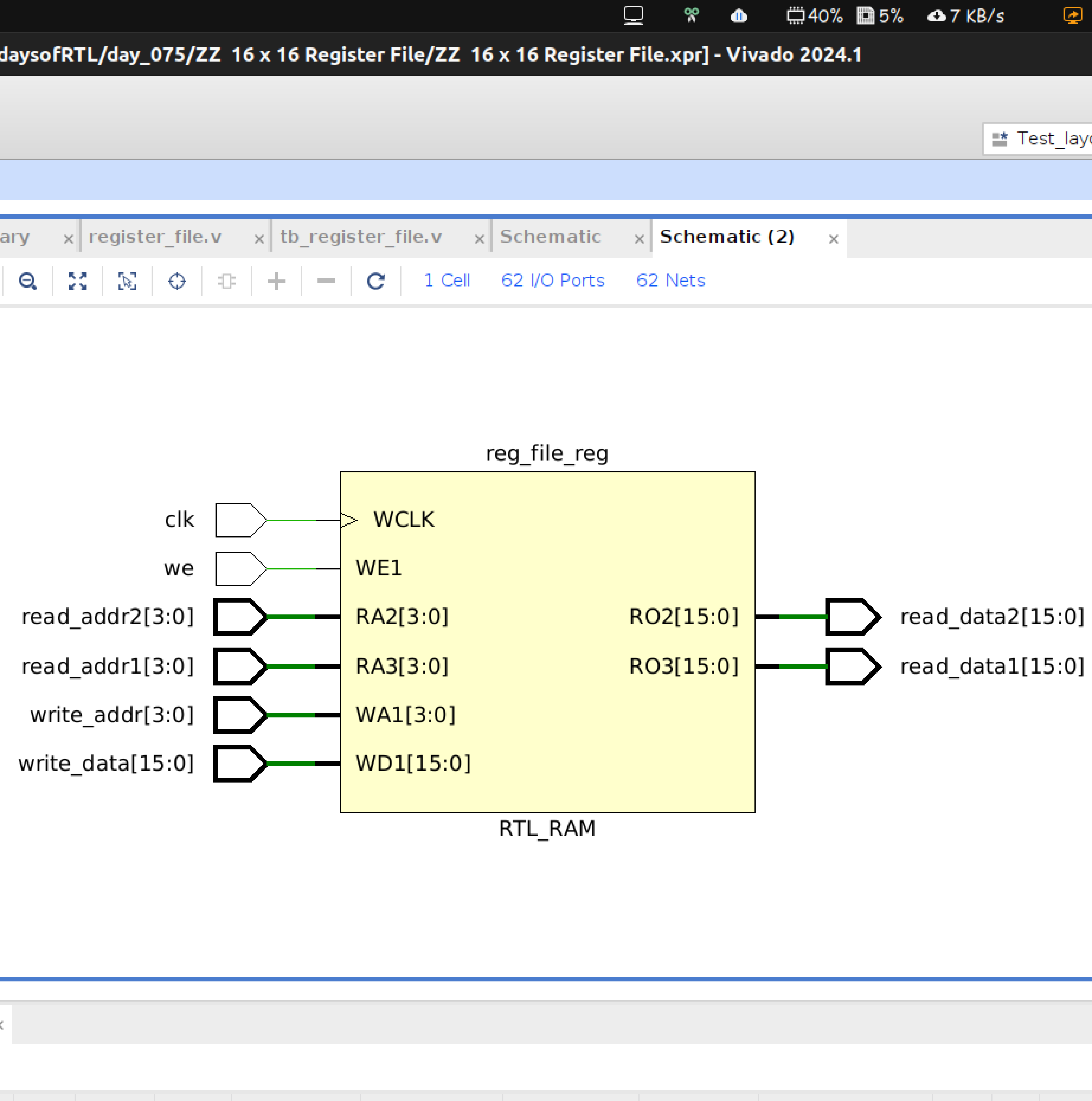
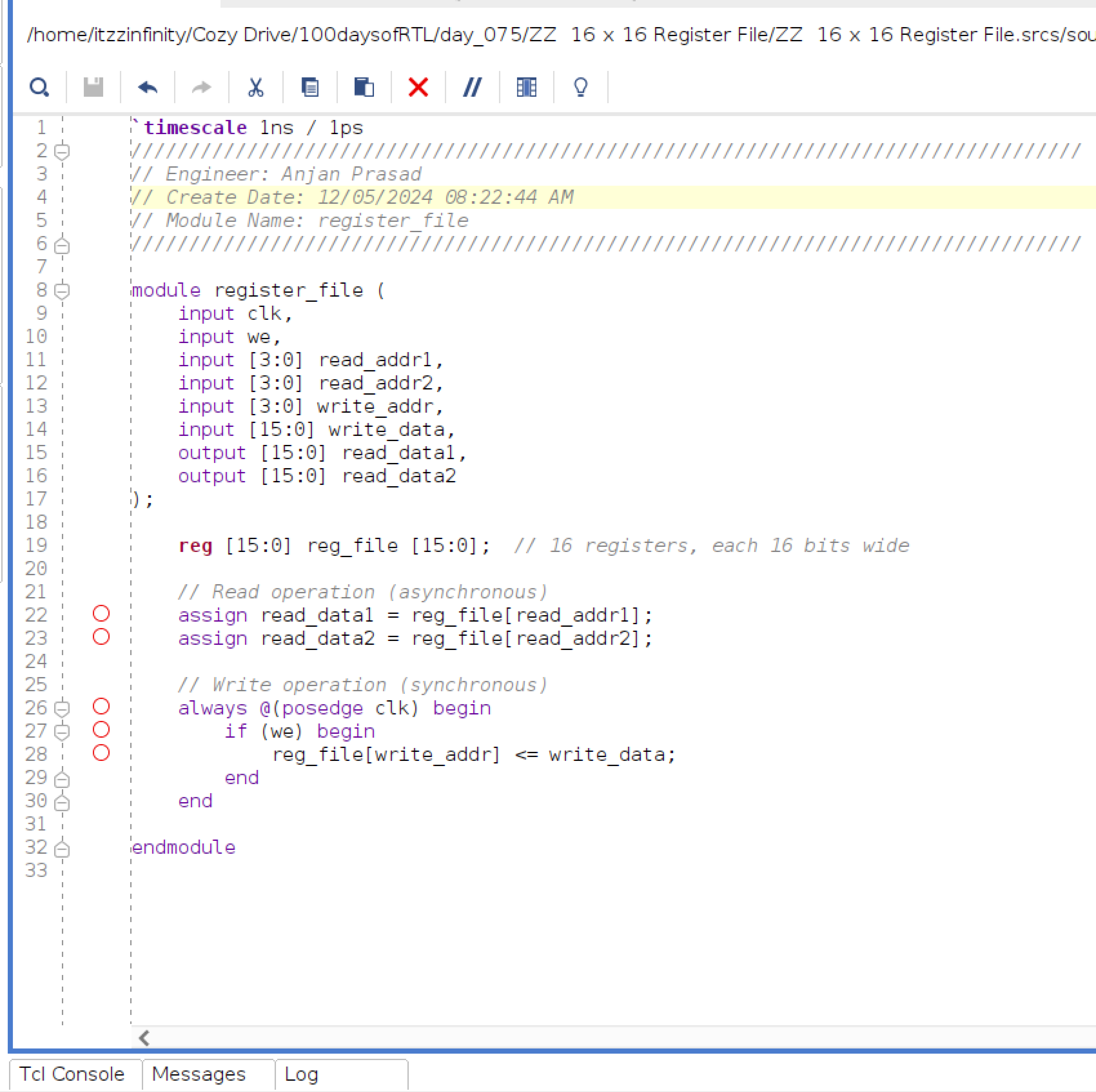
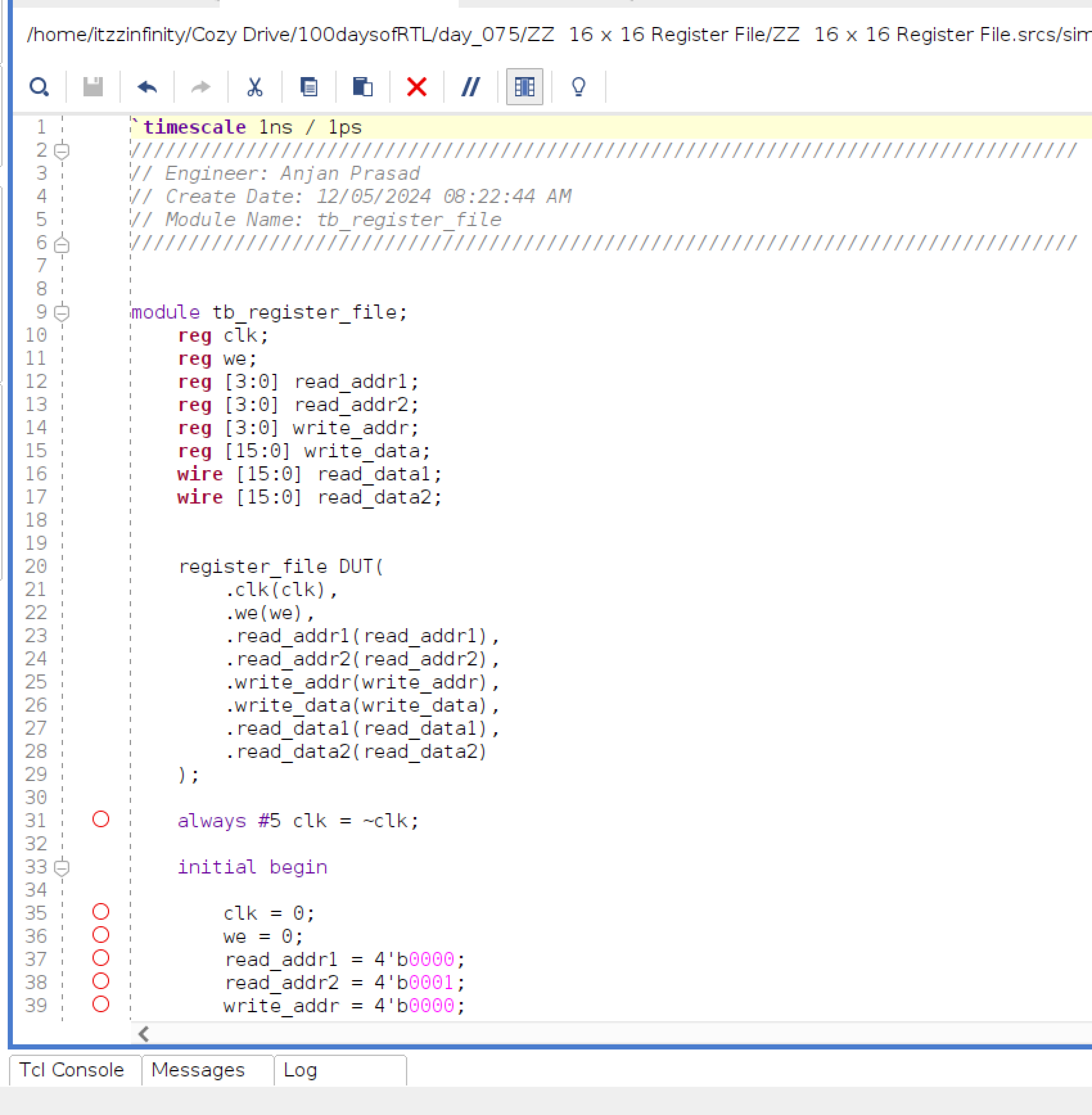

daysofRTL/day_075/ZZ 16 x 16 Register File/ZZ 16 x 16 Register File.xpr] - Vivado 2024.1

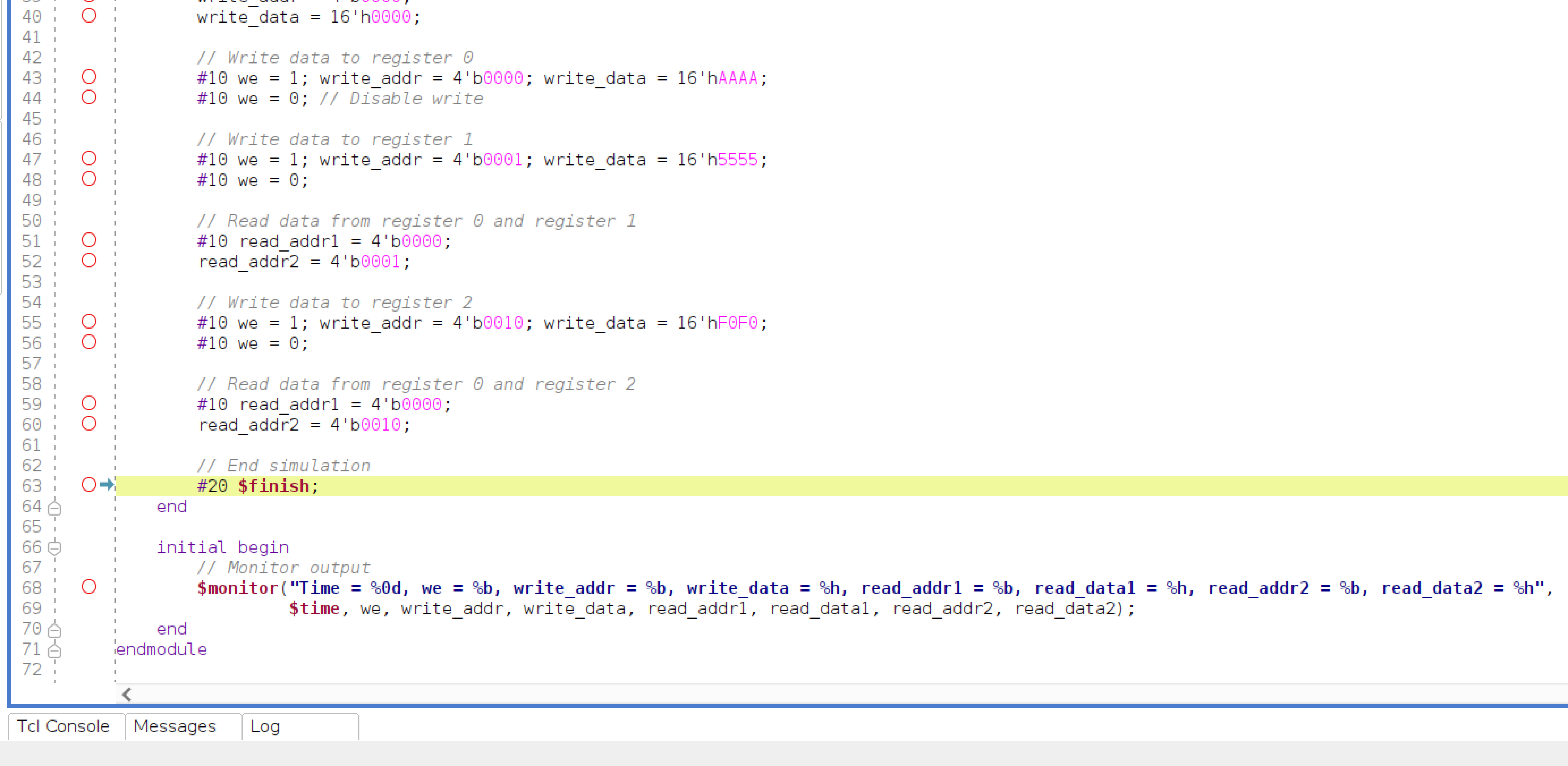

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_075/ZZ 16 x 16 Register File/ZZ 16 x 16 Register File.srcs/sou
Tcl Console
Messages
Log

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/05/2024 08:22:44 AM
// Module Name: register_file
//////////////////////////////////////////////////////////////////////////////////

module register_file (
    input clk,
    input we,
    input [3:0] read_addr1,
    input [3:0] read_addr2,
    input [3:0] write_addr,
    input [15:0] write_data,
    output [15:0] read_data1,
    output [15:0] read_data2
);

    reg [15:0] reg_file [15:0];  // 16 registers, each 16 bits wide

    // Read operation (asynchronous)
    assign read_data1 = reg_file[read_addr1];
    assign read_data2 = reg_file[read_addr2];

    // Write operation (synchronous)
    always @(posedge clk) begin
        if (we) begin
            reg_file[write_addr] <= write_data;
        end
    end

endmodule
```

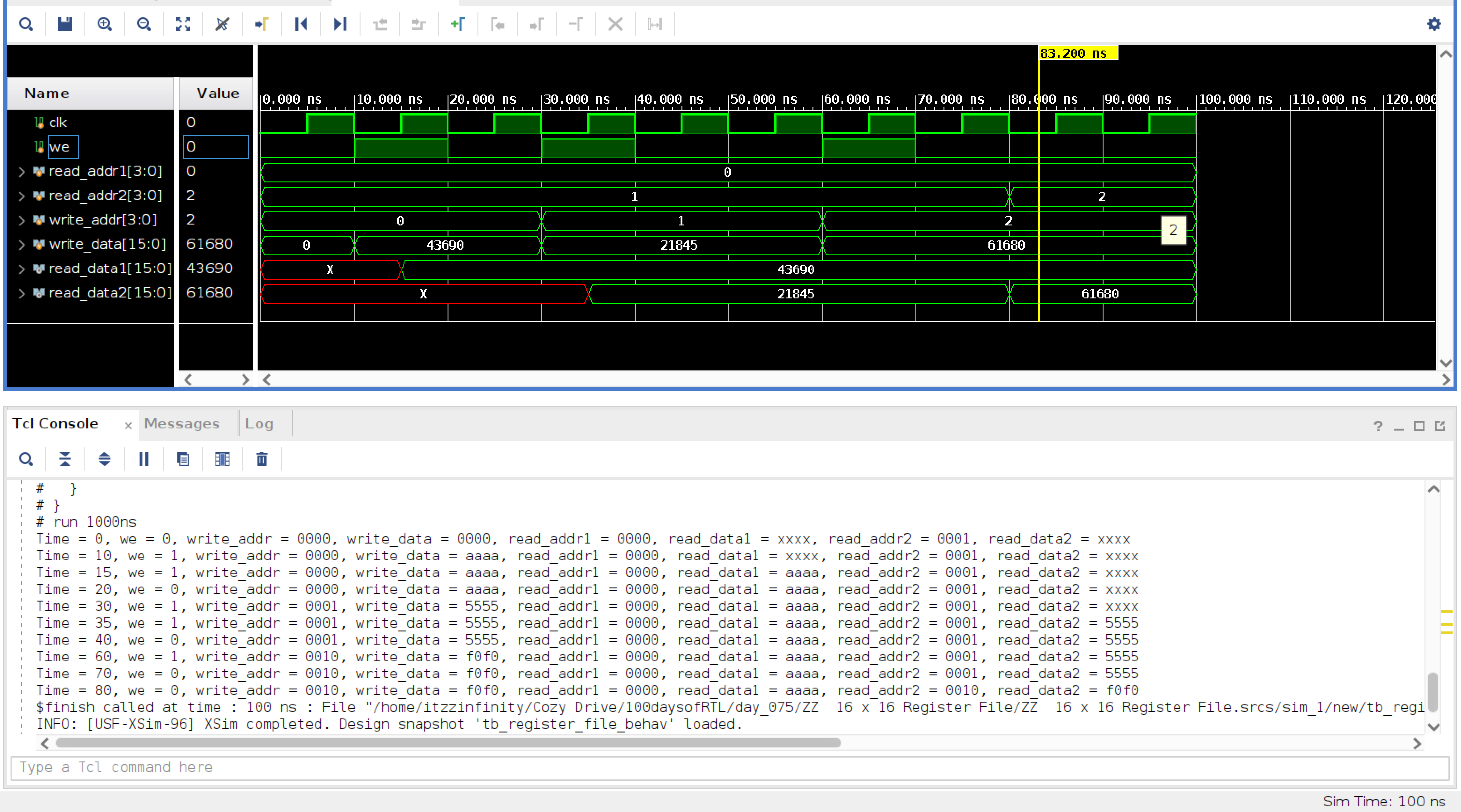


/home/itzzinfinity/Cozy Drive/100daysofRTL/day_075/ZZ 16 x 16 Register File/ZZ 16 x 16 Register File.srcs/sim

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/05/2024 08:22:44 AM
// Module Name: tb_register_file
//////////////////////////////////////////////////////////////////////////////////


module tb_register_file;
    reg clk;
    reg we;
    reg [3:0] read_addr1;
    reg [3:0] read_addr2;
    reg [3:0] write_addr;
    reg [15:0] write_data;
    wire [15:0] read_data1;
    wire [15:0] read_data2;


    register_file DUT(
        .clk(clk),
        .we(we),
        .read_addr1(read_addr1),
        .read_addr2(read_addr2),
        .write_addr(write_addr),
        .write_data(write_data),
        .read_data1(read_data1),
        .read_data2(read_data2)
    );

    always #5 clk = ~clk;

    initial begin

        clk = 0;
        we = 0;
        read_addr1 = 4'b0000;
        read_addr2 = 4'b0001;
        write_addr = 4'b0000;
```



```
        write_addr = 4'b0000;
        write_data = 16'h0000;

        // Write data to register 0
        #10 we = 1; write_addr = 4'b0000; write_data = 16'hAAAA;
        #10 we = 0; // Disable write

        // Write data to register 1
        #10 we = 1; write_addr = 4'b0001; write_data = 16'h5555;
        #10 we = 0;

        // Read data from register 0 and register 1
        #10 read_addr1 = 4'b0000;
        read_addr2 = 4'b0001;

        // Write data to register 2
        #10 we = 1; write_addr = 4'b0010; write_data = 16'hF0F0;
        #10 we = 0;

        // Read data from register 0 and register 2
        #10 read_addr1 = 4'b0000;
        read_addr2 = 4'b0010;

        // End simulation
        #20 $finish;
    end

    initial begin
        // Monitor output
        $monitor("Time = %0d, we = %b, write_addr = %b, write_data = %h, read_addr1 = %b, read_data1 = %h, read_addr2 = %b, read_data2 = %h",
                 $time, we, write_addr, write_data, read_addr1, read_data1, read_addr2, read_data2);
    end
endmodule
```



```
#   }
# }
# run 1000ns
Time = 0, we = 0, write_addr = 0000, write_data = 0000, read_addr1 = 0000, read_data1 = xxxx, read_addr2 = 0001, read_data2 = xxxx
Time = 10, we = 1, write_addr = 0000, write_data = aaaa, read_addr1 = 0000, read_data1 = xxxx, read_addr2 = 0001, read_data2 = xxxx
Time = 15, we = 1, write_addr = 0000, write_data = aaaa, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0001, read_data2 = xxxx
Time = 20, we = 0, write_addr = 0000, write_data = aaaa, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0001, read_data2 = xxxx
Time = 30, we = 1, write_addr = 0001, write_data = 5555, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0001, read_data2 = xxxx
Time = 35, we = 1, write_addr = 0001, write_data = 5555, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0001, read_data2 = 5555
Time = 40, we = 0, write_addr = 0001, write_data = 5555, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0001, read_data2 = 5555
Time = 60, we = 1, write_addr = 0010, write_data = f0f0, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0001, read_data2 = 5555
Time = 70, we = 0, write_addr = 0010, write_data = f0f0, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0001, read_data2 = 5555
Time = 80, we = 0, write_addr = 0010, write_data = f0f0, read_addr1 = 0000, read_data1 = aaaa, read_addr2 = 0010, read_data2 = f0f0
$finish called at time : 100 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_075/ZZ  16 x 16 Register File/ZZ  16 x 16 Register File.srcs/sim_1/new/tb_regi
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_register_file_behav' loaded.
```