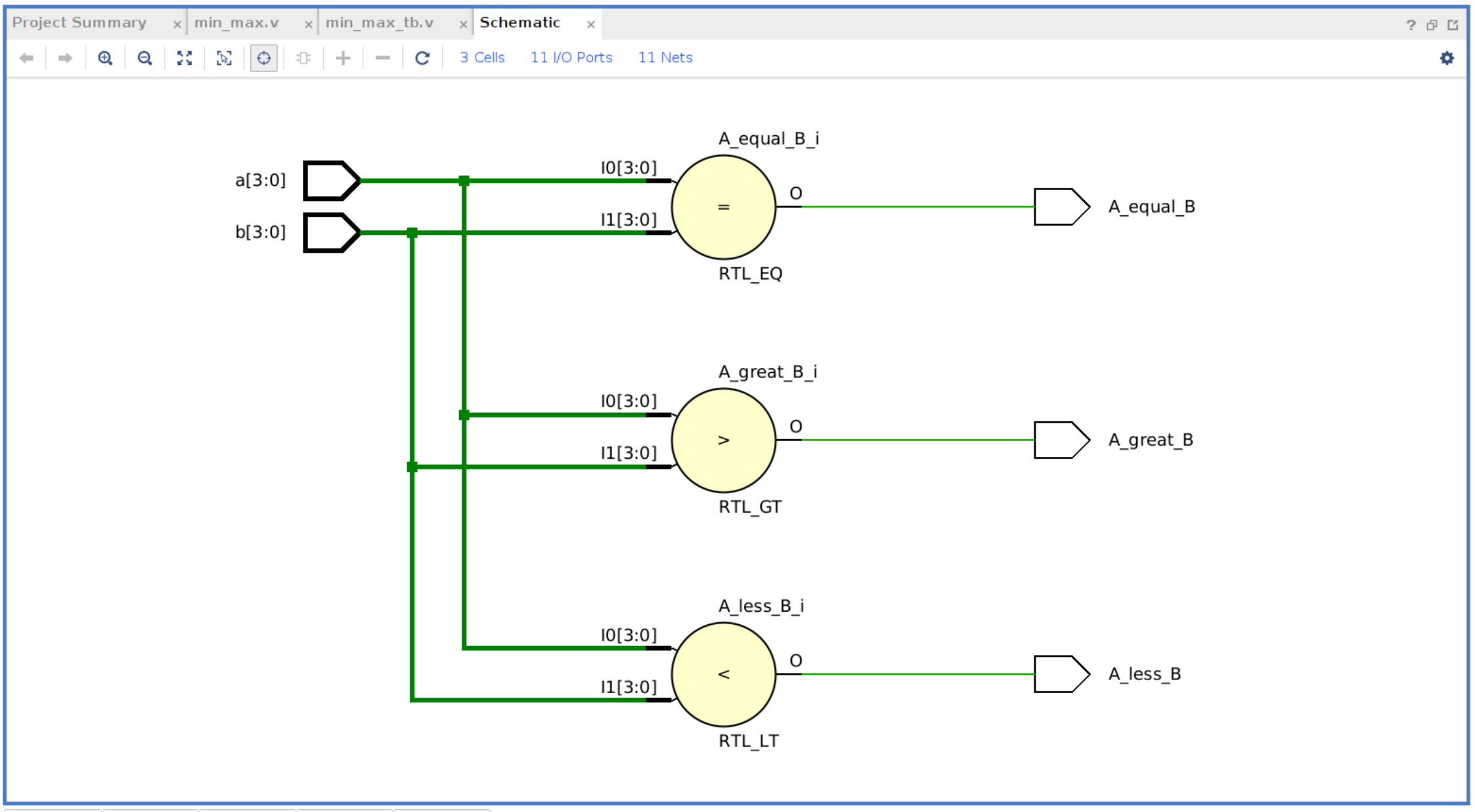
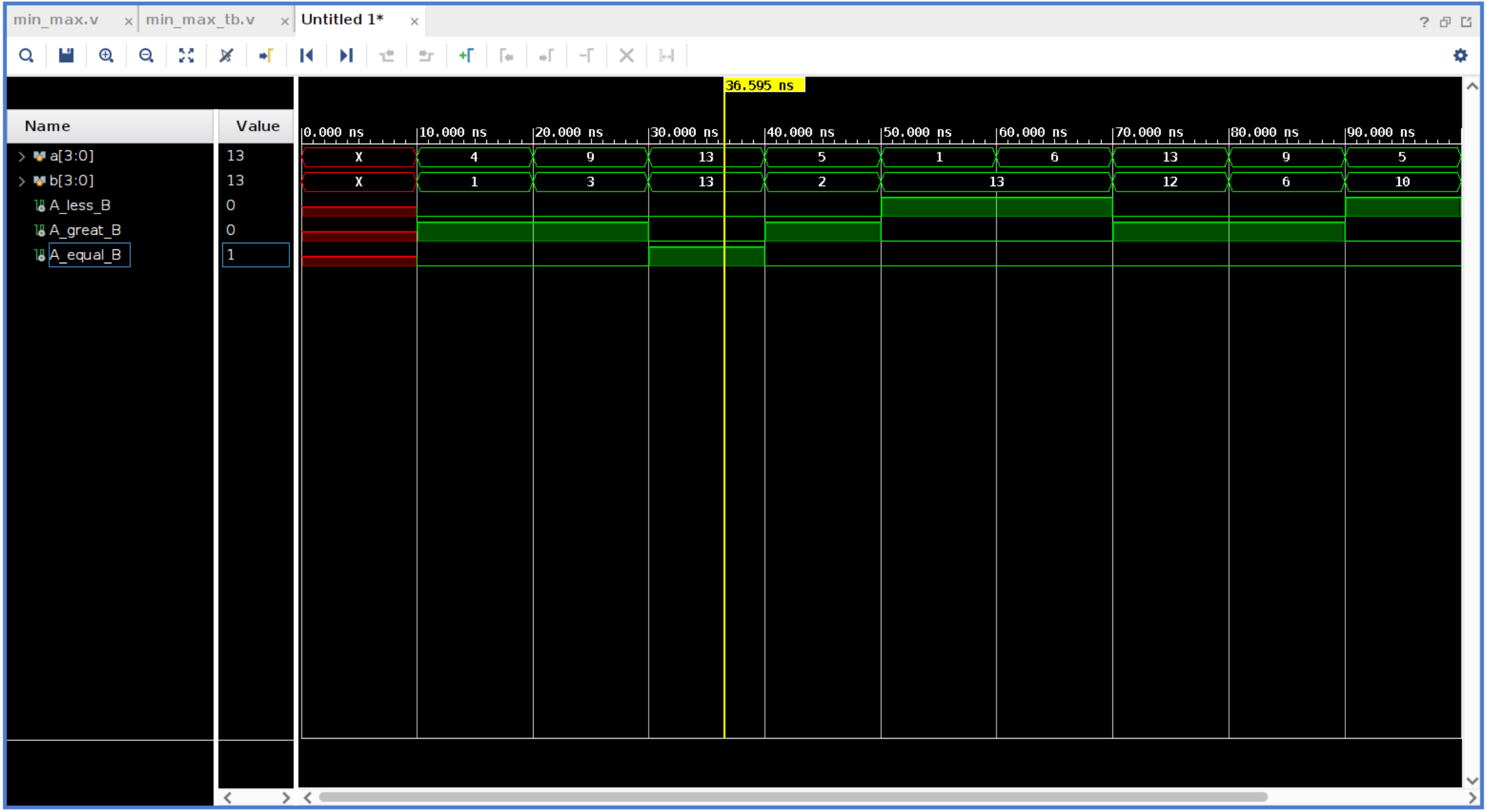

Project Summary
min_max.v
min_max_tb.v
Schematic
3 Cells
11 I/O Ports
11 Nets
a[3:0]
b[3:0]
A_equal_B_i
I0[3:0]
I1[3:0]
=
O
RTL_EQ
A_equal_B
A_great_B_i
I0[3:0]
I1[3:0]
>
O
RTL_GT
A_great_B
A_less_B_i
I0[3:0]
I1[3:0]
<
O
RTL_LT
A_less_B


min_max.v
min_max_tb.v
Untitled 1*
Name
Value
a[3:0]
13
b[3:0]
13
A_less_B
0
A_great_B
0
A_equal_B
1
36.595 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
X 4 9 13 5 1 6 13 9 5
X 1 3 13 2 13 12 6 10

Tcl Console | Messages | Log

```
#   }
# }
# run 1000ns
in between  a  and  b    A_lessThan_B  A_greaterThan_B  A_equalTo_B
             x       x    x             x                x
             4       1    0             1                0
             9       3    0             1                0
            13      13    0             0                1
             5       2    0             1                0
             1      13    1             0                0
             6      13    1             0                0
            13      12    0             1                0
             9       6    0             1                0
             5      10    1             0                0
$finish called at time : 100 ns : File "/home/itzzinfinity/Cozy Drive/100daysofF
INFO: [USF-XSim-96] XSim completed. Design snapshot 'min_max_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB):
```

min_max.v | min_max_tb.v | Untitled 1*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_015/project_1/project_1.srcs/sources_1/new/min_max.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Engineer: Anjan Prasad
3  // Create Date: 10/06/2024 10:25:08 AM
4  // Module Name: min_max
5  //////////////////////////////////////////////////////////////////////////////////
6
7  module min_max(
8      input [3:0] a,b,
9      output A_less_B,A_great_B,A_equal_B
10 );
11
12 assign A_great_B = (a>b)?1'b1:1'b0;
13 assign A_less_B = (a<b)?1'b1:1'b0;
14 assign A_equal_B = (a==b)?1'b1:1'b0;
15 endmodule
16
17
18
19
20
21
22
```

min_max.v | min_max_tb.v | Untitled 1*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_015/project_1/project_1.srcs/sim_1/new/min_max_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/06/2024 10:25:08 AM
5   // Module Name: min_max_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module min_max_tb;
10  reg [3:0] a,b;
11  wire A_less_B,A_great_B,A_equal_B;
12   min_max DUT (a,b,A_less_B,A_great_B,A_equal_B);
13   initial begin
14          $display("in between  a  and  b    A_lessThan_B  A_greaterThan_B  A_equalTo_B ");
15          $monitor("           %d      %d    %b            %b                %b ", a, b,A_less_B,A_great_B,A_equal_B);
16  repeat(10) begin
17  #10
18          a= $random %16 ;
19          b= $random %16 ;
20
21  end
22  $finish;
23  end
24
25  endmodule
26
```