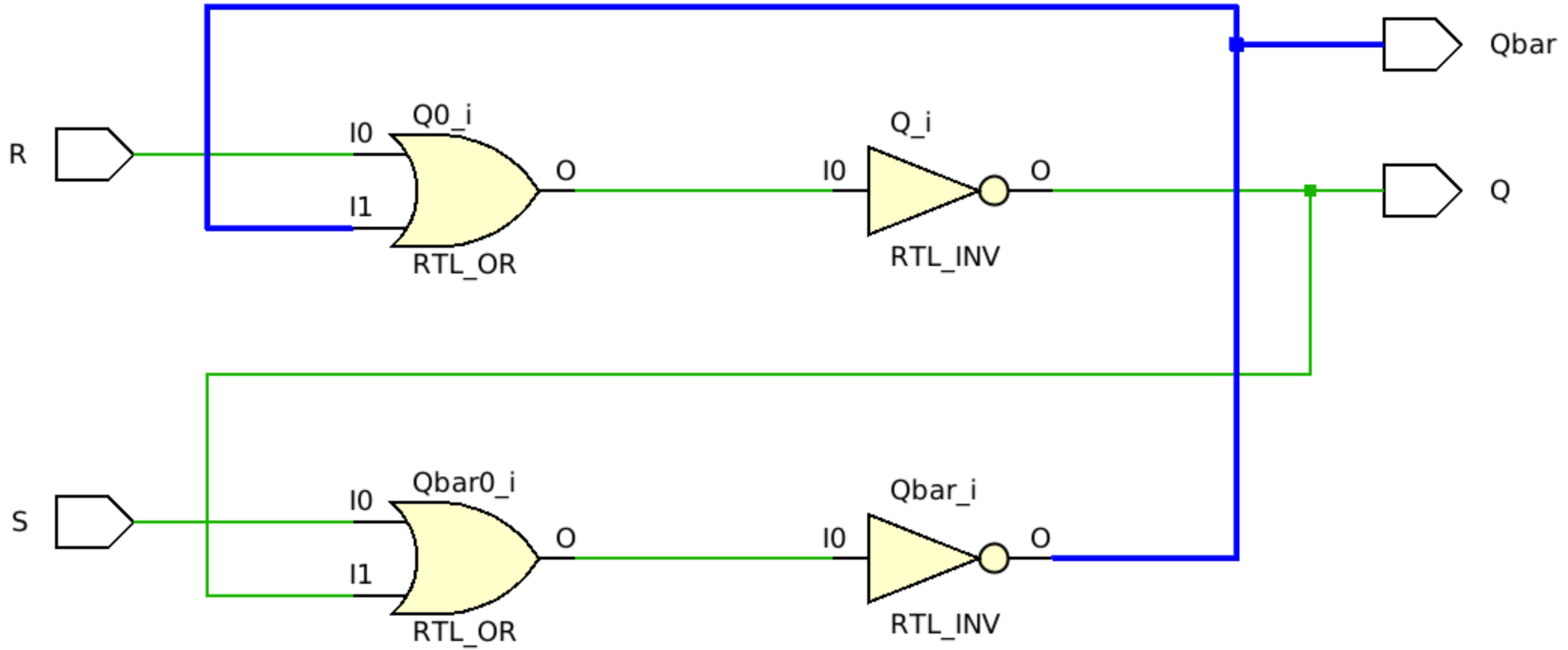
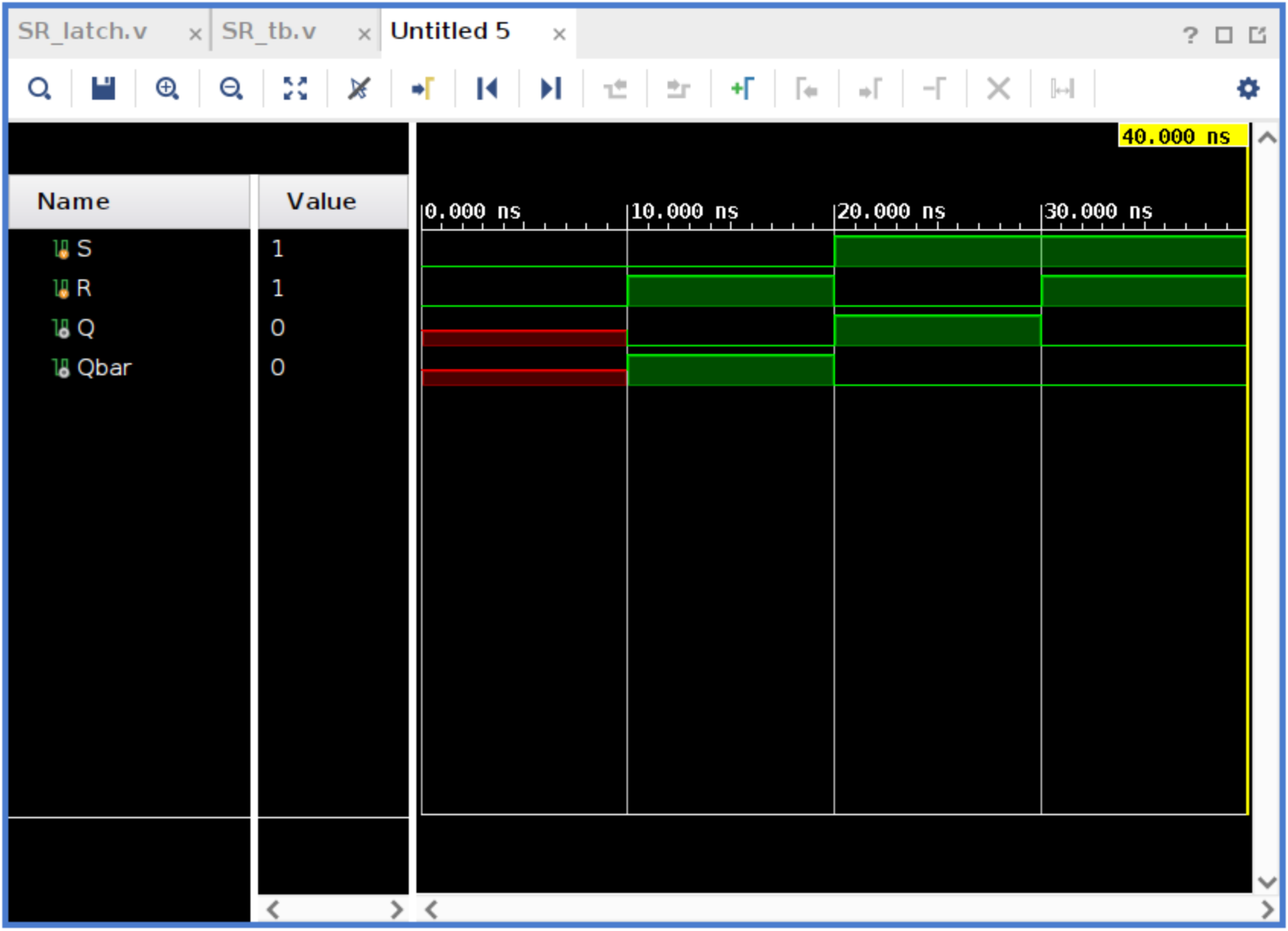
Project Summary | SR_latch.v | Schematic

4 Cells | 4 I/O Ports | 6 Nets




SR_latch.v
SR_tb.v
Untitled 5
Name
Value
S
1
R
1
Q
0
Qbar
0
40.000 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns

SR_latch.v | SR_tb.v | Untitled 5

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_046/project_1/project_1.srcs/sources_1/new/SR_latch.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/06/2024 06:17:44 AM
5  // Module Name: SR_latch
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module SR_latch(
10 input S,R,
11 output Q,Qbar
12     );
13
14     assign Q = ~ (R | Qbar);
15     assign Qbar = ~ (S | Q);
16
17
18 endmodule
19
```

SR_latch.v | SR_tb.v | Untitled 5

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_046/project_1/project_1.srcs/sim_1/new/SR_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/06/2024 06:21:28 AM
5  // Module Name: SR_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module SR_tb;
10  reg S,R;
11 wire Q,Qbar;
12
13 SR_latch DUT(S,R,Q,Qbar);
14  initial begin
15 S = 0 ; R = 0;
16 #10 S = 0 ; R = 1;
17 #10 S = 1 ; R = 0;
18 #10 S = 1 ; R = 1;
19 #10 $finish;
20 end
21 endmodule
22
```