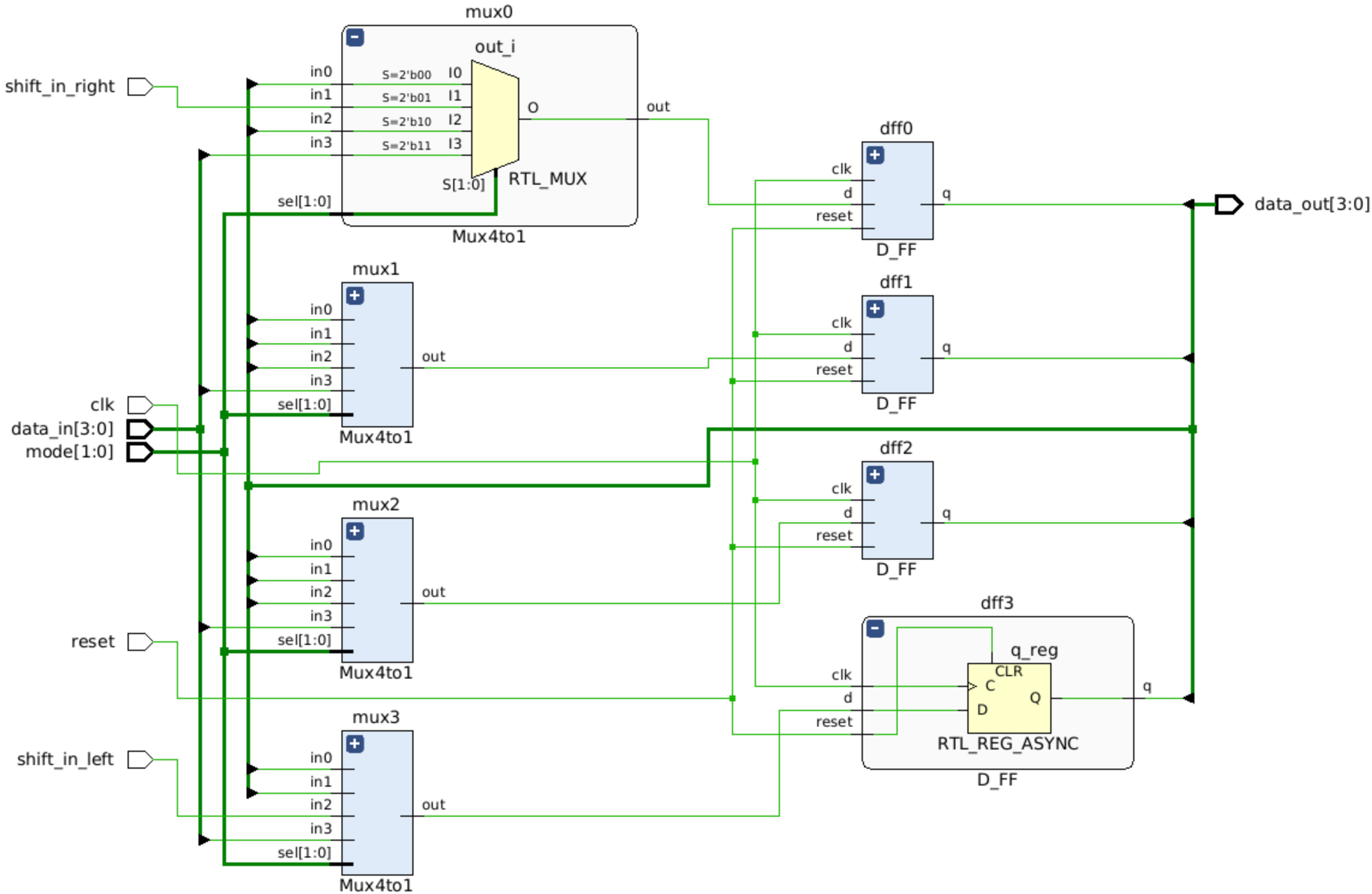
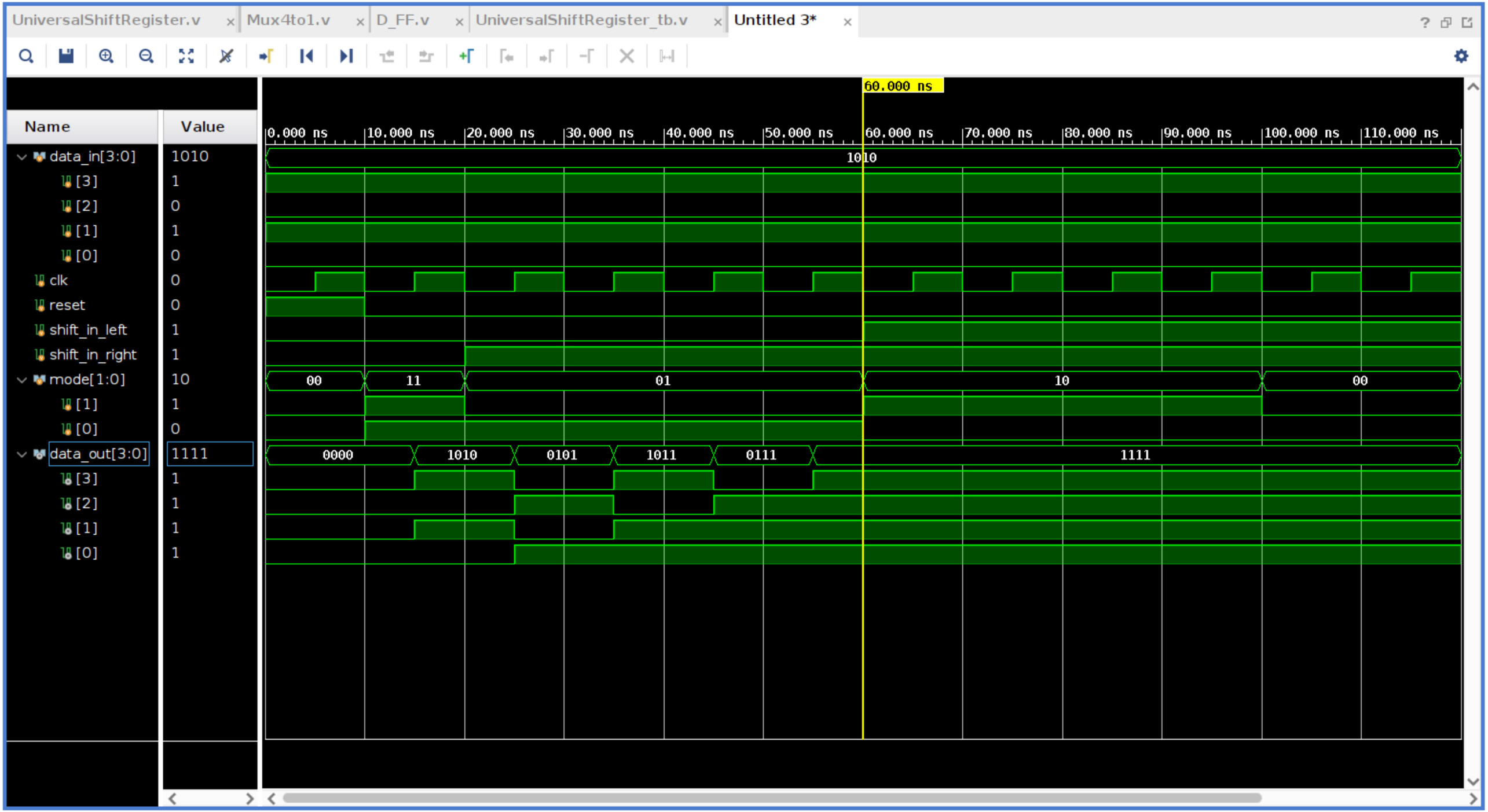
10 Cells 14 I/O Ports 29 Nets




UniversalShiftRegister.v
Mux4to1.v
D_FF.v
UniversalShiftRegister_tb.v
Untitled 3*
Name
Value
data_in[3:0]
1010
[3]
1
[2]
0
[1]
1
[0]
0
clk
0
reset
0
shift_in_left
1
shift_in_right
1
mode[1:0]
10
[1]
1
[0]
0
data_out[3:0]
1111
[3]
1
[2]
1
[1]
1
[0]
1
60.000 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
100.000 ns
110.000 ns
1010
00
11
01
10
00
0000
1010
0101
1011
0111
1111

UniversalShiftRegister.v | Mux4to1.v | D_FF.v | UniversalShiftRegister_tb.v | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_061/project_1/project_1.srcs/sources_1/new/UniversalShiftRegister.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 11/21/2024 08:55:45 AM
// Module Name: UniversalShiftRegister
//////////////////////////////////////////////////////////////////////////////////


module UniversalShiftRegister (
    input wire [3:0] data_in,
    input wire clk, reset,
    input wire shift_in_left,
    input wire shift_in_right,
    input wire [1:0] mode,          // Mode select: 00-Hold, 01-Shift Right, 10-Shift Left, 11-Parallel Load
    output wire [3:0] data_out
);

    wire [3:0] mux_out;             // Outputs of the multiplexers
    wire [3:0] q;                   // Outputs of the D flip-flops

    Mux4to1 mux0 (.in0(q[0]), .in1(shift_in_right), .in2(q[1]), .in3(data_in[0]), .sel(mode), .out(mux_out[0]));
    Mux4to1 mux1 (.in0(q[1]), .in1(q[0]), .in2(q[2]), .in3(data_in[1]), .sel(mode), .out(mux_out[1]));
    Mux4to1 mux2 (.in0(q[2]), .in1(q[1]), .in2(q[3]), .in3(data_in[2]), .sel(mode), .out(mux_out[2]));
    Mux4to1 mux3 (.in0(q[3]), .in1(q[2]), .in2(shift_in_left), .in3(data_in[3]), .sel(mode), .out(mux_out[3]));

    D_FF dff0 (.d(mux_out[0]), .clk(clk), .reset(reset), .q(q[0]));
    D_FF dff1 (.d(mux_out[1]), .clk(clk), .reset(reset), .q(q[1]));
    D_FF dff2 (.d(mux_out[2]), .clk(clk), .reset(reset), .q(q[2]));
    D_FF dff3 (.d(mux_out[3]), .clk(clk), .reset(reset), .q(q[3]));

    assign data_out = q;

endmodule
```

UniversalShiftRegister.v | Mux4to1.v | D_FF.v | **UniversalShiftRegister_tb.v** | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_061/project_1/project_1.srcs/sim_1/new/UniversalShiftRegister_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/21/2024 09:01:48 AM
5  // Module Name: UniversalShiftRegister_tb
6  //////////////////////////////////////////////////////////////////////////////////
7  module UniversalShiftRegister_tb;
8
9      reg [3:0] data_in;
10     reg clk, reset, shift_in_left, shift_in_right;
11     reg [1:0] mode;
12     wire [3:0] data_out;
13
14     UniversalShiftRegister UUT (
15         .data_in(data_in),.clk(clk),.reset(reset),.shift_in_left(shift_in_left),.shift_in_right(shift_in_right),.mode(mode),.data_out(data_out)
16     );
17     initial begin
18         clk = 0;
19         forever #5 clk = ~clk; // 10 ns clock period
20     end
21
22     initial begin
23         // Initialize inputs
24         reset = 1; shift_in_left = 0; shift_in_right = 0; data_in = 4'b1010; mode = 2'b00;
25         // Reset the register
26         #10 reset = 0;
27         // Parallel load
28         mode = 2'b11; #10;
29         // Shift Right
30         mode = 2'b01; shift_in_right = 1; #40;
31         // Shift Left
32         mode = 2'b10; shift_in_left = 1; #40;
33         // Hold
34         mode = 2'b00; #20;
35         $stop;
36     end
37
38 endmodule
39
```

UniversalShiftRegister.v | Mux4to1.v | D_FF.v | UniversalShiftRegister_tb.v | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_061/project_1/project_1.srcs/sources_1/new/D_FF.v

```
1   module D_FF (
2       input wire d, clk, reset,
3       output reg q
4   );
5       always @(posedge clk or posedge reset) begin
6           if (reset)
7               q <= 1'b0;
8           else
9               q <= d;
10      end
11  endmodule
12
```

UniversalShiftRegister.v | Mux4to1.v | D_FF.v | UniversalShiftRegister_tb.v | Untitled 3*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_061/project_1/project_1.srcs/sources_1/new/Mux4to1.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/21/2024 08:58:36 AM
5  // Module Name: Mux4to1
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module Mux4to1 (
10     input wire in0, in1, in2, in3,
11     input wire [1:0] sel,
12     output reg out
13 );
14     always @(*) begin
15         case (sel)
16             2'b00: out = in0; // Hold
17             2'b01: out = in1; // Shift Right
18             2'b10: out = in2; // Shift Left
19             2'b11: out = in3; // Parallel Load
20             default: out = in0;
21         endcase
22     end
23 endmodule
24
25
```