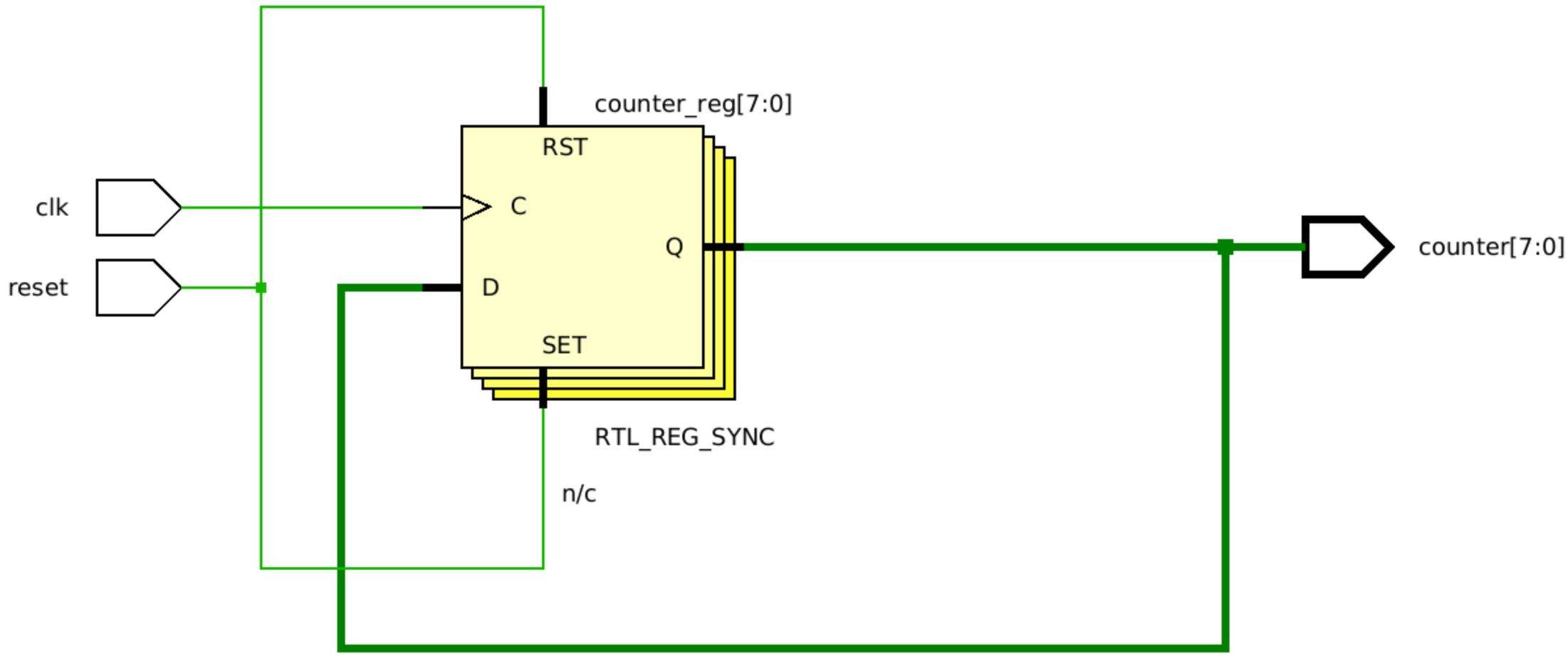
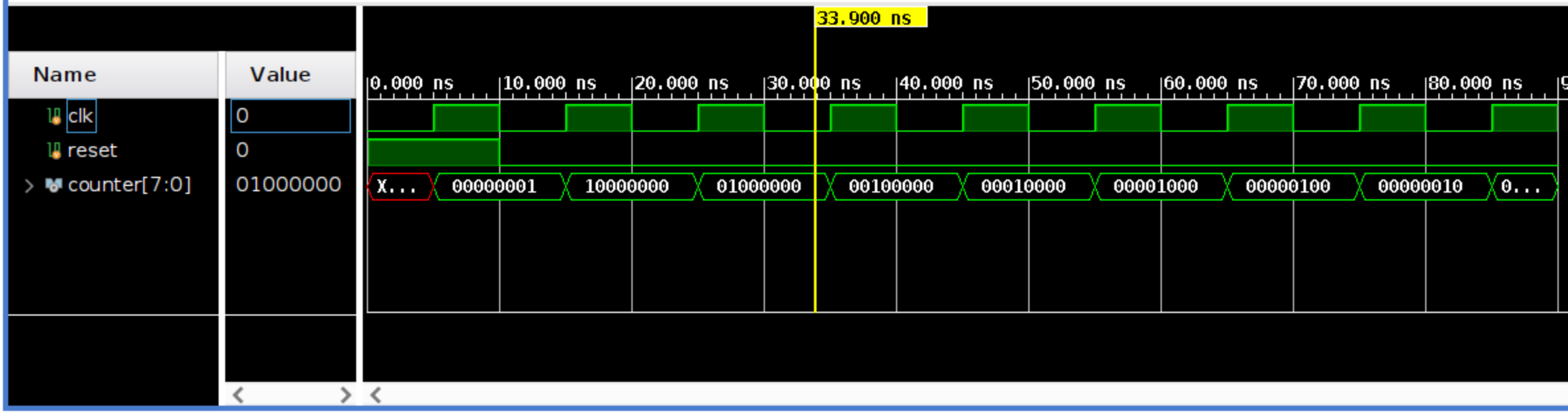
8 Cells 10 I/O Ports 10 Nets



ring_counter.v | ring_counter_tb.v | Untitled 6*



Tcl Console | Messages | Log

```
#      send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to op
#   }
# }
# run 1000ns
          counter:   x
          counter:   1
          counter: 128
          counter:  64
          counter:  32
          counter:  16
          counter:   8
          counter:   4
          counter:   2
          counter:   1
$finish called at time : 90 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_068/project_1/project_1.srcs/sim_1/new/rin
INFO: [USF-XSim-96] XSim completed. Design snapshot 'ring_counter_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:05 . Memory (MB): peak = 9114.918 ; gain = 9.996 ; free physical =
```

Type a Tcl command here

Project Summary | ring_counter.v | ring_counter_tb.v | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_068/project_1/project_1.srcs/sources_1/new/ring_counter.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/28/2024 08:58:07 AM
5  // Module Name: ring_counter
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module ring_counter #(parameter N=8)
10     (input clk, reset,
11     output reg [N-1:0] counter );
12
13 always @(posedge clk)
14     begin
15
16     if (reset)
17         counter <= 1;
18
19     else
20         counter <= {counter[0], counter[N-1:1]};
21
22     end
23 endmodule
24
```

Tcl Console | Messages | Log | Reports | Design Runs

Project Summary | ring_counter.v | ring_counter_tb.v | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_068/project_1/project_1.srcs/sim_1/new/ring_counter_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/28/2024 04:45:04 AM
5  // Module Name: ring_counter_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module ring_counter_tb;
9  parameter N=8;
10
11 reg clk, reset;
12 wire [N-1:0] counter;
13
14 ring_counter DUT(clk, reset, counter);
15
16 initial begin
17     clk= 1'b0;
18     forever #5 clk= ~clk;
19     end
20
21 initial begin
22     reset = 1;
23     #10;
24     reset = 0;
25     end
26
27 initial begin
28     $monitor("\t\t counter: %d", counter);
29     #90 $finish;
30 end
31 endmodule
32
```

Tcl Console | Messages | Log | Reports | Design Runs