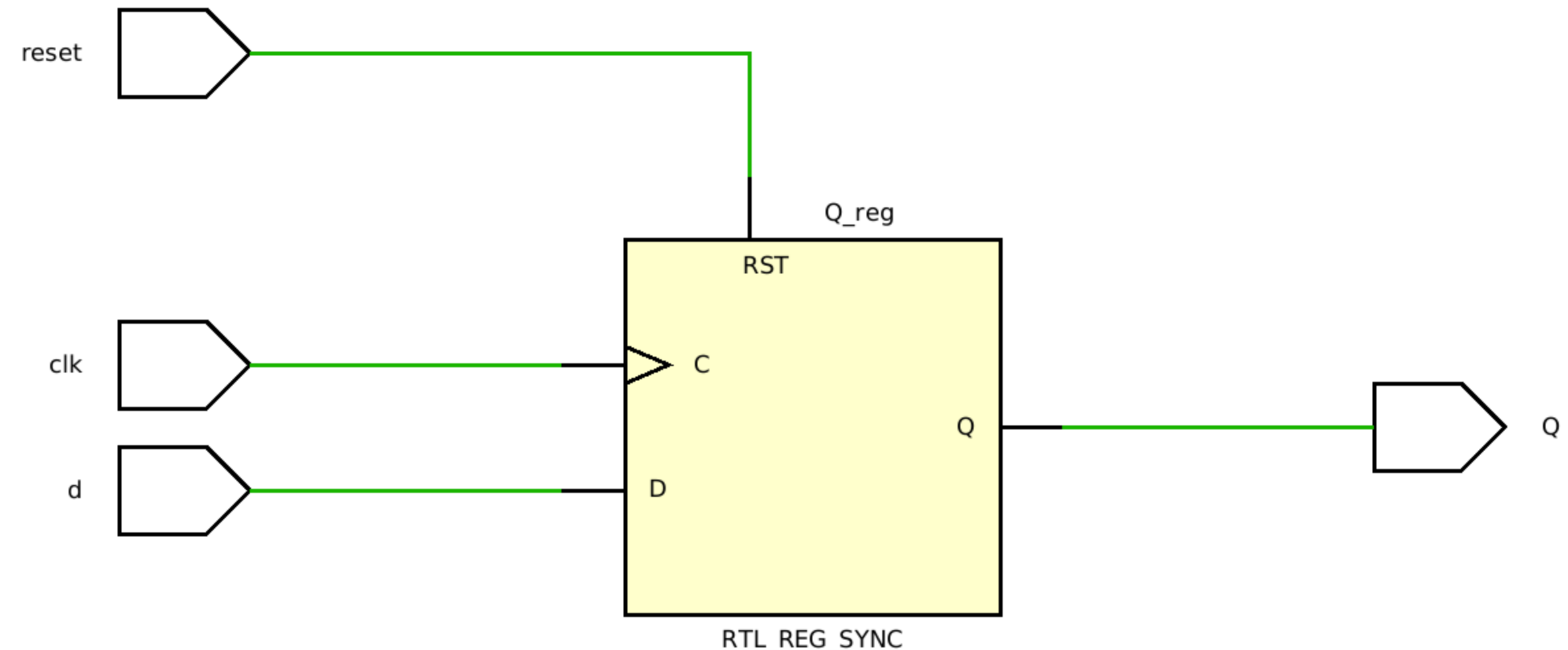
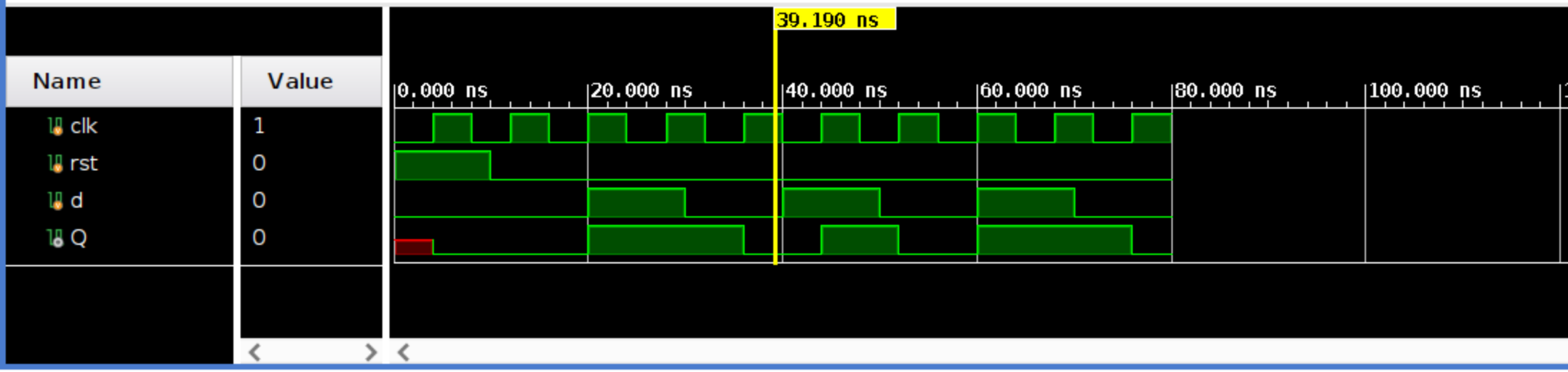
flipflop.v | Dff_tb.v | Schematic | Schematic (2)

1 Cell 4 I/O Ports 4 Nets



D_flipflop.v | Dff_tb.v | Untitled 2



Tcl Console | Messages | Log

```
# run 1000ns
      clk: 0  D: 0  Q: x
      clk: 1  D: 0  Q: 0
      clk: 0  D: 0  Q: 0
      clk: 1  D: 0  Q: 0
      clk: 0  D: 0  Q: 0
      clk: 1  D: 1  Q: 1
      clk: 0  D: 1  Q: 1
      clk: 1  D: 1  Q: 1
      clk: 1  D: 0  Q: 1
      clk: 0  D: 0  Q: 1
      clk: 1  D: 0  Q: 0
      clk: 0  D: 1  Q: 0
      clk: 1  D: 1  Q: 1
      clk: 0  D: 1  Q: 1
      clk: 0  D: 0  Q: 1
      clk: 1  D: 0  Q: 0
      clk: 0  D: 0  Q: 0
      clk: 1  D: 1  Q: 1
      clk: 0  D: 1  Q: 1
      clk: 1  D: 1  Q: 1
      clk: 1  D: 0  Q: 1
```

Type a Tcl command here

D_flipflop.v | Dff_tb.v | Untitled 2

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_048/DFF/DFF.srcs/sources_1/new/D_flipflop.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/08/2024 06:44:52 AM
5   // Module Name: D_flipflop
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module D_flipflop(
9       input clk, reset, d,
10      output reg Q
11      );
12
13      always@(posedge clk)
14            begin
15              if({reset})
16                  Q<= 1'b0;
17              else
18                  Q <= d;
19              end
20
21  endmodule
```

Tcl Console | Messages | Log

D_flipflop.v | Dff_tb.v | Untitled 2

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_048/DFF/DFF.srcs/sim_1/new/Dff_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/08/2024 06:45:52 AM
5  // Module Name: Dff_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module Dff_tb;
10 reg clk,rst,d;
11 wire Q;
12
13   D_flipflop DUT(clk,rst,d,Q);
14
15   initial begin
16   clk=0;
17   d=0;
18   forever #4 clk=~clk;
19   end
20
21   initial
22     begin
23      rst=1;
24      #10;
25      rst=0;
26     forever #10 d= ~d;
27     end
28
29     initial begin
30     $monitor("\t clk: %d  D: %d  Q: %d", clk, d, Q);
31     #80 $finish;
32     end
33 endmodule
34
```

Tcl Console | Messages | Log