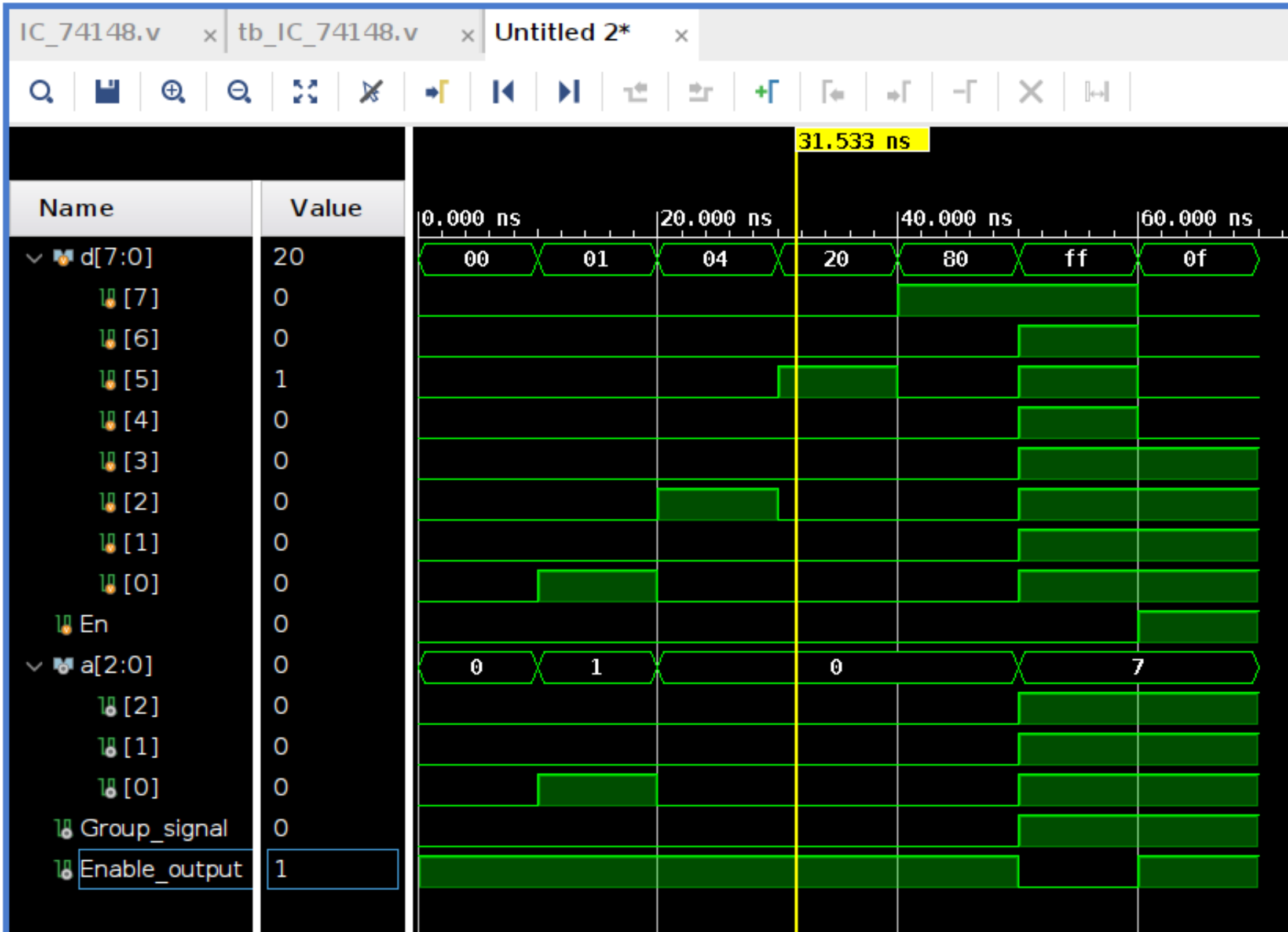
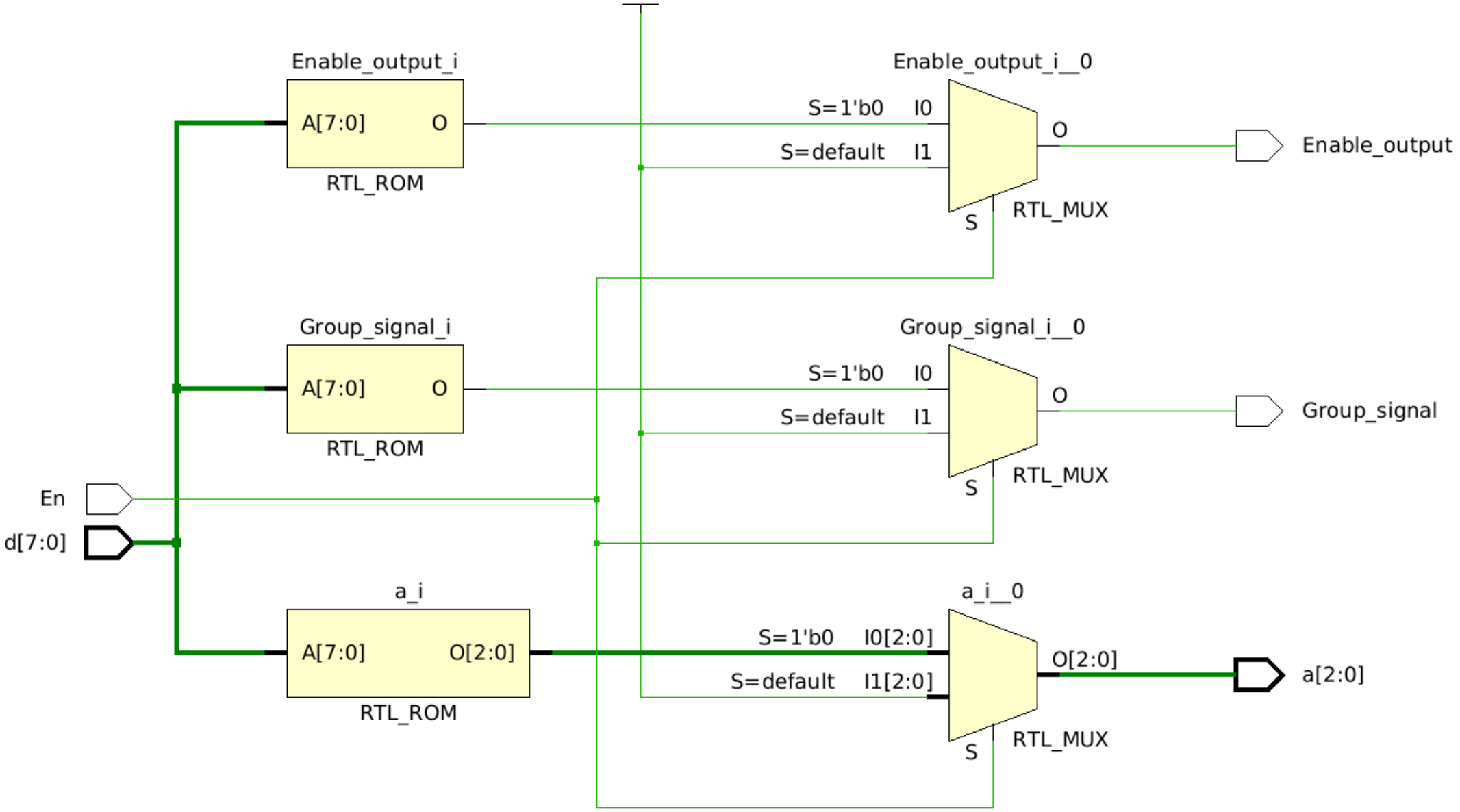

IC_74148.v
tb_IC_74148.v
Untitled 2*
31.533 ns
Name
Value
0.000 ns
20.000 ns
40.000 ns
60.000 ns
d[7:0]
20
00
01
04
20
80
ff
0f
[7]
0
[6]
0
[5]
1
[4]
0
[3]
0
[2]
0
[1]
0
[0]
0
En
0
a[2:0]
0
0
1
0
7
[2]
0
[1]
0
[0]
0
Group_signal
0
Enable_output
1

IC_74148.v | tb_IC_74148.v | Schematic

6 Cells | 14 I/O Ports | 20 Nets



IC_74148.v * | tb_IC_74148.v | Untitled 2*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_034/project_1/project_1.srcs/sources_1/new/IC_74148.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/25/2024 07:01:43 AM
5   // Module Name: priority_encoder
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module IC_74148(
9       input[7:0]d,
10      input En,
11      output reg [2:0]a,
12      output reg Group_signal,Enable_output);
13
14      always @(*)begin
15          if(~En)begin
16              casex(d)
17                  8'b11111111:begin
18                      a = 3'b111;Group_signal = 1;Enable_output = 0;
19                  end
20                  8'bxxxxxxx0:begin
21                      a = 3'b000;Group_signal = 0;Enable_output = 1;
22                  end
23                  8'bxxxxxx01:begin
24                      a = 3'b001;Group_signal = 0;Enable_output = 1;
25                  end
26                  8'bxxxxx011:begin
27                      a = 3'b010;Group_signal = 0;Enable_output = 1;
28                  end
29                  8'bxxxx0111:begin
30                      a = 3'b011;Group_signal = 0;Enable_output = 1;
31                  end
32                  8'bxxx01111:begin
33                      a = 3'b100;Group_signal = 0;Enable_output = 1;
34                  end
35                  8'bxx011111:begin
36                      a = 3'b101;Group_signal = 0;Enable_output = 1;
37                  end
38                  8'bx0111111:begin
39                      a = 3'b110;Group_signal = 0;Enable_output = 1;
40                  end
41                  8'b01111111:begin
42                      a = 3'b111;Group_signal = 0;Enable_output = 1;
43                  end
44                endcase
45              end
46         else begin
47            casex(d)
48                  8'bxxxxxxxx:begin
49                      a = 3'b111;Group_signal = 1;Enable_output = 1;
50                  end
51            endcase
52          end
53      end
54  endmodule
55
```

IC_74148.v × | tb_IC_74148.v × | Untitled 2* ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_034/project_1/project_1.srcs/sim_1/new/tb_IC_74148.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/25/2024 07:11:35 AM
5   // Module Name: tb_IC_74148
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module tb_IC_74148;
9       reg [7:0] d;
10      reg En;
11      wire [2:0] a;
12      wire g;
13      wire e;
14
15      IC_74148 DUT (.d(d),.En(En),.a(a),.Group_signal(g),.Enable_output(e));
16
17      initial begin
18          En = 0;                                     // Enable the encoder
19          d = 8'b00000000; #10;                       // Test case 1: All inputs are low
20          $display("Input: %b, Output: a=%b, g=%b, e=%b", d, a, g, e);
21          d = 8'b00000001; #10;                       // Test case 2: Input 0 is high
22          $display("Input: %b, Output: a=%b, g=%b, e=%b", d, a, g, e);
23          d = 8'b00000100; #10;                       // Test case 3: Input 3 is high
24          $display("Input: %b, Output: a=%b, g=%b, e=%b", d, a, g, e);
25          d = 8'b00100000; #10;                       // Test case 4: Input 5 is high
26          $display("Input: %b, Output: a=%b, g=%b, e=%b", d, a, g, e);
27          d = 8'b10000000; #10;                       // Test case 5: Input 7 is high
28          $display("Input: %b, Output: a=%b, g=%b, e=%b", d, a, g, e);
29          d = 8'b11111111; #10;                       // Test case 6: All inputs high
30          $display("Input: %b, Output: a=%b, g=%b, e=%b", d, a, g, e);
31          En = 1;                                     // Test case 7: Enable signal high
32          d = 8'b00001111; #10;                       // Irrelevant when En is high
33          $display("Input: %b, Output: a=%b, g=%b, e=%b", d, a, g, e);
34          $finish;
35      end
36
37  endmodule
```

Tcl Console × Messages | Log

```
# }
# run 1000ns
Input: 00000000, Output: a=000, g=0, e=1
Input: 00000001, Output: a=001, g=0, e=1
Input: 00000100, Output: a=000, g=0, e=1
Input: 00100000, Output: a=000, g=0, e=1
Input: 10000000, Output: a=000, g=0, e=1
Input: 11111111, Output: a=111, g=1, e=0
Input: 00001111, Output: a=111, g=1, e=1
$finish called at time : 70 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_0
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_IC_74148_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:11 ; elapsed = 00:00:09 . Memory (MB): peak =
```

Type a Tcl command here