88.309 ns

Name	Value																							
x[15:0]	33989	13604	54793	31501	33893	58113	61814	22509	59897	33989	63461	54802	27122	31464	18780	22573	25187	8832	17834	16022	14349			
y[15:0]	53930	24193	22115	39309	21010	52493	52541	63372	9414	53930	29303	56207	38606	20165	10429	9829	34570	8480	52381	47123	54867			
sel...ub	0																							
s[15:0]	22127	33701	32934	1162	12883	40974	13385	20073	50483	22127	34174	41361	54068	47277	8623	32386	60265	17312	35101	59049	25274			
cout	1																							

20.000 ns   40.000 ns   60.000 ns   80.000 ns   100.000 ns   120.000 ns   140.000 ns   160.000 ns   180.000 ns

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_1.srcs/sources_1/new/parallel_adder_subtractor_16b.v

```verilog
1    `timescale 1ns / 1ps
2    ////////////////////////////////////////////////////////////////////////////////
3    // Engineer: Anjan Prasad
4    // Create Date: 09/30/2024 09:14:36 PM
5    // Module Name: parallel_adder_subtractor_16b
6    ////////////////////////////////////////////////////////////////////////////////
7
8
9    module parallel_adder_subtractor_16b(
10       input selAddSub,                 // 0 for addition, 1 for subtraction
11       input [15:0] x, y,               // 16-bit inputs
12       output [15:0] s,                 // 16-bit sum/difference
13       output cout                      // Carry-out/borrow-out from the most significant bit
14   );
15
16       wire [2:0] c;                     // Carry/borrow between the 4-bit adders
17
18       // Instantiate the 4-bit adders/subtractors
19       parallel_adder_4b U0 (
20           .selAddSub(selAddSub), .x(x[3:0]), .y(y[3:0]), .s(s[3:0]), .cout(c[0])
21       );
22
23       parallel_adder_4b U1 (
24           .selAddSub(selAddSub), .x(x[7:4]), .y(y[7:4]), .s(s[7:4]), .cout(c[1])
25       );
26
27       parallel_adder_4b U2 (
28           .selAddSub(selAddSub), .x(x[11:8]),.y(y[11:8]), .s(s[11:8]), .cout(c[2])
29       );
30
31       parallel_adder_4b U3 (
32           .selAddSub(selAddSub), .x(x[15:12]), .y(y[15:12]), .s(s[15:12]), .cout(cout)
33       );
34
35   endmodule
36
```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_1.srcs/sim_1/new/parallel_add_sub_tb.v

```verilog
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 09/30/2024 09:14:36 PM
5   // Module Name: parallel_adder_subtractor_16b
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module parallel_add_sub_tb;
9       reg [15:0] x, y;
10       reg selAddSub;
11       wire [15:0] s;
12       wire cout;
13       parallel_adder_subtractor_16b dut (
14           .x(x),
15           .y(y),
16           .selAddSub(selAddSub),
17           .s(s),
18           .cout(cout)
19       );
20       initial begin
21
22           $display("x      y      selAddSub | s      cout");
23           $monitor("%d %d %b | %d %b", x, y, selAddSub, s, cout);
24
25           // Generate random values for addition (selAddSub = 0) and subtraction (selAddSub = 1)
26           repeat (10) begin
27               selAddSub = 1'b0;  // Test addition
28               x = $random ;
29               y = $random ;
30               #10;
31               selAddSub = 1'b1;  // Test subtraction
32               x = $random ;
33               y = $random ;
34               #10;
35           end
36           $finish;
37       end
38
39   endmodule
```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_1.srcs/sources_1/new/parallel_adder_4b.v

```verilog
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 09/30/2024 09:14:36 PM
5   // Module Name: parallel_adder_subtractor_16b
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module parallel_adder_4b(
10
11     input selAddSub,
12     input [3:0] x,y,
13     output [3:0] s,
14     output cout);
15     wire [2:0] c;
16   full_adder FA0(.a(x[0]),.b(y[0]^selAddSub),.cin(selAddSub),.sum(s[0]),.cout(c[0]));
17   full_adder FA1(.a(x[1]),.b(y[1]^selAddSub),.cin(c[0]),.sum(s[1]),.cout(c[1]));
18   full_adder FA2(.a(x[2]),.b(y[2]^selAddSub),.cin(c[1]),.sum(s[2]),.cout(c[2]));
19   full_adder FA3(.a(x[3]),.b(y[3]^selAddSub),.cin(c[2]),.sum(s[3]),.cout(cout));
20   endmodule
21
```

input

```
# run 1000ns
x     y     selAddSub | s      cout
13604 24193 0 | 33701 0
54793 22115 1 | 32934 1
31501 39309 0 |  1162 1
33893 21010 1 | 12883 1
58113 52493 0 | 40974 1
61814 52541 1 | 13385 1
22509 63372 0 | 20073 1
59897  9414 1 | 50483 1
33989 53930 0 | 22127 1
63461 29303 1 | 34174 1
54802 56207 0 | 41361 1
27122 38606 1 | 54068 0
31464 20165 0 | 47277 0
18780 10429 1 |  8623 1
22573  9829 0 | 32386 0
25187 34570 1 | 60265 0
 8832  8480 0 | 17312 0
17834 52381 1 | 35101 0
16022 47123 0 | 59049 0
14349 54867 1 | 25274 0
$finish called at time : 200 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_
INFO: [USE XSim 96] XSim completed. Design snapshot 'parallel add sub tb behav' loaded
```