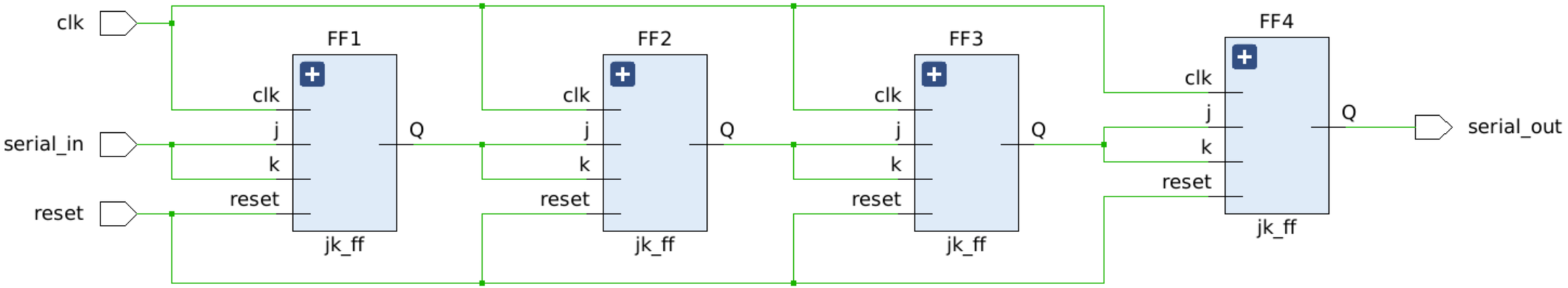
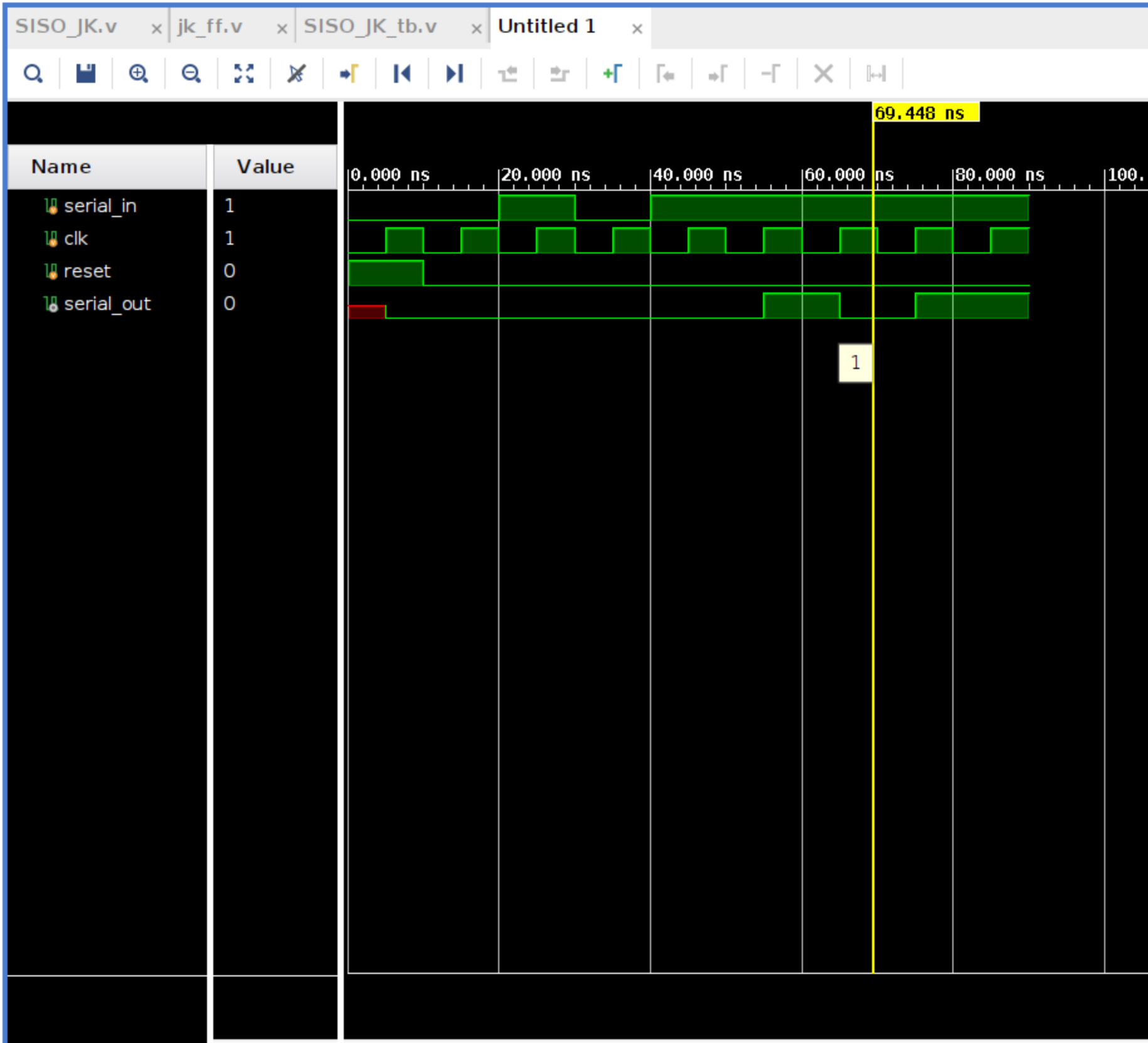
Project Summary | SISO_JK.v | jk_ff.v | Schematic | SISO_JK_tb.v | Schematic (2)

4 Cells 4 I/O Ports 7 Nets




SISO_JK.v
jk_ff.v
SISO_JK_tb.v
Untitled 1
Name
Value
serial_in
1
clk
1
reset
0
serial_out
0
69.448 ns
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
1

SISO_JK.v | jk_ff.v | SISO_JK_tb.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_059/project_1/project_1.srcs/sources_1/new/SISO_JK.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/19/2024 07:33:05 AM
5  // Module Name: SISO_JK
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module SISO_JK(
10     input serial_in, clk, reset,
11     output serial_out
12 );
13     wire Q1, Q2, Q3;
14
15     // Instantiate JK flip-flops in series
16     jk_ff FF1(.j(serial_in), .k(serial_in), .clk(clk), .reset(reset), .Q(Q1));
17     jk_ff FF2(.j(Q1), .k(Q1), .clk(clk), .reset(reset), .Q(Q2));
18     jk_ff FF3(.j(Q2), .k(Q2), .clk(clk), .reset(reset), .Q(Q3));
19     jk_ff FF4(.j(Q3), .k(Q3), .clk(clk), .reset(reset), .Q(serial_out));
20
21 endmodule
22
```

SISO_JK.v | jk_ff.v | SISO_JK_tb.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_047/src/jk_ff.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 11/07/2024 07:43:15 AM
5   // Module Name: jk_ff
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module jk_ff(
10      input j,k,clk,reset,
11      output reg Q
12      );
13      always@(posedge clk)
14            begin
15              if({reset})
16              Q <= 1'b0;
17              else
18                  begin
19                  case({j,k})
20                  2'b00:Q<=Q;
21                  2'b01:Q<=1'b0;
22                  2'b10:Q<=1'b1;
23                  2'b11:Q<=~Q;
24                  endcase
25                  end
26          end
27
28  endmodule
29
30
31
32
```

SISO_JK.v | jk_ff.v | **SISO_JK_tb.v** | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_059/project_1/project_1.srcs/sim_1/new/SISO_JK_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/19/2024 07:36:50 AM
5  // Module Name: SISO_JK_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module SISO_JK_tb;
10     reg serial_in, clk, reset;
11     wire serial_out;
12
13
14     SISO_JK DUT(.serial_in(serial_in), .clk(clk), .reset(reset), .serial_out(serial_out));
15
16     initial begin
17         clk = 0;
18         forever #5 clk = ~clk;
19     end
20
21     initial begin
22
23         reset = 1;
24         serial_in = 0;
25         #10 reset = 0;
26
27         // Shift in a sequence of bits (e.g., 1011)
28         #10 serial_in = 1;
29         #10 serial_in = 0;
30         #10 serial_in = 1;
31         #10 serial_in = 1;
32
33
34         #40;
35         $stop;
36     end
37 endmodule
38
39
```