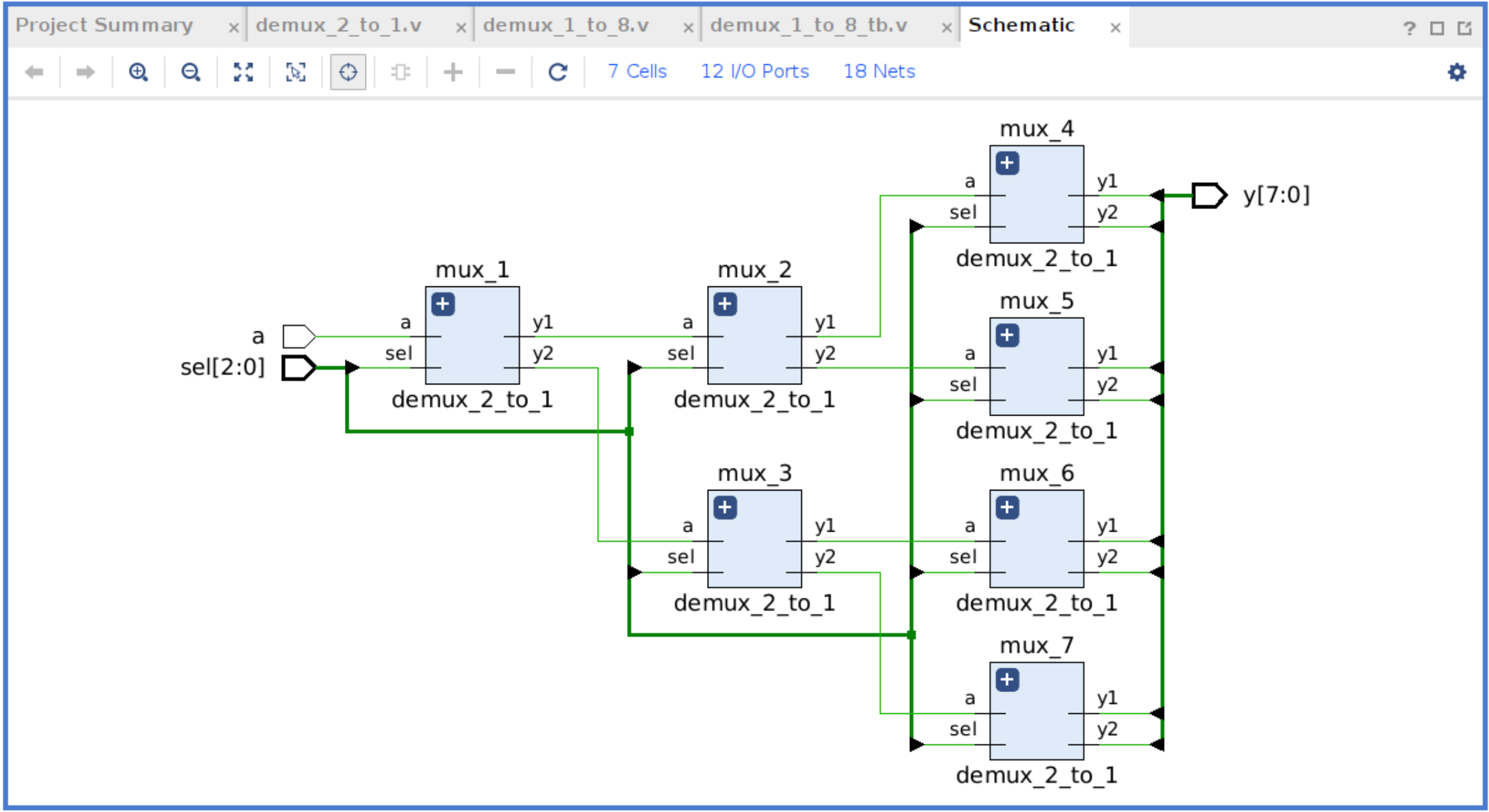
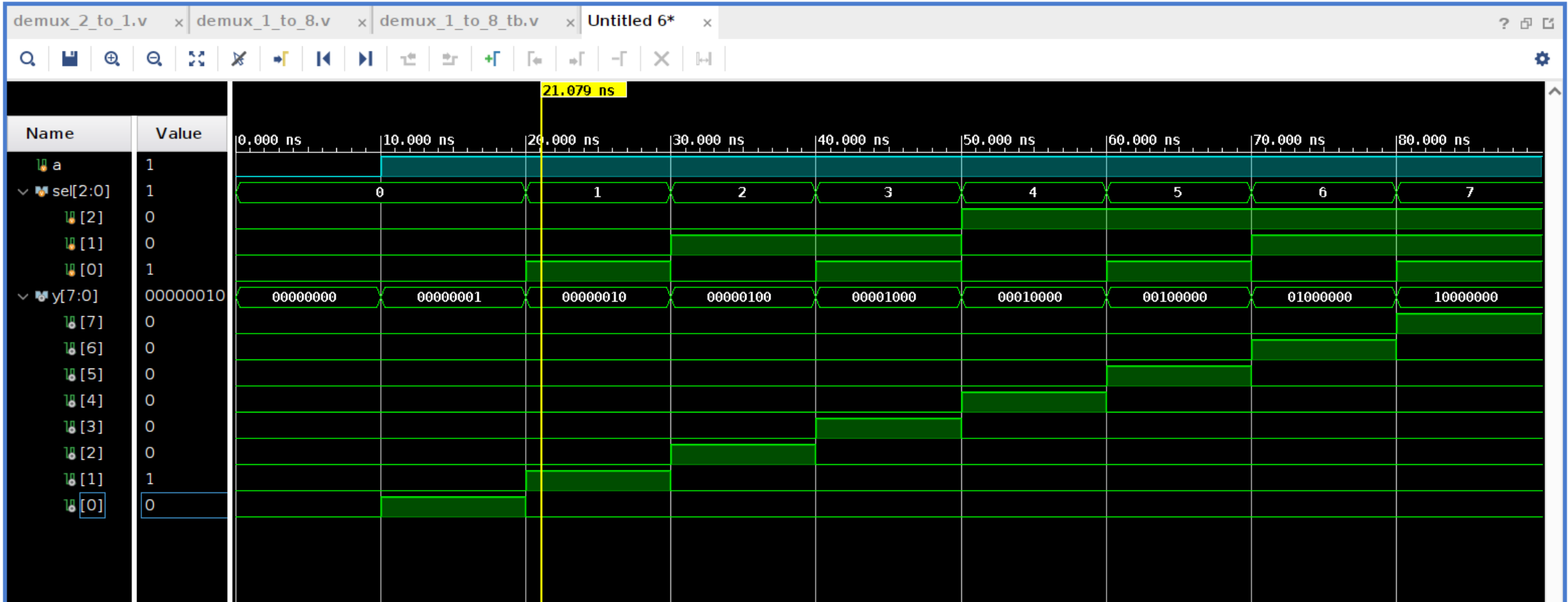

Project Summary
demux_2_to_1.v
demux_1_to_8.v
demux_1_to_8_tb.v
Schematic
7 Cells
12 I/O Ports
18 Nets
mux_4
a
sel
y1
y2
demux_2_to_1
y[7:0]
mux_1
mux_2
mux_5
mux_3
mux_6
mux_7
a
sel[2:0]


demux_2_to_1.v
demux_1_to_8.v
demux_1_to_8_tb.v
Untitled 6*
21.079 ns
Name
Value
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
a
1
sel[2:0]
1
0
1
2
3
4
5
6
7
[2]
0
[1]
0
[0]
1
y[7:0]
00000010
00000000
00000001
00000010
00000100
00001000
00010000
00100000
01000000
10000000
[7]
0
[6]
0
[5]
0
[4]
0
[3]
0
[2]
0
[1]
1
[0]
0

demux_2_to_1.v | **demux_1_to_8.v** | demux_1_to_8_tb.v | Untitled 6*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_029/project_1/project_1.srcs/sources_1/new/demux_1_to_8.v

```
1
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/20/2024 07:15:59 PM
5  // Module Name: demux_1_to_8
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module demux_1_to_8(
10 input a,
11 input [2:0] sel,
12 output [7:0] y
13     );
14     wire x1,x2,x3,x4,x5,x6;
15     // level 1
16     demux_2_to_1 mux_1 (a,sel[2],x1,x2);
17     // level 2
18     demux_2_to_1 mux_2 (x1,sel[1],x3,x4);
19     demux_2_to_1 mux_3 (x2,sel[1],x5,x6);
20     // level 3
21     demux_2_to_1 mux_4 (x3,sel[0],y[0],y[1]);
22     demux_2_to_1 mux_5 (x4,sel[0],y[2],y[3]);
23     demux_2_to_1 mux_6 (x5,sel[0],y[4],y[5]);
24     demux_2_to_1 mux_7 (x6,sel[0],y[6],y[7]);
25 endmodule
26
```

demux_2_to_1.v | demux_1_to_8.v | **demux_1_to_8_tb.v** | Untitled 6*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_029/project_1/project_1.srcs/sim_1/new/demux_1_to_8_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/06/2024 08:31:43 AM
5   // Module Name: demux_1_to_8_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module demux_1_to_8_tb;
10   reg a;
11   reg [2:0] sel;
12   wire [7:0] y;
13
14      demux_1_to_8 DUT (a,sel,y);
15
16      initial begin
17    a = 0; sel = 3'b000 ; #10;
18
19    a = 1; sel = 3'b000 ; #10;
20    a = 1; sel = 3'b001 ; #10;
21    a = 1; sel = 3'b010 ; #10;
22    a = 1; sel = 3'b011 ; #10;
23    a = 1; sel = 3'b100 ; #10;
24    a = 1; sel = 3'b101 ; #10;
25    a = 1; sel = 3'b110 ; #10;
26    a = 1; sel = 3'b111 ; #10;
27
28
29      $finish;
30
31
32      end
33
34
35  endmodule
36
```

demux_2_to_1.v | demux_1_to_8.v | demux_1_to_8_tb.v | Untitled 6*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_029/project_1/project_1.srcs/sources_1/new/demux_2_to_1.v

```
1   module demux_2_to_1(
2
3   input a,
4   input sel,
5   output y1,y2
6     );
7   //  assign y1 = a &  sel;
8   //  assign y2 = a & ~sel;
9    assign {y1,y2} = sel?{1'b0,a}: {a,1'b0};
10  endmodule
```