half_adder.v | ha_tb.v | Untitled 5

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_006/project_1/project_1.srcs/sources_1/new/half_adder.v

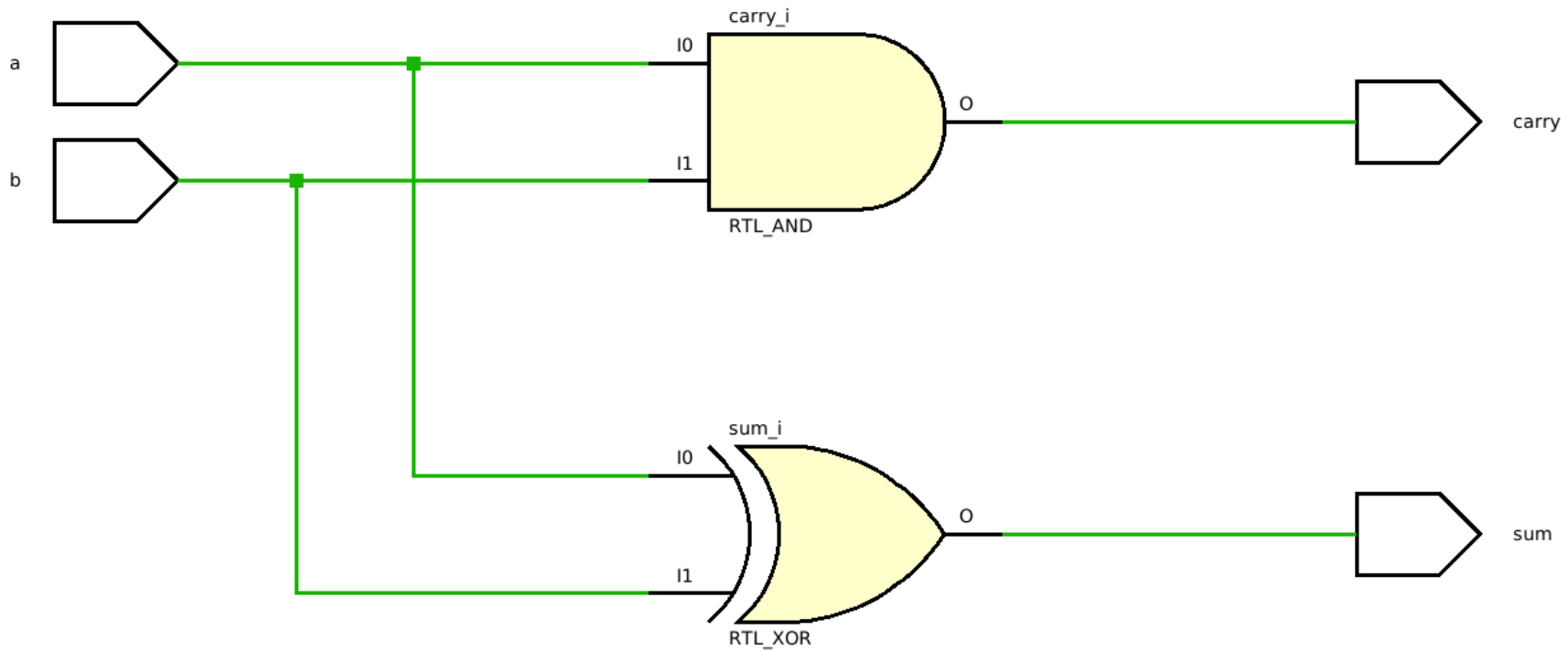
```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 09/27/2024 08:41:55 PM
5   // Module Name: half_adder
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module half_adder (
10      input a,
11      input b,
12      output sum,
13       output carry);
14      assign carry = a & b;
15      assign sum = (a ^ b);
16  endmodule
17
```

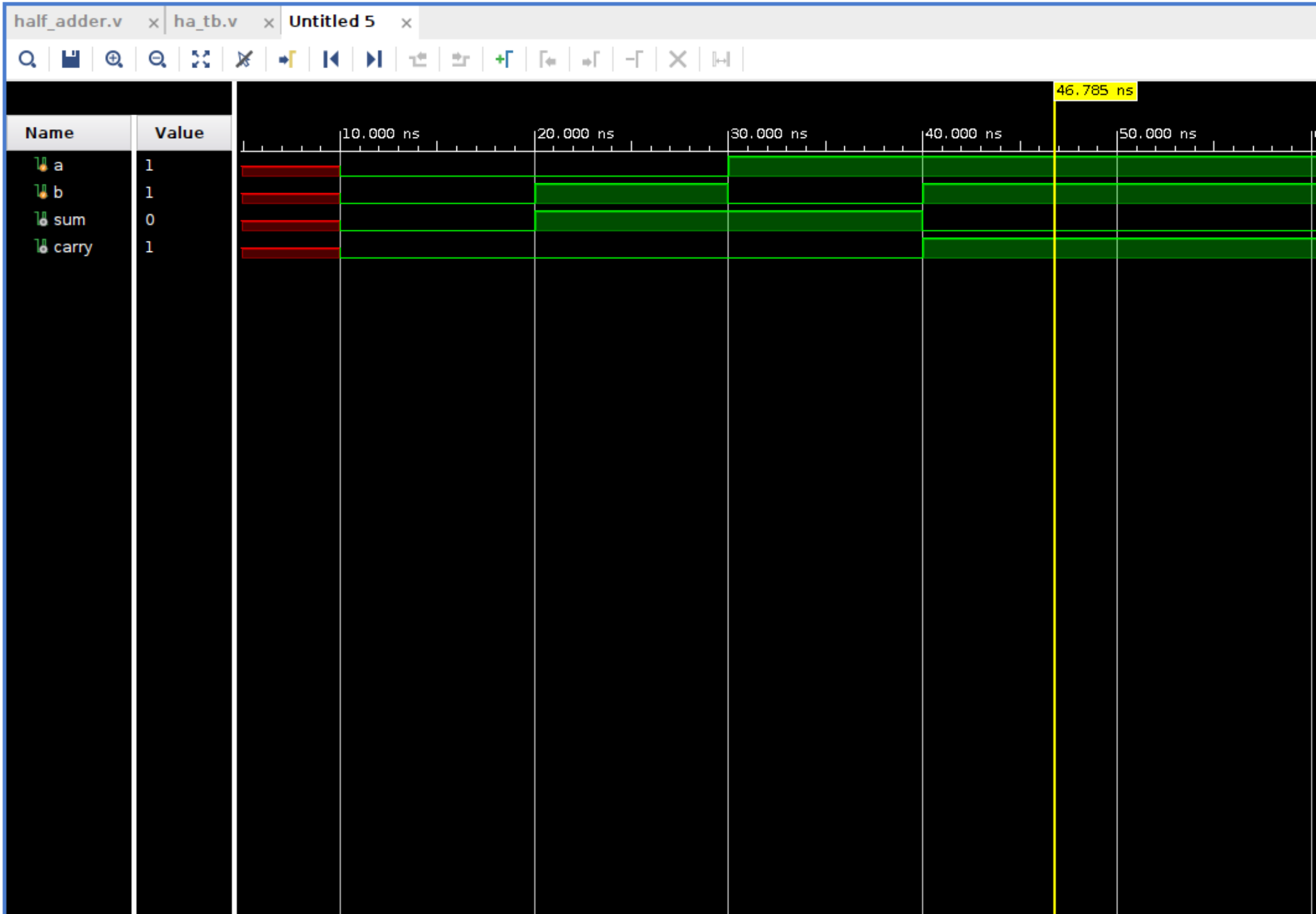
half_adder.v | ha_tb.v | Untitled 5

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_006/project_1/project_1.srcs/sim_1/new/ha_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/27/2024 08:41:55 PM
5  // Module Name: half_adder
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module ha_tb;
10 reg a,b;
11 wire sum,carry;
12 half_adder DUT (a,b,sum,carry);
13
14
15 initial begin
16 #10 a = 0; b = 0;
17 #10 a = 0; b = 1;
18 #10 a = 1; b = 0;
19 #10 a = 1; b = 1;
20 end
21
22 endmodule
23
```

2 Cells 4 I/O Ports 4 Nets




half_adder.v
ha_tb.v
Untitled 5
Name
Value
a
1
b
1
sum
0
carry
1
10.000 ns
20.000 ns
30.000 ns
40.000 ns
46.785 ns
50.000 ns

half_adder.v | ha_tb.v | full_adder.v | fa_tb.v | Untitled 8

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_006/project_1/project_1.srcs/sources_1/new/full_adder.v

```
1   `timescale 1ns/1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 09/27/2024 08:41:55 PM
5   // Module Name: half_adder
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module full_adder (
9   input a,
10  input b,
11  input cin,
12  output sum,
13  output cout);
14  assign sum = (a^b^cin);
15  assign cout = (a&&b)||(b&&cin)||(a&&cin);
16  endmodule
```

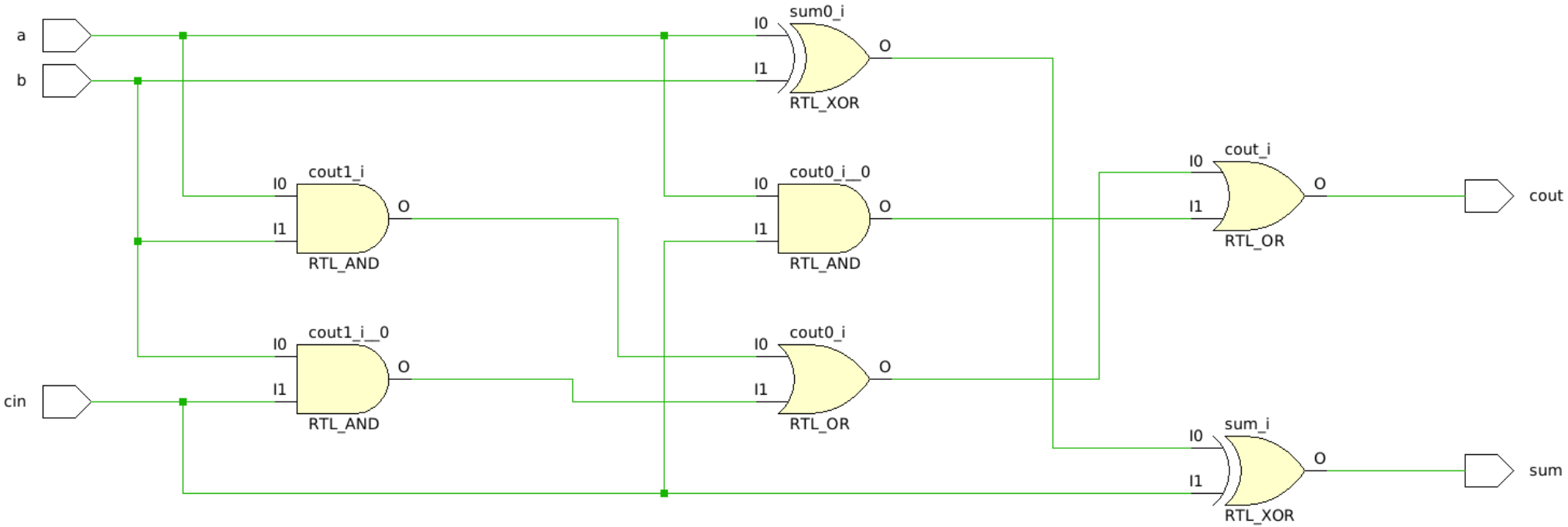
half_adder.v | ha_tb.v | full_adder.v | **fa_tb.v** | Untitled 8

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_006/project_1/project_1.srcs/sim_1/new/fa_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 09/27/2024 08:41:55 PM
5   // Module Name: half_adder
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module fa_tb;
10  reg a,b,cin;
11  wire sum,cout;
12  full_adder DUT (a,b,cin,sum,cout);
13
14
15  initial begin
16  #10 a = 0; b = 0; cin = 0;
17  #10 a = 0; b = 0; cin = 1;
18  #10 a = 0; b = 1; cin = 0;
19  #10 a = 0; b = 1; cin = 1;
20  #10 a = 1; b = 0; cin = 0;
21  #10 a = 1; b = 0; cin = 1;
22  #10 a = 1; b = 1; cin = 0;
23  #10 a = 1; b = 1; cin = 1;
24
25
26  end
27
28  endmodule
```

Project Summary | Schematic | half_adder.v | ha_tb.v | full_adder.v | fa_tb.v | Schematic (2)

7 Cells 5 I/O Ports 10 Nets



half_adder.v | ha_tb.v | full_adder.v | fa_tb.v | Untitled 8