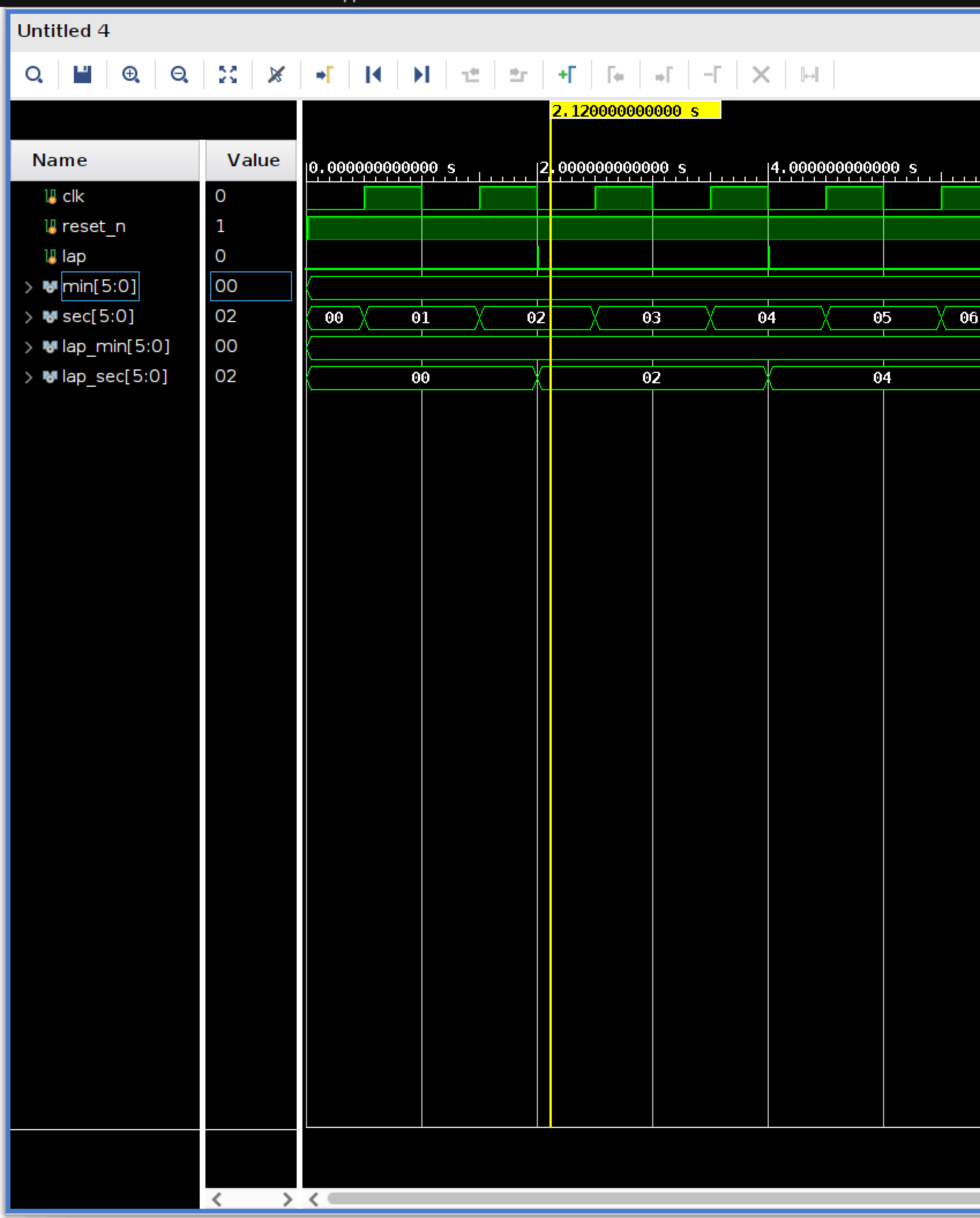
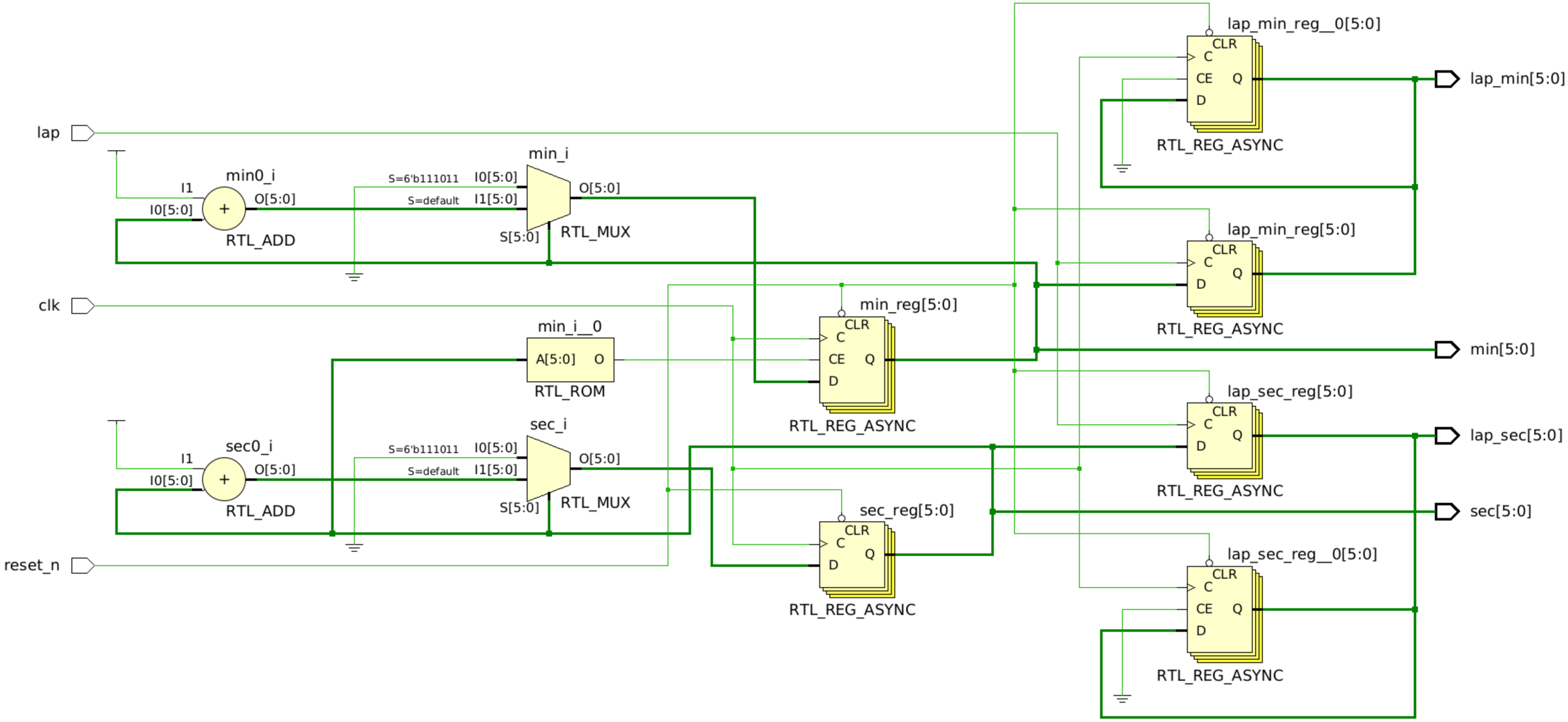

Untitled 4
Name
Value
clk
0
reset_n
1
lap
0
min[5:0]
00
sec[5:0]
02
lap_min[5:0]
00
lap_sec[5:0]
02
2.120000000000 s
0.000000000000 s
2.000000000000 s
4.000000000000 s
00
01
02
03
04
05
06
00
02
04

Schematic

41 Cells 27 I/O Ports 54 Nets



stopwatch.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_083/project_1/project_1.srcs/sources_1/new/stopwatch.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 12/13/2024 09:23:36 AM
5  // Module Name: stopwatch
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module stopwatch (
9      input clk,              // Clock input (1Hz)
10     input reset_n,          // Active low reset
11     input lap,              // LAP button
12     output reg [5:0] sec,
13     output reg [5:0] min,
14     output reg [5:0] lap_sec,
15     output reg [5:0] lap_min
16 );
17
18     always @(posedge clk or negedge reset_n) begin
19         if (!reset_n) begin
20             sec <= 0;
21             min <= 0;
22             lap_sec <= 0;
23             lap_min <= 0;
24         end else begin
25             if (sec == 59) begin
26                 sec <= 0;
27                 if (min == 59)
28                     min <= 0;
29                 else
30                     min <= min + 1;
31             end else begin
32                 sec <= sec + 1;
33             end
34         end
35     end
36    always @(posedge lap or negedge reset_n) begin
37         if (!reset_n) begin
38             lap_sec <= 0;
39             lap_min <= 0;
40         end else begin
41             lap_sec <= sec;
42             lap_min <= min;
43         end
44     end
45
46 endmodule
47
```

stopwatch_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_083/project_1/project_1.srcs/sim_1/new/stopwatch_tb.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Engineer: Anjan Prasad
3  // Create Date: 12/13/2024 09:26:09 AM
4  // Module Name: stopwatch_tb
5  //////////////////////////////////////////////////////////////////////////////////
6
7  `timescale 1ms / 1us  // (1ms time unit, 1us precision)
8
9  module stopwatch_tb;
10     reg clk;
11     reg reset_n;
12     reg lap;
13     wire [5:0] min;
14     wire [5:0] sec;
15     wire [5:0] lap_min;
16     wire [5:0] lap_sec;
17
18     stopwatch DUT (
19         .clk(clk),.reset_n(reset_n),
20         .lap(lap),.sec(sec),.min(min),
21         .lap_sec(lap_sec),.lap_min(lap_min));
22
23     always begin
24         #500 clk = ~clk;
25     end
26
27     initial begin
28         clk = 0; reset_n = 0; lap = 0;
29
30         #1 reset_n = 1;  // Reset the stopwatch
31         #2000;
32
33            lap = 1;
34         #5 lap = 0;
35         #2000;
36
37            lap = 1;
38         #5 lap = 0;
39         #2000;
40
41            reset_n = 0;
42         #1 reset_n = 1;
43         #2000;
44
45         $stop;
46     end
47 endmodule
48
```