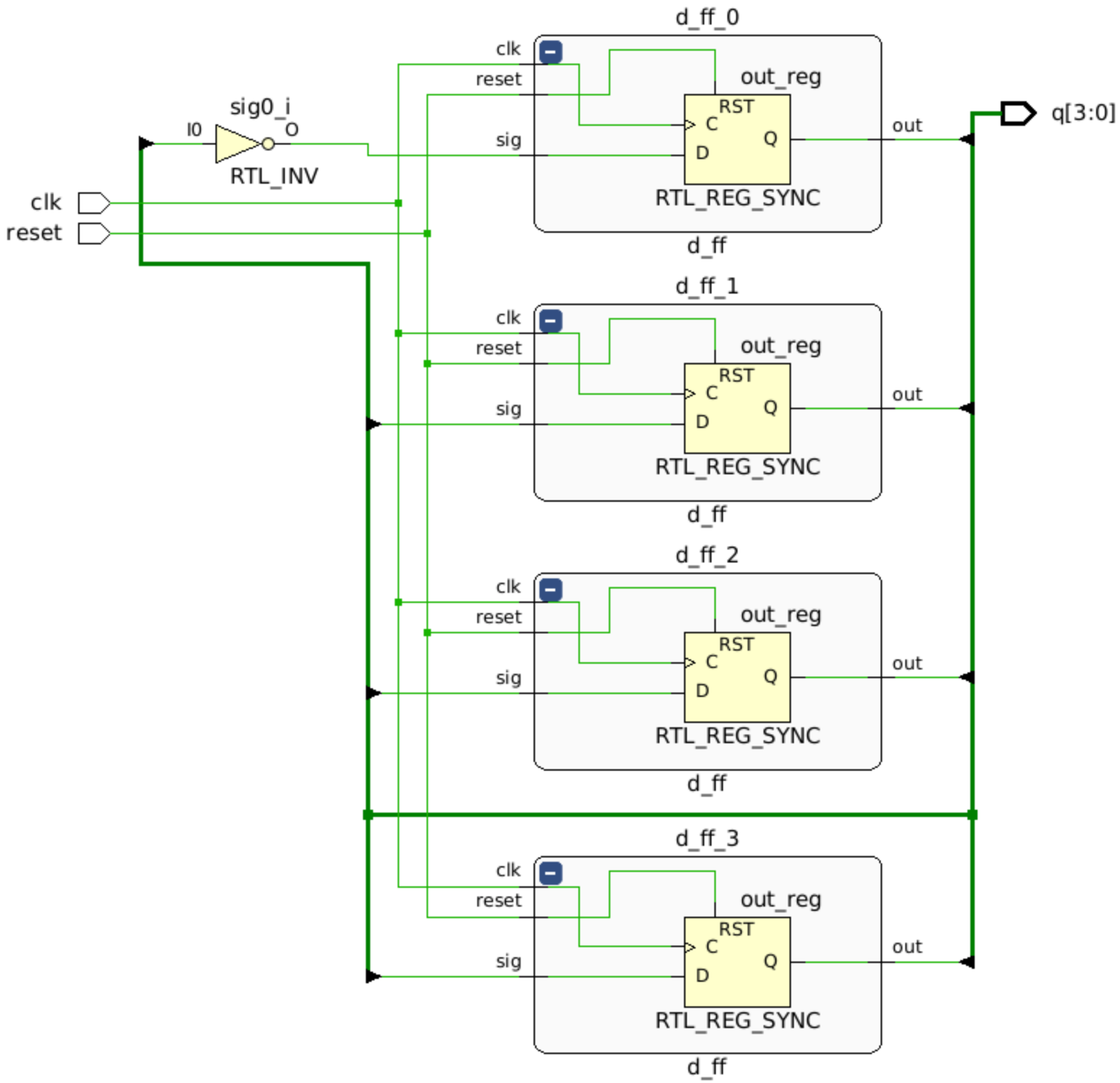
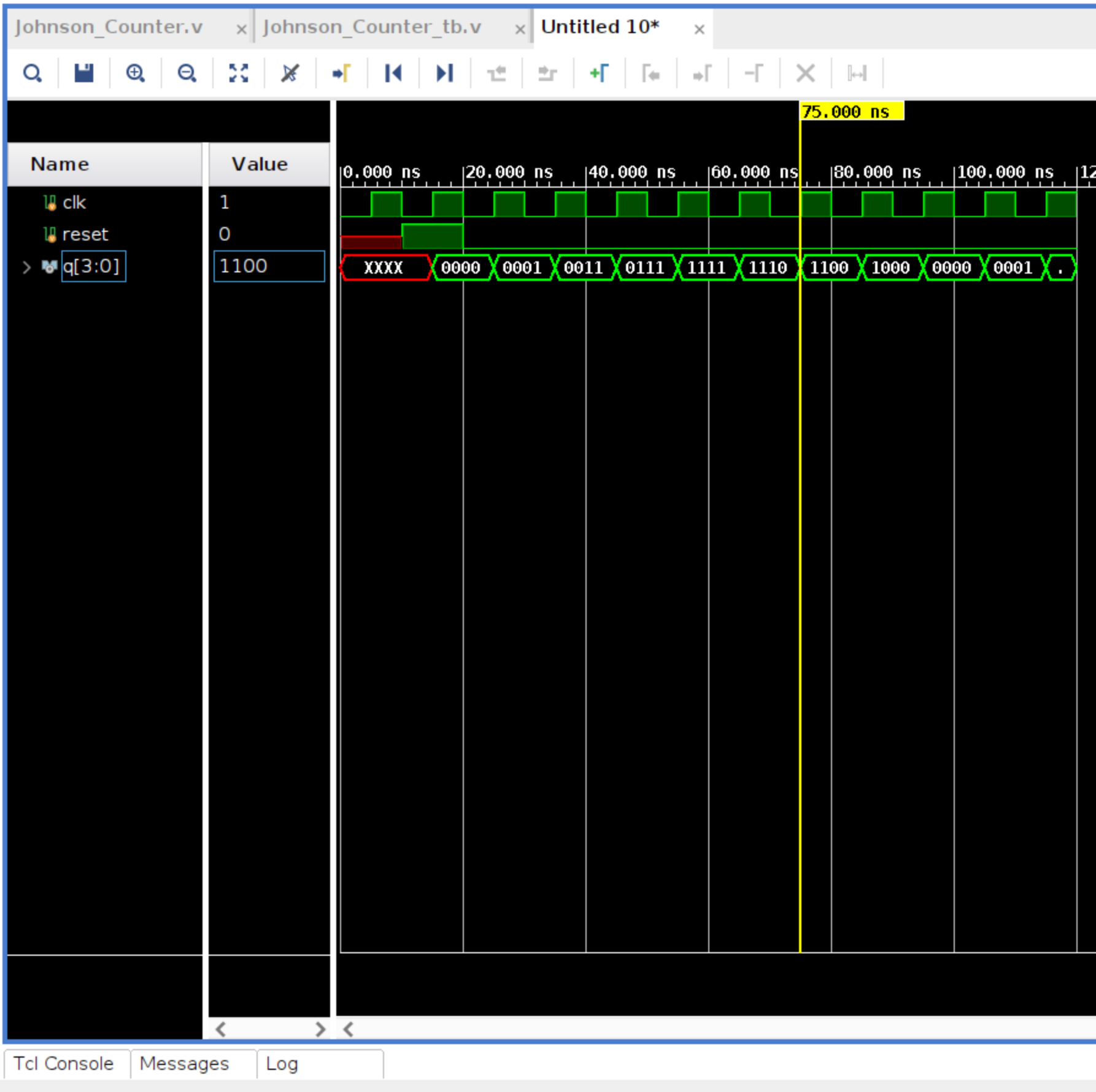
er.v | Johnson_Counter_tb.v | Schematic

9 Cells 6 I/O Ports 23 Nets



Reports | Design Runs


Johnson_Counter.v
Johnson_Counter_tb.v
Untitled 10*
Name
Value
clk
1
reset
0
q[3:0]
1100
75.000 ns
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
XXXX
0000
0001
0011
0111
1111
1110
1100
1000
0000
0001
Tcl Console
Messages
Log

Project Summary | Johnson_Counter.v | Johnson_Counter_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_069/project_1/project_1.srcs/sources_1/new/Johnson_Counter.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer:
4  // Create Date: 11/29/2024 05:27:09 AM
5  // Module Name: Johnson_Counter
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module Johnson_Counter(input clk,reset,
10 output [3:0] q);
11  wire q_bar_3;
12
13    d_ff d_ff_0(.sig(~q[3]), .clk(clk), .out(q[0]), .reset(reset));
14    d_ff d_ff_1(.sig(q[0]),  .clk(clk), .out(q[1]), .reset(reset));
15    d_ff d_ff_2(.sig(q[1]),  .clk(clk), .out(q[2]), .reset(reset));
16    d_ff d_ff_3(.sig(q[2]),  .clk(clk), .out(q[3]), .reset(reset));
17
18 endmodule
19
20
21 module d_ff(
22     input clk, reset, sig,
23     output reg out
24     );
25
26     always@(posedge clk)
27           begin
28             if({reset})
29                 out<= 1'b0;
30             else
31                 out <= sig;
32             end
33
34 endmodule
```

Tcl Console | Messages | Log | Reports | Design Runs

Project Summary | Johnson_Counter.v | **Johnson_Counter_tb.v**

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_069/project_1/project_1.srcs/sim_1/new/Johnson_Counter_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/29/2024 05:55:49 AM
5  // Module Name: Johnson_Counter_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module Johnson_Counter_tb;
9
10     reg clk,reset;
11
12     wire [3:0] q;
13
14     Johnson_Counter DUT (
15         .clk(clk),
16         .q(q),
17         .reset(reset)
18     );
19     initial begin
20         clk = 0;
21         forever #5 clk = ~clk;
22     end
23
24     initial begin
25         $monitor("Time = %0d, clk = %b, q = %b", $time, clk, q);
26     end
27     initial begin
28         #10 reset = 1;
29         #10 reset = 0;
30         #100 $finish;
31     end
32
33 endmodule
34
```

Tcl Console | Messages | Log | Reports | Design Runs