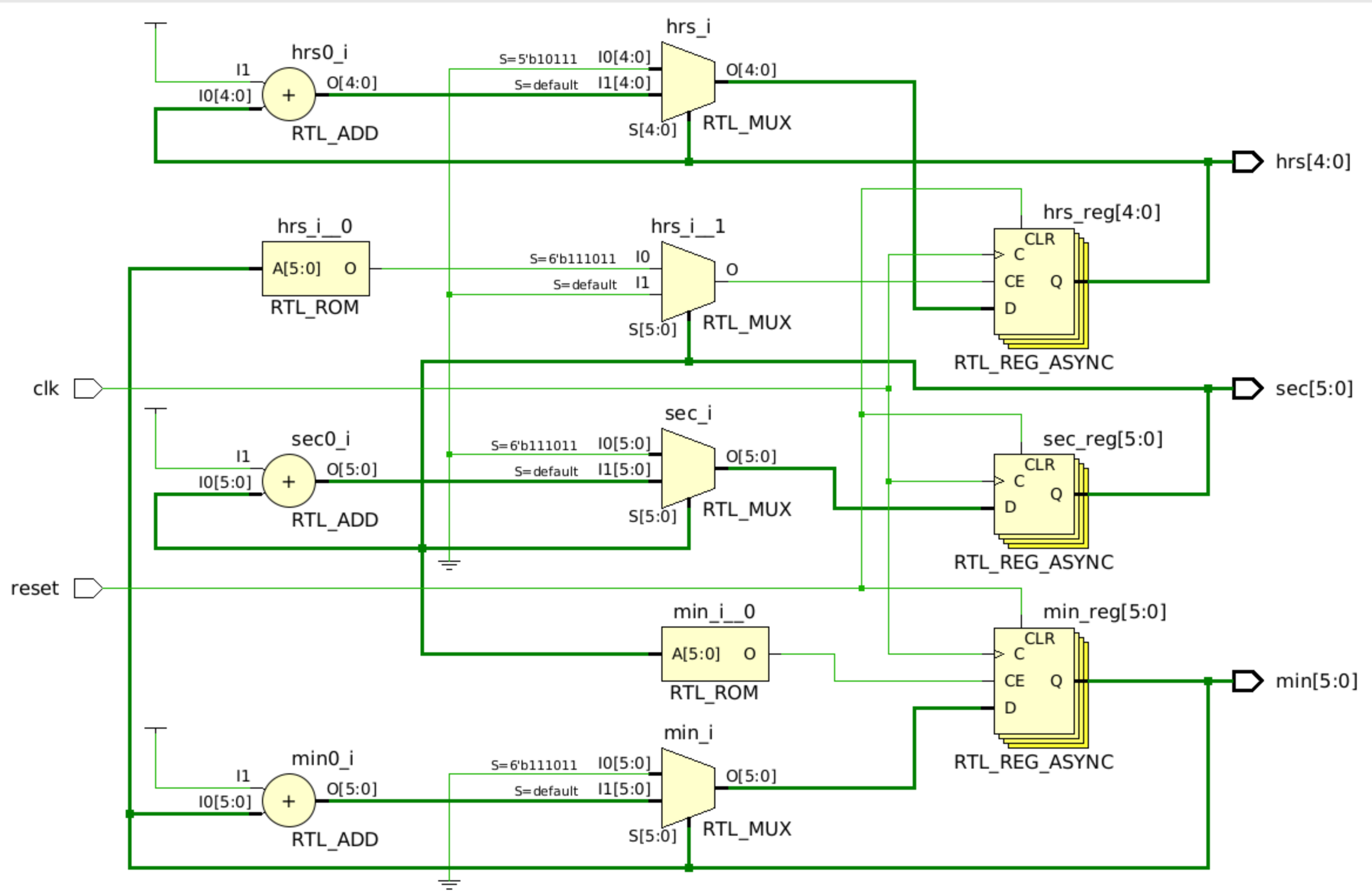
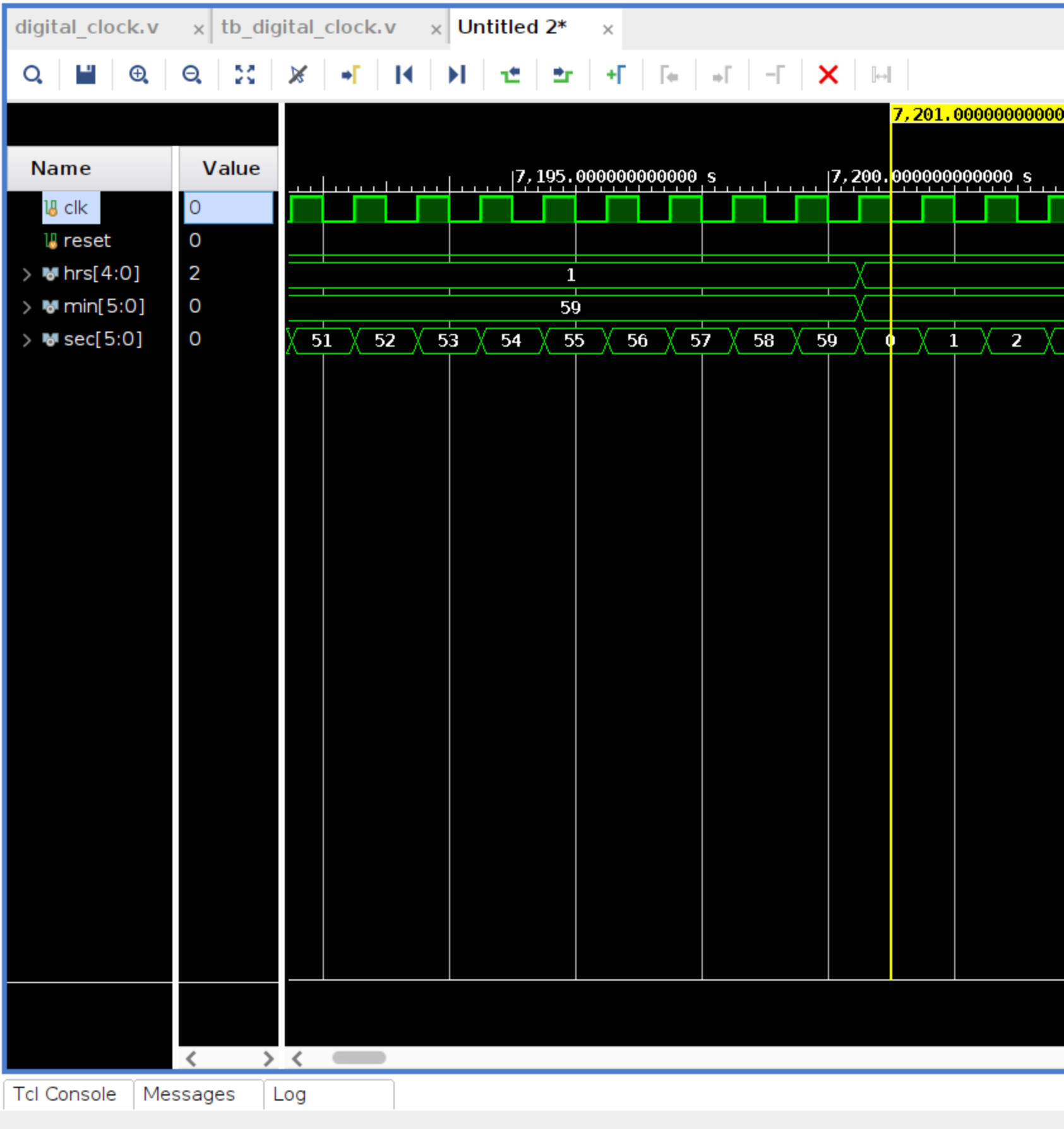
digital_clock.v | tb_digital_clock.v | Schematic

26 Cells | 19 I/O Ports | 58 Nets



Log | Reports | Design Runs


digital_clock.v
tb_digital_clock.v
Untitled 2*
Name
Value
clk
0
reset
0
hrs[4:0]
2
min[5:0]
0
sec[5:0]
0
7,195.000000000000 s
7,200.000000000000 s
7,201.000000000000
1
59
51
52
53
54
55
56
57
58
59
0
1
2
Tcl Console
Messages
Log

digital_clock.v | tb_digital_clock.v | Untitled 2*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_082/project_1/project_1.srcs/sources_1/new/digital_clock.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 12/12/2024 10:33:33 AM
5  // Module Name: digital_clock
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module digital_clock (
9      input clk,       // 1 Hz clock input
10     input reset,     // Active high reset
11     output reg [5:0] sec,
12     output reg [5:0] min,
13     output reg [4:0] hrs);
14
15     always @(posedge clk or posedge reset) begin
16         if (reset) begin
17             sec <= 6'b0;
18             min <= 6'b0;
19             hrs <= 5'b0;
20         end else begin
21
22             if (sec == 59) begin
23                 sec <= 0;
24                 if (min == 59) begin
25                     min <= 0;
26                     if (hrs == 23) begin
27                         hrs <= 0;
28                     end else begin
29                         hrs <= hrs + 1;
30                     end
31                 end else begin
32                     min <= min + 1;
33                 end
34             end else begin
35                 sec <= sec + 1;
36             end
37         end
38     end
39 endmodule
```

Tcl Console | Messages | Log

digital_clock.v | tb_digital_clock.v | Untitled 2*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_082/project_1/project_1.srcs/sim_1/new/tb_digital_clock.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 12/12/2024 10:34:56 AM
5  // Module Name: tb_digital_clock
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module tb_digital_clock;
9
10     reg clk;
11     reg reset;
12     wire [5:0] sec;
13     wire [5:0] min;
14     wire [4:0] hrs;
15
16     digital_clock DUT (
17         .clk(clk),.reset(reset),.sec(sec),.min(min),.hrs(hrs)
18     );
19
20     // Clock generation (1 Hz simulation)
21     initial begin
22         clk = 0;
23         forever #500000000 clk = ~clk; // 1 Hz clock (500ms period)
24     end
25
26     initial begin
27         reset = 1;
28         #1000000000 reset = 0;
29
30         #2000000000 $finish;
31     end
32
33     initial begin
34         $monitor("Time: %0t | Hours: %0d, Minutes: %0d, Seconds: %0d",
35         $time, hrs, min, sec);
36     end
37 endmodule
38
39
```

Tcl Console | Messages | Log