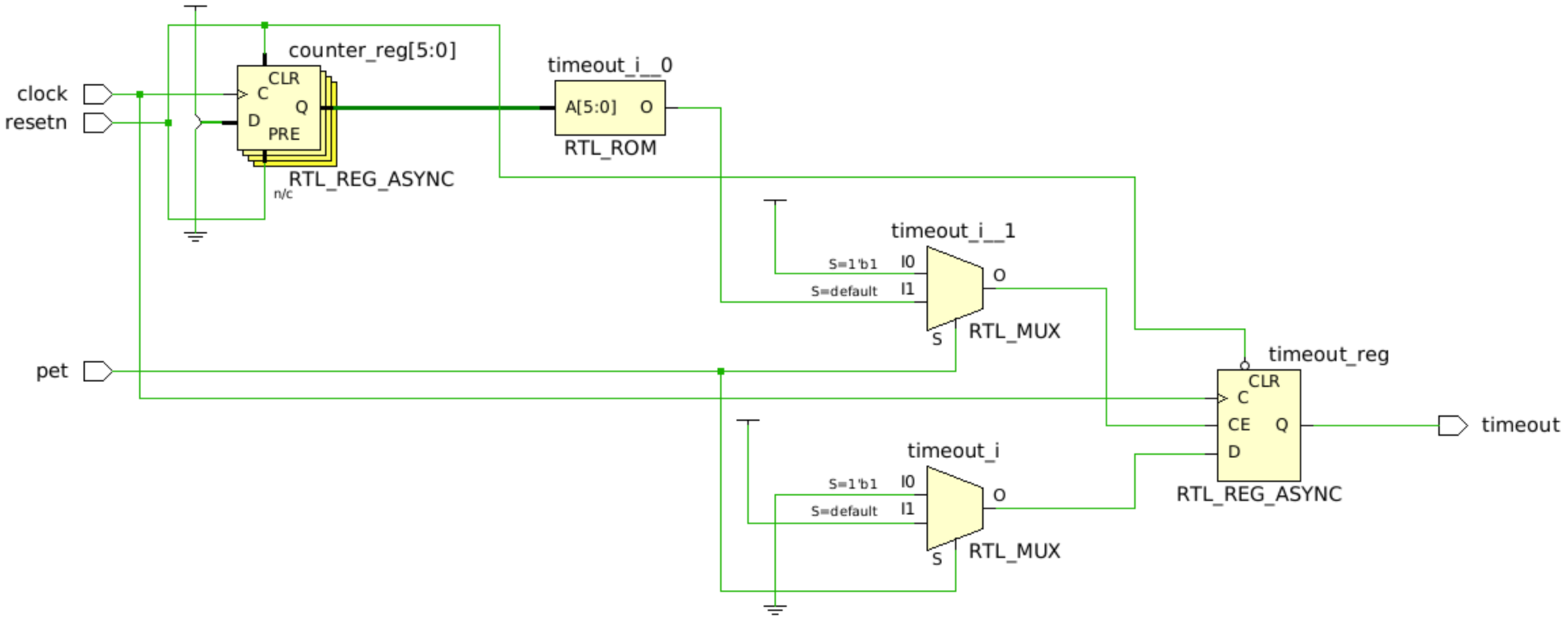
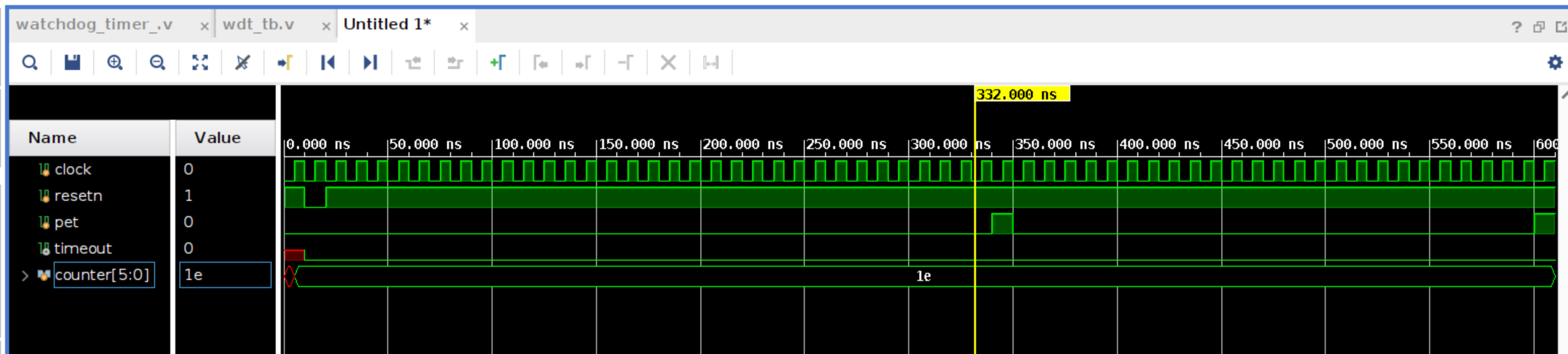
10 Cells 4 I/O Ports 15 Nets




watchdog_timer_.v
wdt_tb.v
Untitled 1*
Name
Value
clock
0
resetn
1
pet
0
timeout
0
counter[5:0]
1e
332.000 ns
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns
500.000 ns
550.000 ns
1e

Project Summary | watchdog_timer_.v | wdt_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_039/project_1/project_1.srcs/sources_1/new/watchdog_timer

```
1
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/30/2024 07:24:27 AM
5  // Module Name: watchdog_timer_
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module watchdog_timer_ (clock, resetn, pet, timeout);
10 input clock,
11 resetn,
12 pet;
13 output reg timeout;
14 localparam PERIOD = 30;
15 reg [5:0] counter;
16 always @(posedge clock or negedge resetn)
17      if(! resetn) begin counter <= PERIOD;
18         timeout <= 1 'b0;
19 end
20
21 else begin
22  if (pet) begin
23  timeout<=1'b0;
24 end
25 else if (counter == 0)
26      timeout <= 1 'b1;
27 else counter<=counter-1'b1;
28      counter <= PERIOD;
29 end
30 endmodule
31
```

Project Summary | watchdog_timer_.v | wdt_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_039/project_1/project_1.srcs/sim_1/new/wdt_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/30/2024 07:31:00 AM
5  // Module Name: wdt_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module wdt_tb;
10
11 reg clock=0, resetn=1, pet=0;
12 wire timeout;
13 watchdog_timer_ WDT(clock, resetn, pet, timeout);
14
15   always clock=#5 ~clock;
16   task reset;
17     begin
18     #10;
19     resetn=0;
20     #10;
21     resetn=1;
22     end
23   endtask
24 initial begin
25     reset; #320; pet=1;
26     #10;
27     pet=0;
28
29     #250;
30     pet=1; #10;
31     $finish;
32 end
33
34 endmodule
35
```