Project Summary | Schematic | gate_level.v | gate_level_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_003/project_1/project_1.srcs/sources_1/new/gate_level.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/24/2024 10:42:52 PM
5  // Module Name: gate_level
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module gate_level(
10     input i1,i2,ctrl,
11     output o_and,o_or,o_nand,o_nor,o_xnor,o_xor,buf_0,buf_1
12 );
13
14     and and_1 (o_and,i1,i2);
15     or or_1 (o_or,i1,i2);
16     nand nand_1 (o_nand,i1,i2);
17     nor nor_1 (o_nor,i1,i2);
18     xnor xnor_1 (o_xnor,i1,i2);
19     xor xor_1 (o_xor,i1,i2);
20     bufif0 buf_o (buf_0,i1,ctrl);
21     bufif1 buf_n (buf_1,i1,crtl);
22 endmodule
```

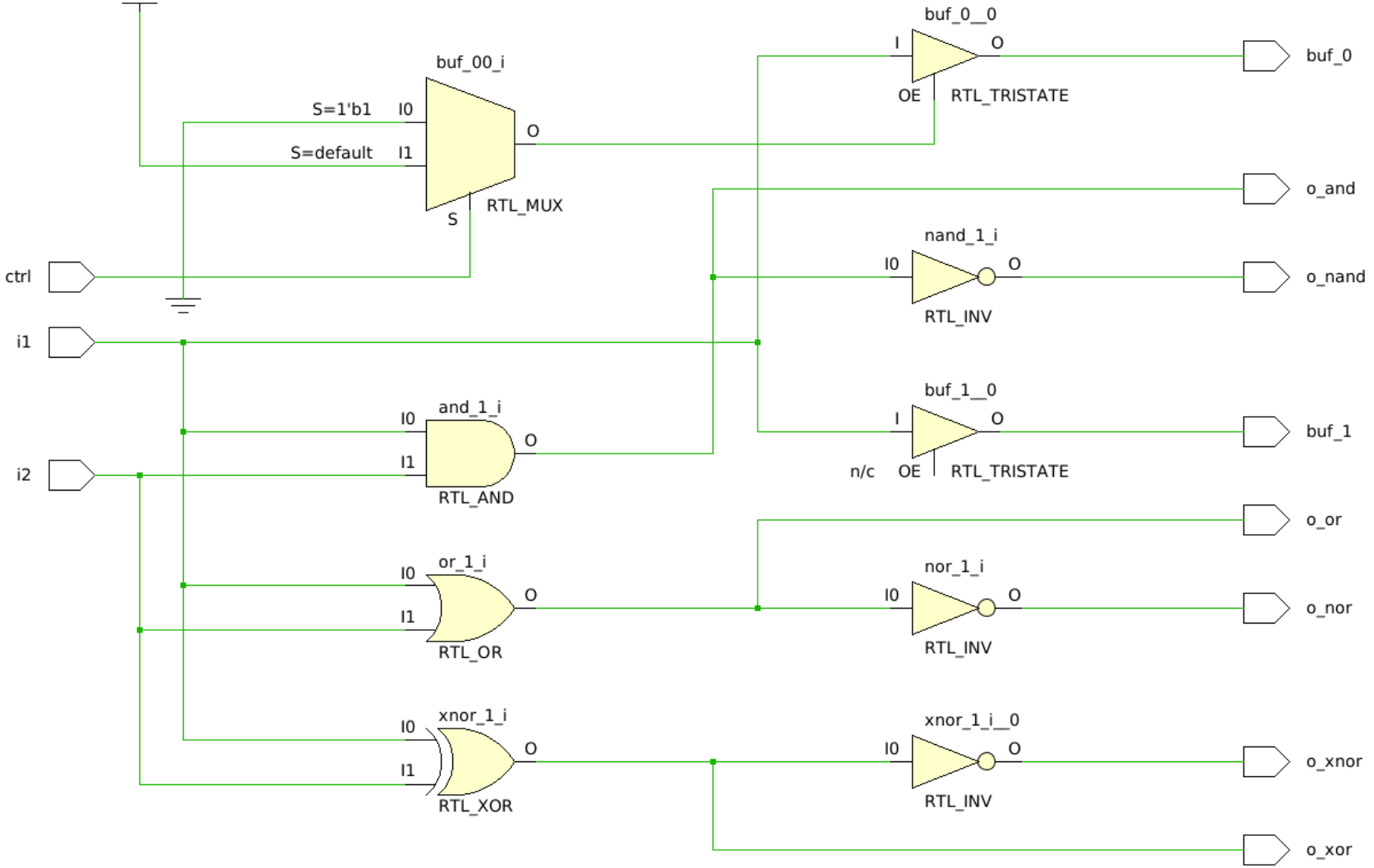
Project Summary | Schematic | gate_level.v | **gate_level_tb.v**

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_003/project_1/project_1.srcs/sim_1/new/gate_level_tb.v

```
1  `timescale 10ns / 10ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/24/2024 10:42:52 PM
5  // Module Name: gate_level
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module gate_level_tb;
10     reg i1,i2,ctrl;
11     wire o_and,o_or,o_nand,o_nor,o_xnor,o_xor,buf_0,buf_1;
12  gate_level DUT (i1,i2,ctrl,o_and,o_or,o_nand,o_nor,o_xnor,o_xor,buf_0,buf_1);
13         initial begin
14             #10 i1 = 1'b0; i2 = 1'b0;
15             #10 i1 = 1'b0; i2 = 1'b1;
16             #10 i1 = 1'b1; i2 = 1'b0;
17             #10 i1 = 1'b1; i2 = 1'b1;
18         end
19
20 endmodule
21
```

Project Summary | Schematic | gate_level.v | gate_level_tb.v

9 Cells 11 I/O Ports 14 Nets



gate_level.v | gate_level_tb.v | Untitled 3