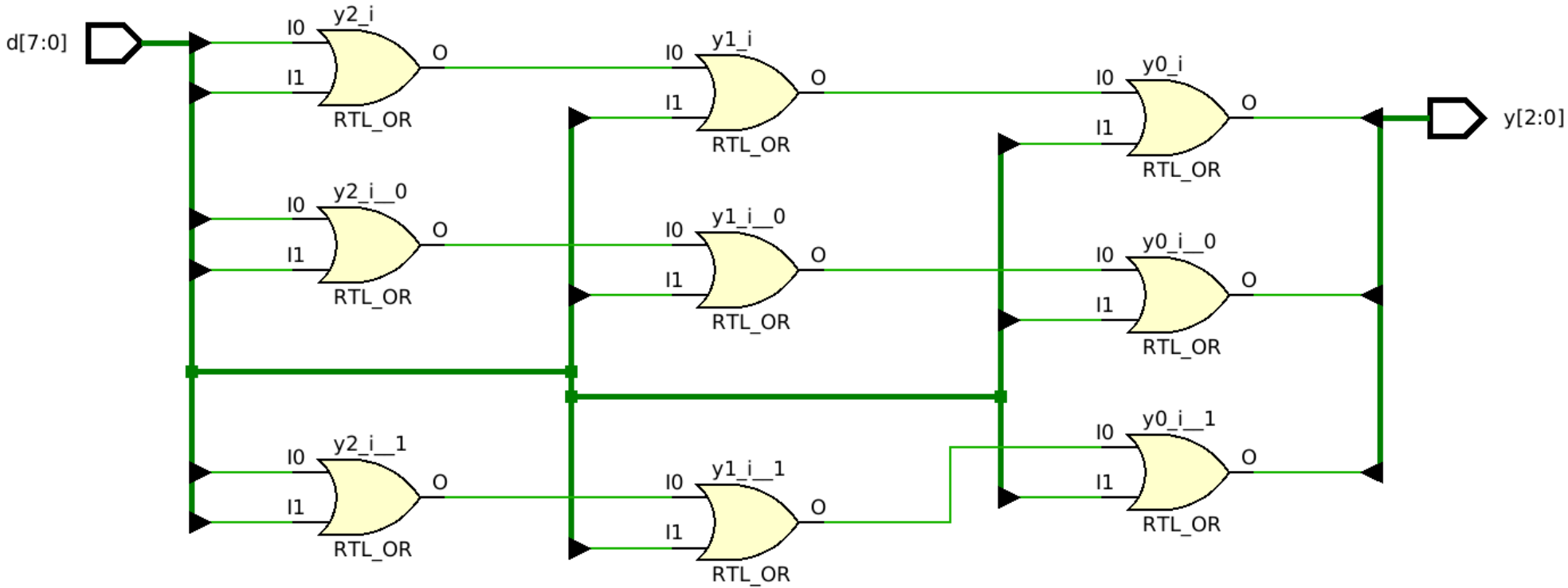
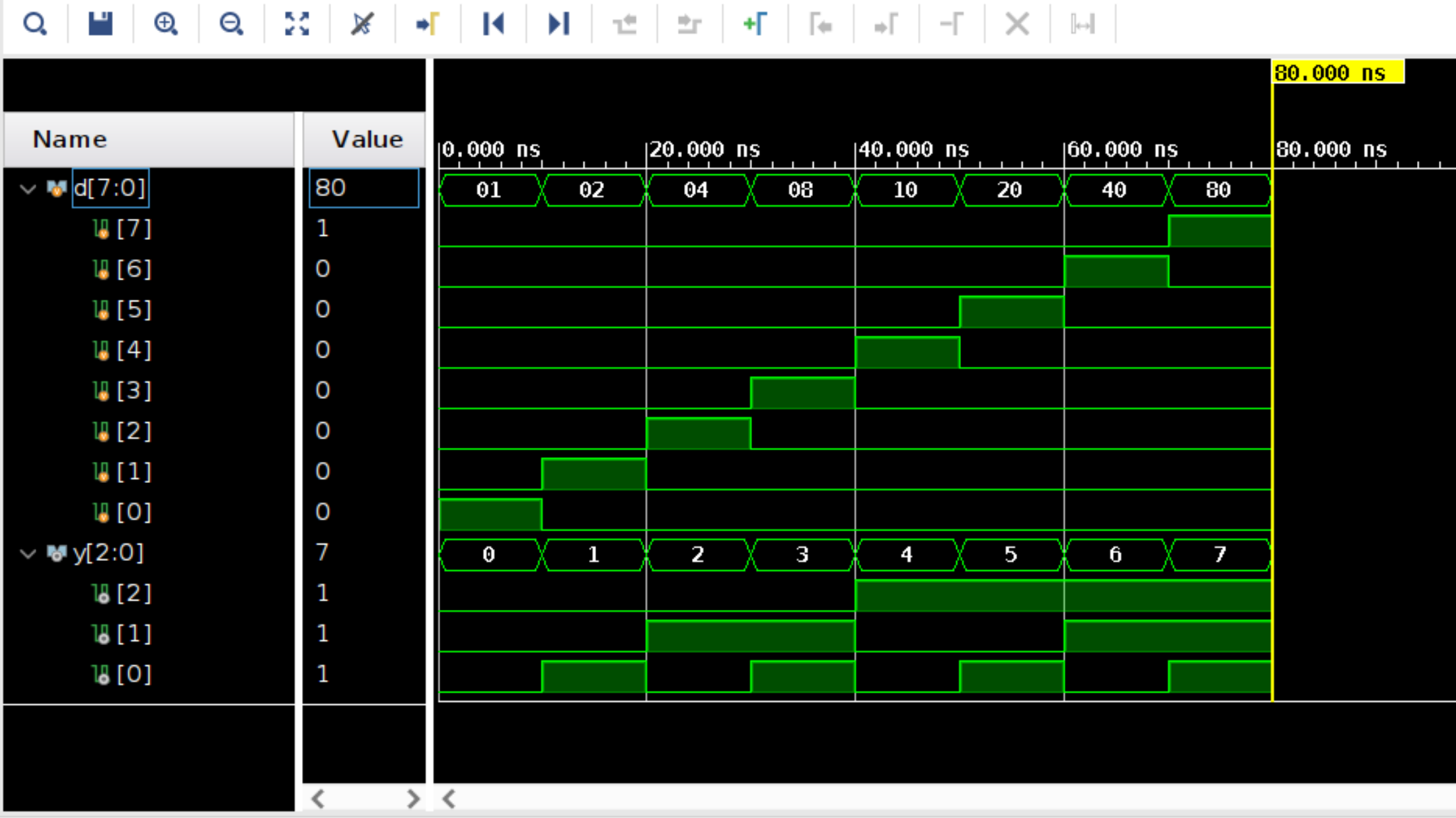
Project Summary | tb_oct_to_bin.v | oct_to_bin.v | Schematic

9 Cells 11 I/O Ports 16 Nets



tb_oct_to_bin.v | oct_to_bin.v | Untitled 3



Tcl Console | Messages | Log

```
Time = 0 | d = 00000001 | y = 000
Time = 10000 | d = 00000010 | y = 001
Time = 20000 | d = 00000100 | y = 010
Time = 30000 | d = 00001000 | y = 011
Time = 40000 | d = 00010000 | y = 100
Time = 50000 | d = 00100000 | y = 101
Time = 60000 | d = 01000000 | y = 110
Time = 70000 | d = 10000000 | y = 111
$stop called at time : 80 ns : File "/home/itzzinfinity/Cozy_Drive/100daysofRTL/day_033/project_1/pr
```

Type a Tcl command here

tb_oct_to_bin.v | oct_to_bin.v | Untitled 3

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_033/project_1/project_1.srcs/sources_1/new/oct_to_bin.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/06/2024 07:23:13 AM
5  // Module Name: oct_to_bin
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module oct_to_bin(
10     input[7:0]d,
11     output[2:0]y);
12
13         or (y[0],d[1],d[3],d[5],d[7]);
14         or (y[1],d[2],d[3],d[6],d[7]);
15         or (y[2],d[4],d[5],d[6],d[7]);
16         //assign y[0] = d[1]|d[3]|d[5]|d[7];
17         //assign y[1] = d[2]|d[3]|d[6]|d[7];
18         //assign y[2] = d[4]|d[5]|d[6]|d[7];
19
20 endmodule
21
22
```

tb_oct_to_bin.v × | oct_to_bin.v × | Untitled 3 ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_033/project_1/project_1.srcs/sim_1/new/tb_oct_to_bin.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/24/2024 07:25:10 AM
5   // Module Name: tb_oct_to_bin
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module tb_oct_to_bin;
9
10    reg [7:0] d;
11    wire [2:0] y;
12
13    oct_to_bin DUT (.d(d),.y(y));
14
15    initial begin
16
17      $monitor("Time = %0t | d = %b | y = %b", $time, d, y);
18
19      d = 8'b00000001; #10; // Octal 0 -> Binary 000
20      d = 8'b00000010; #10; // Octal 1 -> Binary 001
21      d = 8'b00000100; #10; // Octal 2 -> Binary 010
22      d = 8'b00001000; #10; // Octal 3 -> Binary 011
23      d = 8'b00010000; #10; // Octal 4 -> Binary 100
24      d = 8'b00100000; #10; // Octal 5 -> Binary 101
25      d = 8'b01000000; #10; // Octal 6 -> Binary 110
26      d = 8'b10000000; #10; // Octal 7 -> Binary 111
27
28      $stop;
29    end
30
31  endmodule
32
33
```