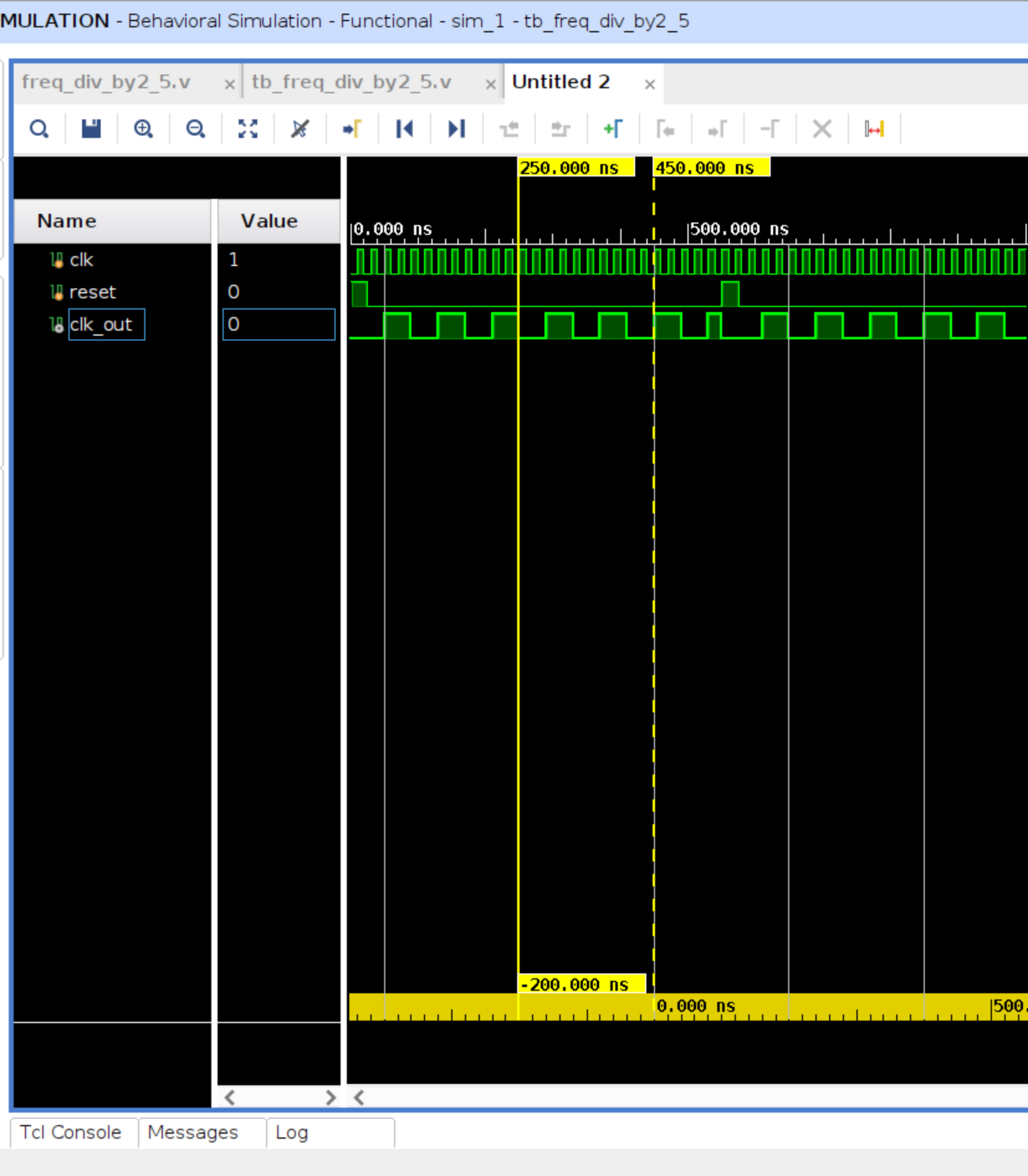
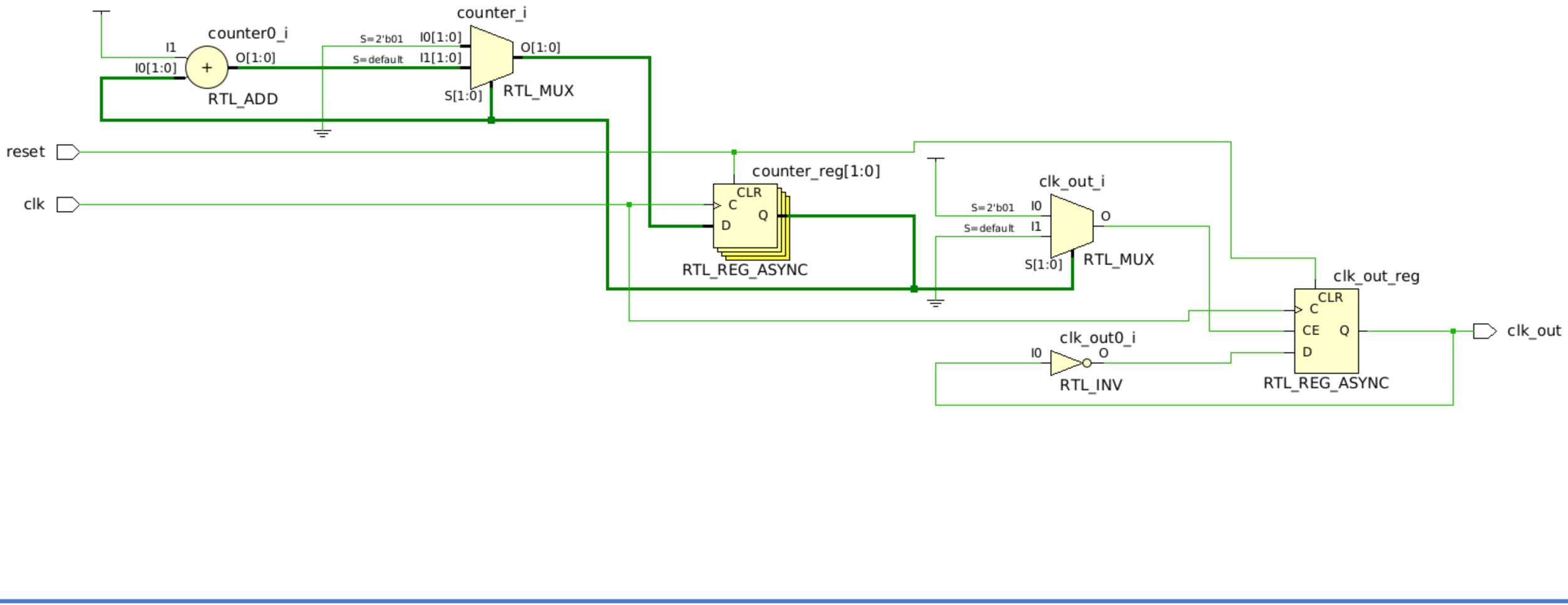

MULATION - Behavioral Simulation - Functional - sim_1 - tb_freq_div_by2_5
freq_div_by2_5.v
tb_freq_div_by2_5.v
Untitled 2
Name
Value
clk
1
reset
0
clk_out
0
250.000 ns
450.000 ns
0.000 ns
500.000 ns
-200.000 ns
0.000 ns
500.
Tcl Console
Messages
Log

Project Summary | freq_div_by2_5.v * | Schematic | tb_freq_div_by2_5.v | Schematic (2)

7 Cells 3 I/O Ports 13 Nets



Tcl Console | Messages | Log | Reports | Design Runs

freq_div_by2_5.v * | tb_freq_div_by2_5.v | Untitled 2

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_073/project_1/project_1.srcs/sources_1/new/freq_div_by2_5.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 12/03/2024 12:05:02 AM
5   // Module Name: freq_div_by2_5
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module freq_div_by2_5 (
9       input clk,
10      input reset,
11      output reg clk_out
12  );
13      reg [1:0] counter;
14      reg [1:0] accumulator; // Accumulator for fractional part
15
16      always @(posedge clk or posedge reset) begin
17          if (reset) begin
18              counter <= 0;
19              accumulator <= 0;
20              clk_out <= 0;
21          end else begin
22              accumulator <= accumulator + 2; // Add fractional part (0.5 = 2 in 4-scale)
23              if (accumulator >= 4) begin
24                  accumulator <= accumulator - 4; // Reset accumulator after a full count
25                  counter <= counter + 1;        // Add extra cycle
26              end
27
28              if (counter == 1) begin
29                  counter <= 0;          // Toggle every 2.5 cycles
30                  clk_out <= ~clk_out; // Toggle clk_out
31              end else begin
32                  counter <= counter + 1;
33              end
34          end
35      end
36  endmodule
37
```

Tcl Console | Messages | Log

freq_div_by2_5.v | **tb_freq_div_by2_5.v** | Untitled 2

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_073/project_1/project_1.srcs/sim_1/new/tb_freq_div_by2_5.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 12/03/2024 12:10:26 AM
5   // Module Name: tb_freq_div_by2_5
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module tb_freq_div_by2_5;
9       reg clk;
10      reg reset;
11      wire clk_out;
12
13      freq_div_by2_5 DUT (
14          .clk(clk),
15          .reset(reset),
16          .clk_out(clk_out)
17      );
18
19      always #10 clk = ~clk;
20
21      initial begin
22          clk = 0;
23          reset = 1;
24          #25 reset = 0;
25          #500;
26          #25 reset = 1;
27          #25 reset = 0;
28          #500;
29          $finish;
30      end
31      initial begin
32          $monitor("Time = %0t | clk = %b | reset = %b | clk_out = %b",
33                   $time, clk, reset, clk_out);
34      end
35  endmodule
36
```

Tcl Console | Messages | Log