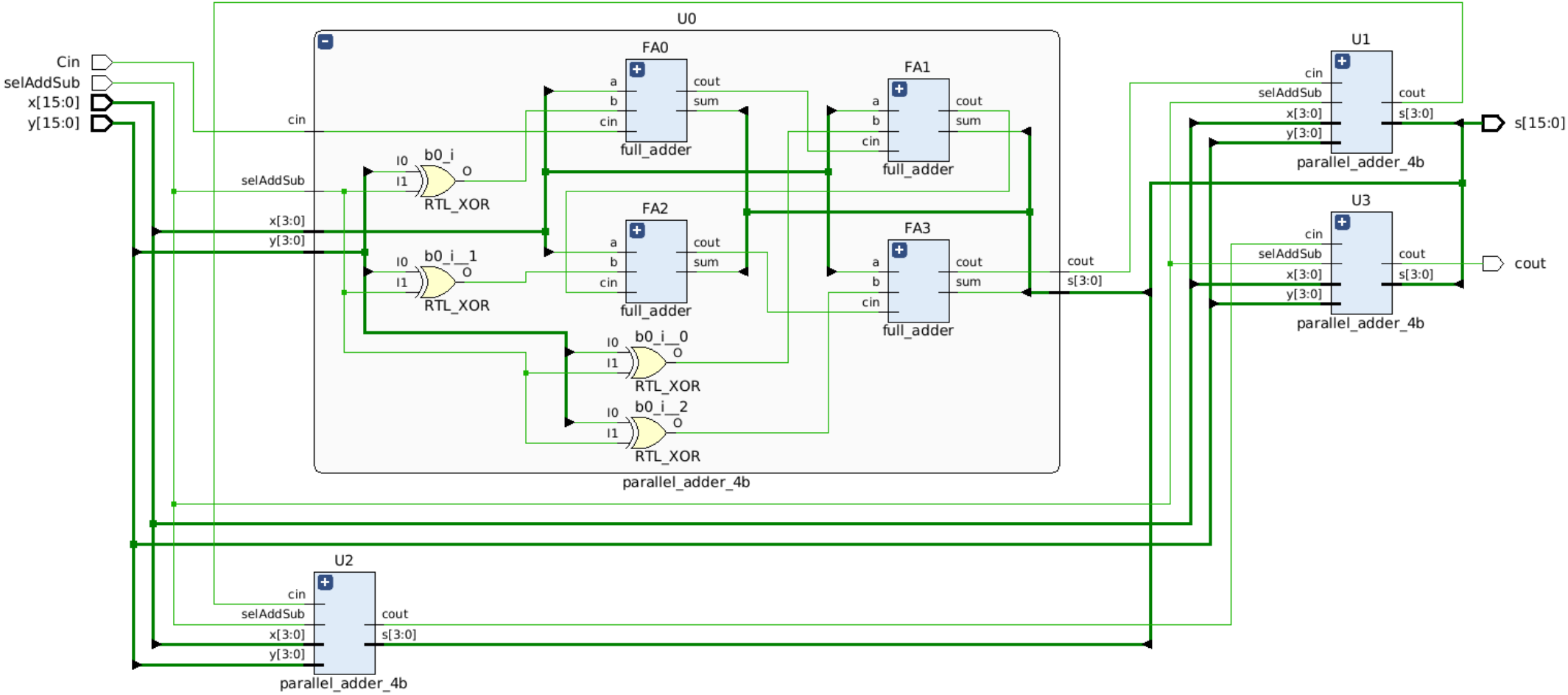
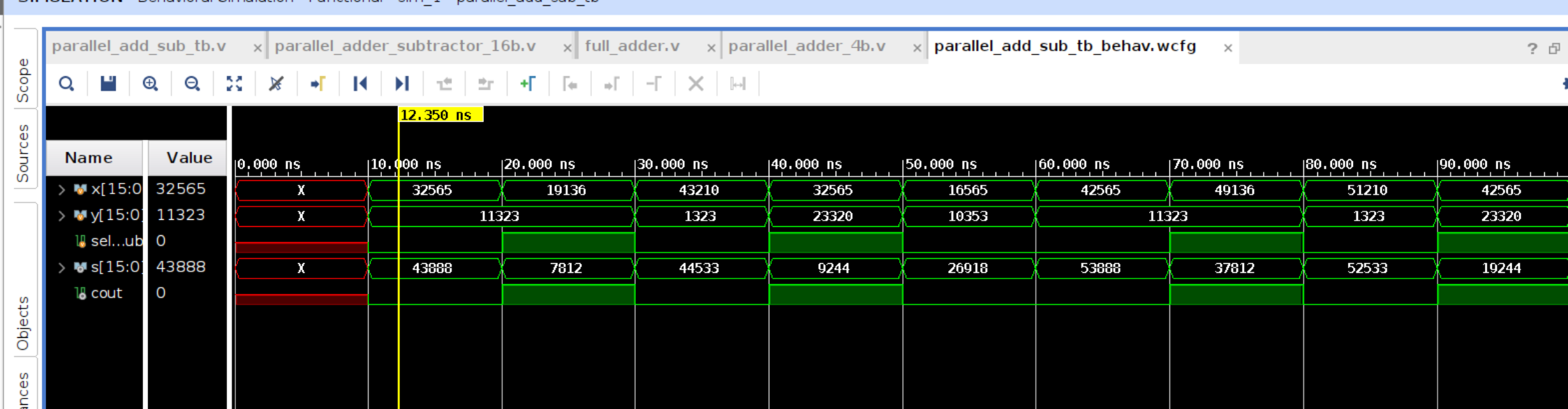
ELABORATED DESIGN - xc7a12ticsg325-1L

Sources

Project Summary | parallel_add_sub_tb.v | parallel_adder_subtractor_16b.v | full_adder.v | parallel_adder_4b.v | Schematic

12 Cells 51 I/O Ports 76 Nets




parallel_add_sub_tb.v
parallel_adder_subtractor_16b.v
full_adder.v
parallel_adder_4b.v
parallel_add_sub_tb_behav.wcfg
Scope
Sources
Objects
12.350 ns
Name
Value
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
x[15:0
32565
X
32565
19136
43210
32565
16565
42565
49136
51210
42565
y[15:0]
11323
X
11323
1323
23320
10353
11323
1323
23320
sel...ub
0
s[15:0]
43888
X
43888
7812
44533
9244
26918
53888
37812
52533
19244
cout
0

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_1.srcs/sources_1/new/parallel_adder_subtractor_16b.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/30/2024 09:14:36 PM
5  // Module Name: parallel_adder_subtractor_16b
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module parallel_adder_subtractor_16b(
10     input selAddSub,              // 0 for addition, 1 for subtraction
11     input [15:0] x, y,            // 16-bit inputs
12     output [15:0] s,              // 16-bit sum/difference
13     output cout,                   // Carry-out/borrow-out from the most significant bit
14     input Cin
15 );
16
17     wire [2:0] c;                 // Carry/borrow between the 4-bit adders
18
19     parallel_adder_4b U0 (
20         .selAddSub(selAddSub),.x(x[3:0]),.y(y[3:0]),.s(s[3:0]),.cout(c[0]),.cin(Cin)
21     );
22
23     parallel_adder_4b U1 (
24         .selAddSub(selAddSub),
25         .x(x[7:4]), .y(y[7:4]),.s(s[7:4]),.cout(c[1]),.cin(c[0])
26     );
27
28     parallel_adder_4b U2 (
29         .selAddSub(selAddSub),.x(x[11:8]),.y(y[11:8]),.s(s[11:8]),.cout(c[2]),.cin(c[1])
30     );
31
32     parallel_adder_4b U3 (
33         .selAddSub(selAddSub), .x(x[15:12]),.y(y[15:12]),.s(s[15:12]),.cout(cout),.cin(c[2])
34     );
35
36 endmodule
37
38
39
```

parallel_add_sub_tb.v | parallel_adder_subtractor_16b.v | full_adder.v | parallel_adder_4b.v | parallel_add_sub_tb_behav.wcfg

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_1.srcs/sim_1/new/parallel_add_sub_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 09/30/2024 09:14:36 PM
5   // Module Name: parallel_adder_subtractor_16b
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module parallel_add_sub_tb;
9       reg [15:0] x, y;
10      reg selAddSub;
11      wire [15:0] s;
12      wire cout;
13      reg Cin;
14
15      parallel_adder_subtractor_16b dut (
16          .x(x),
17          .y(y),
18          .selAddSub(selAddSub),
19          .s(s),
20          .cout(cout),.Cin(Cin)
21      );
22
23      initial begin
24          $display("x          y         Cin    selAddSub       | s          cout");
25          $monitor("x = %d, y = %d, Cin =%b    selAddSub = %b | s = %d, cout = %b", x, y,Cin, selAddSub, s, cout);
26          #10 x = 16'd32565; y = 16'd11323; selAddSub =1'b0; Cin = 0;
27          #10 x = 16'd19136; y = 16'd11323; selAddSub =1'b1; Cin = 0;
28          #10 x = 16'd43210; y = 16'd1323; selAddSub =1'b0;  Cin = 0;
29          #10 x = 16'd32565; y = 16'd23320; selAddSub =1'b1; Cin = 0;
30          #10 x = 16'd16565; y = 16'd10353; selAddSub =1'b0; Cin = 0;
31          #10 x = 16'd42565; y = 16'd11323; selAddSub =1'b0; Cin = 0;
32          #10 x = 16'd49136; y = 16'd11323; selAddSub =1'b1; Cin = 0;
33          #10 x = 16'd51210; y = 16'd1323; selAddSub =1'b0;  Cin = 0;
34          #10 x = 16'd42565; y = 16'd23320; selAddSub =1'b1; Cin = 0;
35          #10 x = 16'd56565; y = 16'd10353; selAddSub =1'b0; Cin = 0;
36
37          $finish;
38      end
39  endmodule
```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_1.srcs/sources_1/new/parallel_adder_4b.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 09/30/2024 09:14:36 PM
5  // Module Name: parallel_adder_subtractor_16b
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module parallel_adder_4b(
9      input selAddSub,
10     input [3:0] x, y,
11     input cin,              // Added carry-in input
12     output [3:0] s,
13     output cout             // Carry-out signal
14 );
15
16     wire [2:0] c;
17
18     full_adder FA0(.a(x[0]), .b(y[0]^selAddSub), .cin(cin),      .sum(s[0]), .cout(c[0]));
19     full_adder FA1(.a(x[1]), .b(y[1]^selAddSub), .cin(c[0]),    .sum(s[1]), .cout(c[1]));
20     full_adder FA2(.a(x[2]), .b(y[2]^selAddSub), .cin(c[1]),    .sum(s[2]), .cout(c[2]));
21     full_adder FA3(.a(x[3]), .b(y[3]^selAddSub), .cin(c[2]),    .sum(s[3]), .cout(cout));
22
23 endmodule
24
25
```

Tcl Console × Messages Log

```
# run 1000ns
x         y         Cin    selAddSub       | s         cout
x =     x, y =     x, Cin =x    selAddSub = x | s =     x, cout = x
x = 32565, y = 11323, Cin =0    selAddSub = 0 | s = 43888, cout = 0
x = 19136, y = 11323, Cin =0    selAddSub = 1 | s =  7812, cout = 1
x = 43210, y =  1323, Cin =0    selAddSub = 0 | s = 44533, cout = 0
x = 32565, y = 23320, Cin =0    selAddSub = 1 | s =  9244, cout = 1
x = 16565, y = 10353, Cin =0    selAddSub = 0 | s = 26918, cout = 0
x = 42565, y = 11323, Cin =0    selAddSub = 0 | s = 53888, cout = 0
x = 49136, y = 11323, Cin =0    selAddSub = 1 | s = 37812, cout = 1
x = 51210, y =  1323, Cin =0    selAddSub = 0 | s = 52533, cout = 0
x = 42565, y = 23320, Cin =0    selAddSub = 1 | s = 19244, cout = 1
$finish called at time : 100 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_009/project_1/project_1.srcs
```

Type a Tcl command here