



Name	Value
clk	0
reset	0
push	1
pop	0
> data_in[7:0]	1
> data_out[7:0]	X
full	0
empty	1



## Tcl Console



```

Compiling module xil_defaultlib.lifo_stack
Compiling module xil_defaultlib.lifo_stack_tb
Compiling module xil_defaultlib.glbl
Built simulation snapshot lifo_stack_tb_behav
INFO: [USF-XSim-69] 'elaborate' step finished in '2' seconds
INFO: [USF-XSim-4] XSim::Simulate design
INFO: [USF-XSim-61] Executing 'SIMULATE' step in '/home/itzzinfinity/Cozy Drive/100days
INFO: [USF-XSim-98] *** Running xsim
    with args "lifo_stack_tb_behav -key {Behavioral:sim_1:Functional:lifo_stack_tb} -tcl
INFO: [USF-XSim-8] Loading simulator feature
Time resolution is 1 ps
source lifo_stack_tb.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#     if { [llength [get_objects]] > 0 } {
#         add_wave /
#         set_property needs_save false [current_wave_config]
#     } else {
#         send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start
#     }
# }
# run 1000ns
Time=0 | push=0, pop=0, data_in= 0, data_out= x, full=0, empty=1
Time=10000 | push=1, pop=0, data_in= 1, data_out= x, full=0, empty=1
Time=15000 | push=1, pop=0, data_in= 1, data_out= x, full=0, empty=0
Time=20000 | push=1, pop=0, data_in= 2, data_out= x, full=0, empty=0
Time=30000 | push=1, pop=0, data_in= 3, data_out= x, full=0, empty=0
Time=40000 | push=1, pop=0, data_in= 4, data_out= x, full=0, empty=0
Time=50000 | push=1, pop=0, data_in= 5, data_out= x, full=0, empty=0
Time=60000 | push=1, pop=0, data_in= 6, data_out= x, full=0, empty=0
Time=70000 | push=1, pop=0, data_in= 7, data_out= x, full=0, empty=0
Time=80000 | push=1, pop=0, data_in= 8, data_out= x, full=0, empty=0
Time=90000 | push=1, pop=0, data_in= 9, data_out= x, full=0, empty=0
Time=100000 | push=1, pop=0, data_in= 10, data_out= x, full=0, empty=0
Time=110000 | push=0, pop=1, data_in= 10, data_out= x, full=0, empty=0
Time=115000 | push=0, pop=1, data_in= 10, data_out= 10, full=0, empty=0
Time=125000 | push=0, pop=1, data_in= 10, data_out= 9, full=0, empty=0
Time=135000 | push=0, pop=1, data_in= 10, data_out= 8, full=0, empty=0
Time=145000 | push=0, pop=1, data_in= 10, data_out= 7, full=0, empty=0
Time=155000 | push=0, pop=1, data_in= 10, data_out= 6, full=0, empty=0
Time=165000 | push=0, pop=1, data_in= 10, data_out= 5, full=0, empty=0
Time=175000 | push=0, pop=1, data_in= 10, data_out= 4, full=0, empty=0
Time=185000 | push=0, pop=1, data_in= 10, data_out= 3, full=0, empty=0
Time=195000 | push=0, pop=1, data_in= 10, data_out= 2, full=0, empty=0
Time=205000 | push=0, pop=1, data_in= 10, data_out= 1, full=0, empty=1
$finish called at time : 210 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lifo_stack_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:06 . Memory (MB): peak =

```

Type a Tcl command here



lifo stack tb.v

```
/home/itzzinfinity/Cozy Drive/100daysofRTL/day_090/project_1/project_1.srscs/sim_1/new/lifo_stack_tb.v
```



```

2 ////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
3 // Engineer: Anjan Prasad
4 // Create Date: 12/20/2024 02:43:07 AM
5 // Module Name: lifo_stack_tb
6 ////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
7
8 module lifo_stack_tb;
9
10     parameter DATA_WIDTH = 8;
11     parameter STACK_DEPTH = 16;
12
13     reg clk, reset, push, pop;
14     reg [DATA_WIDTH-1:0] data_in;
15     wire [DATA_WIDTH-1:0] data_out;
16     wire full, empty;
17
18     lifo_stack #(
19         .DATA_WIDTH(DATA_WIDTH),
20         .STACK_DEPTH(STACK_DEPTH)
21     ) DUT (
22         .clk(clk), .reset(reset),
23         .push(push), .pop(pop),
24         .data_in(data_in), .data_out(data_out),
25         .full(full), .empty(empty)
26     );
27
28     initial clk = 0;
29     always #5 clk = ~clk;
30     integer i;
31     initial begin
32         $monitor("Time=%0t | push=%b, pop=%b, data_in=%d, data_out=%d, full=%b, empty=%b",
33             $time, push, pop, data_in, data_out, full, empty);
34
35         reset = 1; push = 0; pop = 0; data_in = 0;
36         #10 reset = 0;
37         push = 1;
38
39         for (i = 1; i <= 10; i = i + 1) begin    // Push data
40             data_in = i;
41             #10;
42         end
43         push = 0;
44
45         pop = 1;
46         #100;
47         pop = 0;
48         $finish;
49     end
50 endmodule
51

```