⟳ | ⊹ | + | − | C | 1 Cell | 19 I/O Ports | 19 Nets

data0_i

addr[3:0] ▷──── A[3:0]   O[14:0] ────▷ data[14:0]

RTL_ROM

Waveform Viewer

Tabs: rom_15x15.v | tb_rom_15x15.v | Untitled 6*

Name	Value															
addr[3:0]	13	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
data[14:0]	14	257	...	3	4	261	6	...	72	9	10	11	588	...	14	...

Time markers: 0.000 ns, 50.000 ns, 100.000 ns, 131.283 ns

Tcl Console

```
#     }
# }
# run 1000ns
Address    Data
0000        257
0001       1026
0010          3
0011          4
0100        261
0101          6
0110       2055
0111         72
1000          9
1001         10
1010         11
1011        588
1100       2061
1101         14
1110       8271
$stop called at time : 150 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_088
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_rom_15x15_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

Type a Tcl command here

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_088/project_1/project_1.srcs/sources_1/new/rom_15x15.v

```verilog
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 12/18/2024 11:17:26 AM
5   // Module Name: rom_15x15
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module rom_15x15 (
9       input [3:0] addr,          // 4-bit address (15 locations require 4 bits)
10      output reg [14:0] data     // 15-bit data output
11  );
12
13      // ROM storage
14      reg [14:0] rom [14:0];
15
16      initial begin
17          rom[0]  = 15'b000000100000001;
18          rom[1]  = 15'b000010000000010;
19          rom[2]  = 15'b000000000000011;
20          rom[3]  = 15'b000000000000100;
21          rom[4]  = 15'b000000100000101;
22          rom[5]  = 15'b000000000000110;
23          rom[6]  = 15'b000100000000111;
24          rom[7]  = 15'b000000001001000;
25          rom[8]  = 15'b000000000001001;
26          rom[9]  = 15'b000000000001010;
27          rom[10] = 15'b000000000001011;
28          rom[11] = 15'b000001001001100;
29          rom[12] = 15'b000100000001101;
30          rom[13] = 15'b000000000001110;
31          rom[14] = 15'b010000001001111;
32      end
33
34      // Read data based on address
35      always @(*) begin
36          data = rom[addr];
37      end
38
39  endmodule
```

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/18/2024 11:19:40 PM
// Module Name: tb_rom_15x15
//////////////////////////////////////////////////////////////////////

module tb_rom_15x15;
    reg [3:0] addr;
    wire [14:0] data;

    rom_15x15 DUT (
        .addr(addr),
        .data(data)
    );

    initial begin
        $display("Address   Data");
        $monitor("%4b    %d", addr, data);

        addr = 4'b0000; #10; // Read data at address 0
        addr = 4'b0001; #10;
        addr = 4'b0010; #10;
        addr = 4'b0011; #10;
        addr = 4'b0100; #10;
        addr = 4'b0101; #10;
        addr = 4'b0110; #10;
        addr = 4'b0111; #10;
        addr = 4'b1000; #10;
        addr = 4'b1001; #10;
        addr = 4'b1010; #10;
        addr = 4'b1011; #10;
        addr = 4'b1100; #10;
        addr = 4'b1101; #10;
        addr = 4'b1110; #10; // Read data at address 14

        $stop;
    end
endmodule
```

Tcl Console   Messages   Log