Test_layout

| x | even_odd_checker.v | x | tb_even_odd_checker.v | x | Schematic | x | Schematic (2) | x |

1 Cell   9 I/O Ports   2 Nets

is_even0_i

number[7:0]

I0

O

RTL_INV
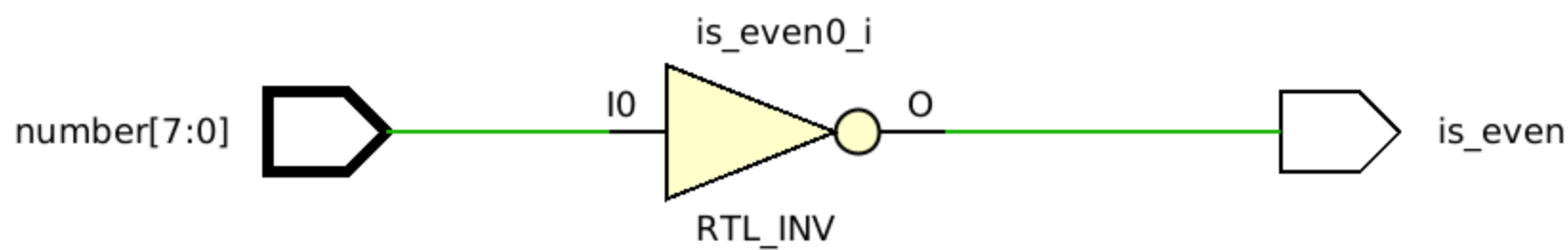
is_even

Name | **Value**

> number[7:0] | 2
is_even | 1

26.561 ns

| 0.000 ns | 20.000 ns | 40.000 ns | 60.000 ns |

number: 0 | 1 | 2 | 255 | 128 | 15

Tcl Console ✕ | Messages | Log
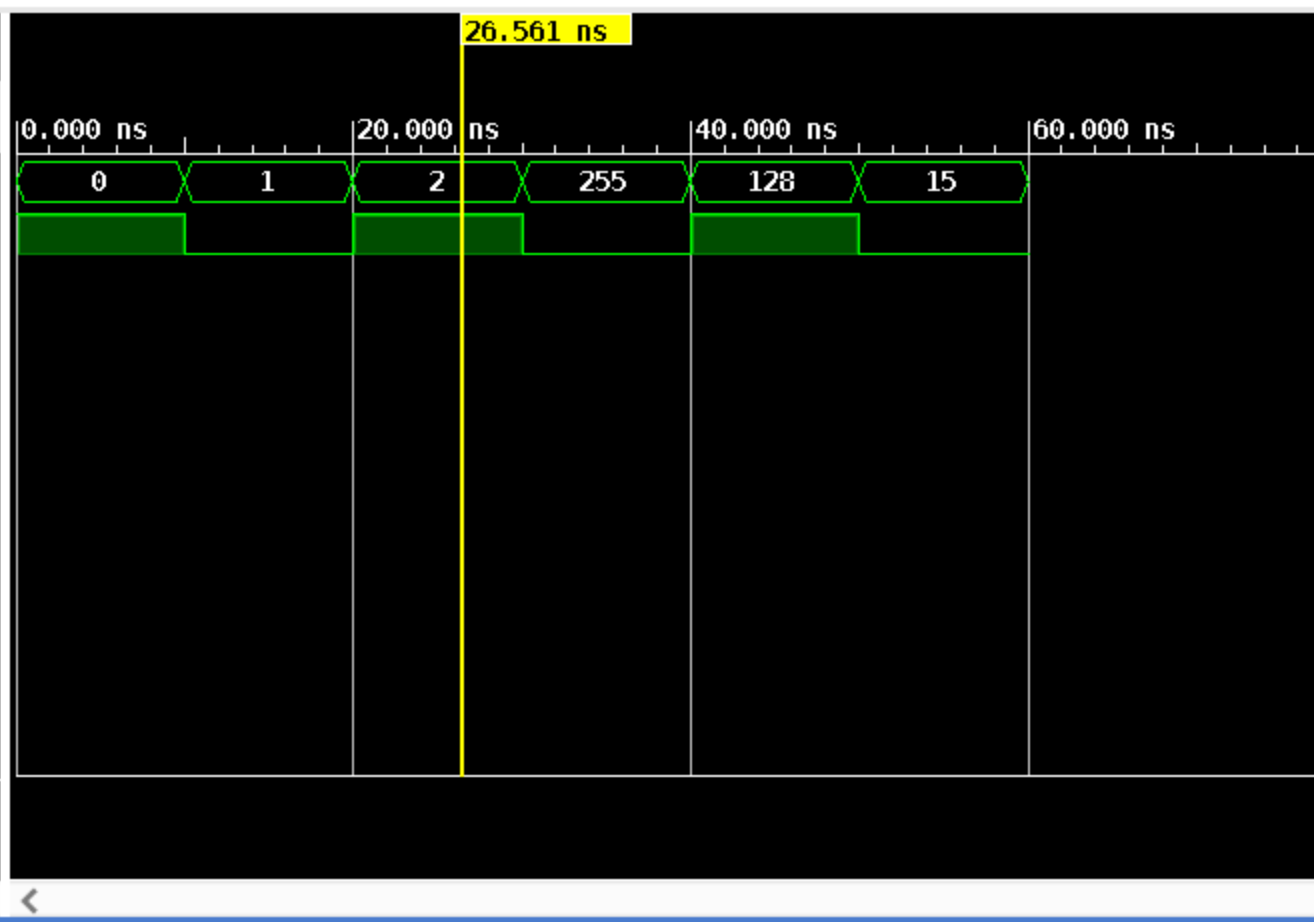
```
# }
# run 1000ns
Time = 0, Number =   0, Is Even = 1
Time = 10, Number =   1, Is Even = 0
Time = 20, Number =   2, Is Even = 1
Time = 30, Number = 255, Is Even = 0
Time = 40, Number = 128, Is Even = 1
Time = 50, Number =  15, Is Even = 0
$finish called at time : 60 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_077/project_1/pro
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_even_odd_checker_behav' loaded.
```

Type a Tcl command here

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/07/2024 09:14:47 AM
// Module Name: even_odd_checker
//////////////////////////////////////////////////////////////////////////////////

module even_odd_checker (
    input [7:0] number,
    output reg is_even   // Output: 1 if even, 0 if odd
);

    always @(*) begin
        is_even = ~number[0]; // Check the least significant bit (LSB)
    end

endmodule
```

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Engineer: Anjan Prasad
// Create Date: 12/07/2024 09:17:31 AM
// Module Name: tb_even_odd_checker
//////////////////////////////////////////////////////////////////////////////////

module tb_even_odd_checker;

    reg [7:0] number;
    wire is_even;

    even_odd_checker DUT (
        .number(number),
        .is_even(is_even)
    );

    initial begin

        $monitor("Time = %0d, Number = %d, Is Even = %b", $time, number, is_even);

        // Test cases
        number = 8'd0; #10;  // Test for 0 (Even)
        number = 8'd1; #10;  // Test for 1 (Odd)
        number = 8'd2; #10;  // Test for 2 (Even)
        number = 8'd255; #10; // Test for 255 (Odd)
        number = 8'd128; #10; // Test for 128 (Even)
        number = 8'd15; #10;  // Test for 15 (Odd)
        $finish;
    end

endmodule
```

Tcl Console | Messages | Log