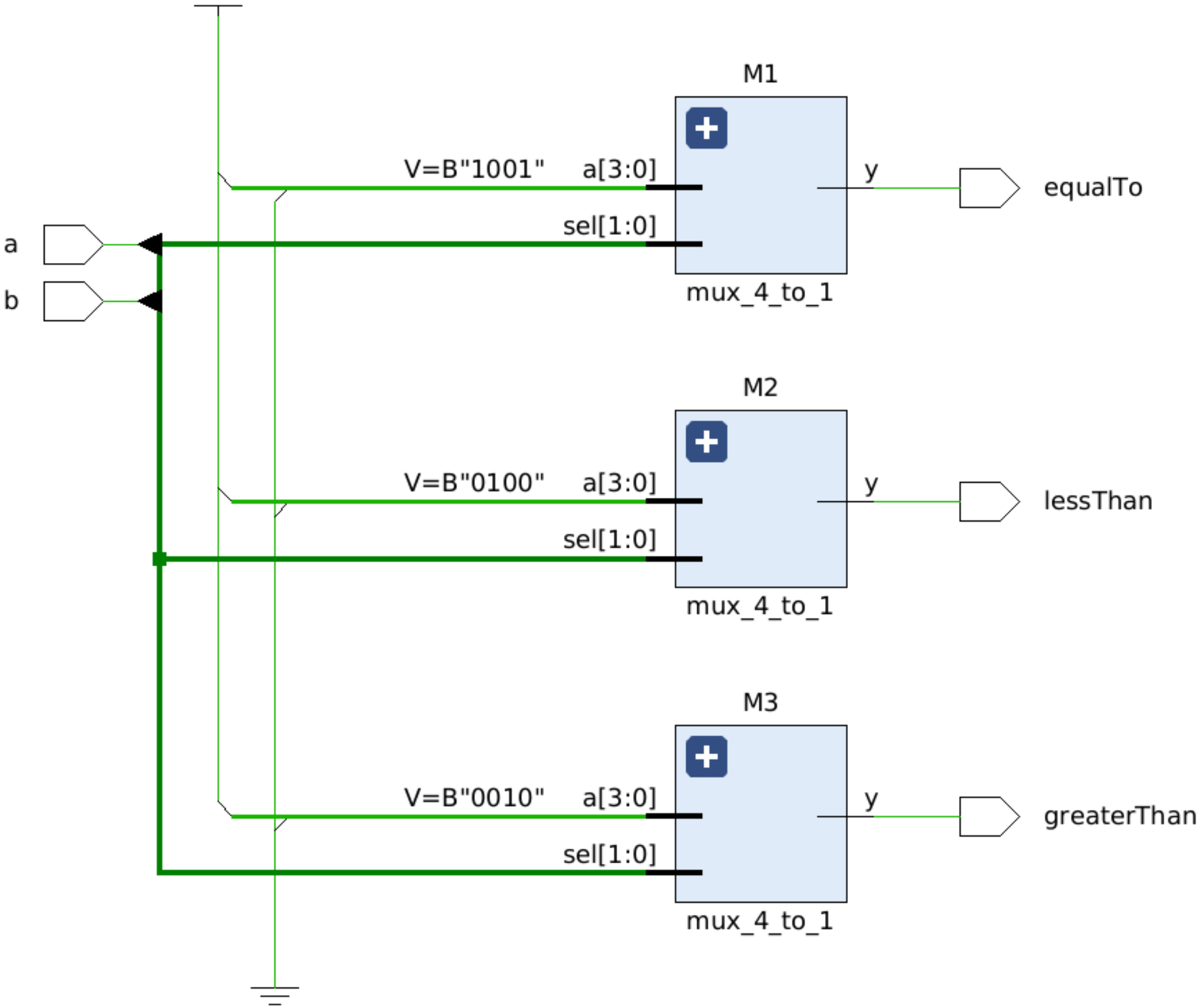
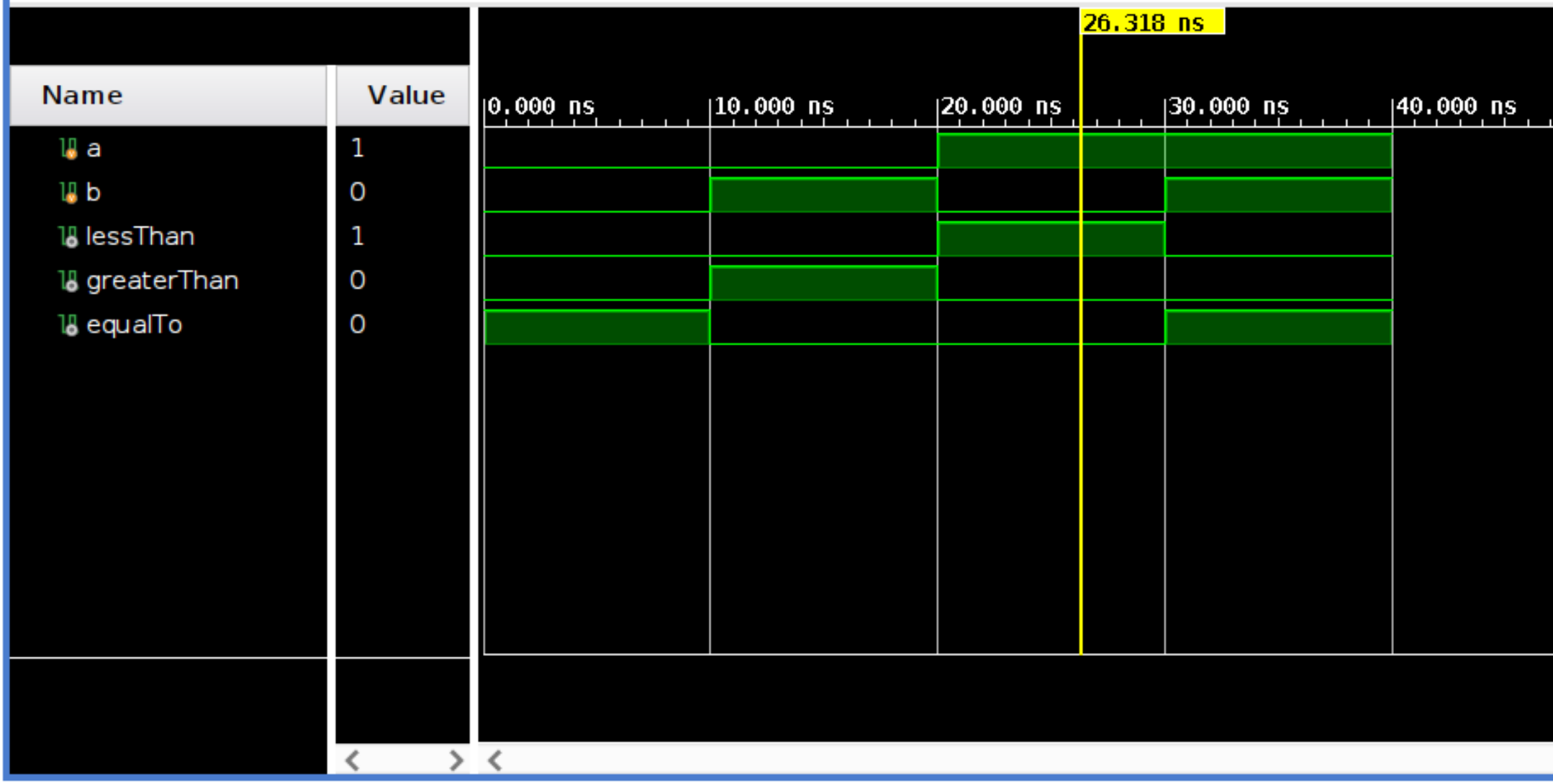
3 Cells 5 I/O Ports 7 Nets



SIMULATION - Behavioral Simulation - Functional - sim_1 - mux_comp_tb

Scope | Sources | Objects | Protocol Instances

mux_comp.v | mux_4_to_1.v | mux_comp_tb.v | Untitled 2



Tcl Console | Messages | Log

```
# }
# run 1000ns
a,  b   lessThan  greaterThan equalTo
0, 0  0         0           1
0, 1  0         1           0
1, 0  1         0           0
1, 1  0         0           1
$finish called at time : 40 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_032/project_
INFO: [USF-XSim-96] XSim completed. Design snapshot 'mux_comp_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

mux_comp.v | mux_4_to_1.v | mux_comp_tb.v | Untitled 2

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_032/project_1/project_1.srcs/sources_1/new/mux_comp.v

```
1
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/23/2024 06:10:57 AM
5  // Module Name: mux_comp
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module mux_comp(
10     input a,b,
11     output lessThan, greaterThan, equalTo
12     );
13
14     mux_4_to_1 M1(4'b1001,{a,b},equalTo);
15     mux_4_to_1 M2(4'b0100,{a,b},lessThan);
16     mux_4_to_1 M3(4'b0010,{a,b},greaterThan);
17
18 endmodule
19
```

mux_comp.v | mux_4_to_1.v | **mux_comp_tb.v** | Untitled 2

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_032/project_1/project_1.srcs/sim_1/new/mux_comp_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/23/2024 06:19:02 AM
5   // Module Name: mux_comp_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module mux_comp_tb;
10      reg a,b;
11      wire lessThan, greaterThan, equalTo;
12      mux_comp DUT(a,b,lessThan, greaterThan, equalTo);
13          initial begin
14              $display("a,  b   lessThan  greaterThan equalTo");
15              $monitor("%b, %b  %b        %b          %b",a,b,lessThan, greaterThan, equalTo);
16              a=0; b=0; #10;
17              a=0; b=1; #10;
18              a=1; b=0; #10;
19              a=1; b=1; #10;
20
21              $finish;
22          end
23  endmodule
24
```

mux_comp.v | **mux_4_to_1.v** | mux_comp_tb.v | Untitled 2

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_032/project_1/project_1.srcs/sources_1/new/mux_4_to_1.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/23/2024 06:11:25 AM
5   // Module Name: mux_4_to_1
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module mux_4_to_1(
10      input [3:0]a,
11      input [1:0] sel,
12      output y);
13
14          assign y = a[sel];
15
16  endmodule
17
```