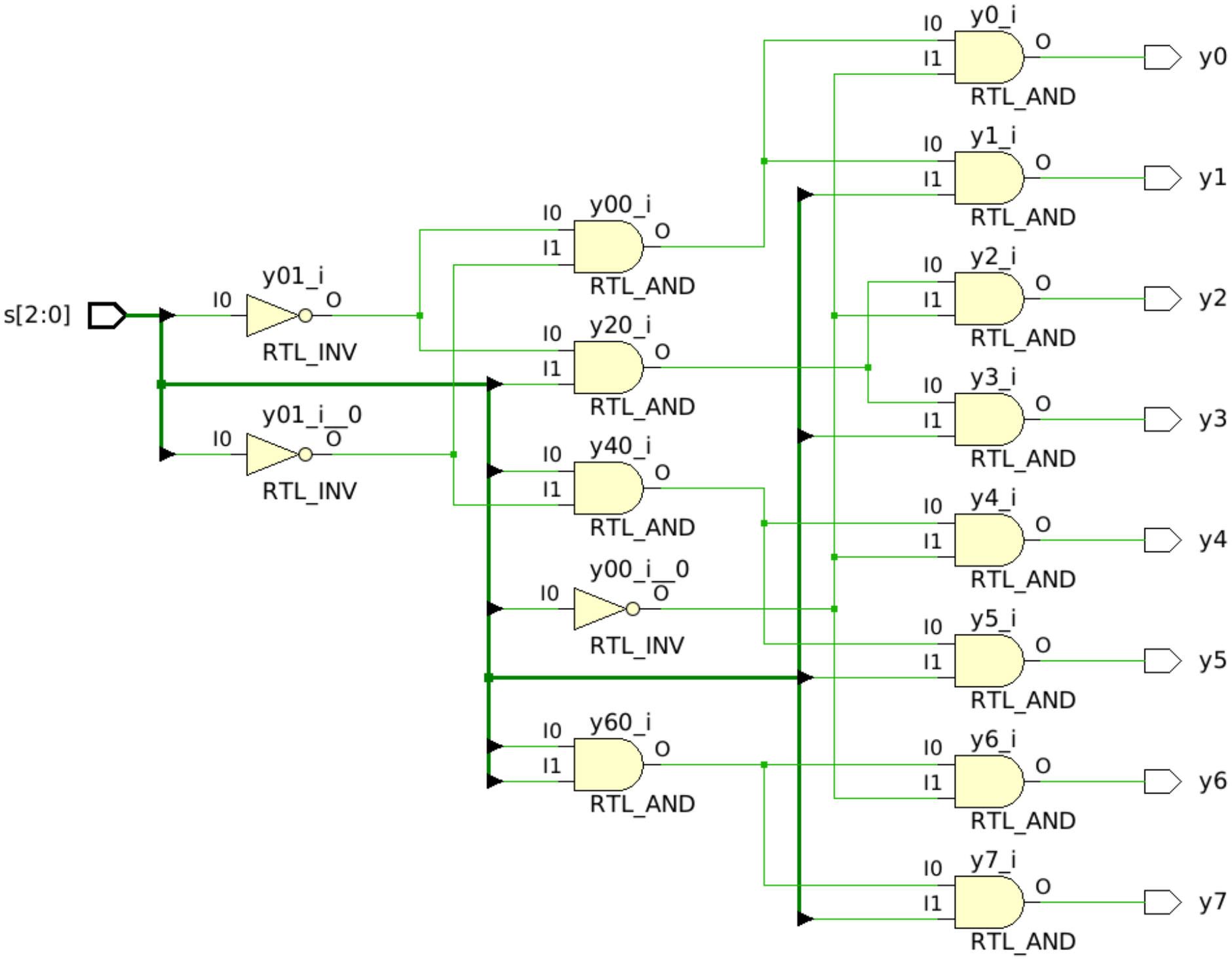
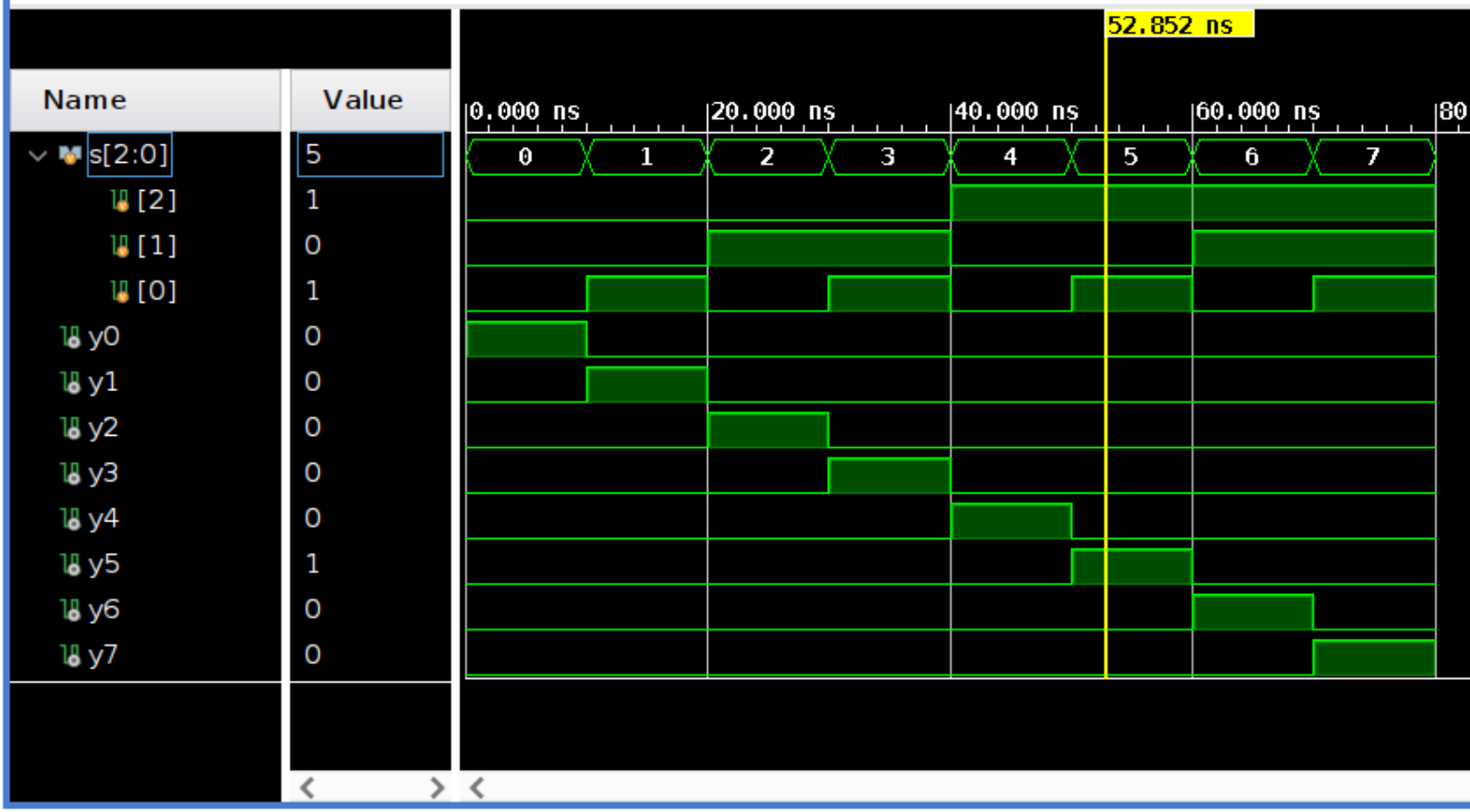
o_eight_decoder.v | Schematic | three_to_eight_decoder_tb.v

15 Cells 11 I/O Ports 18 Nets



three_to_eight_decoder.v | three_to_eight_decoder_tb.v | Untitled 3



Tcl Console | Messages | Log

```
# run 1000ns
s = 000, so at the output y0 = 1,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 001, so at the output y0 = 0,y1 = 1,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 010, so at the output y0 = 0,y1 = 0,y2 = 1,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 011, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 1,y4 = 0,y5 = 0,y6 = 0,y7 = 0
s = 100, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 1,y5 = 0,y6 = 0,y7 = 0
s = 101, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 1,y6 = 0,y7 = 0
s = 110, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 1,y7 = 0
s = 111, so at the output y0 = 0,y1 = 0,y2 = 0,y3 = 0,y4 = 0,y5 = 0,y6 = 0,y7 = 1
$finish called at time : 80 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_035/
```

Type a Tcl command here

Project Summary | three_to_eight_decoder.v | Schematic | three_to_eight_decoder_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_035/project_1/project_1.srcs/sources_1/new/three_to_eight_decoder.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/26/2024 06:41:24 AM
5  // Module Name: three_to_eight_decoder
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module three_to_eight_decoder(
9  input [2:0]s,
10 output y0,y1,y2,y3,y4,y5,y6,y7);
11 assign y0 = ~s[2]&~s[1]&~s[0];
12 assign y1 = ~s[2]&~s[1]&s[0];
13 assign y2 = ~s[2]&s[1]&~s[0];
14 assign y3 = ~s[2]&s[1]&s[0];
15 assign y4 = s[2]&~s[1]&~s[0];
16 assign y5 = s[2]&~s[1]&s[0];
17 assign y6 = s[2]&s[1]&~s[0];
18 assign y7 = s[2]&s[1]&s[0];
19 endmodule
```

Project Summary | three_to_eight_decoder.v | Schematic | three_to_eight_decoder_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_035/project_1/project_1.srcs/sim_1/new/three_to_eight_decoder_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/26/2024 06:43:54 AM
5  // Module Name: three_to_eight_decoder_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module three_to_eight_decoder_tb;
10     reg [2:0]s;
11     wire y0,y1,y2,y3,y4,y5,y6,y7;
12
13     three_to_eight_decoder DUT (s,y0,y1,y2,y3,y4,y5,y6,y7);
14
15       initial begin
16         $monitor("s = %b, so at the output y0 = %b,y1 = %b,y2 = %b,y3 = %b,y4 = %b,y5 = %b,y6 = %b,y7 = %b ",s,y0,y1,y2,y3,y4,y5,y6,y7);
17
18         s = 3'b000; #10;
19         s = 3'b001; #10;
20         s = 3'b010; #10;
21         s = 3'b011; #10;
22         s = 3'b100; #10;
23         s = 3'b101; #10;
24         s = 3'b110; #10;
25         s = 3'b111; #10;
26
27         $finish;
28       end
29
30 endmodule
```