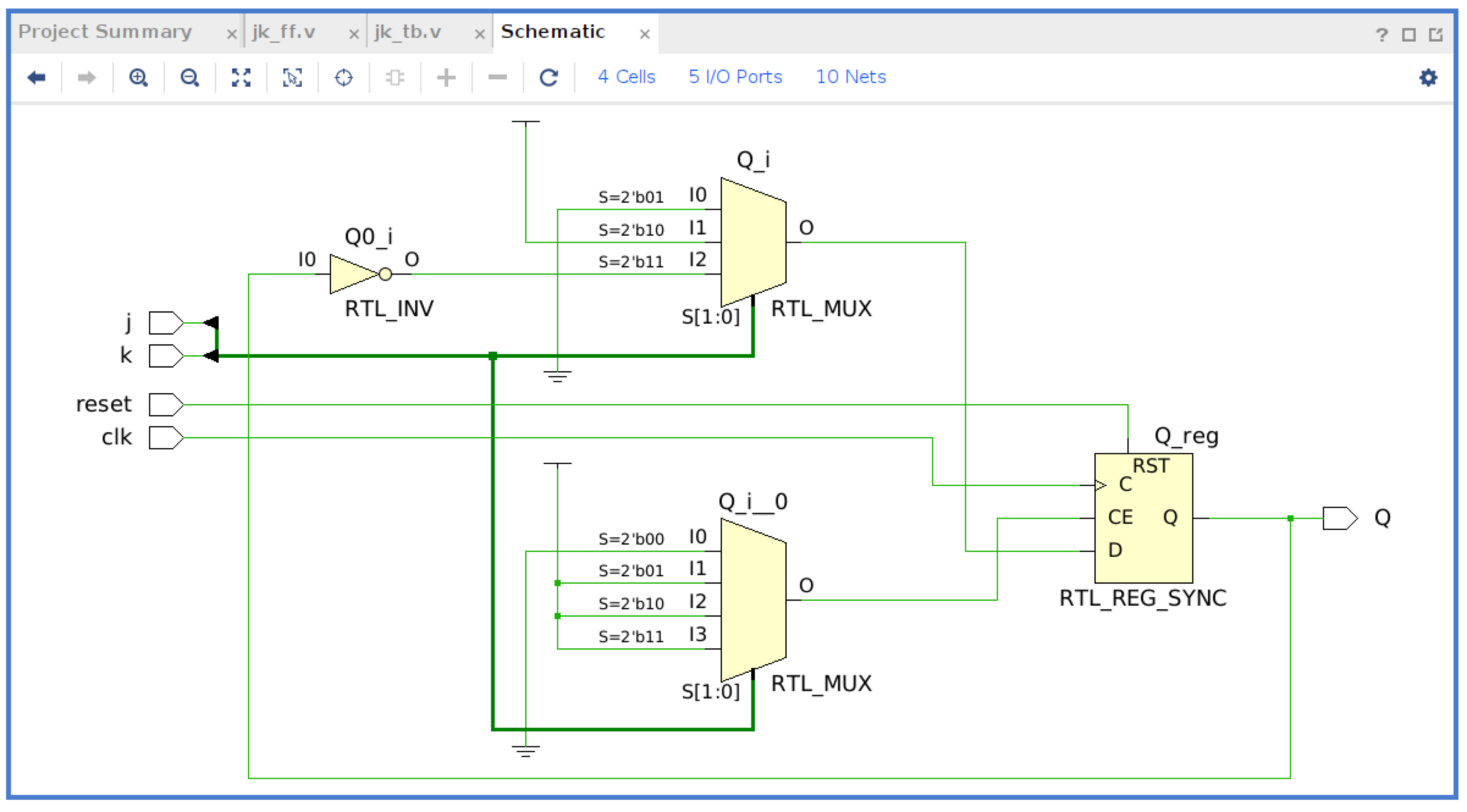
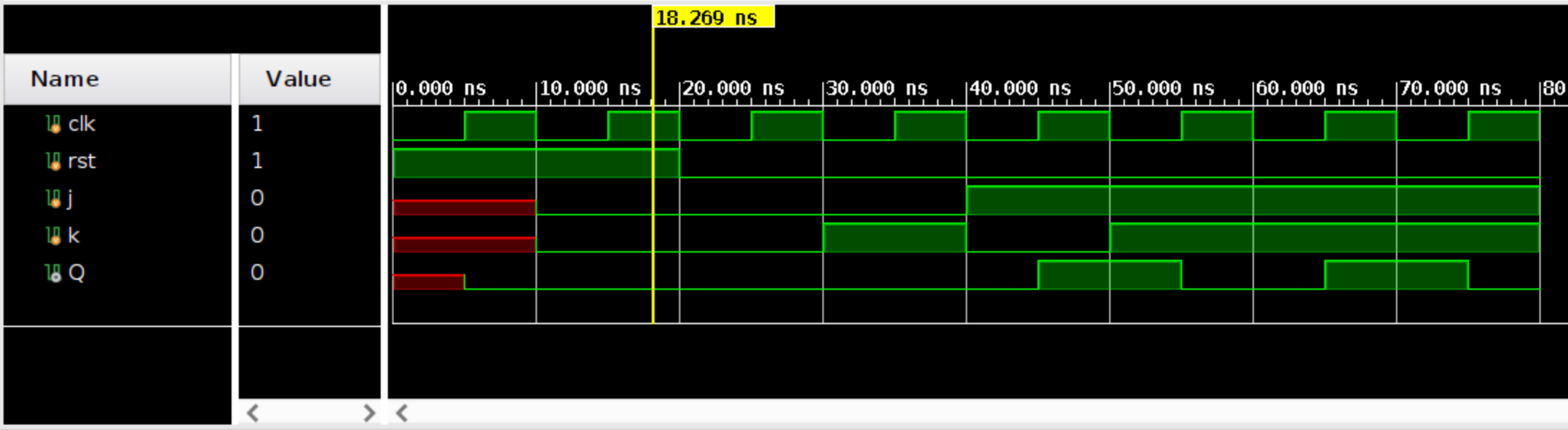

Project Summary
jk_ff.v
jk_tb.v
Schematic
4 Cells
5 I/O Ports
10 Nets
Q_i
S=2'b01
I0
S=2'b10
I1
S=2'b11
I2
O
S[1:0]
RTL_MUX
Q0_i
I0
O
RTL_INV
j
k
reset
clk
Q_i__0
S=2'b00
I0
S=2'b01
I1
S=2'b10
I2
S=2'b11
I3
O
S[1:0]
RTL_MUX
Q_reg
RST
C
CE
Q
D
RTL_REG_SYNC
Q

jk_ff.v | jk_tb.v * | Untitled 1



Tcl Console | Messages | Log

```
# run 1000ns
      clk: 0  J: x  K: x  Q: x
      clk: 1  J: x  K: x  Q: 0
      clk: 0  J: 0  K: 0  Q: 0
      clk: 1  J: 0  K: 0  Q: 0
      clk: 0  J: 0  K: 0  Q: 0
      clk: 1  J: 0  K: 0  Q: 0
      clk: 0  J: 0  K: 1  Q: 0
      clk: 1  J: 0  K: 1  Q: 0
      clk: 0  J: 1  K: 0  Q: 0
      clk: 1  J: 1  K: 0  Q: 1
      clk: 0  J: 1  K: 1  Q: 1
      clk: 1  J: 1  K: 1  Q: 0
      clk: 0  J: 1  K: 1  Q: 0
      clk: 1  J: 1  K: 1  Q: 1
      clk: 0  J: 1  K: 1  Q: 1
      clk: 1  J: 1  K: 1  Q: 0
$finish called at time : 80 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_047/project_1/project_1.srcs/sim
INFO: [USF-XSim-96] XSim completed. Design snapshot 'jk_tb_behav' loaded.
```

Type a Tcl command here

Project Summary | jk_ff.v | jk_tb.v * | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_047/project_1/project_1.srcs/sources_1/new/jk_ff.v

```
1
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/07/2024 07:43:15 AM
5  // Module Name: jk_ff
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module jk_ff(
10     input j,k,clk,reset,
11     output reg Q
12     );
13     always@(posedge clk)
14           begin
15             if({reset})
16             Q <= 1'b0;
17             else
18                 begin
19                 case({j,k})
20                 2'b00:Q<=Q;
21                 2'b01:Q<=1'b0;
22                 2'b10:Q<=1'b1;
23                 2'b11:Q<=~Q;
24                 endcase
25                 end
26         end
27
28 endmodule
29
30
31
32
```

Project Summary | jk_ff.v | jk_tb.v * | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_047/project_1/project_1.srcs/sim_1/new/jk_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/07/2024 07:51:48 AM
5  // Module Name: jk_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module jk_tb;
10 reg clk,rst,j,k;
11 wire Q;
12
13   jk_ff dut(j,k,clk,rst,Q);
14
15   initial begin
16   clk=0;
17   forever #5 clk=~clk;
18   end
19
20   initial
21     begin
22      rst=1; #10;
23
24      j = 1'b0; k = 1'b0; #10;
25
26      rst=0; #10;
27
28      j = 1'b0; k = 1'b1; #10;
29
30      j = 1'b1; k = 1'b0; #10;
31
32      j = 1'b1; k = 1'b1; #10;
33    end
34    initial begin
35    $monitor("\t clk: %d  J: %d  K: %d  Q: %d", clk, j, k, Q);
36    #80 $finish;
37    end
38
39 endmodule
```