```
Project Summary x Schematic x random expression.v x retb.v x
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 005/project 1/project 1.srcs/sources 1/new/random expression.v
`timescale lns / lps
   // Engineer:Anjan Prasad
   // Create Date: 09/26/2024 08:21:52 PM
   // Module Name: random expression
   7 :
8 :
9 (=)
   module random expression(
10 :
      input A,
   input B,
11 :
   input C,
   input D,
13 :
14
    output Y
15
      );
16
      assign Y = ( -A \& B) | (C \& -D) | (A \& -B \& D);
17
18 🗀
   endmodule
19 :
```

```
Project Summary
                  x Schematic
                                x random expression.v
                                                         x retb.v
/home/itzzinfinity/Cozy Drive/100daysofRTL/day 005/project 1/project 1.srcs/sim 1/new/r e tb.v
       ★ | → | ¾ | □ | □ | X | // | Ⅲ | ♀ |
     `timescale lns / lps
 2 🗇
    // Engineer: Anjan Prasad
 3 :
    // Create Date: 09/26/2024 08:21:52 PM
     // Module Name: random expression
 5
     7
 8
     module r_e_tb;
 9
10
        reg A, B, C, D;
11
12
        wire Y:
13
        random expression dut (A, B, C, D, Y);
14
15
        initial begin
16
17
            $display("A B C D | Y");
18
19
            $monitor("%b %b %b %b | %b", A, B, C, D, Y);
20
21
22
            A = 0; B = 0; C = 0; D = 0; #10;
23
            A = 0; B = 0; C = 0; D = 1; #10;
24
            A = 0; B = 0; C = 1; D = 0; #10;
25
            A = 0; B = 0; C = 1; D = 1; #10;
            A = 0; B = 1; C = 0; D = 0; #10;
26
27
            A = 0; B = 1; C = 0; D = 1; #10;
28
            A = 0; B = 1; C = 1; D = 0; #10;
29
            A = 0; B = 1; C = 1; D = 1; #10;
30
            A = 1; B = 0; C = 0; D = 0; #10;
31
            A = 1; B = 0; C = 0; D = 1; #10;
32
            A = 1; B = 0; C = 1; D = 0; #10;
33
            A = 1; B = 0; C = 1; D = 1; #10;
34
            A = 1; B = 1; C = 0; D = 0; #10;
35
            A = 1; B = 1; C = 0; D = 1; #10;
            A = 1; B = 1; C = 1; D = 0; #10;
36
37
            A = 1; B = 1; C = 1; D = 1; #10;
38
39
      $finish;
40
        end
41
42
     endmodule
```

43

