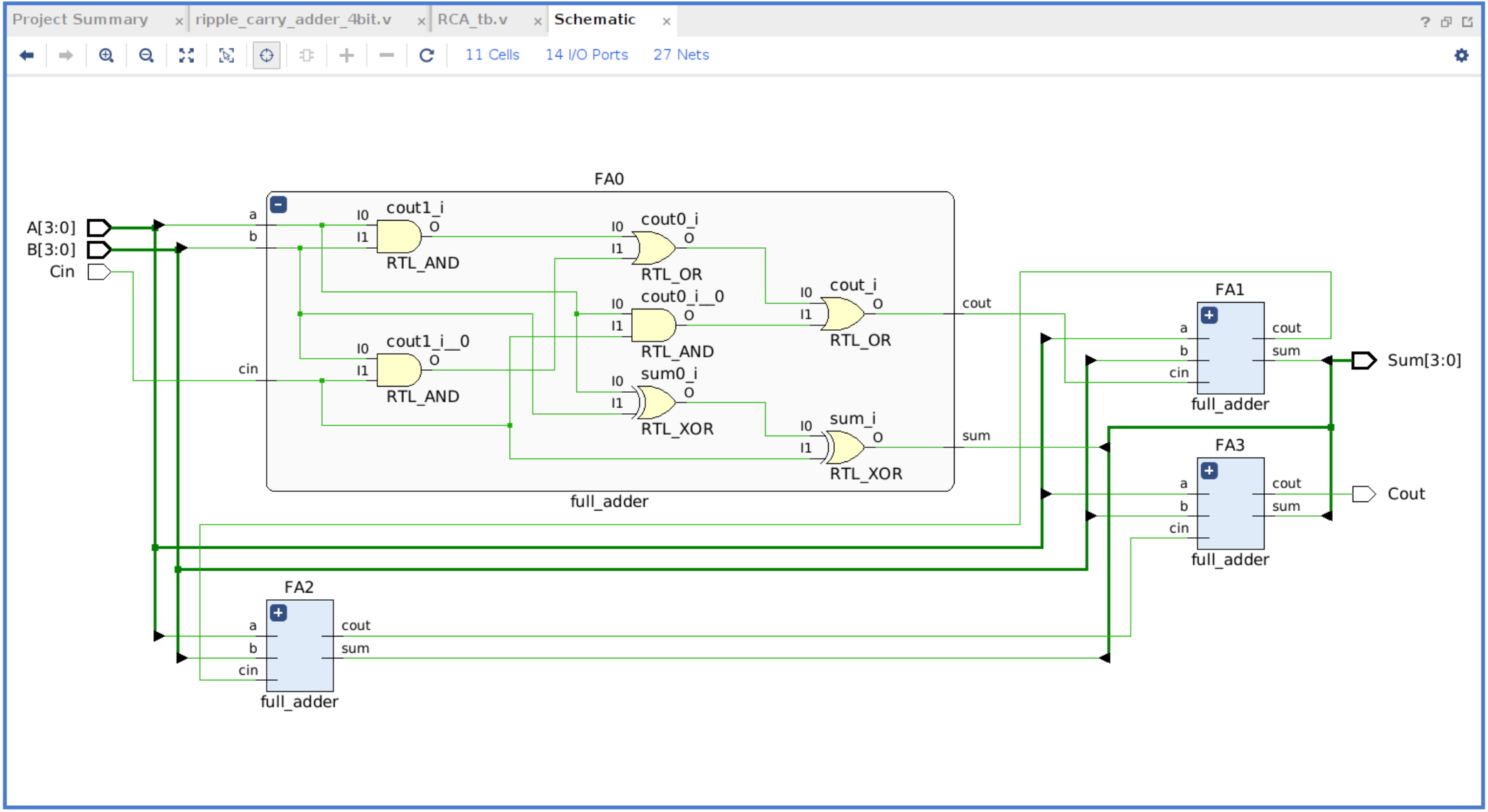

Project Summary
ripple_carry_adder_4bit.v
RCA_tb.v
Schematic
11 Cells
14 I/O Ports
27 Nets
FA0
A[3:0]
B[3:0]
Cin
a
b
cin
I0
I1
O
cout1_i
RTL_AND
cout0_i
RTL_OR
cout0_i__0
RTL_AND
cout1_i__0
RTL_AND
sum0_i
RTL_XOR
cout_i
RTL_OR
sum_i
RTL_XOR
cout
sum
full_adder
FA1
full_adder
FA2
full_adder
FA3
full_adder
Sum[3:0]
Cout

ripple_carry_adder_4bit.v | RCA_tb.v | Untitled 8*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_010/project_1/project_1.srcs/sources_1/new/ripple_carry_adder_4bit.v

```
1
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/01/2024 08:41:17 AM
5  // Module Name: ripple_carry_adder_4bit
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module ripple_carry_adder_4bit (
9      input [3:0] A, B,
10     input Cin,
11     output [3:0] Sum,
12     output Cout
13 );
14     wire c1, c2, c3;
15
16     full_adder FA0 (A[0], B[0], Cin, Sum[0], c1);
17     full_adder FA1 (A[1], B[1], c1, Sum[1], c2);
18     full_adder FA2 (A[2], B[2], c2, Sum[2], c3);
19     full_adder FA3 (A[3], B[3], c3, Sum[3], Cout);
20
21 endmodule
22
```

ripple_carry_adder_4bit.v | RCA_tb.v | Untitled 8*

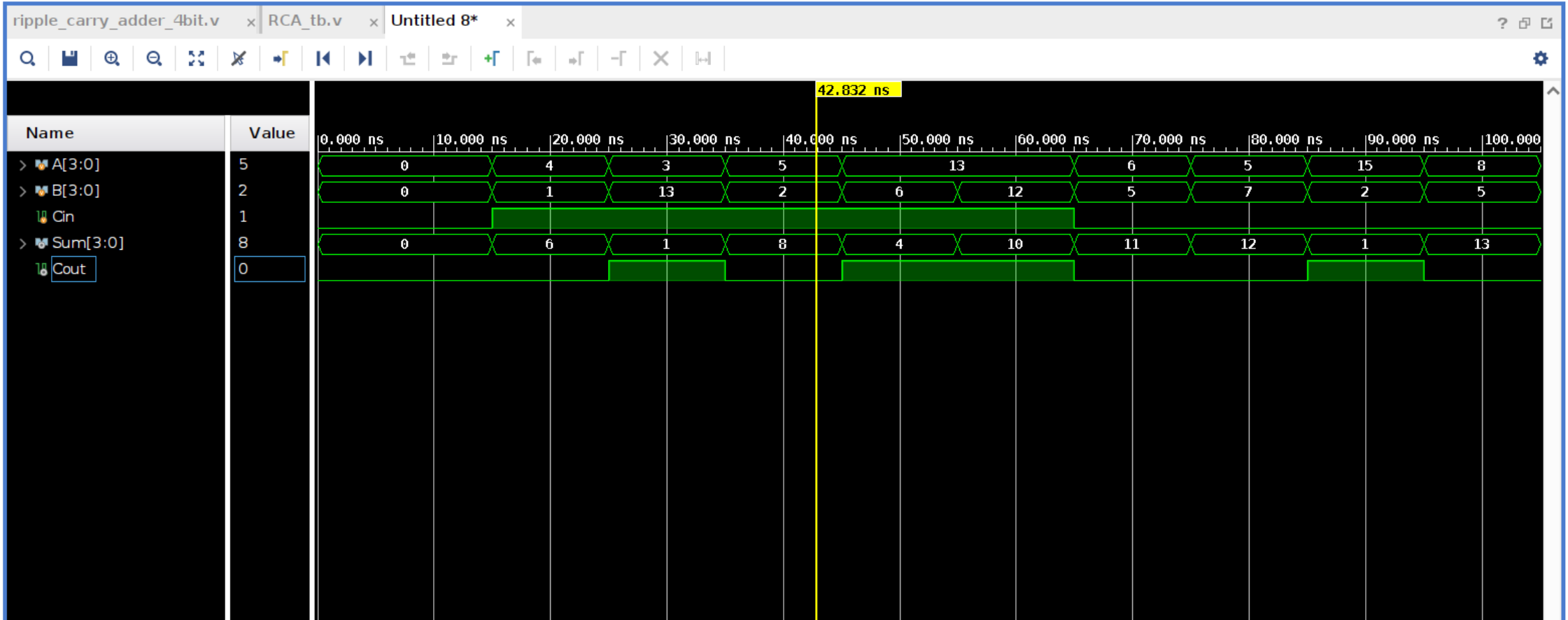
/home/itzzinfinity/Cozy Drive/100daysofRTL/day_010/project_1/project_1.srcs/sim_1/new/RCA_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/01/2024 08:41:17 AM
5   // Module Name: RCA_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module RCA_tb;
9   reg [3:0] A,B;
10  reg Cin;
11  wire [3:0] Sum;
12  wire Cout;
13  ripple_carry_adder_4bit DUT (A, B,Cin,Sum,Cout);
14  initial begin
15      A = 4'b0000;
16      B = 4'b0000;
17      Cin = 1'b0;
18      #5;
19  $display("A  +  B  (Cin)   =    Sum    Cout");
20  $monitor("%d + %d  (%d)    =    %d     %d", A, B,Cin,Sum, Cout*16);
21  repeat(10) begin
22  #10
23  A = $random % 16 ;
24  B = $random % 16 ;
25  Cin = $random;
26  end
27  $finish;
28  end
29
30  endmodule
31
```

Tcl Console | Messages | Log

```
# run 1000ns
A  +  B  (Cin)   =    Sum    Cout
 0 +  0  (0)     =     0              0
 4 +  1  (1)     =     6              0
 3 + 13  (1)     =     1             16
 5 +  2  (1)     =     8              0
13 +  6  (1)     =     4             16
13 + 12  (1)     =    10             16
 6 +  5  (0)     =    11              0
 5 +  7  (0)     =    12              0
15 +  2  (0)     =     1             16
 8 +  5  (0)     =    13              0
$finish called at time : 105 ns : File "/home/itzzinfinity/Cozy Drive/100
INFO: [USF-XSim-96] XSim completed. Design snapshot 'RCA_tb_behav' loaded
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory
```

Type a Tcl command here


ripple_carry_adder_4bit.v
RCA_tb.v
Untitled 8*
42.832 ns
Name
Value
A[3:0]
5
B[3:0]
2
Cin
1
Sum[3:0]
8
Cout
0
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
100.000
0 4 3 5 13 6 5 15 8
0 1 13 2 6 12 5 7 2 5
0 6 1 8 4 10 11 12 1 13