









```

# }
# }
# run 1000ns
3 * 7 = 21
3 * -7 = -21
-3 * -7 = 21
5 * 6 = 30
5 * -6 = -30
-5 * -6 = 30

$finish called at time : 60 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_063/
INFO: SUCCESS: Verilog simulation completed successfully.

```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day\_063/project\_1/project\_1.srscs/sources\_1/new/booth\_multiplier.v



```
1  timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/25/2024 08:30:57 AM
5  // Module Name: booth_multiplier
6  //////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
7
8  module booth_multiplier (
9      input signed [3:0] Q, M,
10     output reg signed [7:0] result
11 );
12     reg [1:0] operation;
13     integer i;
14     reg q0;
15     reg [3:0] M_comp;
16
17     always @(Q,M)
18     begin
19         result = 8'd0;
20         q0 = 1'b0;
21         M_comp = -M;
22
23         for (i=0; i<4; i=i+1)
24         begin
25             operation = { Q[i], q0 };
26             case(operation)
27                 2'b10 : result[7:4] = result[7:4] + M_comp;
28                 2'b01 : result[7:4] = result[7:4] + M;
29             endcase
30             result = result >> 1;
31             result[7] = result[6];
32             q0 = Q[i];
33
34         end
35     end
36 endmodule
37
38
```



/home/itzzinfinity/Cozy Drive/100daysofRTL/day\_063/project\_1/project\_1.srscs/sim\_1/new/booth\_multiplier\_tb.v



```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/25/2024 08:35:29 AM
5  // Module Name: booth_multiplier_tb
6  //////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
7
8  module test_bench;
9  reg signed [3:0] Q,M;
10 wire signed [7:0] result;
11
12 booth_multiplier DUT (Q,M,result);
13
14 initial begin
15     Q= 3; M= 7; #10;
16     Q= 3; M= -7; #10;
17     Q= -3; M= -7; #10;
18     Q= 5; M= 6; #10;
19     Q= 5; M= -6; #10;
20     Q= -5; M= -6; #10;
21 end
22
23 initial begin
24     $monitor("%d * %d = %d", Q,M,result);
25     #60 $finish;
26 end
27 endmodule
28
29
```

