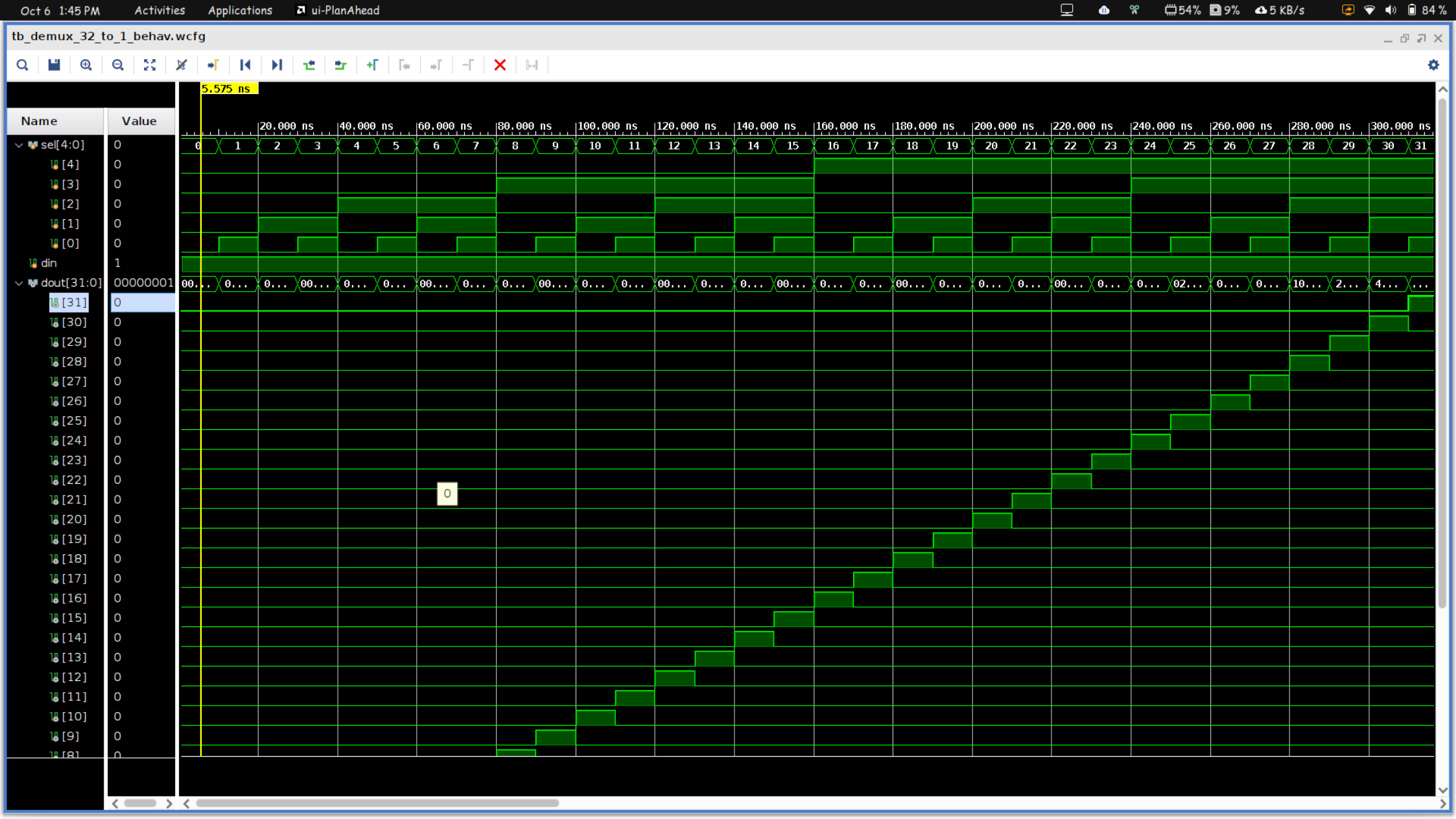
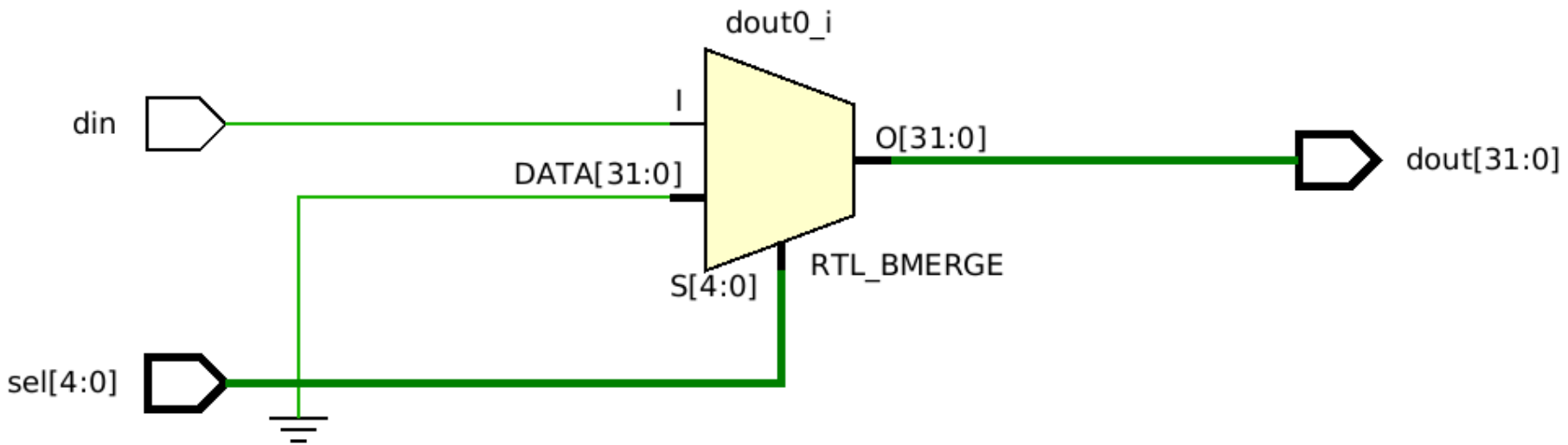

Oct 6 1:45 PM
Activities
Applications
ui-PlanAhead
54%
9%
5 KB/s
84 %
tb_demux_32_to_1_behav.wcfg
5.575 ns
Name
Value
sel[4:0]
[4]
[3]
[2]
[1]
[0]
din
dout[31:0]
[31]
[30]
[29]
[28]
[27]
[26]
[25]
[24]
[23]
[22]
[21]
[20]
[19]
[18]
[17]
[16]
[15]
[14]
[13]
[12]
[11]
[10]
[9]
[8]
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
220.000 ns
240.000 ns
260.000 ns
280.000 ns
300.000 ns

Project Summary | demux_32_to_1.v | tb_demux_32_to_1.v | Schematic

1 Cell | 38 I/O Ports | 39 Nets



Project Summary | demux_32_to_1.v | tb_demux_32_to_1.v | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_030/project_1/project_1.srcs/sources_1/new/demux_32_to_1.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/21/2024 06:13:39 AM
5  // Module Name: demux_32_to_1
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module demux_32_to_1(
10     input wire [4:0] sel,
11     input wire din,
12     output reg [31:0] dout
13 );
14     always @(*) begin
15         dout = 32'b0;
16         dout[sel] = din;
17     end
18 endmodule
19
```

Project Summary | demux_32_to_1.v | tb_demux_32_to_1.v | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_030/project_1/project_1.srcs/sim_1/new/tb_demux_32_to_1.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan prasd
4  // Create Date: 10/21/2024 06:16:36 AM
5  // Module Name: tb_demux_32_to_1
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module tb_demux_32_to_1;
9
10   reg [4:0] sel;
11   reg din;
12   wire [31:0] dout;
13
14   demux_32_to_1 uut (
15     .sel(sel),
16     .din(din),
17     .dout(dout)
18   );
19   initial begin
20     din = 1;
21     for (sel = 5'd0; sel <= 5'd31; sel = sel + 1) begin
22         #10;
23     end
24     $stop;
25   end
26
27 endmodule
28
```