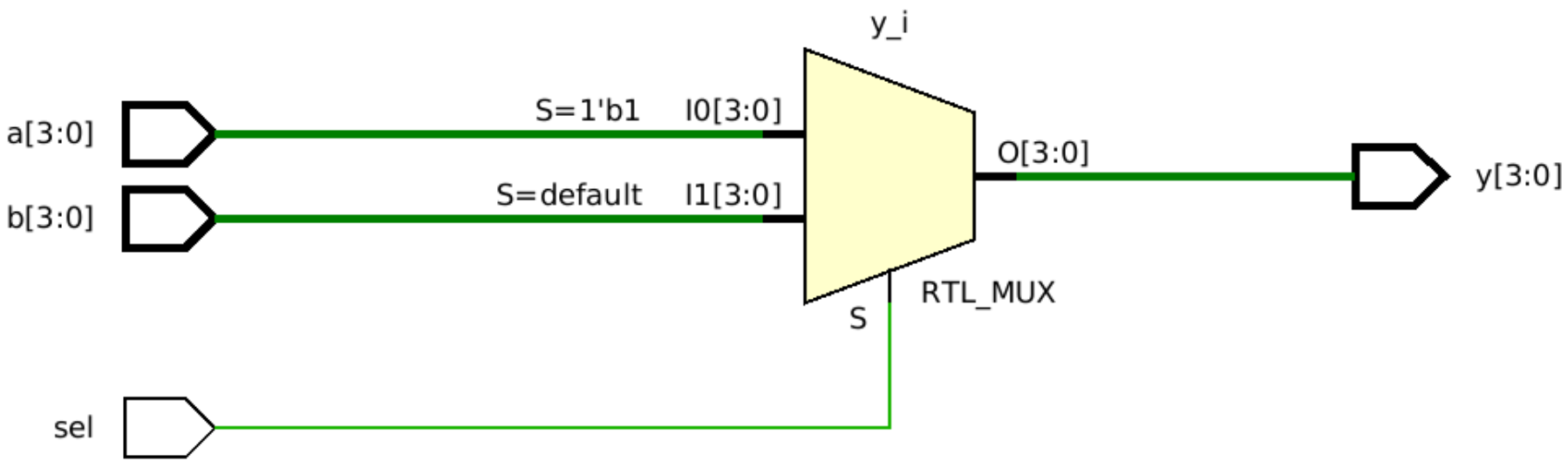
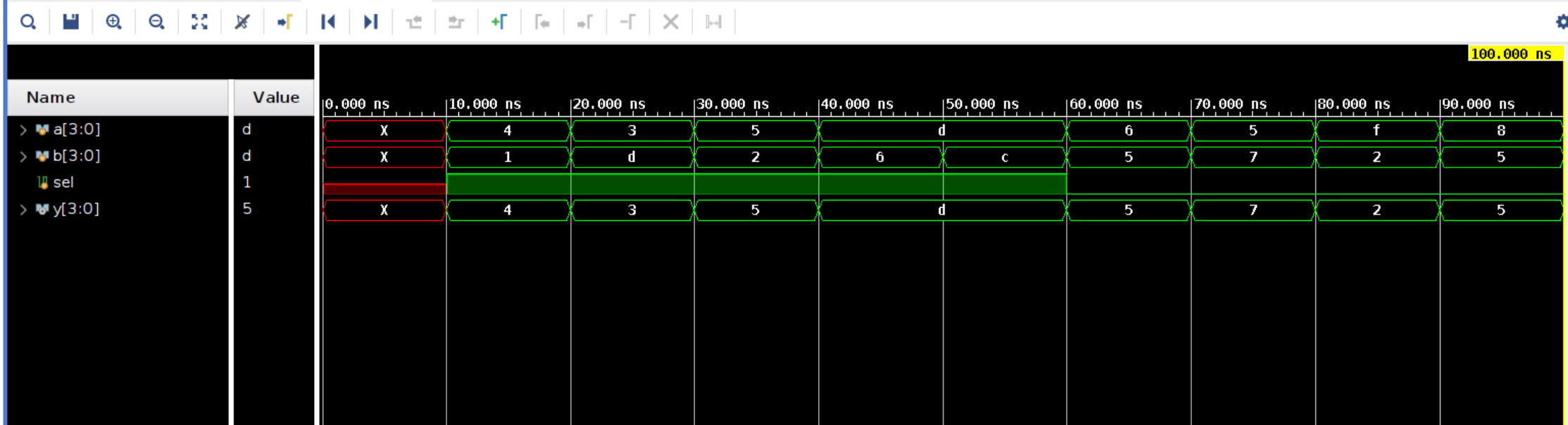
Project Summary | mux_2_to_1.v | Schematic | mux_tb.v

1 Cell | 13 I/O Ports | 13 Nets



mux_2_to_1.v | mux_tb.v | Untitled 1



Tcl Console | Messages | Log

```
# }
# run 1000ns
Select line is Sel  so now the output is y  , where a and b are:
                x                          x,          x     x
                1                          4,          4     1
                1                          3,          3    13
                1                          5,          5     2
                1                         13,         13     6
                1                         13,         13    12
                0                          5,          6     5
                0                          7,          5     7
                0                          2,         15     2
                0                          5,          8     5
$finish called at time : 100 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/da
```

Type a Tcl command here

Project Summary | mux_2_to_1.v | Schematic | mux_tb.v

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_022/project_1/project_1.srcs/sources_1/new/mux_2_to_1.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/13/2024 06:16:57 PM
5  // Module Name: mux_2_to_1
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module mux_2_to_1(
10 input [3:0] a,b,
11 input sel,
12 output [3:0] y);
13
14 assign y = (sel)?a:b;
15
16
17 endmodule
18
```

Project Summary | mux_2_to_1.v | Schematic | **mux_tb.v**

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_022/project_1/project_1.srcs/sim_1/new/mux_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 10/13/2024 06:16:57 PM
5  // Module Name: mux_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module mux_tb;
10 reg [3:0] a,b;
11 reg sel;
12 wire [3:0] y;
13
14 mux_2_to_1 DUT (a,b,sel,y);
15  initial begin
16         $display("Select line is Sel  so now the output is y  , where a and b are:");
17         $monitor("               %b                        %d,         %d    %d", sel,y,a,b);
18 repeat(10) begin
19 #10
20         a= $random %16 ;
21         b= $random %16 ;
22         sel = $random;
23
24 end
25 $finish;
26 end
27 endmodule
```