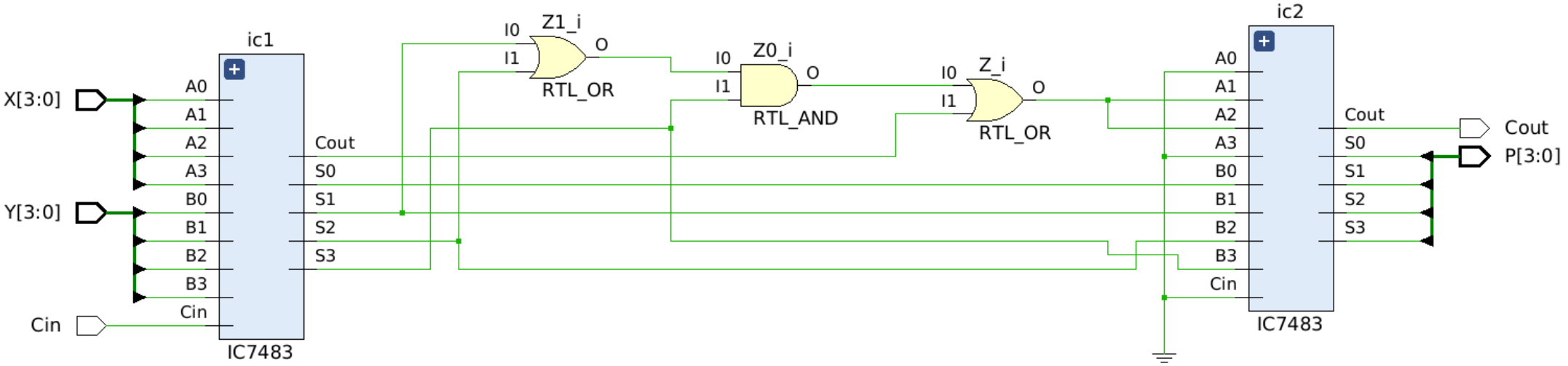
Project Summary | full_adder.v | IC7483.v | BCD_adder.v | BCD_adder_tb.v | Schematic

5 Cells 14 I/O Ports 23 Nets



Project Summary | full_adder.v | IC7483.v | BCD_adder.v | BCD_adder_tb.v | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_013/project_1/project_1.srcs/sources_1/new/BCD_adder.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Engineer: Anjan Prasad
3  // Create Date: 10/04/2024 09:08:42 AM
4  // Module Name: BCD_adder
5  //////////////////////////////////////////////////////////////////////////////////
6
7
8  module BCD_adder(
9  input [3:0] X,Y,
10 input Cin,
11 output [3:0] P,
12 output Cout);
13 wire [3:0] C;
14 wire D,Z;
15 assign Z = ((C[1]|C[2])&C[3])|D;
16 IC7483 ic1 (.A0(X[0]),.A1(X[1]),.A2(X[2]),.A3(X[3]),.B0(Y[0]),.B1(Y[1]),.B2(Y[2]),.B3(Y[3]),.S0(C[0]),.S1(C[1]),.S2(C[2]),.S3(C[3]),.Cin(Cin),.Cout(D));
17 IC7483 ic2 (.A0(0),.A1(Z),.A2(Z),.A3(0),.B0(C[0]),.B1(C[1]),.B2(C[2]),.B3(C[3]),.S0(P[0]),.S1(P[1]),.S2(P[2]),.S3(P[3]),.Cin(0),.Cout(Cout));
18 endmodule
```

Project Summary | full_adder.v | IC7483.v | BCD_adder.v | BCD_adder_tb.v | Schematic

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_013/project_1/project_1.srcs/sim_1/new/BCD_adder_tb.v

```
// Engineer: Anjan Prasad
// Create Date: 10/04/2024 09:08:42 AM
// Module Name: BCD_adder_tb
//////////////////////////////////////////////////////////////////////////////////

`timescale 1ns / 1ps


module BCD_adder_tb;

    reg [3:0] X, Y; // 4-bit inputs
    reg Cin;        // Carry input
    wire [3:0] P; // 4-bit BCD sum
    wire Cout;      // Carry output

    // Instantiate the BCD adder
    BCD_adder UUT (
        .X(X),
        .Y(Y),
        .Cin(Cin),
        .P(P),
        .Cout(Cout)
    );

    initial begin
        // Test cases
        $monitor("X = %d, Y = %d, Cin = %b -> P = %d, Cout = %b (%d)", X, Y, Cin, P, Cout,Cout*10);

        // Initial input values
        X = 4'b0000; Y = 4'b0000; Cin = 0;
        #10 X = 4'b0011; Y = 4'b0101; Cin = 0;  // 3 + 5
        #10 X = 4'b1001; Y = 4'b0101; Cin = 0;  // 9 + 5
        #10 X = 4'b0110; Y = 4'b0111; Cin = 0;  // 6 + 7
        #10 X = 4'b1001; Y = 4'b1001; Cin = 0;  // 9 + 9

        #10 $finish;
    end
endmodule
```

Project Summary | full_adder.v | IC7483.v | BCD_adder.v | BCD_adder_tb.v | Schematic

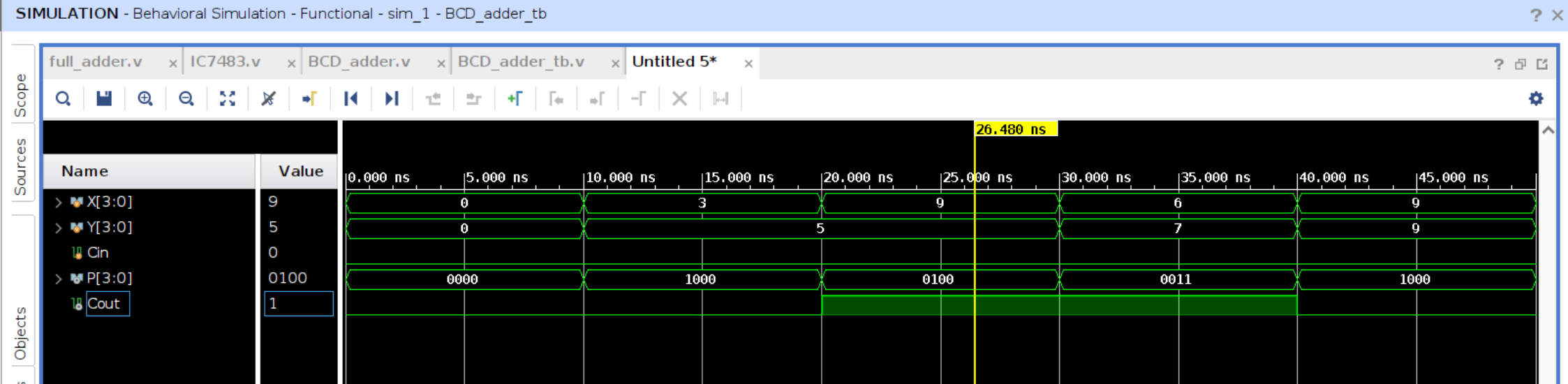
/home/itzzinfinity/Cozy Drive/100daysofRTL/day_013/project_1/project_1.srcs/sources_1/new/IC7483.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // Engineer: Anjan Prasad
3  // Create Date: 10/04/2024 09:08:42 AM
4  // Module Name: IC7483
5  //////////////////////////////////////////////////////////////////////////////////
6
7
8  module IC7483(
9  input A0,
10 input A1,
11 input A2,
12 input A3,
13 input B0,
14 input B1,
15 input B2,
16 input B3,
17 input Cin,
18 output S0,
19 output S1,
20 output S2,
21 output S3,
22 output Cout);
23 wire C1,C2,C3;
24 full_adder FA1(.a(A0), .b(B0), .cin(Cin), .sum(S0), .cout(C1));
25 full_adder FA2(.a(A1), .b(B1), .cin(C1), .sum(S1), .cout(C2));
26 full_adder FA3(.a(A2), .b(B2), .cin(C2), .sum(S2), .cout(C3));
27 full_adder FA4(.a(A3), .b(B3), .cin(C3), .sum(S3), .cout(Cout));
28 endmodule
29
```

Tcl Console | Messages | Log

```
# }
# run 1000ns
X =  0, Y =  0, Cin = 0 -> P =  0, Cout = 0 (          0)
X =  3, Y =  5, Cin = 0 -> P =  8, Cout = 0 (          0)
X =  9, Y =  5, Cin = 0 -> P =  4, Cout = 1 (         10)
X =  6, Y =  7, Cin = 0 -> P =  3, Cout = 1 (         10)
X =  9, Y =  9, Cin = 0 -> P =  8, Cout = 0 (          0)
$finish called at time : 50 ns : File "/home/itzzinfinity/Cozy Drive/
INFO: [USF-XSim-96] XSim completed. Design snapshot 'BCD_adder_tb_beh
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 . Me
```

Type a Tcl command here


SIMULATION - Behavioral Simulation - Functional - sim_1 - BCD_adder_tb
full_adder.v
IC7483.v
BCD_adder.v
BCD_adder_tb.v
Untitled 5*
Scope
Sources
Objects
Name
Value
X[3:0]
9
Y[3:0]
5
Cin
0
P[3:0]
0100
Cout
1
26.480 ns
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
40.000 ns
45.000 ns
0
3
9
6
9
0
5
7
9
0000
1000
0100
0011
1000