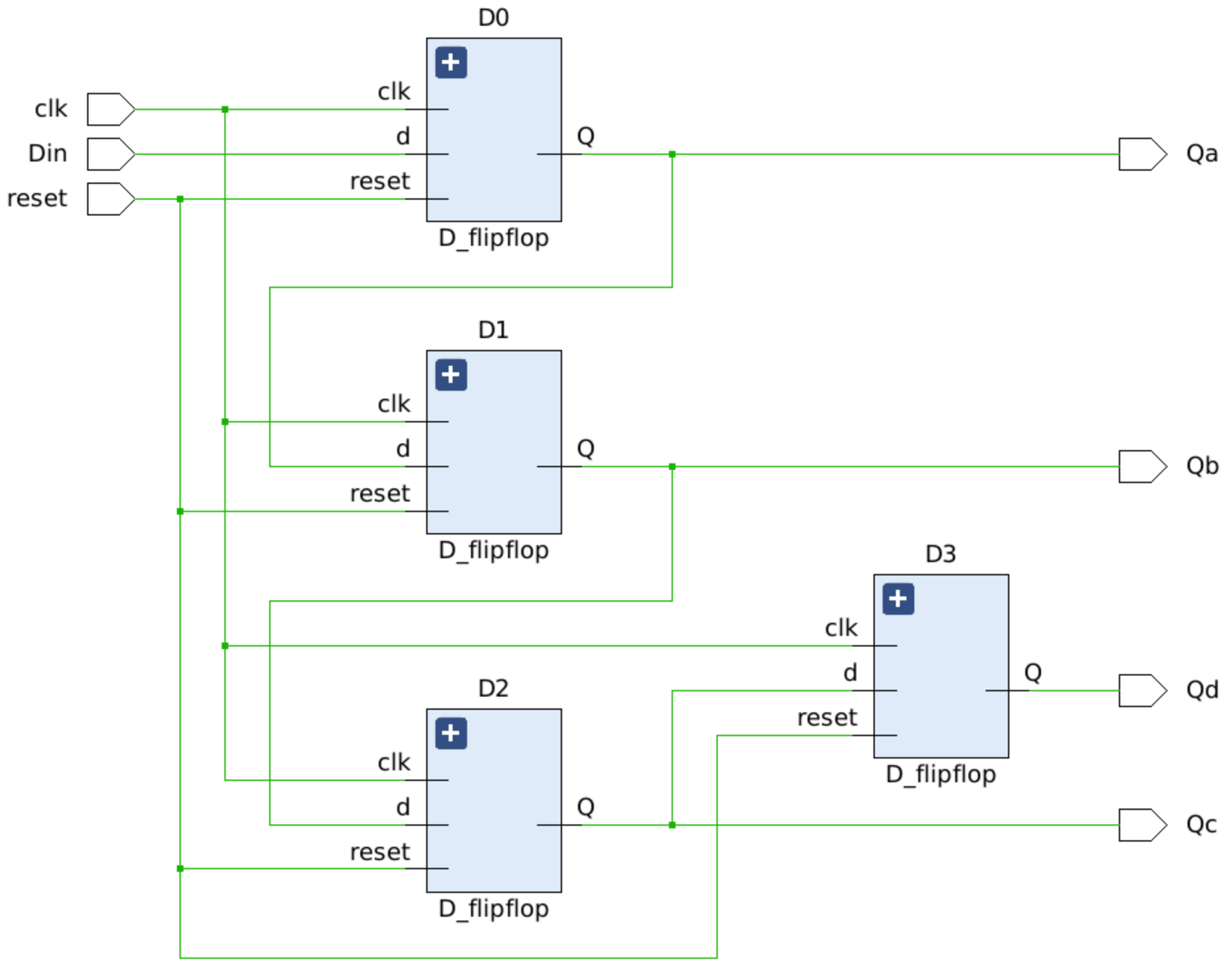
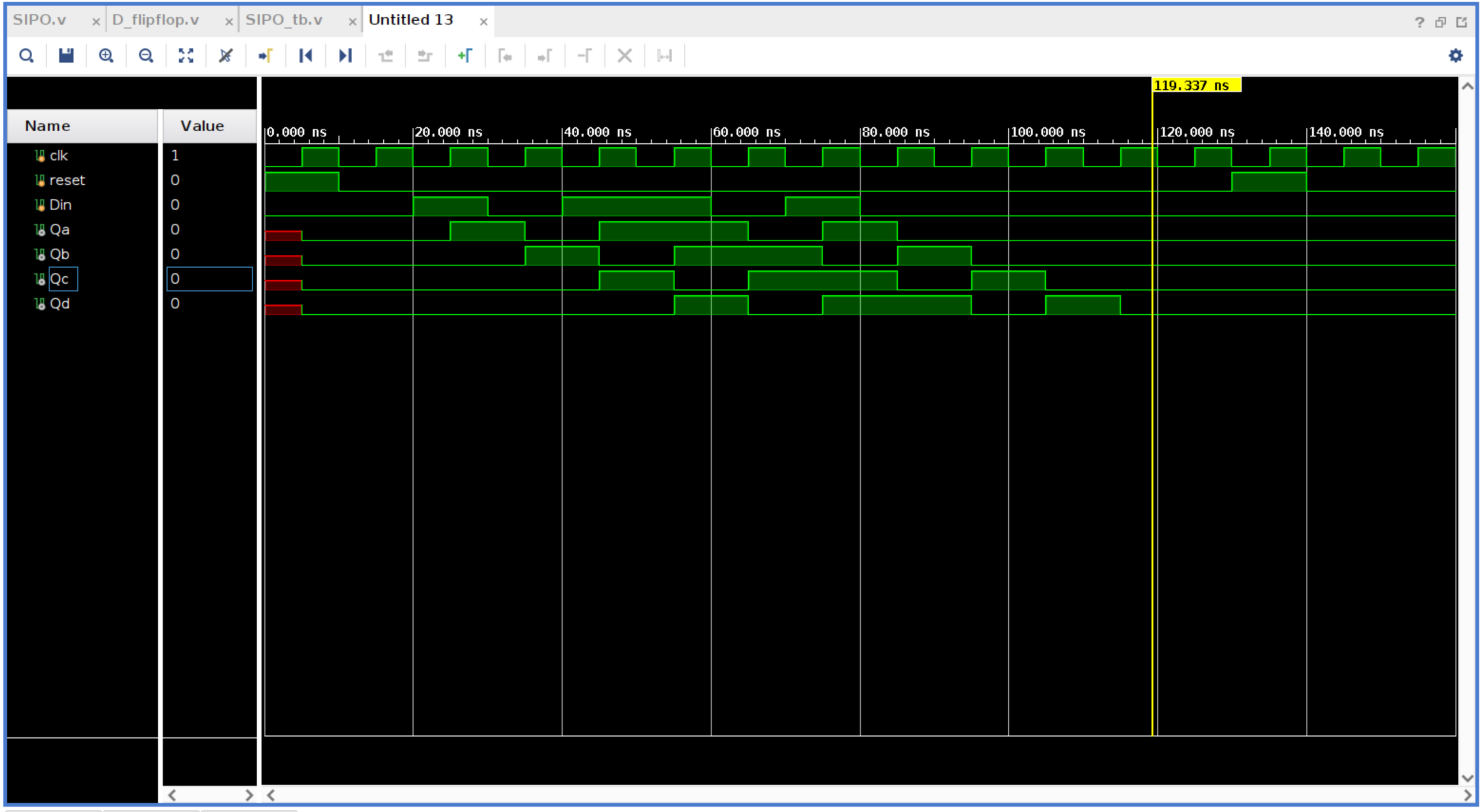
Project Summary | SIPO.v | D_flipflop.v | Schematic | SIPO_tb.v | Schematic (2)

4 Cells 7 I/O Ports 7 Nets




SIPO.v
D_flipflop.v
SIPO_tb.v
Untitled 13
Name
Value
clk
1
reset
0
Din
0
Qa
0
Qb
0
Qc
0
Qd
0
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
119.337 ns

SIPO.v | D_flipflop.v | SIPO_tb.v | Untitled 13

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_056/project_1/project_1.srcs/sources_1/new/SIPO.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/16/2024 10:52:41 AM
5  // Module Name: SIPO
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module SIPO(
10 input clk, Din,reset,
11 output Qa,Qb,Qc,Qd);
12
13  D_flipflop D0 (.d(Din), .clk(clk), .reset(reset), .Q(Qa));
14  D_flipflop D1 (.d(Qa), .clk(clk), .reset(reset), .Q(Qb));
15  D_flipflop D2 (.d(Qb), .clk(clk), .reset(reset), .Q(Qc));
16  D_flipflop D3 (.d(Qc), .clk(clk), .reset(reset), .Q(Qd));
17
18
19 endmodule
20
```

SIPO.v | D_flipflop.v | SIPO_tb.v | Untitled 13

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_056/project_1/project_1.srcs/sources_1/new/D_flipflop.v

```
1
2   module D_flipflop(
3       input clk, reset, d,
4       output reg Q
5       );
6
7       always @(posedge clk) begin
8           if (reset)
9               Q <= 1'b0;
10          else
11              Q <= d;
12      end
13
14  endmodule
```

SIPO.v | D_flipflop.v | SIPO_tb.v | Untitled 13

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_056/project_1/project_1.srcs/sim_1/new/SIPO_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/16/2024 11:00:34 PM
5  // Module Name: SIPO_tb
6  //////////////////////////////////////////////////////////////////////////////////
7  module SIPO_tb;
8   reg clk, reset, Din;
9      wire Qa,Qb,Qc,Qd;
10
11     SIPO DUT (
12         .clk(clk),.reset(reset),.Din(Din),.Qa(Qa),.Qb(Qb),.Qc(Qc),.Qd(Qd)
13     );
14     initial begin
15         clk = 0;
16         forever #5 clk = ~clk; // 10 ns period
17     end
18     initial begin
19         reset = 1;
20         Din = 0;
21         #10 reset = 0;
22         #10 Din = 1; // Input '1' -> expect serial_out = 0 after 4 cycles
23         #10 Din = 0;
24         #10 Din = 1;
25         #10 Din = 1;
26         #10 Din = 0;
27         #10 Din = 1;
28         #10 Din = 0;
29         #50;
30         reset = 1;
31         #10 reset = 0;
32         #20 $stop;
33     end
34 endmodule
35
```