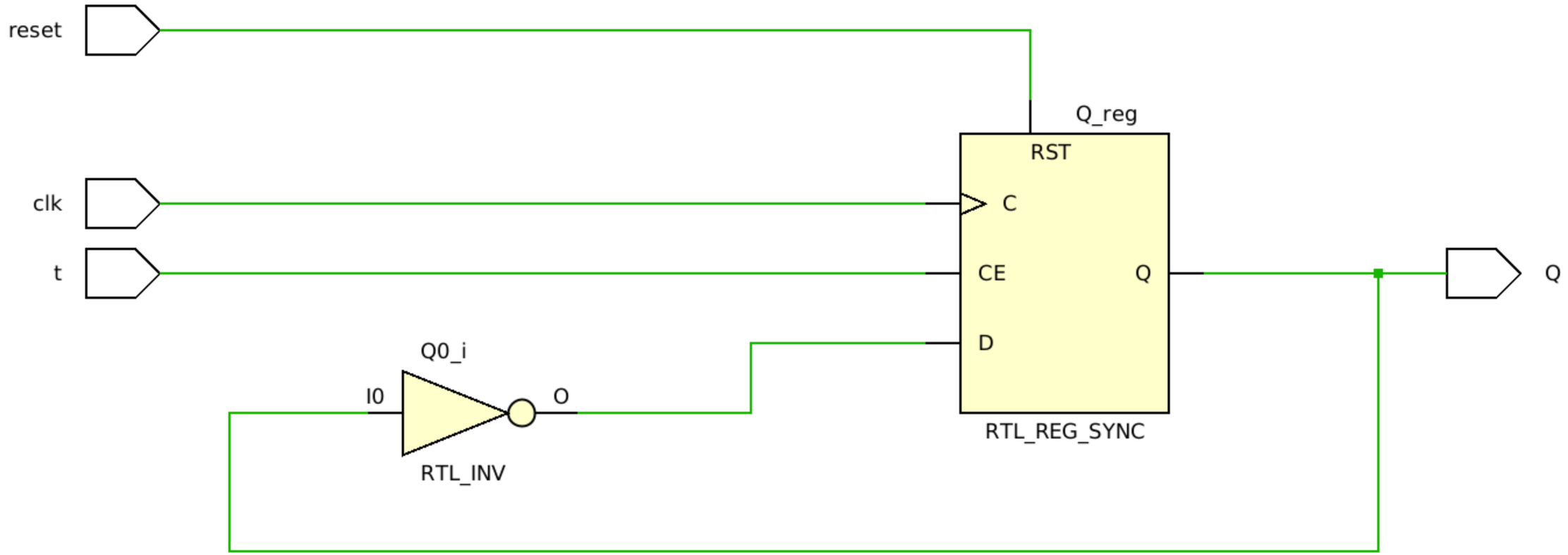
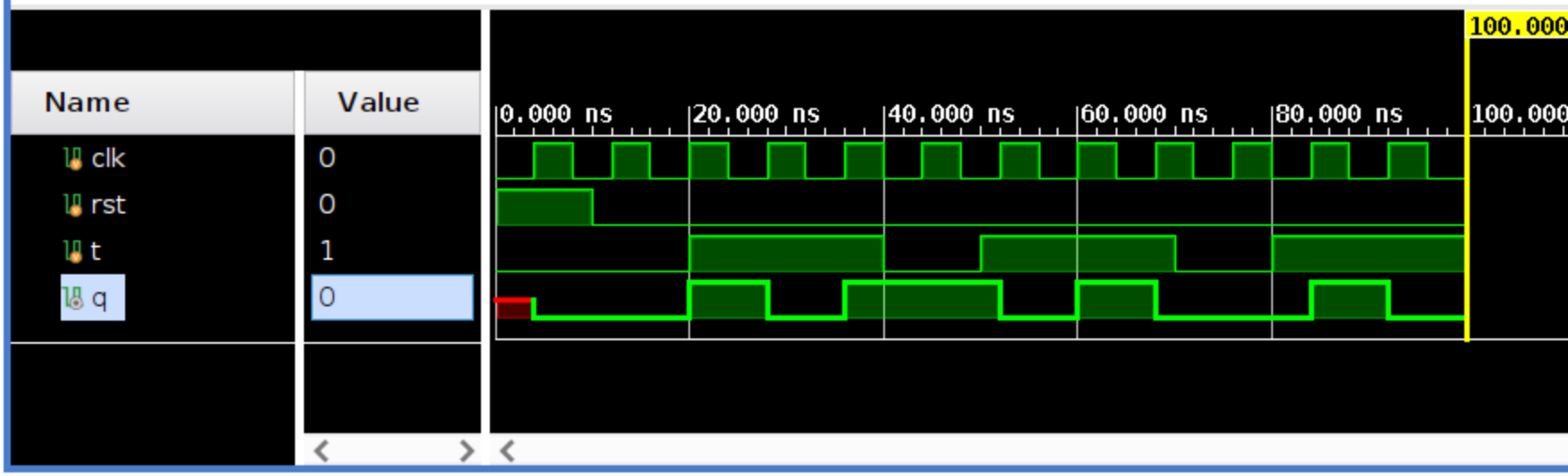
Project Summary | T_ff.v | T_ff_tb.v | Schematic | Schematic (2)

2 Cells 4 I/O Ports 5 Nets



T_ff.v | T_ff_tb.v | Untitled 3



Tcl Console | Messages | Log

```
# run 1000ns
      clock: 0  T: 0  Q: x
      clock: 1  T: 0  Q: 0
      clock: 0  T: 0  Q: 0
      clock: 1  T: 0  Q: 0
      clock: 0  T: 0  Q: 0
      clock: 1  T: 1  Q: 1
      clock: 0  T: 1  Q: 1
      clock: 1  T: 1  Q: 0
      clock: 0  T: 1  Q: 0
      clock: 1  T: 1  Q: 1
      clock: 0  T: 0  Q: 1
      clock: 1  T: 0  Q: 1
      clock: 0  T: 0  Q: 1
      clock: 0  T: 1  Q: 1
      clock: 1  T: 1  Q: 0
      clock: 0  T: 1  Q: 0
      clock: 1  T: 1  Q: 1
      clock: 0  T: 1  Q: 1
      clock: 1  T: 1  Q: 0
      clock: 1  T: 0  Q: 0
```

Type a Tcl command here

T_ff.v | T_ff_tb.v | Untitled 3

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_049/Tff/Tff.srcs/sources_1/new/T_ff.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/09/2024 06:55:45 AM
5  // Module Name: T_ff
6  //////////////////////////////////////////////////////////////////////////////////
7
8  module T_ff(
9      input t,clk,reset,
10     output reg Q
11     );
12     always@(posedge clk)
13           begin
14             if(reset)
15                Q <= 1'b0;
16             else
17                 begin
18                    if(t)
19                     Q<= ~Q;
20                    else
21                     Q<= Q;
22                 end
23           end
24 endmodule
25
```

Tcl Console | Messages | Log

T_ff.v | T_ff_tb.v | Untitled 3

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_049/Tff/Tff.srcs/sim_1/new/T_ff_tb.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Engineer: Anjan Prasad
4  // Create Date: 11/09/2024 06:56:43 AM
5  // Module Name: T_ff_tb
6  //////////////////////////////////////////////////////////////////////////////////
7
8
9  module T_ff_tb;
10 reg clk,rst,t;
11 wire q;
12   T_ff DUT(t,clk,rst,q);
13
14   initial
15   begin
16        clk=0;
17        t=0;
18        forever #4 clk=~clk;
19   end
20
21   initial
22       begin
23           rst=1;
24           #10;
25           rst=0;
26           forever
27           begin
28           #10 t = 1'b1;
29           #20  t = 1'b0;
30           end
31       end
32     initial begin
33     $monitor("\t clock: %b  T: %b  Q: %b",clk,t,q);
34     #100$finish;
35     end
36 endmodule
37
```

Tcl Console | Messages | Log