MULATION - Behavioral Simulation - Functional - sim_1 - fq_divider_odd_tb

fq_divider_odd.v | fq_divider_odd_tb.v | Untitled 1

Name	Value
clk	1
reset	0
clk_out	1

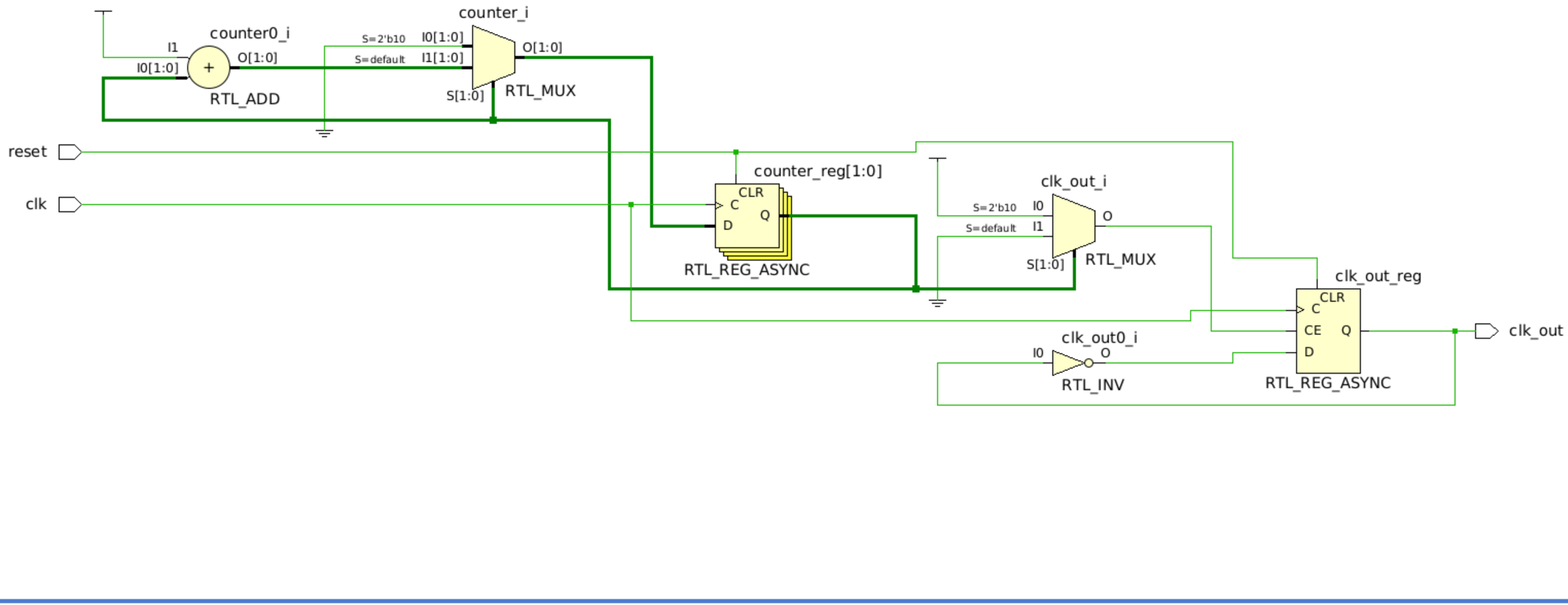
35.000 ns
65.000 ns
0.000 ns
50.000 ns
100.000 ns
-30.000 ns
-50.000 ns
0.000 ns
50.000 ns

Tcl Console | Messages | Log

LABORATED DESIGN - xc7a12ticsg325-1L

Project Summary | fq_divider_odd.v | fq_divider_odd_tb.v | Schematic

7 Cells 3 I/O Ports 13 Nets



Tcl Console | Messages | Log | Reports | Design Runs

fq_divider_odd.v | fq_divider_odd_tb.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_072/project_1/project_1.srcs/sources_1/new/fq_divider_odd.v

Redo (Ctrl+Shift+Z)

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 12/02/2024 11:33:31 AM
5   // Module Name: fq_divider_odd
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module fq_divider_odd(
9       input clk,
10      input reset,
11      output reg clk_out
12  );
13      reg [1:0] counter;
14
15      always @(posedge clk or posedge reset) begin
16          if (reset) begin
17              counter <= 2'b00;
18              clk_out <= 1'b0;
19          end else begin
20              if (counter == 2'b10) begin
21                  counter <= 2'b00;       // Reset counter after 3 cycles
22                  clk_out <= ~clk_out;   // Toggle output clock
23              end else begin
24                  counter <= counter + 1;
25              end
26          end
27      end
28  endmodule
29
```

Tcl Console | Messages | Log

fq_divider_odd.v | fq_divider_odd_tb.v | Untitled 1

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_072/project_1/project_1.srcs/sim_1/new/fq_divider_odd_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 12/02/2024 11:38:20 AM
5   // Module Name: fq_divider_odd_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module fq_divider_odd_tb;
10      reg clk;
11      reg reset;
12      wire clk_out;
13
14      fq_divider_odd DUT (
15          .clk(clk),
16          .reset(reset),
17          .clk_out(clk_out)
18      );
19
20      initial begin
21          clk = 0;
22          forever #5 clk = ~clk;
23      end
24
25      initial begin
26          reset = 1;
27          #10 reset = 0;
28
29          #120;
30          $stop;
31      end
32  endmodule
33
```

Tcl Console | Messages | Log