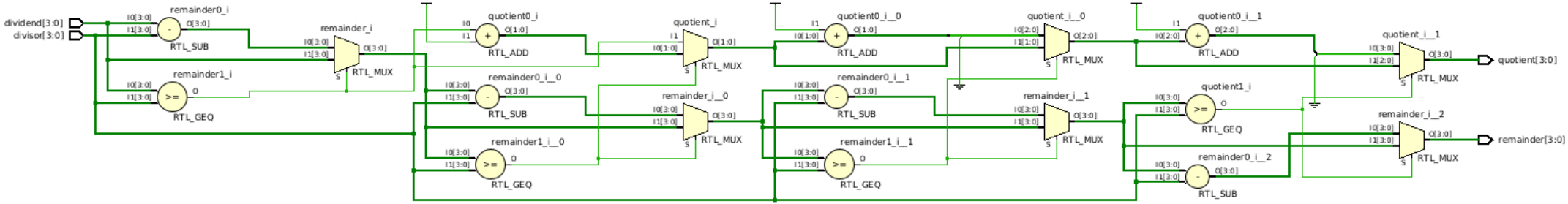
Sources

Project Summary | divider_4b.v | divider_4b_tb.v | Schematic | Schematic (2)

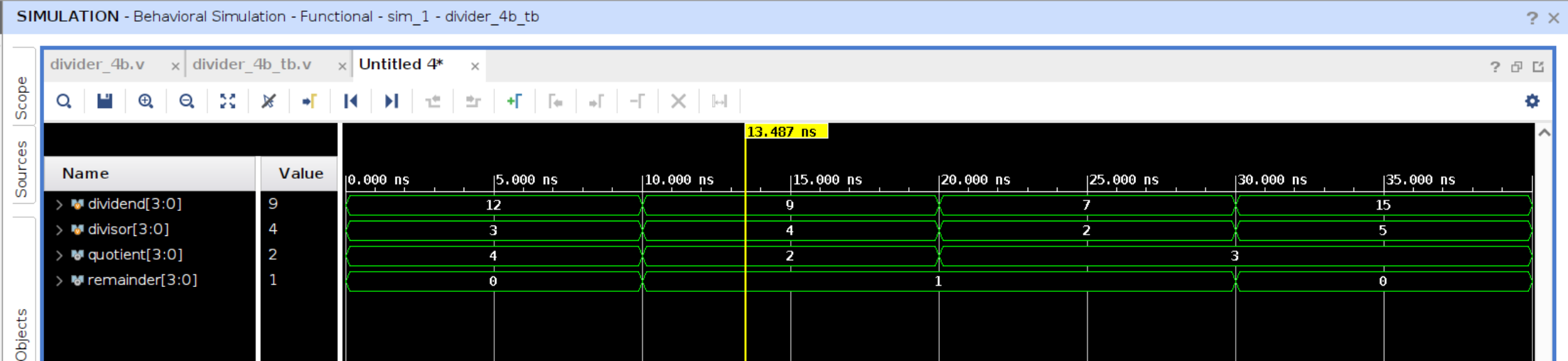
18 Cells 16 I/O Ports 62 Nets



Tcl Console × Messages Log

```
#   }
# }
# run 1000ns
Time = 0 | Dividend = 12 | Divisor =  3 | Quotient =  4 | Remainder =  0
Time = 10000 | Dividend =  9 | Divisor =  4 | Quotient =  2 | Remainder =  1
Time = 20000 | Dividend =  7 | Divisor =  2 | Quotient =  3 | Remainder =  1
Time = 30000 | Dividend = 15 | Divisor =  5 | Quotient =  3 | Remainder =  0
$finish called at time : 40 ns : File "/home/itzzinfinity/Cozy Drive/100daysofRTL/day_014/project_1/project_1.srcs/sim_1/new/divider_4b_tb.v" Line 49
INFO: [USF-XSim-96] XSim completed. Design snapshot 'divider_4b_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:06 . Memory (MB): peak = 8258.984 ; gain = 11.988 ; free physical = 643 ; free virtual = 3604
```

Type a Tcl command here


SIMULATION - Behavioral Simulation - Functional - sim_1 - divider_4b_tb
Scope
Sources
Objects
divider_4b.v
divider_4b_tb.v
Untitled 4*
13.487 ns
Name
Value
dividend[3:0]
9
divisor[3:0]
4
quotient[3:0]
2
remainder[3:0]
1
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
12
9
7
15
3
4
2
5
4
2
3
0
1
0

divider_4b.v × divider_4b_tb.v × Untitled 4* ×

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_014/project_1/project_1.srcs/sources_1/new/divider_4b.v

```
1
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/05/2024 08:34:46 AM
5   // Module Name: divider_4b
6   //////////////////////////////////////////////////////////////////////////////////
7
8
9   module divider_4b(
10      input [3:0] dividend,
11      input [3:0] divisor,
12      output reg [3:0] quotient,
13      output reg [3:0] remainder
14  );
15      integer i;
16
17      always @(*) begin
18          quotient = 0;
19          remainder = dividend;
20
21          // Division algorithm using repeated subtraction
22          for (i = 3; i >= 0; i = i - 1) begin
23              if (remainder >= divisor) begin
24                  remainder = remainder - divisor;
25                  quotient = quotient + 1;
26              end
27          end
28      end
29  endmodule
30
31
32
```

divider_4b.v | divider_4b_tb.v | Untitled 4*

/home/itzzinfinity/Cozy Drive/100daysofRTL/day_014/project_1/project_1.srcs/sim_1/new/divider_4b_tb.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Engineer: Anjan Prasad
4   // Create Date: 10/05/2024 08:34:46 AM
5   // Module Name: divider_4b_tb
6   //////////////////////////////////////////////////////////////////////////////////
7
8   module divider_4b_tb;
9
10      reg [3:0] dividend;
11      reg [3:0] divisor;
12      wire [3:0] quotient;
13      wire [3:0] remainder;
14
15      divider_4b uut (
16          .dividend(dividend),.divisor(divisor),.quotient(quotient),.remainder(remainder)
17      );
18
19      initial begin
20          // Test cases
21          dividend = 4'd12; divisor = 4'd3; #10;
22
23          dividend = 4'd9;divisor = 4'd4; #10;
24
25          dividend = 4'd7;divisor = 4'd2; #10;
26
27          dividend = 4'd15; divisor = 4'd5; #10;
28
29
30          $finish;
31      end
32
33      initial begin
34          $monitor("Time = %0t | Dividend = %d | Divisor = %d | Quotient = %d | Remainder = %d",
35                   $time, dividend, divisor, quotient, remainder);
36      end
37
38  endmodule
39
```