

/home/itzzinfinity/Cozy Drive/100daysofRTL/day\_002/project\_1/project\_1.srscs/sources\_1/new/structural\_gates.v

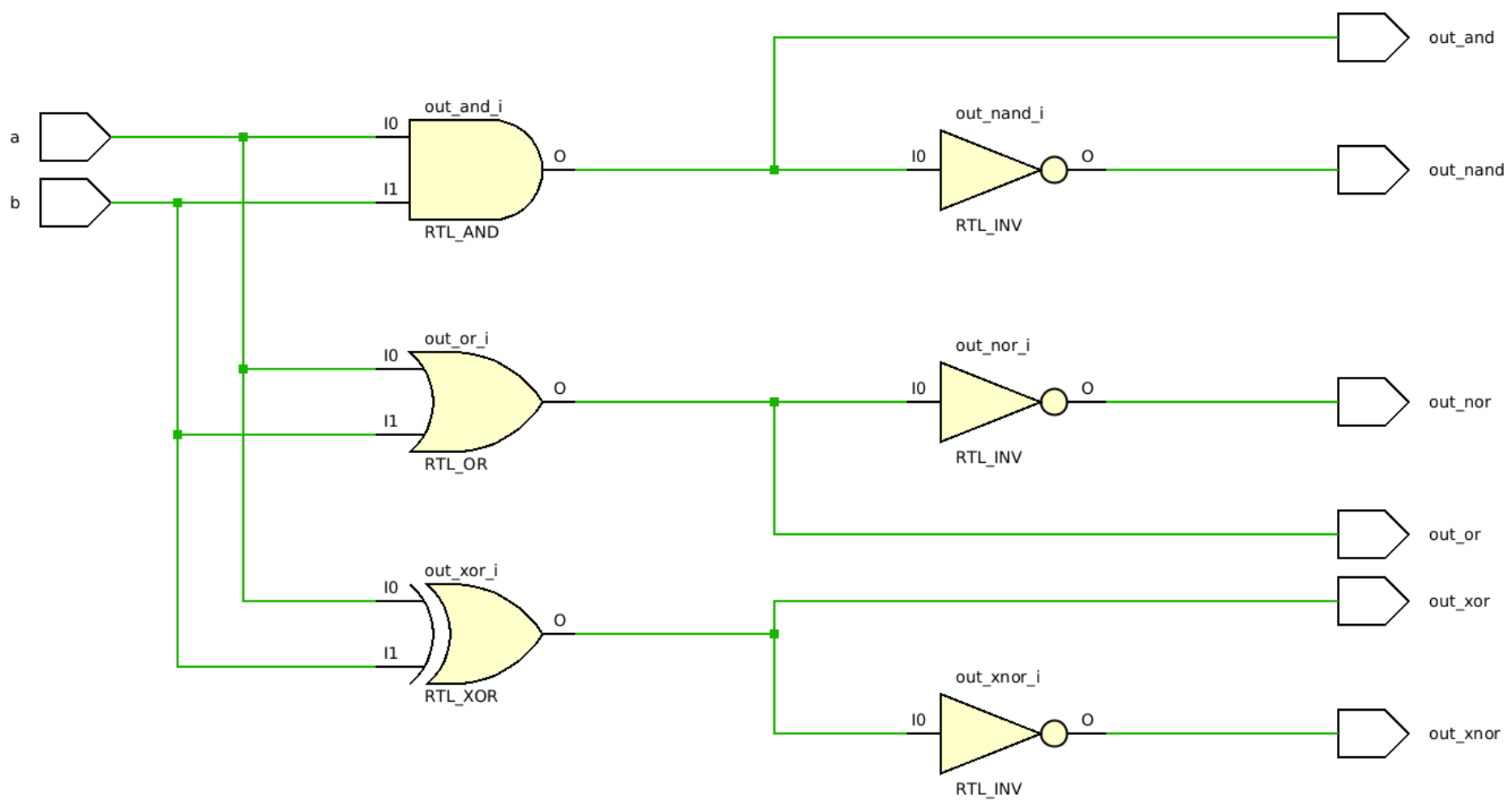










```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
3  // Engineer:
4  // Create Date: 09/23/2024 09:59:32 PM
5  // Module Name: structural_gates
6  //////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
7
8
9  module structural_gates(
10     input a,
11     input b,
12     output out_and,out_or,out_nand,out_nor,out_xor,out_xnor
13 );
14     assign out_and = a&b;
15     assign out_or = a|b;
16     assign out_nand = ~(a&b);
17     assign out_nor = ~(a|b);
18     assign out_xor = a^b;
19     assign out_xnor = ~(a^b);
20 endmodule
21
```

/home/itzzinfinity/Cozy Drive/100daysofRTL/day\_002/project\_1/project\_1.srcs/sim\_1/new/structural\_gates\_tb.v



```
1  `timescale 10ns / 10ps
2  ///////////////////////////////////////////////////////////////////
3  // Engineer:
4  // Create Date: 09/23/2024 09:59:32 PM
5  // Module Name: structural_gates
6  ///////////////////////////////////////////////////////////////////
7
8
9  module structural_gates_tb;
10     reg a,b;
11     wire out_and,out_or,out_nand,out_nor,out_xor,out_xnor;
12     structural_gates DUT (a,b,out_and,out_or,out_nand,out_nor,out_xor,out_xnor);
13     initial begin
14         #10 a= 1'b0; b= 1'b0;
15         #10 a= 1'b0; b= 1'b1;
16         #10 a= 1'b1; b= 1'b0;
17         #10 a= 1'b1; b= 1'b1;
18     end
19
20
21 endmodule
22
```



Name	Value
 a	1
 b	0
 out_and	0
 out_or	1
 out_nand	1
 out_nor	0
 out_xor	1
 out_xnor	0

