Instituto Politécnico Nacional

Escuela Superior de Computo

Materia:

Introducción a los microcontroladores.

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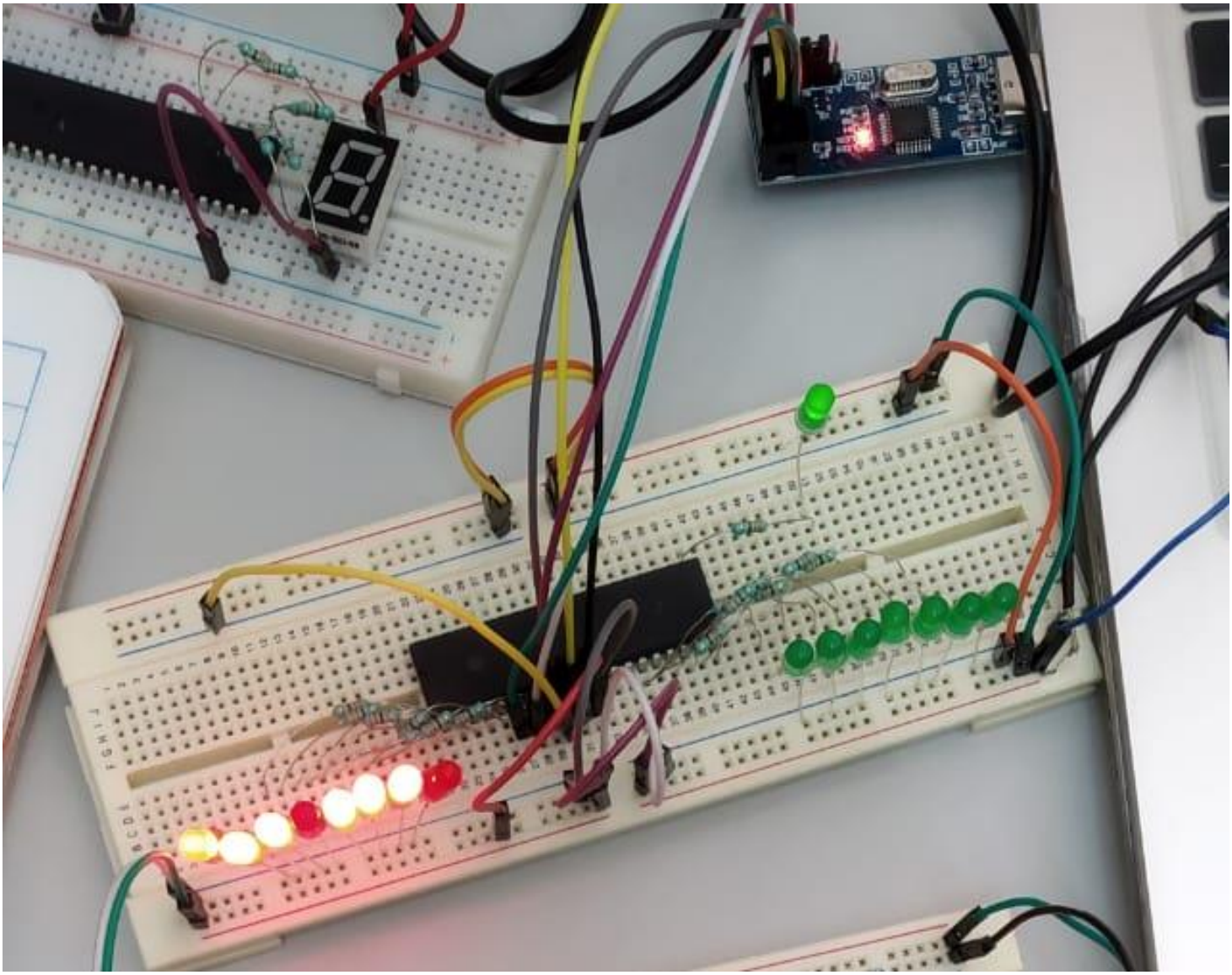
Practica N°2



```
/*****************************************************
This program was created by the
CodeWizardAVR V2.60 Evaluation
Automatic Program Generator
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http://www.hpinfotech.com

Project :
Version :
Date    : 30/01/2019
Author  :
Company :
Comments:


Chip type               : ATmega8535L
Program type            : Application
AVR Core Clock frequency: 1,000000 MHz
Memory model            : Small
External RAM size       : 0
Data Stack size         : 128
*****************************************************/

#include <mega8535.h>
#include <delay.h>

// Declare your global variables here

void main(void)
{
// Declare your local variables here

// Input/Output Ports initialization
// Port A initialization
// Function: Bit7=In Bit6=In Bit5=In Bit4=In Bit3=In Bit2=In Bit1=In Bit0=In
DDRA=(0<<DDA7) | (0<<DDA6) | (0<<DDA5) | (0<<DDA4) | (0<<DDA3) | (0<<DDA2) | (0<<DDA1) | (0<<DDA0);
// State: Bit7=T Bit6=T Bit5=T Bit4=T Bit3=T Bit2=T Bit1=T Bit0=T
PORTA=(0<<PORTA7) | (0<<PORTA6) | (0<<PORTA5) | (0<<PORTA4) | (0<<PORTA3) | (0<<PORTA2) | (0<<PORTA1) | (0<<PORTA0);

// Port B initialization
// Function: Bit7=Out Bit6=Out Bit5=Out Bit4=Out Bit3=Out Bit2=Out Bit1=Out Bit0=Out
DDRB=(1<<DDB7) | (1<<DDB6) | (1<<DDB5) | (1<<DDB4) | (1<<DDB3) | (1<<DDB2) | (1<<DDB1) | (1<<DDB0);
// State: Bit7=1 Bit6=1 Bit5=1 Bit4=1 Bit3=1 Bit2=1 Bit1=1 Bit0=1
PORTB=(1<<PORTB7) | (1<<PORTB6) | (1<<PORTB5) | (1<<PORTB4) | (1<<PORTB3) | (1<<PORTB2) | (1<<PORTB1) | (1<<PORTB0);

// Port C initialization
// Function: Bit7=In Bit6=In Bit5=In Bit4=In Bit3=In Bit2=In Bit1=In Bit0=In
DDRC=(0<<DDC7) | (0<<DDC6) | (0<<DDC5) | (0<<DDC4) | (0<<DDC3) | (0<<DDC2) | (0<<DDC1) | (0<<DDC0);
// State: Bit7=T Bit6=T Bit5=T Bit4=T Bit3=T Bit2=T Bit1=T Bit0=T
PORTC=(0<<PORTC7) | (0<<PORTC6) | (0<<PORTC5) | (0<<PORTC4) | (0<<PORTC3) | (0<<PORTC2) | (0<<PORTC1) | (0<<PORTC0);

// Port D initialization
// Function: Bit7=Out Bit6=Out Bit5=Out Bit4=Out Bit3=Out Bit2=Out Bit1=Out Bit0=Out
```
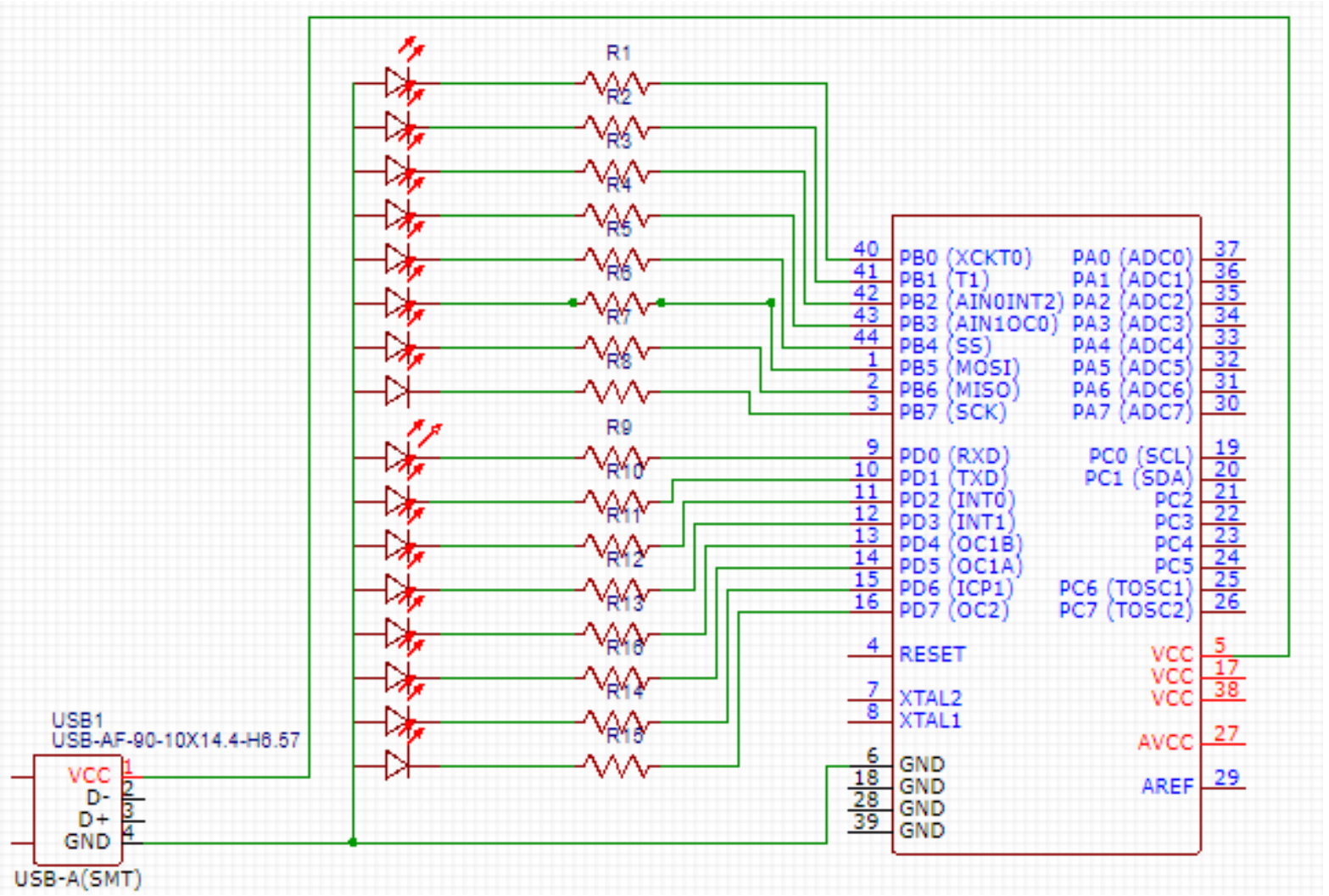

```
54. DDRD=(1<<DDD7) | (1<<DDD6) | (1<<DDD5) | (1<<DDD4) | (1<<DDD3) | (1<<DDD2) | (1<<D
    DD1) | (1<<DDD0);
55. // State: Bit7=0 Bit6=0 Bit5=0 Bit4=0 Bit3=0 Bit2=0 Bit1=0 Bit0=0
56. PORTD=(0<<PORTD7) | (0<<PORTD6) | (0<<PORTD5) | (0<<PORTD4) | (0<<PORTD3) | (0<<PO
    RTD2) | (0<<PORTD1) | (0<<PORTD0);
57.
58. // Timer/Counter 0 initialization
59. // Clock source: System Clock
60. // Clock value: Timer 0 Stopped
61. // Mode: Normal top=0xFF
62. // OC0 output: Disconnected
63. TCCR0=(0<<WGM00) | (0<<COM01) | (0<<COM00) | (0<<WGM01) | (0<<CS02) | (0<<CS01) |
    (0<<CS00);
64. TCNT0=0x00;
65. OCR0=0x00;
66.
67. // Timer/Counter 1 initialization
68. // Clock source: System Clock
69. // Clock value: Timer1 Stopped
70. // Mode: Normal top=0xFFFF
71. // OC1A output: Disconnected
72. // OC1B output: Disconnected
73. // Noise Canceler: Off
74. // Input Capture on Falling Edge
75. // Timer1 Overflow Interrupt: Off
76. // Input Capture Interrupt: Off
77. // Compare A Match Interrupt: Off
78. // Compare B Match Interrupt: Off
79. TCCR1A=(0<<COM1A1) | (0<<COM1A0) | (0<<COM1B1) | (0<<COM1B0) | (0<<WGM11) | (0<<WG
    M10);
80. TCCR1B=(0<<ICNC1) | (0<<ICES1) | (0<<WGM13) | (0<<WGM12) | (0<<CS12) | (0<<CS11) |
     (0<<CS10);
81. TCNT1H=0x00;
82. TCNT1L=0x00;
83. ICR1H=0x00;
84. ICR1L=0x00;
85. OCR1AH=0x00;
86. OCR1AL=0x00;
87. OCR1BH=0x00;
88. OCR1BL=0x00;
89.
90. // Timer/Counter 2 initialization
91. // Clock source: System Clock
92. // Clock value: Timer2 Stopped
93. // Mode: Normal top=0xFF
94. // OC2 output: Disconnected
95. ASSR=0<<AS2;
96. TCCR2=(0<<WGM20) | (0<<COM21) | (0<<COM20) | (0<<WGM21) | (0<<CS22) | (0<<CS21) |
    (0<<CS20);
97. TCNT2=0x00;
98. OCR2=0x00;
99.
100.       // Timer(s)/Counter(s) Interrupt(s) initialization
101.       TIMSK=(0<<OCIE2) | (0<<TOIE2) | (0<<TICIE1) | (0<<OCIE1A) | (0<<OCIE1B) |
    (0<<TOIE1) | (0<<OCIE0) | (0<<TOIE0);
102.
103.       // External Interrupt(s) initialization
104.       // INT0: Off
105.       // INT1: Off
106.       // INT2: Off
107.       MCUCR=(0<<ISC11) | (0<<ISC10) | (0<<ISC01) | (0<<ISC00);
```

```
108.       MCUCSR=(0<<ISC2);
109.
110.       // USART initialization
111.       // USART disabled
112.       UCSRB=(0<<RXCIE) | (0<<TXCIE) | (0<<UDRIE) | (0<<RXEN) | (0<<TXEN) | (0<<U
    CSZ2) | (0<<RXB8) | (0<<TXB8);
113.
114.       // Analog Comparator initialization
115.       // Analog Comparator: Off
116.       ACSR=(1<<ACD) | (0<<ACBG) | (0<<ACO) | (0<<ACI) | (0<<ACIE) | (0<<ACIC) |
    (0<<ACIS1) | (0<<ACIS0);
117.       SFIOR=(0<<ACME);
118.
119.       // ADC initialization
120.       // ADC disabled
121.       ADCSRA=(0<<ADEN) | (0<<ADSC) | (0<<ADATE) | (0<<ADIF) | (0<<ADIE) | (0<<AD
    PS2) | (0<<ADPS1) | (0<<ADPS0);
122.
123.       // SPI initialization
124.       // SPI disabled
125.       SPCR=(0<<SPIE) | (0<<SPE) | (0<<DORD) | (0<<MSTR) | (0<<CPOL) | (0<<CPHA)
    | (0<<SPR1) | (0<<SPR0);
126.
127.       // TWI initialization
128.       // TWI disabled
129.       TWCR=(0<<TWEA) | (0<<TWSTA) | (0<<TWSTO) | (0<<TWEN) | (0<<TWIE);
130.
131.       while (1)
132.             {
133.
134.
135.        PORTB++;
136.             PORTD--;
137.             delay_ms(250);
138.
139.             }
140.       }
```


R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
40 PB0 (XCKT0)
41 PB1 (T1)
42 PB2 (AIN0INT2)
43 PB3 (AIN1OC0)
44 PB4 (SS)
1 PB5 (MOSI)
2 PB6 (MISO)
3 PB7 (SCK)
9 PD0 (RXD)
10 PD1 (TXD)
11 PD2 (INT0)
12 PD3 (INT1)
13 PD4 (OC1B)
14 PD5 (OC1A)
15 PD6 (ICP1)
16 PD7 (OC2)
4 RESET
7 XTAL2
8 XTAL1
6 GND
18 GND
28 GND
39 GND
PA0 (ADC0) 37
PA1 (ADC1) 36
PA2 (ADC2) 35
PA3 (ADC3) 34
PA4 (ADC4) 33
PA5 (ADC5) 32
PA6 (ADC6) 31
PA7 (ADC7) 30
PC0 (SCL) 19
PC1 (SDA) 20
PC2 21
PC3 22
PC4 23
PC5 24
PC6 (TOSC1) 25
PC7 (TOSC2) 26
VCC 5
VCC 17
VCC 38
AVCC 27
AREF 29
USB1
USB-AF-90-10X14.4-H6.57
VCC 1
D- 2
D+ 3
GND 4
USB-A(SMT)